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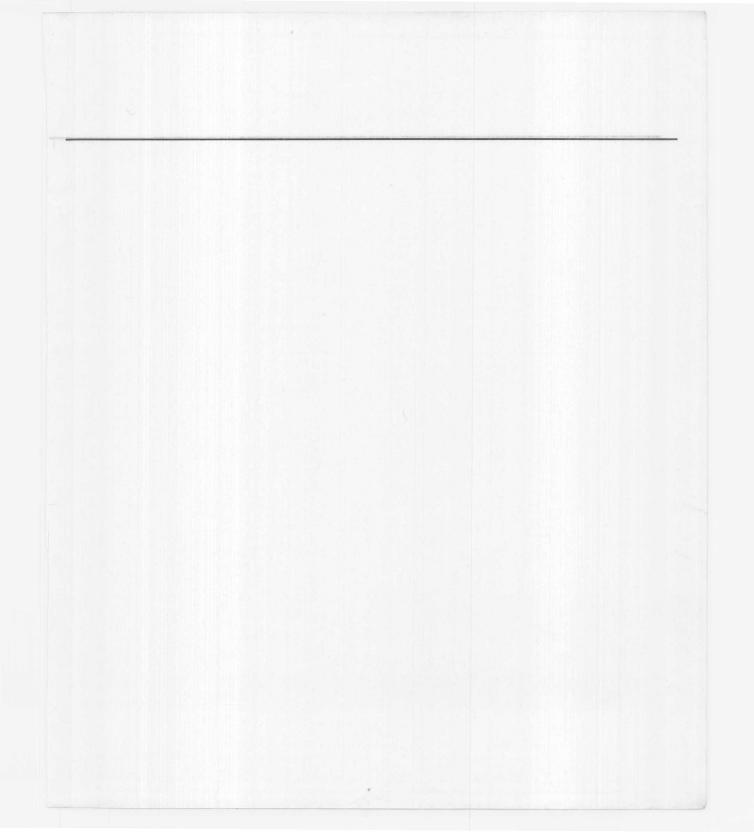
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## Slave Processors 2 sis 0



#### 8041AH/8041AH-2/8641A/8741A UNIVERSAL PERIPHERAL INTERFACE 8-BIT MICROCOMPUTER

8061AH/8041AH-2/8641A/8744A

- 8041AH-2: 12 MHz 8041AH: 8 MHz
- 8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package
- One 8-Bit Status and Two Data
   Registers for Asynchronous Slave-to-Master Interface
- DMA, Interrupt, or Polled Operation Supported
- 1024 x 8 ROM/EPROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins

- Fully Compatible with MCS-48<sup>TM</sup>, MCS-80<sup>TM</sup>, MCS-85<sup>TM</sup>, and iAPX-86,88 Microprocessor Families
- Interchangeable ROM and EPROM Versions
- Expandable I/O
- RAM Power-Down Capability
- Over 90 Instructions: 70% Single Byte
- Single 5V Supply

The Intel® 8041AH/8741A is a general-purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS-48™, MCS-80™, iAPX-85™, iAPX-86, iAPX-88, and other 8- or 16-bit systems.

The UPI-41A<sup>™</sup> has 1K words of program memory and 64 words of data memory on-chip. To allow full user flexibility the program memory is available as ROM in the 8041AH version or as UV-erasable EPROM in the 8741A version. The 8741A and the 8041AH are fully pin compatible for easy transition from prototype to production level designs. The 8741A is a one-time programmable (at the factory) 8741A which can be ordered as the first 25 pieces of a new 8041AH order. The substitution of 8641As for 8041AHs allows for very fast turnaround for initial code verification and evaluation results.

The device has two 8-bit, TTL-compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8041AH), single-step mode for debug and dual working register banks.

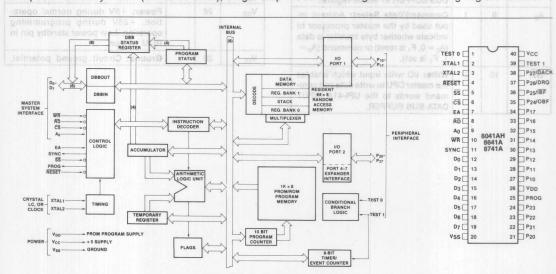


Figure 1. Block Diagram

Figure 2. Pin Configuration



#### Table 1. Pin Description

Symbol	Pin No.	Туре	Name and Function
TEST 0, TEST 1	1 39	86	Test Inputs: Input pins which can be directly tested using conditional branch instructions.
107 C		bne	Frequency Reference: TEST 1 (T <sub>1</sub> ) also functions as the event timer input (under software control). TEST 0 (T <sub>0</sub> ) is used during PROM programming and verification in the 8741A.
XTAL 1, XTAL 2	2 3	S %	Inputs: Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
RESET	4	1	Reset: Input used to reset status flip- flops and to set the program counter to zero.
	data data	OF US	RESET is also used during PROM programming and verification.
SS	5	X9Ai	Single Step: Single step input used in the 8741A in conjunction with the SYNC output to step the program through each instruction.
M in <mark>ZD</mark> otype to ordere	ong i	non i	Chip Select: Chip select input used to select one UPI-41A microcomputer out of several connected to a common data bus.
EA notion	ut de	nes c	External Access: External access input which allows emulation, testing and PROM/ROM verification. This pin should be tied low if unused.
evice <mark>dR</mark> o V supply banks.	gle 5	nie : el	Read: I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
A <sub>0</sub>	9	1 0	Command/Data Select: Address input used by the master processor to indicate whether byte transfer is data $(A_0 = 0, F_1 \text{ is reset})$ or command $(A_0 = 1, F_1 \text{ is set})$ .
WR E SP DAGUES E SE SEGUES E SE SEGUES E SE	10	1 D 10 1 D 28 1 D 28 2 D 28	Write: I/O write input which enables the master CPU to write data and com- mand words to the UPI-41A INPUT DATA BUS BUFFER.

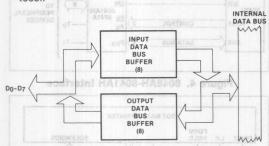
Symbol	Pin No.	Туре	Name and Function
SYNC	CONTROL OF SERVICE BOOK AND ADDRESS.		Output Clock: Output signal which occurs once per UPI-41A instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
D <sub>0</sub> -D <sub>7</sub> (BUS)	12-19	0 0	Data Bus: Three-state, bidirectiona DATA BUS BUFFER lines used to interface the UPI-41A microcompute to an 8-bit master system data bus.
P <sub>10</sub> -P <sub>17</sub>	27-34	1/0	Port 1: 8-bit, PORT 1 quasi-bidirectional I/O lines.
P20-P27	ontain no ci s a p ms. ms. ram rabl	s. It or tion a syste prog is avi	Port 2: 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P <sub>20</sub> -P <sub>23</sub> ) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access. The upper 4 bits (P <sub>24</sub> -P <sub>27</sub> ) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P <sub>24</sub> as Output Buffer Full (IOBF) interrupt, P <sub>25</sub> as Input Buffer Full (IBF) interrupt, P <sub>26</sub> as DMA Request (DRQ), and P <sub>27</sub> as DMA ACKnowledge (DACK).
PROG	25	1/0	<b>Program:</b> Multifunction pin used as the program pulse input during PROM programming.
/O ports ontrot. I/O I progra external		softwa ss. Ar	During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused.
Vcc	40	e 804	Power: +5V main power supply pin.
V <sub>DD</sub>	26		Power: +5V during normal opera- tion. +25V during programming operation. Low power standby pin in ROM version.
V <sub>SS</sub>	20	AHOOMA - 7	Ground: Circuit ground potential

Figure 1. Block Diagram

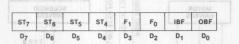


## UPI-41A™ FEATURES AND ENHANCEMENTS

 Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.



2. 8 Bits of Status



ST<sub>4</sub>-ST<sub>7</sub> are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4-7 of the accumulator are moved to bits 4-7 of the status register. Bits 0-3 of the status register are not affected.



 RD and WR are edge triggered. IBF, OBF, F<sub>1</sub> and INT change internally after the trailing edge of RD or WR.



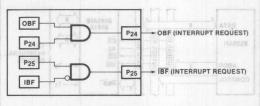
During the time that the host CPU is reading the status register, the 8041AH is prevented from updating this register or is 'locked out.'

 P<sub>24</sub> and P<sub>25</sub> are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

If the "EN FLAGS" instruction has been executed,  $P_{24}$  becomes the OBF (Output Buffer Full) pin. A "1" written to  $P_{24}$  enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to  $P_{24}$  disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI-41A (in Output Data Bus Buffer).

If "EN FLAGS" has been executed,  $P_{25}$  becomes the  $\overline{\text{IBF}}$  (Input Buffer Full) pin. A "1" written to  $P_{25}$  enables the  $\overline{\text{IBF}}$  pin (the pin outputs the inverse of the IBF Status Bit). A "0" written to  $P_{25}$  disables the  $\overline{\text{IBF}}$ 

pin (the pin remains low). This pin can be used to indicate that the UPI-41A is ready for data.



DATA BUS BUFFER INTERRUPT CAPABILITY



 P<sub>26</sub> and P<sub>27</sub> are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

If the "EN DMA" instruction has been executed, P<sub>26</sub> becomes the DRQ (DMA ReQuest) pin. A "1" written to P<sub>26</sub> causes a DMA request (DRQ is activated). DRQ is deactivated by DACK·RD, DACK·WR, or execution of the "EN DMA" instruction.

If "EN DMA" has been executed,  $P_{27}$  becomes the DACK (DMA ACKnowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.



#### **8041AH ENHANCEMENTS OVER 8041A**

- The RESET input on the 8041AH was changed to include a 2 stage synchronizer to support reliable reset operation for 12 MHz operation.
- As noted in the status register description, during the time that the host CPU is reading the status register, the 8041AH is prevented from updating or is 'locked out.'
- When EA is enabled on the 8041A, the program counter is placed on Port 1 and the lower two bits of Port 2. On the 8041AH, this information is multiplexed with PORT DATA (see port timing diagrams at end of this data sheet).
- The 8041AH additionally supports single step mode as described in the pin description section.

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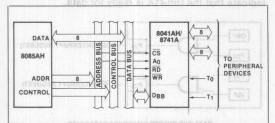


Figure 3. 8085AH-8041AH Interface

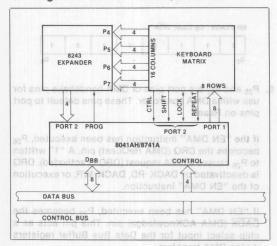


Figure 5. 8041AH-8243 Keyboard Scanner

#### PROGRAMMING, VERIFYING, AND **ERASING THE 8741A EPROM**

#### Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

res Pin Idealor	clude a 2 stage synchronizenoitone
XTAL 1	Clock Input (1 to 6MHz)
Reset	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input
TRO9 driw be	Data Output During Verify
818P20-1	Address Input salmit mod eas) ATAO
V <sub>DD</sub>	Programming Power Supply (1994)
PROG	Program Pulse Input

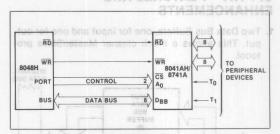


Figure 4. 8048AH-8041AH Interface

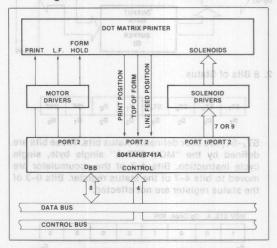


Figure 6. 8041AH Matrix Printer Interface

#### WARNING:

An attempt to program a missocketed 8741A will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

#### The Program/Verify sequence is:

- 1.  $A_0 = 0V$ ,  $\overline{CS} = 5V$ , EA = 5V,  $\overline{RESET} = 0V$ ,  $\overline{TESTO} = 5V$ , V<sub>DD</sub> = 5V, clock applied or internal oscillator operating, BUS and PROG floating.
- Insert 8741A in programming socket
- 3. TEST 0 = 0v (select program mode)
- EA = 23V (activate program model)<sup>1</sup>
- 5. Address applied to BUS and P20-1 80 on a semoned a 9
- RESET = 5v (latch address) 6. Data applied to BUS<sup>2</sup>
- 8. V<sub>DD</sub> = 25v (programming power)<sup>2</sup>
- PROG = 0v followered by one 50ms pulse to 23V<sup>2</sup>
- 10, VDD = 5v as belugaxa need and "20AJR M3" H
- 11. TEST 0 = 5v (verify mode) | III | nettue jugar | Hel

- and of opening nonsimple groups with a strong the strong s
- tion of the device at these or any other covor of the residence.
- 14. RESET = 0v and repeat from step 5 and m betsolbin scort
- 15. Programmer should be at conditions of step 1 when 8741A is removed from socket.

#### NOTE:

- 1. When verifying ROM, EA = 12V.
- 2. Not used in verify ROM procedure.

#### **8741A Erasure Characteristics**

The erasure characteristics of the 8741A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to complete the typical strong level fluorescent lighting could grase the typical

8741A in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8741A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8741A window to prevent unintentional erasure.

AUSULUIE MAAIMUM HAIINUD

The recommended erasure procedure for the 8741A is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 w-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000  $\mu$ W/cm² power rating. The 8741A should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

1.11/	which should be removed before erasure.	al 2.0-	8.0	erase	ng could	t lightii	room level fluorescent	
н	Input High Voltage (Except XTAL1, XTAL2, RESET	2.2	ooV	2.2	oo∀			
	Input High Voltage (XTAL1, XTAL2, RESET)		Vcc	8.6	Vec			
JOV	Output Low Voltage (O <sub>0</sub> -D <sub>7</sub> )		0.45		0.45		$l_{\rm QL}=2.0~{\rm mA}$	
ruoV	Output Low Voltage (P <sub>10</sub> P <sub>17</sub> , P <sub>20</sub> P <sub>27</sub> , Sync)		0.45		0.45		Am 8.1 = 10l	
Vola	Output Low Voltage (Prog)		0.45		0.45		I <sub>OL</sub> = 1.0 mA	
	Output High Voltage (D <sub>0</sub> -D <sub>7</sub> )			2.4		V		
гно <sup>V</sup>	Output High Voltage (All Other Outputs)						Ащ 00- = HO!	
J.	Input Leakage Current (T <sub>0</sub> , T <sub>1</sub> , RD, WR, CS, A <sub>0</sub> , EA)		01±		07±	Ац	V <sub>SS</sub> ≤V <sub>IN</sub> ≥V <sub>CC</sub>	
zol	Output Leakage Current (D <sub>0</sub> -D <sub>7</sub> , High Z State)		±10		01±	Аж	V <sub>SS</sub> + 0.45 ≤ V <sub>OUT</sub> ≤ V <sub>OC</sub>	
i ji	Low input Load Current (P10P17, P20P27)		0.3			Am	V 8.0 = J <sub>1</sub> V	
	Low Input Load Current (RESET, SS)		0.2		0.2		$V_{1L} = 0.8 V$	
	Voo Supply Current		15					
+ 00l			125		125		Typical = 60 mA	
HI	Input Leakage Current		100			AM	DOA = NIA	
	Input Capacitance		01		07			
	I/O Capacitanoe							



#### **ABSOLUTE MAXIMUM RATINGS\***

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. CHARACTERISTICS ( $T_A = 0^{\circ}$ to $+70^{\circ}$ C, $V_{CC} = V_{DD} = +5$ V $\pm$ 10%)

	wavelength of 2537A. The integraled dose (i.e sity x exposure time) for eracure should be of 15 w-sectom <sup>2</sup> . The eracure time with this	47.734	1AH/ AH-2	8641A			'A1A Erasura Chari ra arasura charact
Symbol	ns gniau setur Parameter visita and seturing set	Min.	Max.	Min.	Max.	Units	Test Conditions
tubes jiV tubes jiV their tubes	Input Low Voltage (Except XTAL1, XTAL2, RESET	-0.5	0.8	-0.5	0.8	Edura 1	roms (Å). It should roes of fluorescer
V <sub>IL1</sub>	Input Low Voltage (8XTAL1, XTAL2, RESET)	-0.5	ne typic 0.6	1 easie -0.5	0.6		pou-4000A range. D nom level fluorasce
VIH	Input High Voltage (Except XTAL1, XTAL2, RESET	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>		
V <sub>IH1</sub>	Input High Voltage (XTAL1, XTAL2, RESET)	3.8	Vcc	3.8	Vcc	٧	
V <sub>OL</sub>	Output Low Voltage (D <sub>0</sub> -D <sub>7</sub> )		0.45	10/12	0.45	V	I <sub>OL</sub> = 2.0 mA
V <sub>OL1</sub>	Output Low Voltage (P <sub>10</sub> P <sub>17</sub> , P <sub>20</sub> P <sub>27</sub> , Sync)		0.45		0.45	V	I <sub>OL</sub> = 1.6 mA
V <sub>OL2</sub>	Output Low Voltage (Prog)		0.45		0.45	٧	I <sub>OL</sub> = 1.0 mA
V <sub>OH</sub>	Output High Voltage (D <sub>0</sub> -D <sub>7</sub> )	2.4		2.4		٧	$I_{OH} = -400 \mu A$
V <sub>OH1</sub>	Output High Voltage (All Other Outputs)	2.4		2.4		٧	$I_{OH} = -50 \mu\text{A}$
hг	Input Leakage Current (T <sub>0</sub> , T <sub>1</sub> , $\overline{\text{RD}}$ , $\overline{\text{WR}}$ , $\overline{\text{CS}}$ , A <sub>0</sub> , EA)		±10		±10	μΑ	V <sub>SS</sub> ≤ V <sub>IN</sub> ≥ V <sub>CC</sub>
loz	Output Leakage Current (D <sub>0</sub> -D <sub>7</sub> , High Z State)		±10		±10	μΑ	V <sub>SS</sub> + 0.45 ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>
ILI	Low Input Load Current (P <sub>10</sub> P <sub>17</sub> , P <sub>20</sub> P <sub>27</sub> )		0.3		0.3	mA	V <sub>IL</sub> = 0.8 V
I <sub>LI1</sub>	Low Input Load Current (RESET, SS)		0.2		0.2	mA	V <sub>IL</sub> = 0.8 V
I <sub>DD</sub>	V <sub>DD</sub> Supply Current		15		15	mA	Typical = 5 mA
I <sub>CC</sub> +	Total Supply Current		125		125	mA	Typical = 60 mA
I <sub>IH</sub>	Input Leakage Current		100		100	NA	V <sub>IN</sub> = V <sub>CC</sub>
CIN	Input Capacitance		10		10	pF	
C <sub>I</sub> /O	I/O Capacitance		20		20	pF	



#### D.C. CHARACTERISTICS—PROGRAMMING (TA = 25°C ±5°C, VCC = 5V ±5%, VDD = 25V ± 1V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
VDOH	V <sub>DD</sub> Program Voltage High Level	24.0	26.0	T au V 2 22	whhA lead
VDDL	V <sub>DD</sub> Voltage Low Level	4.75	5.25	T block ass	twa Addie
VPH	PROG Program Voltage High Level	21.5	24.5	Va2 o	ets0 wat
VPL	PROG Voltage Low Level	1.00	0.2	V NOW O	two Data
VEAH	EA Program or Verify Voltage High Level	21.5	24.5	ort blott T	TER RES
VEAL	EA Voltage Low Level		5.25	emi Vaute	lyppy Vans
IDD	V <sub>DD</sub> High Voltage Supply Current		30.0	mA	SocV Hogy)
IPROG	PROG High Voltage Supply Current		16.0	mA	tiess Produ
IEA	EA High Voltage Supply Current	anobi ma	1.0	mA	Man T Mar

## A.C. CHARACTERISTICS (T<sub>CC</sub> = 0°C to +70°C, V<sub>SS</sub> = 0V, V<sub>CC</sub> = V<sub>DD</sub> = +5V ±10%)

		804	1AH	8041	AH-2	8641A	vat	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
t <sub>AR</sub>	CS, A <sub>0</sub> Setup to RD↓	0		0	R vd bure	O O	a) is high. La	ns ns
t <sub>RA</sub>	CS, A <sub>0</sub> Hold After RD↑	0		0		0		ns
t <sub>RR</sub>	RD Pulse Width					250	BIJAR	ns
t <sub>AD</sub>	CS, A <sub>0</sub> to Data Out Delay	MATA	130		130		225	ns <sup>[1]</sup>
t <sub>RD</sub>	RD↓ to Data Out Delay	.xaM	130		130	Paran	225	ns <sup>[1]</sup>
tDF	RD↑ to Data Float Delay		85		85	9 10 FW o	100	ns
tcy	Cycle Time (Except 8741A-8)	2	0 15	1.25	15	DAG 2.5	15	μs <sup>[2]</sup>
tcy	Cycle Time (8741A-8)	180			1	4.17	15	μs <sup>[3]</sup>

#### **DBB WRITE**

Symbol	Parameter	Min.	Max.	- Min-	Max.	Min.	Max.	Units
t <sub>AW</sub>	CS, A <sub>0</sub> Setup to WR↓	0	ea I	0		0		ns
t <sub>WA</sub>	CS, A <sub>0</sub> Hold After WR↑	.waM	nité	0 paille <sup>3</sup>	meter a Belore	O Para	Port C	today8 ns
tww	WR Pulse Width	160	901	160		250	Edge d	ns
t <sub>DW</sub>	Data Setup to WR↑ 00	130		130	After Fall	150	Port C	ns
twp	Data Hold After WR↑	0	- b	0	ing conel	0_	angg	ns

#### NOTES:

- 1.  $C_L = 150 pF$ .
- 2. 8, 12, 6 MHz XTAL respectively.
- 3. 3.6 MHz XTAL.

#### A.C. CHARACTERISTICS—PROGRAMMING ( $T_A = 25^{\circ}C \pm 5^{\circ}C$ , $V_{CC} = 5V \pm 5\%$ , $V_{DD} = 25V \pm 1V$ )

Symbol	Diser tinu Parameter nim	Min.	Max.	Unit	Test	Conditions
taw	Address Setup Time to RESET 1	4tcy	tage riign L	rogram Vo	agy	HOOV
twa	Address Hold Time After RESET 1	4tCy	Level	voitage Low	ggV	100/
tow	Data in Setup Time to PROG 1	4tCy	onage High	msigory c	UPI	Hav
twp	Data in Hold Time After PROG I	4tCy	ievel W	3 Voltage L	OPP	14,
tрн	RESET Hold Time to Verify	4tCy	enty Voltag	rogram or v	9 AB	EAH
tvDDW	V <sub>DD</sub> Setup Time to PROG 1	4tCy	1879	ollage Low	V AD	EAL
tvddh	VDD Hold Time After PROG I	0,000	вирріу Сп	hgh voitage	day	100
tpw	Program Pulse Width	50	Yiuque ag	mS	ORA	PURP
trw	Test 0 Setup Time for Program Mode	4tCy	Supply Cur	gn Voltage	1 43	I AS
twr	Test 0 Hold Time After Program Mode	4tcy			27.11	
tpo	Test 0 to Data Out Delay		4tCy			
tww	RESET Pulse Width to Latch Address	4tCy	100 = 001	SOITSIA	BIOA	HAHO .
tr, tf	V <sub>DD</sub> and PROG Rise and Fall Times	0.5	2.0	μS		TOPISITE O
tcy	CPU Operation Cycle Time	5.0		μS		Lordon
tre	RESET Setup Time Before EA 1.	4tCy	10	restante		10000
an TEST	is high to a can be triggered by RESET 1	0	Į0	Setup to R	CS, A	9,4

Note: If TEST 0 is high, t<sub>DO</sub> can be triggered by RESET 1.

## A.C. CHARACTERISTICS

80-	1 335 081			804	8041AH		8041AH-2		8641A/8741A	
Symbol	225	Parameter		Min.	Max.	Min.	Max.	Min.	Max.	Units
tACC	DACK to	o WR or RD 88		0 85		o ya	Float De	of o Date	IA	ns
tCAC	RD or W	VR to DACK	1.25	0 15	S .	7410-8)	(Except 6	emiTo lov	0	ns
tACD	DACK to	o Data Valid			130		8-130 (8)	emil ela	225	ns <sup>[1]</sup>
tCRQ	RD or WR to DRQ Cleared				90		90		200	ns

CS, Ao Hold After RD↑

Parameter

A.C. CHARACTERISTICS PORT 2  $(T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}, V_{CC} = +5\text{V} \pm 10\%)$ 

	0 0	804	8041AH		8041AH-2		8641A/8741A	
Symbol	Parameter	Min.	Max.	Min.	Max.	otoMin.	Max.	Units
tCP	Port Control Setup Before Falling Edge of PROG	100	160	100	rithi	110 = 011 Pulse W	W	ns <sup>[1]</sup>
t <sub>PC</sub>	Port Control Hold After Falling		130	60	↑ĀW o	qui100si	a	√ns <sup>[2]</sup>
tPR	PROG to Time P2 Input Must Be Valid		0		18W reff	A blold A	810	ns <sup>[1]</sup>
tpF	Input Data Hold Time	0	150	0	150	0	150	ns <sup>[2]</sup>
t <sub>DP</sub>	Output Data Setup time			200		250	Aq 08	ns <sup>[1]</sup>
t <sub>PD</sub>	Output Data Hold Time				ivery.	65	E XTAL	ns <sup>[2]</sup>
tpp	PROG Pulse Width			700		1200		ns

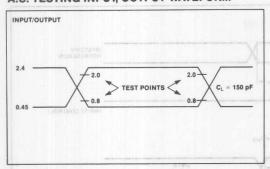
**NOTES:** 1. C<sub>L</sub> = 80 pF.

AFN-001885

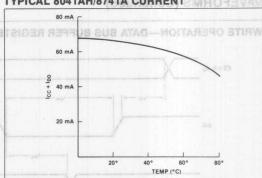
2.  $C_L = 20 pF$ .



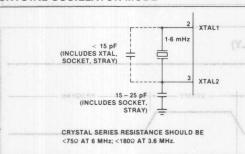
#### A.C. TESTING INPUT, OUTPUT WAVEFORM



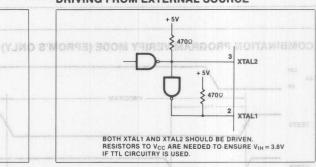
#### TYPICAL 8041AH/8741A CURRENT



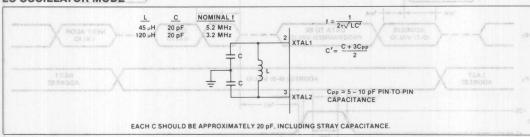
#### **CRYSTAL OSCILLATOR MODE**



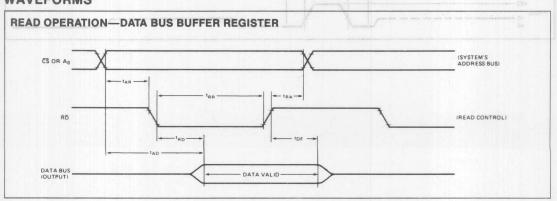
#### **DRIVING FROM EXTERNAL SOURCE**



#### LC OSCILLATOR MODE

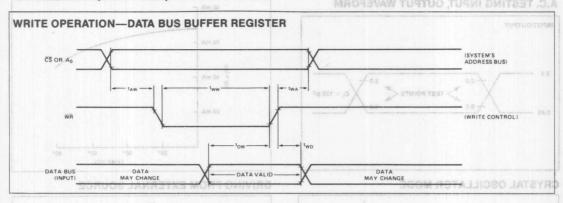


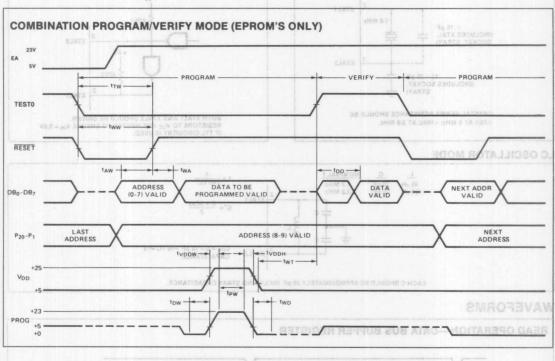
#### WAVEFORMS

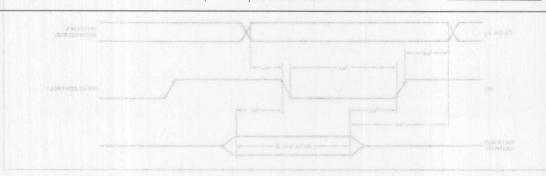




#### WAVEFORMS (Continued) 8 HATAGE JACIETT





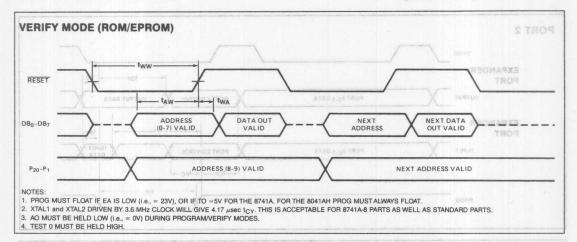




#### **WAVEFORMS (Continued)**

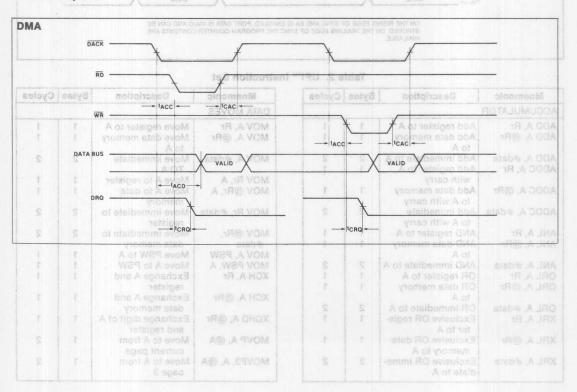
WAVEFORMS (Continued)

PORT TIMING DURING EA



The 8741A EPROM can be programmed by either of two Intel products:

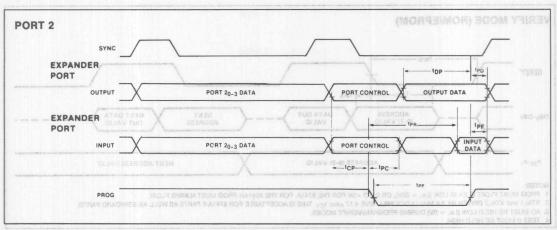
- 1. PROMPT-48 Microcomputer Design Aid, or
- Universal PROM Programmer (UPP series) peripheral of the Intellec® Development System with a UPP-848 Personality Card.



WAVEFORMS (Continued)



#### **WAVEFORMS** (Continued)



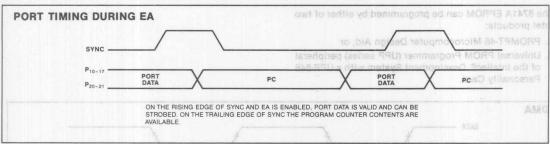


Table 2. UPI™ Instruction Set

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A, Rr	Add register to A	1 7	1
ADD A, @Rr	Add data memory to A	1 .	1 1
ADD A, #data	Add immediate to A	V2	2
ADDC A, Rr Add register to A with carry		^1_	11
ADDC A, @Rr	Add data memory to A with carry	1	1
ADDC A, #data	Add immediate to A with carry	_ 2	2
ANL A, Rr	AND register to A	PROP	1
ANL A, @Rr	AND data memory to A	1	1
ANL A, #data	AND immediate to A	2	2
ORL A, Rr	OR register to A	1	1
ORL A, @Rr	OR data memory to A	1	1
ORL A, #data	OR immediate to A	2	2
XRL A, Rr	Exclusive OR regis- ter to A	1	1
XRL A, @Rr	1	1	
XRL A, #data	memory to A Exclusive OR imme- diate to A	2	2

Mnemonic	Description	Bytes	Cycles
DATA MOVES			
MOV A, Rr	Move register to A	1	+1
MOV A, @Rr Move data memory to A		1	1
MOV A, #data   Move immediate   TO A		2	2
MOV Rr, A	Move A to register	1	1
MOV @Rr, A	Move A to data memory	1	1
MOV Rr, #data	Move immediate to register	2	2
MOV @Rr, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, Rr	Exchange A and register	1	1
XCH A, @Rr	Exchange A and data memory	1	1
XCHD A, @Rr	Exchange digit of A and register	1	1
MOVP A, @A	Move to A from current page	1	2
MOVP3, A, @A	Move to A from page 3	1	2

## Table 2. UPI™ Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
INC A	Increment A	HOD I	MAN IN
DEC A	Decrement A	SET 4 73 - 5	PO IN
	Clear A	101	- A 101
CLRA	Clear A	8 88-1	1APX
CPL A		a folia :	40.10
DAA	Decimal Adjust A	1	1
SWAP A	Swap nibbles of A	molto	atril .
RLA	Rotate A left	1	1.
RLCA	Rotate A left through	anoi	1619
112071	carry		
RR A	Rotate A right	- 1	1
	Rotate A right	dson	EXP
RRC A	Tiotate A right		
	through carry	183 co (1)	18 A D
INPUT/OUTPUT	er-Down Capabili	WO T	MPLA I
IN A, Pp	Input port toA	1	2
OUTL Pp, A	Output A to port	ni de	13 (2)
ANL Pp, #data	AND immediate to	2	2
F,	port		
ORL Pp, #data	OR immediate to	100	2
Onit i p, #data	port		-
IN A DDD		4	4
IN A, DBB	Input DBB to A, clear IBF	ace tha	heini le
	clear IBF	enion to	an wal o
OUT DBB, A	Output A to DBB,	101111 10	G12-17-121-10
s 40-pin packagi		no cto	unier, a
MOV STS, A	A <sub>4</sub> -A <sub>7</sub> to Bits 4-7 of	S 81 m	function
			16-bit.
MOVD A, Pp			
2 doubles the or	Input Expander port to A	8041A	with the
MOVD Pp, A	Quitout A to	10 00	ence
rom of Igsonoo	Expander port	the 804	ance of
ANLD Pp. A	AND A to Expander	oilons	ortona :
ANLU PP, A			
MORGE eldess	port polerey SM	8 erji ni	IS POM
ORLD Pp, A	Off A to Expander	ensit ve	2
Spieces of a new	port se berebro er	neo do	Jack value
TIMER/COUNTE	d for initial code veri R	naroun	rut tast tur
MOV A, T	Read Timer/Counter	1	1
		1	1
MOV T, A STRT T	Start Timer	ts. Indi	est inpu
STRT CNT	Start Timer start Counter	8243	est inpu
OTOD TONE	Stop Timer/Counter	ab Mu	ed in the
STOP TONT	Enable Timer/	vlanus	Va alro
EN TONTI		fiedding	A Park
	Counter Interrupt		
DIS TCNTI	Disable Timer/	1	1
	Counter Interrupt		
CONTROL			
	Enoble DMA Head	1	1
EN DMA	Enable DMA Hand-		1
2012/05/24	shake Lines		
ENI	Enable IBF Interrupt	1	1
DIS I	Disable IBF Inter-	1	1
24.0[] 40	rupt		
EN FLAGS	Enable Master	11000	1
	Interrupts		0.00
	Select register	1	1
SEL RBO			- Index
SEL RB0		100	(825)
	bank 0	1	1
SEL RB0 SEL RB1	bank 0 Select register	1	T.
	bank 0	1	( 161 - Linguist 2 100 h

Mnemonic	Description	Bytes	Cycles
REGISTERS			200
INC Rr INC @Rr	Increment register Increment data		a Pin
DEC ROSA	memory Decrement register	and du	104
SUBROUTINE	plus HOM, HAM	UMILI	18-5 a
CALL addr RET RETR	Jump to subroutine Return Return and restore status	81x 8	2 2 2
FLAGS		0.547	011
CLR C CPL C CLR F0 CPL F0 CLR F1	Clear Carry Complement Carry Clear Flag 0 Complement Flag 0 Clear F1 Flag Complement F1 Flag	istons e-to-t e, inte	Reg Reg Slav B DNI Suc
BRANCH			
JMP addr JMPP @A DJNZ Rr, addr JC addr JNC addr JZ addr JNZ addr JTO addr JNTO addr	Jump unconditional Jump indirect Decrement register and jump Jump on Carry=1 Jump on Carry=0 Jump on A Zero Jump on A not Zero Jump on T0=1 Jump on T0=1	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
JT1 addr JNT1 addr JF0 addr JF1 addr JTF addr	Jump on T1=1 Jump on T1=0 Jump on F0 Flag=1 Jump on F1 Flag=1 Jump on Timer Flag =1, Clear Flag	2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
JNIBF addr	Jump on IBF Flag	_	eer goolt
JOBF addr	Jump on OBF Flag		The dev
JBb addr	= 1 Jump on Accumula- tor Bit		has 16 l

Figure 2. Pin Configuration

Figure 1. Block Diagram



Bytes Cycles

# 8042/8742 UNIVERSAL PERIPHERAL INTERFACE 8-BIT MICROCOMPUTER

- 8042/8742: 12 MHz
- Pin, Software and Architecturally Compatible with 8041A/8741A/8041AH
- 8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package
- 2048 × 8 ROM/EPROM, 128 × 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins
- One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface
- DMA, Interrupt, or Polled Operation Supported

- Fully Compatible with MCS-48<sup>™</sup>, MCS-51<sup>™</sup>, MCS-80<sup>™</sup>, MCS-85<sup>™</sup>, and iAPX-86. 88 Microprocessor Families
- Interchangeable ROM and EPROM Versions
- Expandable I/O
- RAM Power-Down Capability Tuo Tugali
- Over 90 Instructions: 70% Single Byte
- Single 5V Supply

The Intel 8042/8742 is a general-purpose Universal Peripheral Interface that allows the designer to grow his own customized solution for peripheral device control. It contains a low-cost microcomputer with 2K of program memory, 128 bytes of data memory, 8-bit CPU, I/O ports, 8-bit timer/counter, and clock generator in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in the MCS-48<sup>TM</sup>, MCS-80<sup>TM</sup>, MCS-80<sup>TM</sup>, MCS-85<sup>TM</sup>, iAPX-88, iAPX-86 and other 8-, 16-bit systems.

The 8042/8742 is software, pin, and architecturally compatible with the 8041AH, 8741A. The 8042/8742 doubles the onchip memory space to allow for additional features and performance to be incorporated in upgraded 8041AH/8741A designs. For new designs, the additional memory and performance of the 8042/8742 extends the UPI concept to more complex motor control tasks, 80-column printers and process control applications as examples.

To allow full user flexibility, the program memory is available as ROM in the 8042 version or as UV-erasable EPROM in the 8742 version. The 8742 and the 8042 are fully pin compatible for easy transition from prototype to production level designs. The 8642 is a one-time programmable (at the factory) 8742 which can be ordered as the first 25 pieces of a new 8042 order. The substitution of 8642's for 8042's allows for very fast turnaround for initial code verification and evaluation results.

The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8042), single-step mode for debug, and dual working register banks.

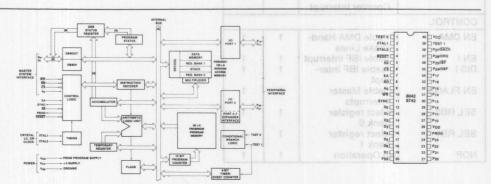


Figure 1. Block Diagram

Figure 2. Pin Configuration



#### of beau ed rep nig sidt (wol anisme) nigTable 1. Pin Description

Symbol	Pin No.	Туре	Name and Function
TEST 0, TEST 1	1 39	TWN RSC	Test Inputs: Input pins which can be directly tested using conditional branch instructions.
TEQUEST		BF (INTE	Frequency Reference: TEST 1 (T <sub>1</sub> ) also functions as the event timer input (under software control). TEST 0 (T <sub>0</sub> ) is used during PROM programming and verification in the 8742.
XTAL 1, XTAL 2	2	I	Inputs: Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
RESET	4	1	Reset: Input used to reset status flip- flops and to set the program counter to zero.
	Ishak	anan A	RESET is also used during PROM programming and verification.
SS OF H	5	e gins	Single Step: Single step input used in conjunction with the SYNC output to step the program through each instruction.
CS IW People of the contion	etival		Chip Select: Chip select input used to select one UPI microcomputer out of several connected to a common data bus.
EA mos the ote as a		I id, P <sub>2</sub> i This	External Access: External access input which allows emulation, testing and PROM/ROM verification. This pin should be tied low if unused.
RD	8	ı	Read: I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
Ao	9	HOAN	Command/Data Select: Address input used by the master processor to indicate whether byte transfer is data $(A_0 = 0, F1 \text{ is reset})$ or command $(A_0 = 1, F1 \text{ is set})$ .
WR	10	1	Write: I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER.

Symbol	Pin No.	Туре	Name and Function
AMABYMI BUB AYAQ	8/ <b>11</b> (8)	MO	Output Clock: Output signal which occurs once per UPI-42 instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
D <sub>0</sub> -D <sub>7</sub> (BUS)	12-19	I/O	Data Bus: Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI-42 microcomputer to an 8-bit master system data bus.
P <sub>10</sub> -P <sub>17</sub>	27-34	1/0	Port 1: 8-bit, PORT 1 quasi-bidirectional I/O lines.
P20-P27	Thes		Port 2: 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P <sub>20</sub> -P <sub>23</sub> ) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access. The upper 4 bits (P <sub>24</sub> -P <sub>27</sub> ) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P <sub>24</sub> as Output Buffer Full (OBF) interrupt, P <sub>25</sub> as Input Buffer Full (IBF) interrupt, P <sub>26</sub> as DMA Request (DRQ), and P <sub>27</sub> as DMA ACKnowledge (DACK).
PROG	25	1/0	Program: Multifunction pin used as the program pulse input during PROM programming.
00	0	0	During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused.
Vcc	40	BF, O	Power: +5V main power supply pin.
V <sub>DD</sub> 10 C	26	0 edg	Power: +5V during normal opera- tion. +21V during programming operation. Low power standby pin in ROM version.
V <sub>SS</sub>	20		Ground: Circuit ground potential

 The RESET input on the 8642/8742 includes a 2-stage synchronizer to support reliable reset operation for 12 MHz operation.

When EA is enabled on the 8042/8742, the program counter is placed on Port 1 and the lower three bits of Port 2 (MSB = P<sub>22</sub>, LSB = P<sub>10</sub>). On the 8042/8742 this information is multiplexed with PORT DATA (see port timing diagrams at end of this data sheet).

8. The 8042/8742 supports single step mode as described to the ole descriptor service.

can be used to interrupt a master processor. These pins default to port pins on Resel.

If the "EN FLAGS" instruction has been executed, F24 becomes the OBF (Output Buffer Full) pin. A "1" written to P24 enables the OBF pin (the pin outputs the OBF pin (the pin outputs bit) A "0" written to P24 disables the OBF pin (the pin remains low). This pin can be used to meticate that valid data is available from the UP4 41A (in Output Data Bus Buffer).

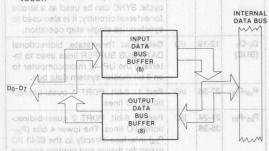
If "EN FLAGS" has been executed, P25 becomes the IBF (Input Buffer Full) pin. A "f" written to P25



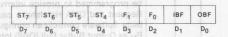
#### **UPI-42 FEATURES**

Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.

 Section 2007



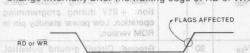
2. 8 Bits of Status amoini slub bas



ST<sub>4</sub>-ST<sub>7</sub> are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4-7 of the accumulator are moved to bits 4-7 of the status register. Bits 0-3 of the status register are not affected.



 RD and WR are edge triggered. IBF, OBF, F₁ and INT change internally after the trailing edge of RD or WR.



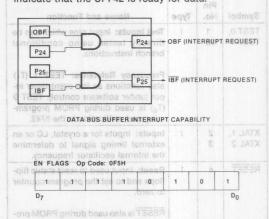
During the time that the host CPU is reading the status register, the 8042/8742 is prevented from updating this register or is 'locked out.'

 P<sub>24</sub> and P<sub>25</sub> are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

If the "EN FLAGS" instruction has been executed,  $P_{24}$  becomes the OBF (Output Buffer Full) pin. A "1" written to  $P_{24}$  enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to  $P_{24}$  disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI-41A (in Output Data Bus Buffer).

If "EN FLAGS" has been executed,  $P_{25}$  becomes the  $\overline{\rm IBF}$  (Input Buffer Full) pin. A "1" written to  $P_{25}$  enables the  $\overline{\rm IBF}$  pin (the pin outputs the inverse of the IBF Status Bit). A "0" written to  $P_{25}$  disables the  $\overline{\rm IBF}$ 

pin (the pin remains low). This pin can be used to indicate that the UPI-42 is ready for data.

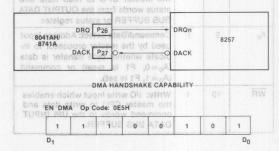


 P<sub>26</sub> and P<sub>27</sub> are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

put to step the program through

If the "EN DMA" instruction has been executed, P<sub>26</sub> becomes the DRQ (DMA ReQuest) pin. A "1" written to P<sub>26</sub> causes a DMA request (DRQ is activated). DRQ is deactivated by DACK·RD, DACK·WR, or execution of the "EN DMA" instruction.

If "EN DMA" has been executed,  $P_{27}$  becomes the DACK (DMA ACKnowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.



- The RESET input on the 8042/8742 includes a 2-stage synchronizer to support reliable reset operation for 12 MHz operation.
- 7. When EA is enabled on the 8042/8742, the program counter is placed on Port 1 and the lower three bits of Port 2 (MSB =  $P_{22}$ , LSB =  $P_{10}$ ). On the 8042/8742 this information is multiplexed with PORT DATA (see port timing diagrams at end of this data sheet).
- The 8042/8742 supports single step mode as described in the pin description section.



#### APPLICATIONS a equal of sleew and yielsmixorg

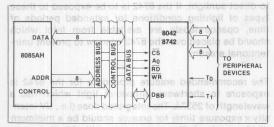


Figure 3. 8085AH-8042/8742 Interface

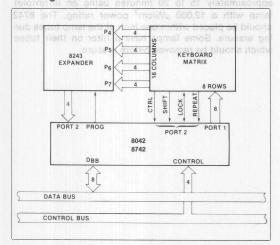


Figure 5. 8042/8742-8243 Keyboard Scanner

#### 

Figure 4. 8048H-8042/8742 Interface

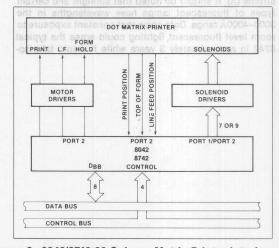


Figure 6. 8042/8742 80-Column Matrix Printer Interface

## PROGRAMMING, VERIFYING, AND ERASING THE 8742 EPROM

#### **Programming Verification**

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (1 to 12MHz)
Reset	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output During Verify
P20-1	Address Input
V <sub>DD</sub>	Programming Power Supply
PROG	Program Pulse Input

#### WARNING

An attempt to program a missocketed 8742 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

#### The Program/Verify sequence is:

- A<sub>0</sub> = 0V, <del>CS</del> = 5V, EA = 5V, <del>RESET</del> = 0V, TEST0 = 5V, V<sub>DD</sub> = 5V, clock applied or internal oscillator operating, BUS and PROG floating.
- 2. Insert 8742 in programming socket
- 3. TEST 0 = 0v (select program mode)
- 4. EA = 21V (active program mode)\*
- 5. Address applied to BUS and P20-22
- 6. RESET = 5v (latch address)
- 7. Data applied to BUS\*\*
- 8. V<sub>DD</sub> = 21V (programming power)\*\*
- 9. PROG = 0v followed by one 50 ms pulse to 21V\*\*
- 10. V<sub>DD</sub> = 5v
- 11. TEST 0 = 5v (verify mode)



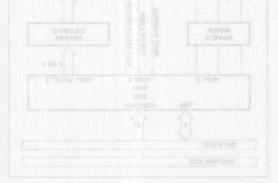
- 12. Read and verify data on BUS
- 13. TEST 0 = 0v
- 14. RESET = 0v and repeat from step 5
- Programmer should be at conditions of step 1 when 8742 is removed from socket

\*When verifying ROM, EA = 12V.

\*\*Not used in verifying ROM procedure.

#### 8742 Erasure Characteristics

The erasure characteristics of the 8742 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8742 in approximately 3 years while it would take ap-



proximately one week to cause erasure when exposed to direct sunlight. If the 8742 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8742 window to prevent unintentional erasure.

The recommended erasure procedure for the 8742 is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 w-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000  $\mu\text{W/cm}^2$  power rating. The 8742 should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.



Figure 5. 8042/8742-8243 Keyboard Scenner

#### PROGRAMMING, VERIFYING, AND ERASING THE 8742 EPROM

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a varification step. The following is a list of the pins used for programming and a descrip-

	Clock Input (1 to 12MHz)
	Activation of Program/Verity Modes
P20-1	
	Program Pulse Input

EA = 21V (active program mode Address applied to 5US and Pr PESET = 5v (latch address)

Data applied to BUS\*\*
Vota = 21V (programming

PRIOG = 0x followed by one 50 ms p VDD = 5x



#### ABSOLUTE MAXIMUM RATINGS\*

	2001 7000
Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	65°C to + 150°C
Voltage on Any Pin With Respect	VANIETY
to Ground	-0.5V  to  +7V
Power Dissipation	1.5 Watt

"NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### D.C. CHARACTERISTICS (TA = 0° to +70°C, V<sub>CC</sub>=V<sub>DD</sub>= +5V ± 10%) to sind of 10R

8/1		85	85		42 Vals	8742	8642	dt tOFL	
Symbol		Parameter at	1.25	Min.	Max.	Min.	Max.	Units	Notes
V <sub>IL</sub>	Input Low Volt	age (Except XTAL1, XTAL2,	RESET)	- 0.5	0.8	- 0.5	0.8	٧	
V <sub>IL1</sub>	Input Low Volt	age (XTAL1, XTAL2, RESET	)	- 0.5	0.6	- 0.5	0.6	٧	DBS WRITE
VIH	Input High Vol	tage (Except XTAL1, XTAL2	, RESET)	2.2	V <sub>CC</sub>	2.2	Vcc	٧	Symbol
V <sub>IH1</sub>	Input High Vol	tage (XTAL1, XTAL2, RESE	n o	3.8	Vcc	3.8	Vcc	V	WAI
VoL	Output Low Vo	oltage (D-D7)	0		0.45	Vialia	0.45	V	I <sub>OL</sub> = 2.0 mA
V <sub>OL1</sub>	Output Low Vo	oltage (P <sub>10</sub> P <sub>17</sub> , P <sub>20</sub> P <sub>27</sub> , Syno	o) Car		0.45	-dip	0.45	٧	I <sub>OL</sub> = 1.6 mA
V <sub>OL2</sub>	Output Low Vo	oltage (PROG)	130		0.45	IAW o	0.45	NO.	I <sub>OL</sub> = 1.0 mA
V <sub>OH</sub>	Output High V	oltage (D <sub>0</sub> -D <sub>7</sub> )	0	2.4	- 1	2.4	A bioh	e V	$I_{OH} = -400  \mu A$
V <sub>OH1</sub>	Output High V	oltage (All Other Outputs)		2.4		2.4		٧	$I_{OH} = -50 \mu A$
I <sub>IL</sub>	Input Leakage	Current (T <sub>0</sub> , T <sub>1</sub> , RD, WR, C	S, A <sub>0</sub> , EA)		± 10		± 10	μΑ	V <sub>SS</sub> ≤V <sub>IN</sub> ≥V <sub>CC</sub>
loz	Output Leakage Current (D <sub>0</sub> -D <sub>7</sub> , High Z State)				± 10		± 10	μΑ	$V_{SS} + 0.45$ $\leq V_{OUT} \leq V_{CC}$
ILI (V	Low Input Loa	d Current (P <sub>10</sub> P <sub>17</sub> , P <sub>20</sub> P <sub>27</sub> )	ING (TA	AMAI	0.3	98	0.3	mA	V <sub>IL</sub> = 0.8V
I <sub>U1</sub>	Low Input Loa	d Current (RESET, SS)	***************************************		0.2		0.2	mA	V <sub>IL</sub> = 0.8V
I <sub>DD</sub>	V <sub>DD</sub> Supply Cu	rrent		1.70	15	130	15	mA	Typical = 5 mA
I <sub>CC</sub> +I <sub>DD</sub>	Total Supply C	urrent		1 7 3 3	125	A second	125	mA	Typical=60 mA
I <sub>IH</sub>	Input Leakage	Current			100	d.emil	100	μА	$V_{IN} = V_{CC}$
CIN	Input Capacita	nce york		1.0	10	A enu	10	pF	owi I
CI/O	I/O Capacitano	e york			20	al sin	20	pF	

#### D.C. CHARACTERISTICS—PROGRAMMING (TA = 25°C ±5°C, V<sub>CC</sub> = 5V ±5%, V<sub>DD</sub> = 21V ± 1V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
VDOH	V <sub>DD</sub> Program Voltage High Level	20.0	22.0	V	P VUI
VDDL	V <sub>DD</sub> Voltage Low Level	4.75	5.25	V BEID 1 130	AM WW.
VPH	PROG Program Voltage High Level	21.5	24.5	V	OV 10 TO THE
VPL	PROG Voltage Low Level		0.2	V	40 Y31
VEAH	EA Program or Verify Voltage High Level	21.5	24.5	dayse 130	387
VEAL	EA Voltage Low Level		5.25	on sove co	Note: If TEST 0 is high.
IDD	V <sub>DD</sub> High Voltage Supply Current		30.0	mA	
IPROG	PROG High Voltage Supply Current		16.0	mA	
IEA	EA High Voltage Supply Current		1.0	mA.	



# **A.C. CHARACTERISTICS** ( $T_A = 0$ °C to +70°C, $V_{SS} = 0$ V, $V_{CC} = V_{DD} = +5$ V $\pm 10$ %) DBB READ

onditions abov	the device at these or any other o	16 not 8042 01000		8642/8742		Ambient Tem	
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	
oivelot <sub>AR</sub> ha vas	cS, A <sub>0</sub> Setup to RDI	grits 0 v	-0.6V to +7	0	1 111111 111 4 (11	bayons of	
t <sub>RA</sub>	CS, A <sub>0</sub> Hold After RD1	it oreliabil	1.5 Wa	0	noite	glas Cns wor	
t <sub>RR</sub>	RD Pulse Width	160		160		ns	
t <sub>AD</sub>	CS, A <sub>0</sub> to Data Out Delay		130		130	ns <sup>[1]</sup>	
t <sub>RD</sub>	RDI to Data Out Delay	+ = ggV = opV	0° 9\13001 ° 0	STICS (TA=	130	ns[1]	
t <sub>DF</sub>	RD1 to Data Float Delay		85		85	ns	
tcy	Cycle Time AM Make	1.25	15	1.25	15	μS <sup>[2]</sup>	

Symbol	Parameter	e Min.	Max.	Min.	Max.	Units
t <sub>AW</sub>	CS, A <sub>0</sub> Setup to WRI	8.8 0.	TALZ, RESET	CILIA O ans	loV dolH tugal	ns
twa	CS, A <sub>0</sub> Hold After WR1	Ö		(cCl+cO) spati	Swinger Low Ve	ns
Artww = 10	WR Pulse Width	160	PonPost Sync	260	Output Low Ve	ns
Artow =	Data Setup to WR1	130		(200150,081)	N woul tuched	ns
two Ho	Data Hold After WR1	0		(-C-oO ansile	M circlet Auraba D	ns

Input Low Voltage (Except XTAL1, XTAL2, RESET) = 0.5 0.8

#### A.C. CHARACTERISTICS—PROGRAMMING (T<sub>A</sub> = 25 °C ± 5 °C, V<sub>CC</sub> = 5V ± 5%, V<sub>DD</sub> = 21V ± 1V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
taw	Address Setup Time to RESET 1	4tCy		membo yic	deg 60 a 00
twa	Address Hold Time After RESET 1	4tCy		HOTHU VIC	ns 1810 1 1991 + 30
tow	Data in Setup Time to PROG 1	4tCy		smuO egazi	eJ rugnt   H
two	Data in Hold Time After PROG I	4tcy		eonsticae	sO tugal wi
tрн	RESET Hold Time to Verify	4tcy		eonatio	No WO Capa
tvddw	V <sub>DD</sub> Setup Time to PROG 1	4tcy			
tvDDH	V <sub>DD</sub> Hold Time After PROG ↓	0			
tpw	Program Pulse Width	50	60	mS	
trw v	Test 0 Setup Time for Program Mode	4tcy	089	ENISTIC	C. CHARACT
twr	Test 0 Hold Time After Program Mode	4tCy			
too	Test 0 to Data Out Delay		4tCy		Symplet
tww	RESET Pulse Width to Latch Address	4tcy		100000	CV 100V
tr, tf	V <sub>DD</sub> and PROG Rise and Fall Times	0.5	2.0	μS	02 1007
tcy	CPU Operation Cycle Time	5.0	Veltural	μS	ag way
tre	RESET Setup Time Before EA1.	4tCy	TOYOU WE	Costie V D	25 - Jan 194V

Note: If TEST 0 is high, t<sub>DO</sub> can be triggered by RESET 1.

NOTES: 1. C<sub>L</sub> = 100 pF. 2. 12 MHz XTAL.



#### A.C. CHARACTERISTICS DMA

		80	8042		8642/8742	
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t <sub>ACC</sub>	DACK to WR or RD	0	H 20 ps	0		ns
tCAC	RD or WR to DACK	=0		0		ns
t <sub>ACD</sub>	DACK to Data Valid	1	130		130	ns <sup>[1]</sup>
tcRQ	RD or WR to DRQ Cleared	1 7 =	90		90	ns

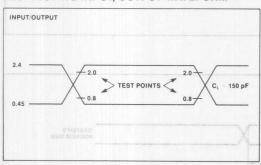
NOTE:

#### A.C. CHARACTERISTICS PORT 2 (TA = 0°C to +70°C, VCC = +5V ± 10%)

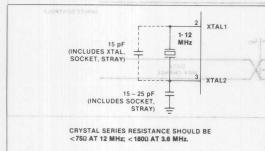
		80	)42	8642		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t <sub>CP</sub>	Port Control Setup Before Falling Edge of PROG	100		100		ns[1]
tPC	Port Control Hold After Falling Edge of PROG		1908 808	60	PERATION	ns[2]
tPR	PROG to Time P2 Input Must Be Valid		650		650	ns <sup>[1]</sup>
tpF	Input Data Hold Time	0	150	0	150	ns <sup>[2]</sup>
t <sub>DP</sub>	Output Data Setup Time	200		200	V	ns <sup>[1]</sup>
t <sub>PD</sub>	Output Data Hold Time	60		60		ns <sup>[2]</sup>
tpp	PROG Pulse Width	700		700		ns

NOTES: DONTHOD CARN

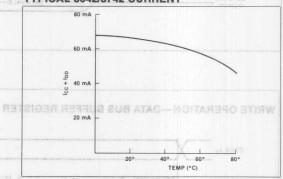
#### A.C. TESTING INPUT, OUTPUT WAVEFORM



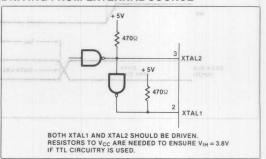
#### **CRYSTAL OSCILLATOR MODE**



#### TYPICAL 8042/8742 CURRENT



#### **DRIVING FROM EXTERNAL SOURCE**

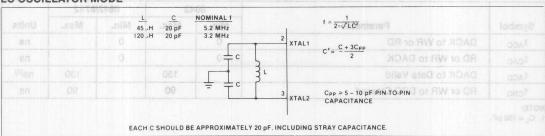


<sup>1.</sup> C<sub>L</sub> = 150 pF.

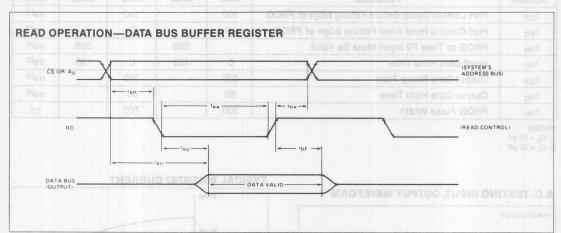
<sup>1.</sup> C<sub>L</sub> = 80 pF. 2. C<sub>L</sub> = 20 pF.

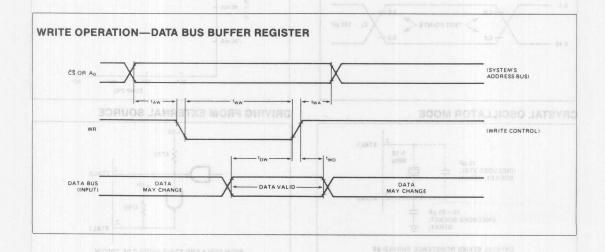






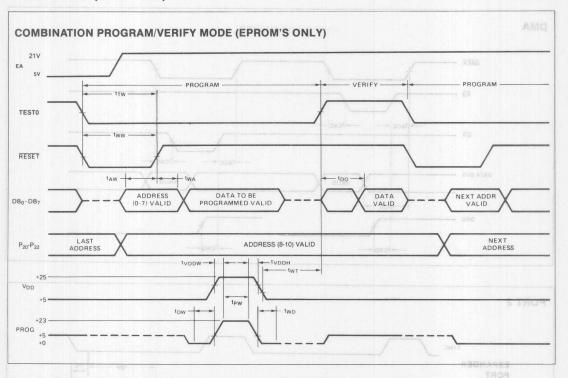
#### **WAVEFORMS**

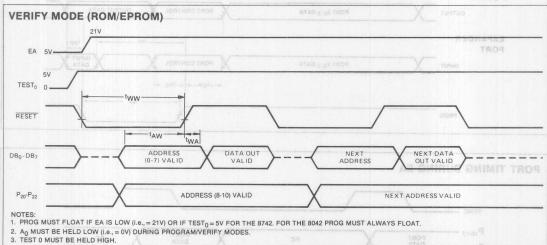






#### **WAVEFORMS (Continued)**





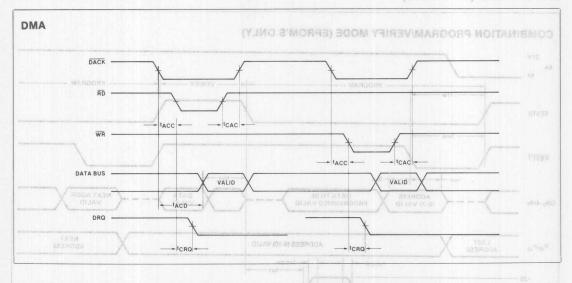
The 8742 EPROM can be programmed by the following Intel product:

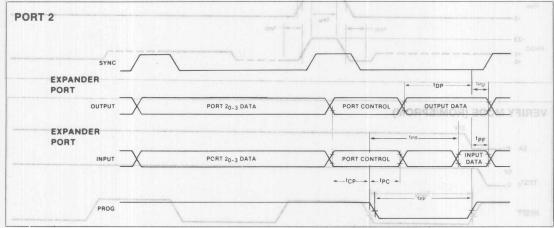
 Universal PROM Programmer (UPP series) peripheral of the Intellec® Development System with a UPP-549 Personality Card.



#### **WAVEFORMS** (Continued)

#### WAVEFORMS (Continued)





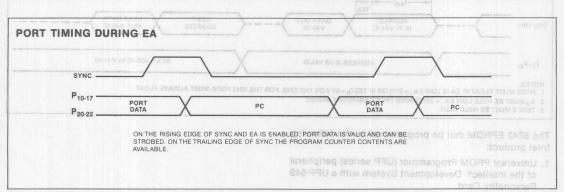




Table 2. UPI™ Instruction Set 3) to 2 noite artist #19U SetdeT

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A. Rr	Add register to A	1	1
ADD A, @Rr	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, Rr	Add register to A with carry	1	1
ADDC A, @Rr	Add data memory to A with carry	1	1
ADDC A, #data	Add immediate to A with carry	2	2
ANL A, Rr	AND register to A	1	1
ANL A, @Rr	AND data memory	1	1
ANL A, #data	AND immediate to A	2	2
ORL A, Rr	OR register to A	1	1
ORL A, @Rr	OR data memory	i	1
ORL A, #data	OR immediate to A	2	2
XRL A, Rr	Exclusive OR regis- ter to A	1	1
XRL A, @Rr	Exclusive OR data memory to A	- 1	1
XRL A, #data	Exclusive OR immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLRA	Clear A	1	1
CPL A	Complement A	1	1
DAA	Decimal Adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RLA	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A RRC A	Rotate A right Rotate A right through carry	1	1
INPUT/OUTPUT	tinough carry		
	Innut now to A	4	1 0
IN A, Pp	Input port toA	1	2 2
OUTL Pp, A ANL Pp, #data	Output A to port AND immediate to port	2	2
ORL Pp, #data	OR immediate to	2	2
IN A, DBB	Input DBB to A, clear IBF	1	1
OUT DBB, A	Output A to DBB, set OBF	1	1
MOV STS, A	A <sub>4</sub> -A <sub>7</sub> to Bits 4-7 of Status	1	1
MOVD A, Pp	Input Expander port to A	1	2
MOVD Pp, A	Output A to Expander port	1	2
ANLD Pp, A	AND A to Expander	1	2
ORLD Pp, A	OR A to Expander port	1	2

Mnemonic	Description	Bytes	Cycles
DATA MOVES			20A 13
MOV A, Rr	Move register to A	1	อ หนือ
MOV A, @Rr	Move data memory	1	0 40
	Clear Flag 0 A of		OLR FI
MOV A, #data	Move immediate	2	2
	Clear F1 FLA OT		OLR P
MOV Rr, A	Move A to register	1	a to
MOV @Rr, A	Move A to data	1	1
	memory	R	BRANC
MOV Rr, #data		210	2
2 1	registeron amut	A(6)	PHML
MOV @Rr,	Move immediate to	15-12	2
#data	data memory		
MOV A, PSW	Move PSW to A	1 1	obs DL
MOV PSW, A	Move A to PSW	1 10	os Olfil
XCH A, Rr	Exchange A and		obs15L
	register no qualif		JALE SIG
XCH A, @Rr	Exchange A and		bs OTL
2 2	data memory	100	S OTML
XCHD A, @Rr	Exchange digit of A		os itt
MOVERA	and register		S FTMU
MOVP A, @A	Move to A from		bs 2
MOVED A SA	current page	1 10	Da Mil
MOVP3, A, @A	Move to A from page 3	1 10	05 2
		wish.	SIGNLE.
TIMER/COUNTE	R part round quitte	70,02	38WL
MOV A, T	Read Timer/Counter	1 <sub>bb</sub>	aabu
MOV T, A	Load Timer/Counter	1	1
STRTT	Start Timer	1 115	os olst
STRT CNT	start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/	1	1
DIO TOLITI	Counter Interrupt		
DIS TCNTI	Disable Timer/	1	1
	Counter Interrupt		
CONTROL			
EN DMA	Enable DMA Hand-	1	1
	shake Lines		
ENI	Enable IBF Interrupt	1	1
DIS I	Disable IBF Inter-	1	1
	rupt		
EN FLAGS	Enable Master	1	-1
OFL DDO	Interrupts		
SEL RB0	Select register	1	1
OFL DD4	bank 0	-	4
SEL RB1	Select register	1	1
NOP	bank 1 No Operation	1	1
	140 Operation	1	
REGISTERS			
INC Rr	Increment register	1	1
INC @Rr	Increment data	1	1
	memory		1 1 2 1 5
DEC Rr	Decrement register	1	1
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore	1	2



Table 2. UPI™ Instruction Set (Continued) stant \*19U & side?

Mnemonic	Description	Bytes	Cycles
FLAGS		IOVES	DATA N
CLR C CPL C CLR F0 CPL F0 CLR F1 CPL F1	Clear Carry Complement Carry Clear Flag 0 Complement Flag 0 Clear F1 Flag Complement F1 Flag	stele .	VGM VGM 1 A VGM 1 R VGM
BRANCH		25 ,3270	a voin
JMP addr JMPP @A DJNZ Rr, addr JC addr JNC addr JZ addr JNZ addr JNT0 addr JNT1 addr JNT1 addr JF0 addr JF1 addr JF1 addr JF1 addr JF1 addr	Jump unconditional Jump indirect Decrement register and jump Jump on Carry=1 Jump on Carry=0 Jump on A Zero Jump on A not Zero Jump on T0=1 Jump on T0=0 Jump on T1=0 Jump on T1=0 Jump on T1=1 Jump on T1=1 Jump on T1 Flag=1	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
	=0	MOOO	HEIGHT
JOBF addr JBb addr	Jump on OBF Flag =1 Jump on Accumula- tor Bit	2 2	2
	legunoc/teutra dote	18151	2010
	Enable Timer/ Counter Interrupt Disable Timer/ Counter Interrupt		EN TO
		.10/	
	Enable DMA Hand- shake Lines Enable IBF Interrupt Disable IBF Inter-	A	
	rupt Enable Master	808	EN FL
	Interrupts Select register bank 0	08	SEL R
	Select register bank 1	81	
			NOP
	Increment register Increment data memory	INC Rr	
	Decrement register		DEC R
		addr	

Cycles	Bytes	Description	Minemonic
			<b>ACCUMULATOR</b>
-		A of rataiper bbA	ADD A. Br
		Add data memory	ADD A. @Rr
			ing , a uur
		A of	
2	2	Add immediate to A	stable A GOA
		Add register to A	ADDC A, Rt
		with carry	
1	1	Add data memory	ADDC A, @Rr
		to A with carry	
		Add immediate	ADDC A. #data
		to A with carry	
	1	AND register to A	ANL A, Rr
		AND date memory	ANL A. @Rr
4			HILLY MILE
0		A of	
S	S	AND immediate to A	ANL A. #data
1	- 1	OR register to A	
T	1	OR data memory	ORL A. @Ar
		A or	
	2	OR immediate to A	ORL A, #data
1		Exclusive OR regis-	KRLA, Br
		A of net	
1	1	Exclusive OR data	XRL A CORE
		memory to A	
0	S	Exclusive OR imme-	XRL A. #data
		A at staib	MINUTE AND SERVING
			1.00
		Increment A	NC A
1	1	Decrement A	DEC A
1		Clear A	A RJO
		Complement A	
			A AO
	. 8	Swap nibbles of A	
		Rotate A left	AUR
	*	Rotate A left through	A DJA
		carry	
		Rotate A right	A RR
	1	Rotate A right	
		through carry	
			NPUT/OUTPUT
		Input port toA	N A, Pp
		Output A to port	OUTL Pp. A
2		AND immediate to	ANL Pp, #data
8	S	of etsiberum RO	ORL Pp. #data
		nort	The state of the state of
		Input DBB to A.	000 000
			IN A, DBB
		clear IBF	
1	1	Output A to DBB,	OUT DBB, A
		set OBF	
		A4-A7 to Bits 4-7 of	MOV STS, A
		Status	
	1	Input Expander	MOVD A, Pp
		A of hea	
	-	Output A to	MOVD Pp. A
0		Expander port	4 -0 0 114
	- 1	AND A to Expander	ANLO Pp. A
	1	OF A to Expander	ORLD Pp, A



#### notigh 8231 A r stdaT

#### ARITHMETIC PROCESSING UNIT

- Fixed Point Single and Double Precision (16/32 Bit)
- Floating Point Single Precision (32 Bit)
- Binary Data Formats
- Add, Subtract, Multiply and Divide
- Trigonometric and Inverse
   Trigonometric Functions
- Square Roots, Logarithms, Exponentiation
- Float to Fixed and Fixed to Float Conversions
- Stack Oriented Operand Storage

- Compatible with MCS-80<sup>TM</sup> and MCS-85<sup>TM</sup> Microprocessor Families
- Direct Memory Access or Programmed I/O Data Transfers
- End of Execution Signal
- General Purpose 8-Bit Data Bus Interface
- Standard 24 Pin Package
- + 12 Volt and + 5 Volt Power Supplies
- Advanced N-Channel Silicon Gate HMOS Technology

The Intel® 8231A Arithmetic Processing Unit (APU) is a monolithic HMOS LSI device that provides high performance fixed and floating point arithmetic and floating point trigonometric operations. It may be used to enhance the mathematical capability of a wide variety of processor-oriented systems. Chebyshev polynomials are used in the implementation of the APU algorithms.

All transfers, including operand, result, status and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and commands are issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack.

Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end of execution signal that may be used as an interrupt by the CPU to help coordinate program execution.

In January 1981 Intel will be converting from 8231 to 8231A. The 8231A provides enhancements over the 8231 to allow use in both asynchronous and synchronous systems.

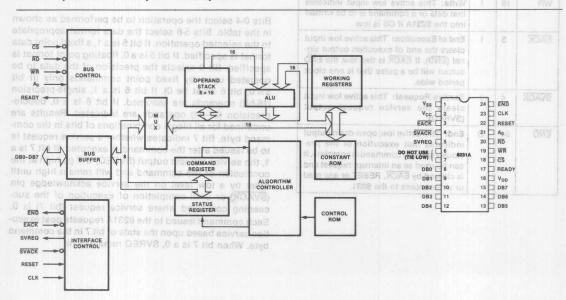


Figure 1. Block Diagram

Figure 2. Pin Configuration



#### Table 1. Pin Description

Symbol	Pin No.	Туре		Name and Function		
Vcc	2	ne "	Power	: +5 Volt power supply.		
V <sub>DD</sub>	16	641	Power	Power: +12 Volt power supply.		
V <sub>SS</sub>	1	- 1	Groun			
CLK	23	งร้างIcus	127 127 667 1	An external, TTL compatible,		
		1000		source is applied to the CLK pin.		
RESET	22	ews	Reset: The active high reset signal provides initialization for the chip. RESET also terminates any operation in progress. RESET clears the status register and places the 8231A into the idle state. State contents and command registers are not affected (5 clock cycles).			
CS et	18	1	signal	Chip Select: CS is an active low inpu signal which selects the 8231A and en ables communication with the data bus		
A <sub>0</sub> sometive rematica	ism	edt es	and W tablish that is t	<b>88:</b> In conjunction with the $\overline{\text{RD}}$ R signals, the $A_0$ control line esses the type of communication to be performed with the 8231A as below:		
Ao		RD	WR	Function		
d vanto	pile DUI	1 0 1 0	0 1 0	Enter data byte into stack Read data byte from stack Enter command Read status		
RD ituos	20	rojnar rojnar ine 82	that da	This active low input indicates ta or status is to be read from the if CS is low.		
WR	19	- 1	that da	This active low input indicates ta or a command is to be written e 8231A if CS is low.		
EACK	3	1	End of Execution: This active low input clears the end of execution output signal (END). If EACK is tied low, the END output will be a pulse that is one clock period wide.			
SVACK	4 GRE MAD TRANS		Service Request: This active low input clears the service request output (SVREQ).			
END	24° din NW 25 YOARA GEV 100	0 00 00 00 00 00 00 00 00 00 00 00 00 0	indicativiously can be is clear	This active low, open-drain output tes that execution of the pre- rentered command is complete. It used as an interrupt request and red by EACK, RESET or any read e access to the 8231.		

Symbol	Pin No.	Туре	Name and Function
SVREQ	5	0.	Service Request: This active high output signal indicates that command execution is complete and that post execution service was requested in the previous command byte. It is cleared by SVACK, the next command output to the device, or by RESET.
READY	17	.81 01 1	Ready: This active high output indicates that the 8231A is able to accept communication with the data bus. When an attempt is made to read data, write data or to enter a new command while the 8231A is executing a command, READY goes low until execution of the current command is complete (See READY Operation, p. 5).
DB0- DB7 s m s el (U	8- 15	I/O Sto InU or onits	Data Bus: These eight bidirectional lines provide for transfer of commands, status and data between the 8231A and the CPU. The 8231A can drive the data bus only when CS and RD are low.

#### COMMAND STRUCTURE

Each command entered into the 8231A consists of a single 8-bit byte having the format illustrated below:

SVREQ (R)	an actuacy to de lane			OPERATION			
	SINGLE	FIXED	havna	CODE	XO II	ante ma	Sanas
-	Parallel	o it gan	ondanu	DESCRIPTION OF THE PERSON OF T	200	dom en	PITISU I

Bits 0-4 select the operation to be performed as shown in the table. Bits 5-6 select the data format appropriate to the selected operation. If bit 5 is a 1, a fixed point data format is specified. If bit 5 is a 0, floating point format is specified. Bit 6 selects the precision of the data to be operated upon by fixed point commands only (if bit 5 = 0, bit 6 must be 0). If bit 6 is a 1, single-precision (16-bit) operands are assumed. If bit 6 is a 0, doubleprecision (32-bit) operands are indicated. Results are undefined for all illegal combinations of bits in the command byte. Bit 7 indicates whether a service request is to be issued after the command is executed. If bit 7 is a 1, the service request output (SVREQ) will go high at the conclusion of the command and will remain high until reset by a low level on the service acknowledge pin (SVACK) or until completion of execution of the succeeding command where service request (bit 7) is 0. Each command issued to the 8231A requests post execution service based upon the state of bit 7 in the command byte. When bit 7 is a 0, SVREQ remains low.

Figure 1. Slock Diagram



Table 2. 32-Bit Floating Point Instructions

Instruction of	mantissa value notification of and 1 multiple on a seprential to an appropriate power. This is express	Hex <sup>(1)</sup> Code	Stack Contents <sup>(2)</sup> After Execution A B C D	Status Flags <sup>(4)</sup> Affected
ACOS	Inverse Cosine of A	0 6	RUUU	S, Z, E
ASIN	Inverse Sine of A M = 90 EV	0 5	RUUU	S, Z, E
ATAN	Inverse Tangent of A	0 7	RBUU	S, Z
CHSF	Sign Change of A	1 5	RBCD	S, Z
cos	Cosine of A (radians)	0 3	R B U U	S, Z
EXP	e <sup>A</sup> Function	0 A	RBUU	S, Z, E
FADD	Add A and B	1 0	RCDU	S, Z, E
FDIV	Divide B by A	1 3	R C D U	S, Z, E
FLTD	32-Bit Integer to Floating Point Conversion	1 C	RBCU	S, Z
FLTS	16-Bit Integer to Floating Point Conversion	1 D	RBCU	S, Z
FMUL	Multiply A and B	1 2	SCISION FUND SORT FORMA	S, Z, E
FSUB	Subtract A from B	1,1	RCDU	S, Z, E
LOG	Common Logarithm (base 10) of A	0 8	RBUU	S, Z, E
LN	Natural Logarithm of A	0 9	R B U U	S, Z, E
POPF	Stack Pop	1 8	BCDA	S, Z
PTOF	Stack Push	1 7	AABC	S, Z
PUPI	Push π onto Stack	1 A	RABC	S, Z
PWR	BA Power Function	0 B	RCUU	S, Z, E
SIN	Sine of A (radians)	0 2	R B U U	S, Z
SQRT	Square Root of A	0 1 -8	R B C University	S, Z, E
TAN ORINO	Tangent of A (radians)	0 4 60	betsbomRioBolUoU am tant as	May S, Z, E at of
XCHF	Exchange A and B	1 9 9 10	alpaie tot TBT AC C D 887 SE - el	atenS, Z eacht lo

Table 3. 32-Bit Integer Instructions

Instruction	Description tweworks	Hex <sup>(1)</sup> Code	Stack Contents <sup>(2)</sup> After Execution B B C D	Status Flags <sup>(4)</sup> Affected
CHSD	Sign Change of A	3 04 229	dxa sanlar Bash copilw another	90 S, Z, O 00 80
DADD	Add A and B	2 C	RCDA	S, Z, C, E
DDIV	Divide B by A	2 F	RCDU	S, Z, E
DMUL	Multiply A and B (R = lower 32-bits)	2 E	RCDU	S, Z, O
DMUU	Multiply A and B (R = upper 32-bits)	3 6	RCDU	S, Z, O
DSUB	Subtract A from B	2 D	RCDA	S, Z, C, O
FIXD	Floating Point to Integer Conversion	1 E	R B C U	S, Z, O
POPD	Stack Pop	3 8	B C D A	S, Z
PTOD	Stack Push sa ant of analysis sand part	3 7	nothod-et A A B C STOVA	S, Z snoime
XCHD	Exchange A and B	3 9	B A C D	ada is cost at a

Table 4. 16-Bit Integer Instructions

Instruction	precision fixed point of floating point allows may be stored a stack in these	Hex <sup>(1)</sup> Code	Stack Contents <sup>(3)</sup> After Execution A <sub>U</sub> A <sub>L</sub> B <sub>U</sub> B <sub>L</sub> C <sub>U</sub> C <sub>L</sub> D <sub>U</sub> D <sub>L</sub>	Status Flags <sup>(4)</sup> Affected
CHSS	Change Sign of A <sub>U</sub>	7 4 0 0	R AL BU BL CU CL DU DL	S, Z, O 8 000
FIXS	Floating Point to Integer Conversion	1 PELLS	R BU BL CU CL U U U	S, Z, O 90110
POPS	Stack Pop	7 8	AL BU BL CU CL DU DL AU	S, Z
PTOS	Stack Push	7 7	AU AU AL BU BL CU CL DU	S, Z
SADD	Add A <sub>U</sub> and A <sub>L</sub>	6 C	R BU BL CU CL DU DL AU	S, Z, C, E
SDIV	Divide A <sub>L</sub> by A <sub>U</sub>	6 F	R BU BL CU CL DU DL U	S, Z, E
SMUL	Multiply A <sub>L</sub> by A <sub>U</sub> (R = lower 16-bits)	6 E	R BU BL CU CL DU DL U	S, Z, E
SMUU	Multiply A <sub>L</sub> by A <sub>U</sub> (R = upper 16-bits)	7 6	R BU BL CU CL DU DL U	S, Z, E
SSUB	Subtract A <sub>U</sub> from A <sub>L</sub>	6 D	R BU BL CU CL DU DL AU	S, Z, C, E
XCHS	Exchange A <sub>U</sub> and A <sub>L</sub>	7 9 9 9 8 9	AL AU BU BL CU CL DU DL	m nS, Ziebisoalt
NOP 18 81	No Operation and ofno netting are stad	0 10 880	AU AL BU BL CU CL DU DL	ange of values

Notes: 1. In the hex code column, SVREQ is a 0.

2. The stack initially is composed of four 32-bit numbers (A, B, C, D). A is equivalent to Top Of Stack (TOS) and B is Next On Stack (NOS). Upon completion of a command the stack is composed of: the result (R); undefined (U); or the initial contents (A, B, C, or D).

3. The stack initially is composed of eight 16-bit numbers (A<sub>U</sub>, A<sub>L</sub>, B<sub>U</sub>, B<sub>L</sub>, C<sub>U</sub>, C<sub>L</sub>, D<sub>U</sub>, D<sub>L</sub>). A<sub>U</sub> is the TOS and A<sub>L</sub> is NOS. Upon completion of a command the stack is composed of: the result (R); undefined (U); or the initial contents (A<sub>U</sub>, A<sub>L</sub>, B<sub>U</sub>, B<sub>L</sub>, . . .).

4. Nomenclature: Sign (S); Zero (Z); Overflow (O); Carry (C); Error Code Field (E).



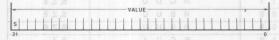
# DATA FORMATS

The 8231A arithmetic processing unit handles operands in both fixed point and floating point formats. Fixed point operands may be represented in either single (16-bit operands) or double precision (32-bit operands), and are always represented as binary, two's complement values.

# SINGLE PRECISION FIXED POINT FORMAT



# DOUBLE PRECISION FIXED POINT FORMAT



The sign (positive or negative) of the operand is located in the most significant bit (MSB). Positive values are represented by a sign bit of zero (S = 0). Negative values are represented by the two's complement of the corresponding positive value with a sign bit equal to 1 (S = 1). The range of values that may be accommodated by each of these formats is  $-32,768\ to +32,767\ for\ single\ precision and <math display="inline">-2,147,483,648\ to +2,147,483,647\ for\ double\ precision.$ 

Floating point binary values are represented in a format that permits arithmetic to be performed in a fashion analogous to operations with decimal values expressed in scientific notation.

$$(5.83 \times 10^2) (8.16 \times 10^1) = (4.75728 \times 10^4)$$

In the decimal system, data may be expressed as values between 0 and 10 times 10 raised to a power that effectively shifts the implied decimal point right or left the number of places necessary to express the result in conventional form (e.g., 47,572.8). The value-portion of the data is called the mantissa. The exponent may be either negative or positive.

The concept of floating point notation has both a gain and a loss associated with it. The gain is the ability to represent the significant digits of data with values spanning a large dynamic range limited only by the capacity of the exponent field. For example, in decimal notation if the exponent field is two digits wide, and the mantissa is five digits, a range of values (positive or negative) from  $1.0000 \times 10^{-99}$  to  $9.9999 \times 10^{+99}$  can be accommodated. The loss is that only the significant digits of the value can be represented. Thus there is no distinction in this representation between the values 123451 and 123452, for example, since each would be expressed as: 1.2345 x 105. The sixth digit has been discarded. In most applications where the dynamic range of values to be represented is large, the loss of significance, and hence accuracy of results, is a minor consideration. For greater precision a fixed point format could be chosen, although with a loss of potential dynamic range.

The 8231A is a binary arithmetic processor and requires that floating point data be represented by a fractional mantissa value between .5 and 1 multiplied by 2 raised to an appropriate power. This is expressed as follows:

For example, the value 100.5 expressed in this form is  $0.1100\ 1001 \times 2^7$ . The decimal equivalent of this value may be computed by summing the components (powers of two) of the mantissa and then multiplying by the exponent as shown below:

value = 
$$(2^{-1} + 2^{-2} + 2^{-5} + 2^{-8}) \times 2^7$$
  
=  $0.5 + 0.25 + 0.03125 + 0.00290625) \times 128$   
=  $0.78515625 \times 128$   
=  $100.5$ 

# FLOATING POINT FORMAT

The format for floating point values in the 8231A is given below. The mantissa is expressed as a 24-bit (fractional) value; the exponent is expressed as a two's complement 7-bit value having a range of -64 to +63. The most significant bit is the sign of the mantissa (0 = positive, 1 = negative), for a total of 32 bits. The binary point is assumed to be to the left of the most significant mantissa bit (bit 23). All floating point data values must be normalized. Bit 23 must be equal to 1, except for the value zero, which is represented by all zeros.

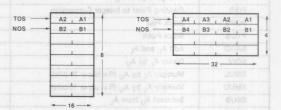


The range of values that can be represented in this format is  $\pm (2.7 \times 10^{-20} \text{ to } 9.2 \times 10^{18})$  and zero.

# **FUNCTIONAL DESCRIPTION**

#### STACK CONTROL

The user interface to the 8231A includes access to an 8 level 16-bit wide data stack. Since single precision fixed point operands are 16-bits in length, eight such values may be maintained in the stack. When using double precision fixed point or floating point formats four values may be stored. The stack in these two configurations can be visualized as shown below:



Data are written onto the stack, eight bits at a time, in the order shown (A1, A2, A3, ...). Data are removed from the stack in reverse byte order (A4, A3, A2...). Data should be entered onto the stack in multiples of the number of bytes appropriate to the chosen data format.



# cution, these times will be heavily influYRTMA ATAC

Data entry is accomplished by bringing the chip select  $(\overline{CS})$ , the command/data line  $(A_0)$ , and  $\overline{WR}$  low, as shown in the timing diagram. The entry of each new data word "pushes down" the previously entered data and places the new byte on the top of stack (TOS). Data on the bottom of the stack prior to a stack entry are lost.

#### DATA REMOVAL

Data are removed from the stack in the 8231A by bringing chip select  $(\overline{CS})$ , command/data  $(A_0)$ , and  $\overline{RD}$  low as shown in the timing diagram. The removal of each data word redefines TOS so that the next successive byte to be removed becomes TOS. Data removed from the stack rotates to the bottom of the stack.

### **COMMAND ENTRY**

After the appropriate number of bytes of data have been entered onto the stack, a command may be issued to perform an operation on that data. Commands which require two operands for execution (e.g., add) operate on the TOS and NOS values. Single operand commands operate only on the TOS.

Commands are issued to the 8231A by bringing the chip select  $(\overline{CS})$  line low, command data  $(A_0)$  line high, and  $\overline{WR}$  line low as indicated by the timing diagram. After a command is issued, the CPU can continue execution of its program concurrently with the 8231A command execution.

# COMMAND COMPLETION

The 8231A signals the completion of each command execution by lowering the End Execution line (END). Simultaneously, the busy bit in the status register is cleared and the Service Request bit of the command register is checked. If it is a "1" the service request output level (SVREQ) is raised. END is cleared on receipt of an active low End Acknowledge (EACK) pulse. Similarly, the service request line is cleared by recognition of an active low Service Acknowledge (SVACK) pulse.

#### **READY OPERATION**

An active high ready (READY) is provided. This line is high in its quiescent state and is pulled low by the 8231A under the following conditions:

- A previously initiated operation is in progress (device busy) and Command Entry has been attempted. In this case, the READY line will be pulled low and remain low until completion of the current command execution. It will then go high, permitting entry of the new command.
- A previously initiated operation is in progress and stack access has been attempted. In this case, the READY line will be pulled low, will remain in that state until execution is complete, and will then be raised to permit completion of the stack access.
- 3. The 8231A is not busy, and data removal has been requested. READY will be pulled low for the length of time necessary to transfer the byte from the top of stack to the interface latch, and will then go high, indicating availability of the data.

- 4. The 8231A is not busy, and a data entry has been requested. READY will be pulled low for the length of time required to ascertain if the preceding data byte, if any, has been written to the stack. If so READY will immediately go high. If not, READY will remain low until the interface latch is free and will then go high.
- 5. When a status read has been requested, READY will be pulled low for the length of time necessary to transfer the status to the interface latch, and will then be raised to permit completion of the status read. Status may be read whether or not the 8231A is busy.

When READY goes low, the APU expects the bus control signals present at the time to remain stable until READY goes high.

# **DEVICE STATUS**

Device status is provided by means of an internal status register whose format is shown below:



BUSY: Indicates that 8231A is currently executing a command (1=Busy)

SIGN: Indicates that the value on the top of stack is negative (1 = Negative)

ZERO: Indicates that the value on the top of stack is zero (1 = Value is zero)

ERROR CODE: This field contains an indication of the validity of the result of the last operation. The error codes are:

(A) 0000 — No error, A 4 8 X A 4 8 X A 4 X A 4 A A = (X)

1000 - Divide by zero

0100 — Square root or log of negative number

1100 — Argument of inverse sine, cosine, or e<sup>x</sup> too large

MOXX10 - Underflow a dilW Jiame et |X| nodw Ilame

Vne XX01 - Overflow sham at not fud high none ent

CARRY: Previous operation resulted in carry or borrow from most significant bit. (1 = Carry/Borrow, 0 = No Carry/No Borrow.)

If the BUSY bit in the status register is a one, the other status bits are not defined; if zero, indicating not busy, the operation is complete and the other status bits are defined as given above.

### **READ STATUS**

The 8231A status register can be read by the CPU at any time (whether an operation is in progress or not) by bringing the chip select  $\overline{(CS)}$  low, the command/data line  $(A_0)$  high, and lowering  $\overline{RD}$ . The status register is then gated onto the data bus and may be input by the CPU.

# **EXECUTION TIMES**

Timing for execution of the 8231A command set is contained below. All times are given in terms of clock cycles. Where substantial variation of execution times



is possible, the minimum and maximum values are quoted; otherwise, typical values are given. Variations are data dependent.

Total execution times may require allowances for operand transfer into the APU, command execution, and result retrieval from the APU. Except for command exe-

cution, these times will be heavily influenced by the nature of the data, the control interface used, the speed of memory, the CPU used, the priority allotted to DMA and Interrupt operations, the size and number of operands to be transferred, and the use of chained calculations, etc.

euista ent to noiteigmoo timeg of Table 5. Command Execution Times

Command Mnemonic	Clock Cycles	Command Mnemonic	Clock Cycles	Command Mnemonic	Clock Cycles	Command Mnemonic	Clock
SADD	ner d7smit	FADD	54-368	LN	4298-6956	POPF	12
SSUB	30	FSUB	70-370	EXP	3794-4878	XCHS	18
SMUL	84-94 80-98	FMUL	146-168	PWR	8290-12032	XCHD	26
SDIV	84-94	FDIV SUT	154-184	NOP	4	XCHF	26
DADD	21	SORT	800	CHSS	st to 2823 To 18	dmuPUPIngoto	gs e16101
DSUB	38	SIN	4464	CHSD	vem 027 mos	o the stack, a	ino bened
DMUL	194-210	cos	4118	CHSF	ammo 18 tsb tr	operation on the	ns mroh
DMUU	182-218			no estate on	oution (e.g., add	perands for exe	o owi eni
DDIV	208	TAN	5754	PTOS	Sing 81 operand	d NOS values.	e TOS an
FIXS	92-216	ASIN	7668	PTOD	20	on the TOS.	ino siste
FIXD	100-346	ACOS	7734	PTOF	20 000	at at hauppi one	ahaamm
FLTS	98-186	ATAN	6006	POPS	10	evenon wat anii	15751 sool
FLTD	98-378	LOG	4474-7132	POPD	12	THE PART OF THE	(OO) IOHI

# DERIVED FUNCTION DISCUSSION DELICARIO

Computer approximations of transcendental functions are often based on some form of polynomial equation, such as:

$$F(X) = A_0 + A_1X + A_2X^2 + A_3X^3 + A_4X^4 + \cdots$$
 (1-1)

The primary shortcoming of an approximation in this form is that it typically exhibits very large errors when the magnitude of |X| is large, although the errors are small when |X| is small. With polynomials in this form, the error distribution is markedly uneven over any arbitrary interval.

A set of approximating functions exists that not only minimizes the maximum error but also provides an even distribution of errors within the selected data representation interval. These are known as Chebyshev Polynomials and are are based upon cosine functions. These functions are defined as follows:

$$T_n(X) = \cos n\theta$$
; where  $n = 0,1,2...$  (1-2  $\theta = \cos^{-1}X$ 

The various terms of the Chebyshev series can be computed as shown below:

$$T_0(X) = Cos(0 \cdot \theta) = Cos(0) = 1$$
 (1-4)  
 $T_1(X) = Cos(Cos^{-1}X) = X$  (1-5)

$$T_2(X) = \cos 2\theta = 2\cos^2 \theta - 1 = 2\cos^2(\cos^{-1}X) - 1$$
 (1-6)  
=  $2X^2 - 1$ 

In general, the next term in the Chebyshev series can be recursively derived from the previous term as follows:

$$T_n(X) = 2X [T_n - 1(X)] - T_n - 2(X); n \ge 2\pi i$$
 visuoenati (1-7) bnammoo adi to iid iseupen soivie2 adi bna berselo

Common logarithms are computed by multiplication of the natural logarithm by the conversion factor 0.43429448 and the error function is therefore the same as that for natural logarithm. The power function is realized by combination of natural log and exponential functions according to the equation:

$$X^{Y} = e^{yLnx}$$
.

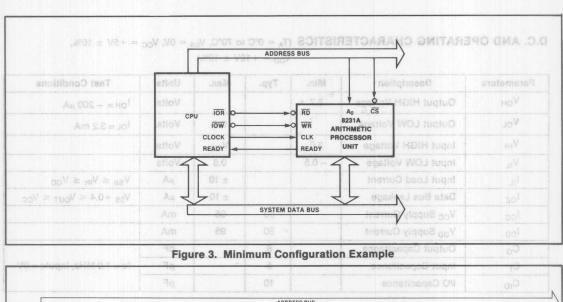
The error for the power function is a combination of that for the logarithm and exponential functions.

Each of the derived functions is an approximation of the true function. Thus the result of a derived function will have an error. The absolute error is the difference between the function's result and the true result. A more useful measure of the function's error is relative error (absolute error/true result). This gives a measurement of the significant digits of algorithm accuracy. For the derived functions except LN, LOG, and PWR the relative error is typically  $4\times 10^{-7}.$  For PWR the relative error is the summation of the EXP and LN errors,  $7\times 10^{-7}.$  For LN and LOG, the absolute error is  $2\times 10^{-7}.$ 

tions for the APU with operand transfers handled by an 8237 DMA controller, and CPU coordination handled by an Interrupt Controller. The APU interrupts the CPU to indicate that a command has been completed. When the performance enhancements provided by the DMA and Interrupt operations are not required, the APU interface

any general 8-bit processor.

In many systems it will be convenient to use the microcomputer system clock to drive the APU clock input. In the case of 8080A systems it would be the \$\phi2TTL\$ signal. Its cycle time will usually fall in the range of 250 ns to 1000 ns, depending on the system speed.



ADDRESS BUS A8-A15 8205 DECODER A0-A7 STB 8282 8237 DMA CONTROLLER HLD/ HI DA HOLD CLOCK MEME MEMW IOF IOW READY O Vcc CS WR BD END 8259A 8231A ARITHMETIC EACK PROCESSOR UNIT SYSTEM DATA BUS

Figure 4. High Performance Configuration Example



# ABSOLUTE MAXIMUM RATINGS\*

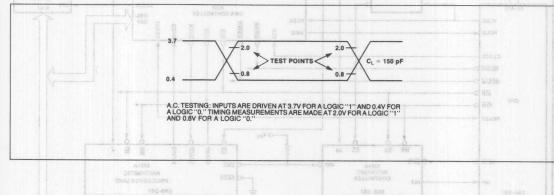
Storage Temperature	-65°C to +150°C
Ambient Temperature Under Bias	0°C to 70°C
V <sub>DD</sub> with Respect to V <sub>SS</sub>	
V <sub>CC</sub> with Respect to V <sub>SS</sub>	
All Signal Voltages with Respect	microcomputer sy
anto V <sub>SS</sub> ucw.V.sme.zvz.ADADA.to.	0.5V to $+7.0V$
Power Dissipation	

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

# D.C. AND OPERATING CHARACTERISTICS ( $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$ , $V_{SS} = 0\text{V}$ , $V_{CC} = +5\text{V} \pm 10\%$ , $V_{DD} = +12\text{V} \pm 10\%$ )

Parameters	Description	Min.	Тур.	Max.	Units	Test Conditions
V <sub>OH</sub>	Output HIGH Voltage	3.7			Volts	I <sub>OH</sub> = - 200 μA
V <sub>OL</sub>	Output LOW Voltage	RA W		0.4	Volts	I <sub>OL</sub> = 3.2 mA
V <sub>IH</sub>	Input HIGH Voltage	2.0		V <sub>CC</sub>	Volts	
VIL	Input LOW Voltage	- 0.5		0.8	Volts	
I <sub>IL</sub>	Input Load Current			± 10	μА	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
loz	Data Bus Leakage	7		± 10	μА	V <sub>SS</sub> +0.4 ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>
Icc	V <sub>CC</sub> Supply Current	RUB ATA	50	95	mA	
I <sub>DD</sub>	V <sub>DD</sub> Supply Current		50	95	mA	
Co	Output Capacitance	noitemento	8	IniM E ar	pF	
Cı	Input Capacitance		5		pF	fc = 1.0 MHz, Inputs = 0V
C <sub>IO</sub>	I/O Capacitance		10		pF	







**A.C. CHARACTERISTICS**  $(T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}, V_{SS} = 0\text{V}, V_{CC} = +5\text{V} \pm 10\%, V_{DD} = +12\text{V} \pm 10\%)$ 

#### **READ OPERATION**

Symbol	Parameter		8231	A-8	823	1A-3	823	1A	Units
-,			Min.	Max.	Min.	Max.	Min.	Max.	
taR	A <sub>0</sub> , CS Setup to RD	-	0	- Interested	0	/e	0		ns
t <sub>RA</sub>	A <sub>0</sub> , CS Hold from RD		0	4	0/	+	0		ns
t <sub>RY</sub>	READY ↓ from RD ↓ Delay (No	ote 2)	topt -==	150	H	100		100	ns
tyR	READY † to RD †		0		0	X	0 85,	A	ns
terr	READY Pulse Width (Note 3)	Data	3.5 t <sub>CY</sub> + 50		3.5 t <sub>CY</sub> + 50		3.5 t <sub>CY</sub> + 50		ns
чнн	TIEAD I False Width (Note 5)	Status	1.5 t <sub>CY</sub> + 50		1.5 t <sub>CY</sub> + 50		1.5 t <sub>CY</sub> + 50		ns
tRDE	Data Bus Enable from RD ↓		50	4	50	e comment of	50		ns
t <sub>DRY</sub>	Data Valid to READY †	1	0	7	0		O YGA	Я	ns
t <sub>DF</sub>	Data Float after RD †		50	200	50	150	50	100	ns

# WRITE OPERATION

Symbol	Parameter		8231	A-8	823	1A-3	823	1A	Units
,			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>AW</sub>	A <sub>0</sub> , CS Setup to WR		0	6	0		0 140	PERATI	o ans
t <sub>WA</sub>	A <sub>0</sub> , $\overline{\text{CS}}$ Hold after $\overline{\text{WR}}$		60		30		25		ns
t <sub>WY</sub>	READY ↓ from WR ↓ Delay (Note 2)			150		100		100	ns
t <sub>YW</sub>	READY † to WR †		0		0		0		ns
t <sub>RRW</sub>	READY Pulse Width (Note 4)			50		50	A	50	ns
twi	Write Inactive Time (Note 4)	Command	4 t <sub>CY</sub>		4 t <sub>CY</sub>	~~ WaJ	4 t <sub>CY</sub>		ns
-441	With machine time (Note 4)	Data	5 t <sub>CY</sub>		5 t <sub>CY</sub>	/	5 t <sub>CY</sub>		ns
t <sub>DW</sub>	Data Setup to WR		150	wast	100		100		ns
twp	Data Hold after WR		20		20		20		ns

# OTHER TIMINGS

Symbol	Parameter Jusara	8231A-8		82	31A-3	A 8231A		Units
		Min.	Max.	Min.	Max.	Min.	Max.	- Oillito
tcy	Clock Period	480	5000	320	3300	250	2500	ns
t <sub>CPH</sub>	Clock Pulse High Width	200		140		100		ns
tCPL	Clock Pulse Low Width	240 .		160		120	190 79	ns
t <sub>EE</sub>	END Pulse Width (Note 5)	400		300		200		ns
t <sub>EAE</sub>	EACK ↓ to END ↑ Delay		200		175		150	ns
t <sub>AA</sub>	EACK Pulse Width	100	3	75		50		ns
tsa	SVACK ↓ to SVREQ ↓ Delay	1	300		200	END	150	ns
tss	SVACK Pulse Width	100	- BY33	75		50		ns

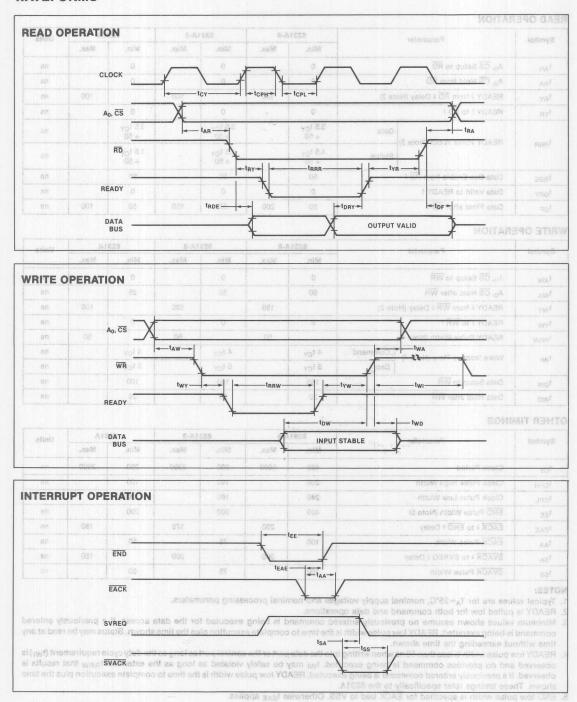
#### NOTES

- 1. Typical values are for T<sub>A</sub>=25°C, nominal supply voltages and nominal processing parameters.
- 2. READY is pulled low for both command and data operations.
- Minimum values shown assume no previously entered command is being executed for the data access. If a previously entered command is being executed, READY low pulse width is the time to complete execution plus the time shown. Status may be read at any time without exceeding the time shown.
- 4. READY low pulse width is less than 50 ns when writing into the data port or the control port as long as the duty cycle requirement (t<sub>WI</sub>) is observed and no previous command is being executed. t<sub>WI</sub> may be safely violated as long as the extended t<sub>RRW</sub> that results is observed. If a previously entered command is being executed, READY low pulse width is the time to complete execution plus the time shown. These timings refer specifically to the 8231A.
- 5. END low pulse width is specified for EACK tied to VSS. Otherwise teae applies.

EACK



# **WAVEFORMS**





# FLOATING POINT PROCESSING UNIT

- Compatible with Proposed IEEE Format and Existing Intel Floating Point Standard
- Single (32-Bit) and Double (64-Bit)
   Precision Capability
- Add, Subtract, Multiply and Divide Functions
- Stack Oriented Operand Storage
- General Purpose 8-Bit Data Bus Interface

- Standard 24-Pin Package
- 12V and 5V Power Supplies
- Compatible with MCS-80<sup>TM</sup>, MCS-85<sup>TM</sup> and MCS-86<sup>TM</sup> Microprocessor Families
- Error Interrupt
- Direct Memory Access or Programmed
   I/O Data Transfers
- End of Execution Signal
- Advanced N-Channel Silicon Gate HMOS Technology

The Intel® 8232 is a high performance floating-point processor unit (FPU). It provides single precision (32-bit) and double precision (64-bit) add, subtract, multiply and divide operations. The 8232's floating point arithmetic is a subset of the proposed IEEE standard. It can be easily interfaced to enhance the computational capabilities of the host microprocessor.

The operand, result, status and command information transfers take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack by the host processor and a command is issued to perform an operation on the data stack. The results of the operation are available to the host processor from the stack.

Information transfers between the 8232 and the host processor can be handled by using programmed I/O or direct memory access techniques. After completing an operation, the 8232 activates an "end of execution" signal that can be used to interrupt the host processor.

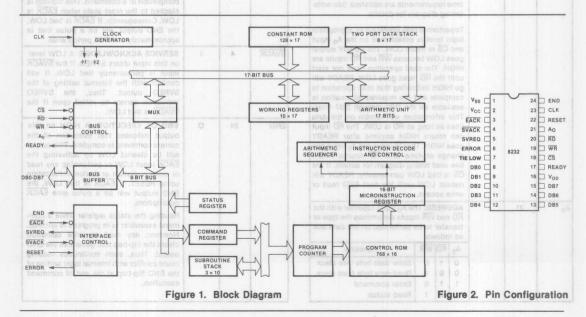




Table 1. Pin Description

Symbol	Pin No.	Туре	2 10	0.0	Nar	ne and Description		
V <sub>CC</sub>	2		PO	NER	SUF	PLY: +5V power supply		
V <sub>DD</sub>	16		PO	WEF	SUF	PLY: +12V power supply		
V <sub>SS</sub>	1		GROUND					
CLK	23	160 M . M	CLOCK: An external timing source cornected to the CLK input provides the necessary clocking.					
RESET	22	esbai ar Pro	initi tion regi is ir may out; out; tion CLK	in ster nitia be out, out , RE	programmer to zero dized affer the E will be SET eriod	GH level on this input causes Reset terminates any opera- ress, and clears the status or on the status or on the internal stack pointer and the contents of the stack cted. After a reset the END RROR output and the SVREQ be LOW. For proper initializamust be HIGH for at least five s following stable power ges and stable clock.		
CS	18	nosi		plis	h an	T: input must be LOW to ac- y read or write operation to		
	1 (32-b to is a s s of the cation ration tiO or	rithmet abilitier onat da ran ope ammed	data line put ever CS actunti writt sitio will tion put The put time	a is s, a and r WF is L ual will Will will will will will will wil	pres pprop the C and OW, writin R is n perati n the HIGH s bee go H a line quirer	write operation, appropriate ented on DB0 through DB7 rirate logic level on the A <sub>0</sub> in: Si input is made LOW. When-RD inputs are both HIGH and READY goes LOW. However, g into the 8232 cannot start nade LOW. After initiating the on by the HIGH to LOW tran-WR input, the READY output, indicating the write operan acknowledged. The WR in-IGH after READY goes HIGH. s, the A <sub>0</sub> input and the CS innege when appropriate hold nents are satisfied. See write am for details.		
CHO CONTROL CO	05 05 05 05 05 05 05 05 05 05 05 05 05 0	1   apt   1   apt   2   ap	logiand goes HIG unti go h com avai This can goes chair See CS rem	C le CS S LC CS LC CS S LC CS LC CS S LC CS LC	vel is is made in the received in the analytic and anytic anytic district and the anytic anytic district and the anytic district and the anytic anyti	read operation an appropriate established on the A <sub>0</sub> input date LOW. The READY output scause WR and RD inputs are ad operation does not start input goes LOW. READY will ideating that read operation is d the required information is the DB0 through DB7 lines. It ion will remain on the data as RD is LOW. The RD input HIGH anytime after READY him after READY in eather RD returns HIGH. Ing diagram for details. If the DW permanently, READY will until the next 8232 read or until the read as 200 custom and a control of the READY will until the next 8232 read or control of the READY will u		
A <sub>0</sub>	21	- 1 - sec	RD	and sfer	WR i	he A <sub>0</sub> input together with the nputs determines the type of e performed on the data bus		
			A <sub>0</sub>		WR	Function		
			0	1	0	Enter data byte into stack		
			0	0	1_0	Read data byte from stack Enter command		

Symbol	Pin No.	Туре	Name and Description
RD	20	1	READ: A LOW level on this input is used to read information from an internal
	FI 38	Bl ba	location and gate that information onto
	09 p	niteol	the data bus. The CS input must be LOW
	0.1.6	11110001	to accomplish the read operation. The Acinput determines what internal location is
			to be read. See A <sub>0</sub> , CS input descriptions and read timing diagram for details. If the
	BID	08) el	END output was HIGH, performing any read operation will make the END output go LOW after the HIGH to LOW transition of the RD input (assuming CS is LOW). If
	ebivi	g bas	the ERROR output was HIGH, performing a status register read operation will make the ERROR output LOW. This will happen after the HIGH to LOW transition of the
	6100	maia	RD input (assuming CS is LOW).
WR -161	19	eta B	WRITE: A LOW level on this input is used to transfer information from the data bus into an internal location. The CS must be
			LOW to accomplish the write operation.  A <sub>0</sub> determines which internal location is to be written. See A <sub>0</sub> , $\overline{\text{CS}}$ input descriptions and write timing diagram for details.
		off some	
		ict, mul can be	any write operation will make the END output go LOW after the LOW to HIGH transition of the WR input (assuming CS is LOW).
ni nolis	mioln	brismit	he operand, result, status and co-
EACK		acidby	END ACKNOWLEDGE: When LOW,
			makes the END output go LOW. As men- tioned earlier, HIGH on the END output signals completion of a command exe-
	១៩ ខ្លួក	enplet esor.	cution. The END signal is derived from an internal flip-flop which is clocked at the completion of a command. This flip-flop is clocked to the reset state when EACK is LOW. Consequently, if EACK is tied LOW,
CONST			the END output will be a pulse that is approximately one CLK period wide.
SVACK	4	1	SERVICE ACKNOWLEDGE: A LOW level on this input clears SVREQ. If the SVACK input is permanently tied LOW, it will conflict with the internal setting of the SVREQ output. Thus, the SVREQ indication cannot be relied upon if
NACERCINIS			SVACK is tied LOW.
END	24	O STATE	END OF EXECUTION: A HIGH on this output indicates that execution of the current command is complete. This output will be cleared LOW by activating the EACK input LOW or performing any read or write operation or device initialization using RESET. If EACK is tied LOW, the END output will be a pulse (see EACK description)
	83	Teloge L.	description).  Reading the status register while a com-
Ma	- GH	AMAIGO NECIST	mand execution is in progress is allowed. However, any read or write operation clears the flip-flop that generates the END
1			oldars the hip hop that generates the Live
1 8		Worldist DATS RX.4	output. Thus, such continuous reading could conflict with internal logic setting of the END flip-flop at the end of command execution.



Table 1. Pin Description (Continued) Table 1. Pin Description (Continued)

Symbol	Pin No.	Туре	Name and Description
SVREQ	5	0	SERVICE REQUEST: A HIGH on this out- put indicates completion of a command.
		11000	In this sense this output is the same as the
ernse si		noitsteo	END output. However, the SVREQ output will go HIGH at the completion of a
		10W 199	command only when the Service Request
		swis at	Enable bit was set to 1. The SVREQ can be
	ni jii		cleared (i.e., go LOW) by activating the SVACK input LOW or initializing the
	aeel x	the star	device using the RESET. Also, the SVREQ will be automatically cleared after completion of any command that has the
	set. The	it byte li	service request bit as 0.
ERROR	ildafes	el o o	ERROR: Output goes HIGH to indicate that the current command execution resulted in an error condition. The error conditions are: attempt to divide by zero, exponent
larif vili	1000 00	tugni o	overflow and exponent underflow. The ERROR output is cleared LOW on a status
	rouge on	Sharata Di	register read operation or upon RESET.
			The ERROR output is derived from the error bits in the status register. These
		Nevertel lw Judit	error bits will be updated internally at an
		nobed f	appropriate time during a command exe- cution. Thus, ERROR output going HIGH
	ing dia	mii eez)	may not coincide with the completion of a command. Reading of the status register can be performed while a command exe-
	muier	Hw YO	cution is in progress. However, it should
		asri no	be noted that reading the status register clears the ERRQR output. Thus, reading
			the status register while a command
	ман	Beop Jud	execution is in progress may result in an
			internal conflict with the ERROR output.
		etshao	inputs can change after app
		b galmi	quirements are satisfied (see
	15a 115a	n holes	The above procedure must be rep
			the operand are pushed into
			noted that for single precision or
			be pushed and 8 byles must be
	w ytity	sup a to	cision. Not pushing all the bytes in byte pointer misalignment.
			The 8232 stack can accommodal quantities or two double prepriate

Symbol	Pin No.	Туре	Name and Description
	o State lise and particular state lise and state li	ksek ar Registe Abroutin Abroutin Abroutin Abroutin Aberuteo Abrahou es variou es acve process arolled Abrouled	READY: Output is a handshake signal used while performing read or write transactions with the 8232. If the WR and RE inputs are both HIGH, the READY output goes LOW with the CS input in anticipation of a transaction. If WR goes LOW to initiate a write transaction with propesignals established on the DBO-DB7, A inputs, the READY will return HIGH-indicating that the write operation has been accomplished. The WR can be made HIGH after this event. On the other hand, it aread operation is desired, the READY will go LOW and establishing proper Ao input. (The READ) will go LOW in response to CS going LOW). The READY will return HIGH indicating completion of read. The RD car return HIGH after this event. It should be noted that a read or write operation can be initiated without any regard to whether a command execution is in progress or not Proper device operation is assured by obeying the READY output indications.
DB0- DB7	8-15	1/0	DATA BUS: Bidirectional lines are used to transfer command, status and operand
		the leas	information between the device and the host processor. DB0 is the least signifi- cant and DB7 is the most significant bi- position. HIGH on a data bus line corre
	1 epiva	a the Sa	sponds to 1 and LOW corresponds to 0.
	rvice fi is to g s: sint	s the Se SVREO nd. stegoric	sponds to 1 and LOW corresponds to 0. When pushing operands on the stack using the data bus, the least significant byte must be pushed first and the most significant byte last. When popping the
	pnia :e	s the Se SVREQ nd. stegonic in arithmetic o	sponds to 1 and LOW corresponds to 0.  When pushing operands on the stack using the data bus, the least significant byte must be pushed first and the most
Halfi c	pnia :e	s the Se SVREQ at appoint a arithr metto d islon (3) mbers:	sponds to 1 and LOW corresponds to 0.  When pushing operands on the stack using the data bus, the least significant byte must be pushed first and the most significant byte last. When popping the stack to read the result of an operation, the most significant byte will be available on the data bus first and the least significant byte will be the last. Moreover, for pushing operands and popping results the number of transactions must be equal
Halfi c	pnia :e	the Se (vd. Service) where the service contract of the service contract of the service of the service of Service contract of the service contract of t	sponds to 1 and LOW corresponds to 0.  When pushing operands on the stack using the data bus, the least significant byte must be pushed first and the most significant byte last. When popping the stack to read the result of an operation, the most significant byte will be available on the data bus first and the least significant byte will be the last. Moreover, for pushing operands and popping results.

# FUNCTIONAL DESCRIPTION

Major functional units of the 8232 are shown in the block diagram. The 8232 employs a microprogram controlled stack oriented architecture with 17-bit wide data paths.

The Arithmetic Unit receives one of its operands from the Operand Stack. This stack is an eight word by 17-bit two port memory with last in-first out (LIFO) attributes. The second operand to the Arithmetic Unit is supplied by the internal 17-bit bus. In addition to supplying the second operand, this bidirectional bus also carries the results from the output of the Arithmetic Unit when required. Writing into the Operand Stack takes place

from this internal 17-bit bus when required. Also connected to this bus are the Constant ROM and Working Registers. The ROM provides the required constants to perform the mathematical operations while the Working Registers provide storage for the intermediate values during command execution.

Communication between the external world and the 8232 takes place on eight bidirectional input/output lines, DB0 through DB7 (Data Bus). These signals are gated to the internal 8-bit bus through appropriate interface and buffer circuitry. Multiplexing facilities exist for bidirectional communication between the internal eight



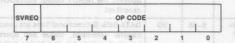
and 17-bit buses. The Status Register and Command and Register are also located on the 8-bit bus.

The 8232 operations are controlled by the microprogram contained in the Control ROM. The Program Counter supplies the microprogram addresses and can be partially loaded from the Command Register. Associated with the Program Counter is the Subroutine Stack where return addresses are held during subroutine calls in the microprogram. The Microinstruction Register holds the current microinstruction being executed. The register facilitates pipelined microprogram execution. The Instruction Decode logic generates various internal control signals needed for the 8232 operation.

The Interface Control logic receives several external inputs and provides handshake related outputs to facilitate interfacing the 8232 to microprocessors.

# **Command Format**

The operation of the 8232 is controlled from the host processor by issuing instructions called commands. The command format is shown below.



The command consists of 8 bits; the least significant 7 bits specify the operation to be performed as detailed in Table 1. The most significant bit is the Service Request Enable bit. This bit must be a 1 if SVREQ is to go HIGH at the end of executing a command.

The commands fall into three categories: single precision arithmetic, double precision arithmetic and data manipulation. There are four arithmetic operations that can be performed with single precision (32-bit) or double precision (64-bit) floating-point numbers; add, subtract. multiply and divide. These operations require two operands. The 8232 assumes that these operands are located in the internal stack as Top of Stack (TOS) and Next on Stack (NOS). The result will always be returned to the previous NOS which becomes the new TOS. Results from an operation are of the same precision and format as the operands. The results will be rounded to preserve the accuracy. The actual data formats and rounding procedures are described in a later section. In addition to the arithmetic operations, the 8232 implements eight data manipulating operations. These include changing the sign of a double or single precision operand located in TOS, exchanging single precision operands located at TOS and NOS, as well as pushing and popping single or double precision operands. See also the sections on status register and operand formats.

The execution times of the commands are all data dependent. Table 3 shows one example of each command execution time.

# **Operand Entry**

The 8232 commands operate on the operands located at the TOS and NOS. Results are returned to the stack at NOS and then popped to TOS. The operands required for the 8232 are one of two formats — single precision floating-point (4 bytes) or double precision floating-point (8 bytes). The result of an operation has the same format as the operands. In other words, operations using single precision quantities always result in a single precision result, while operations involving double precision quantities will result in double precision result.

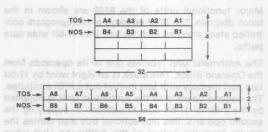
Operands are always entered into the stack least significant byte first and most significant byte last. The following procedure must be followed to enter operands into the stack:

- 1. The lower significant operand byte is established on the DB0-DB7 lines.
- A LOW is established on the A<sub>0</sub> input to specify that data is to be entered into the stack.
- The CS input is made LOW. Whenever the WR and RD inputs are HIGH, the READY output will follow the CS input. Thus, READY output will become LOW.
- After appropriate set up time (see timing diagrams), the WR input is made LOW.
- Sometime after this event, READY will return HIGH to indicate that the write operation has been acknowledged.
- Any time after the READY output goes HIGH, the WR input can be made HIGH. The DB0-DB7, A<sub>0</sub> and CS inputs can change after appropriate hold time requirements are satisfied (see timing diagrams).

The above procedure must be repeated until all bytes of the operand are pushed into the stack. It should be noted that for single precision operands 4 bytes should be pushed and 8 bytes must be pushed for double precision. Not pushing all the bytes of a quantity will result in byte pointer misalignment.

The 8232 stack can accommodate four single precision quantities or two double precision quantities. Pushing more quantities than the capacity of the stack will result in loss of data which is usual with any LIFO stack.

The stack can be visualized as shown below:



required. Writing into the Operand Stack takes place

Table 2. 8232 Command Set

TOS

# Single Precision Instructions

Description	Hex <sup>1</sup> Code	Stack Contents <sup>2</sup> After Execution A B C D	Status Flags Affected <sup>4</sup>
Add A and B 000878	01	R C DOOUSER	S, Z, U, V
Subtract A from B	02	RCDU	S, Z, Ú, V
Multiply A by B	03	RCDU	S, Z, U, V
Divide B by A. If A exponent = 0, then R = B.	04	ROCODO 00000738	S, Z, U, V, D
Change sign of A <sup>5</sup>	05	R B C D	s, z 0909
Push stack <sup>5</sup>	- 06	A* A B C	S, Z
Pop stack 00000998 0000000	00000748	B C C D A	S, Z auad
Exchange 00000000 00000000	08	BACD	S, Z JUMO
	Add A and B  Subtract A from B  Multiply A by B  Divide B by A. If A exponent = 0, then R = B.  Change sign of A <sup>5</sup> Push stack <sup>5</sup> Pop stack	Description         Hex¹ Code           Add A and B         01           Subtract A from B         02           Multiply A by B         03           Divide B by A. If A exponent = 0, then R = B.         04           Change sign of A <sup>5</sup> 05           Push stack <sup>5</sup> 06           Pop stack         07	Description

# **Double Precision Instructions**

	4. Someti noitqinaseQ, READY will cating that the data is available	Hex <sup>1</sup> Code	Stack Contents <sup>3</sup> After Execution A B	Status Flags Affected <sup>4</sup>
DADD	Add A and B	10 29 lubso	ney be issueca the pro	s, z, u, v
DSUB	Subtract A from B some vnA a	2A	tgeoxe RatUs bostego	S, Z, U, V
DMUL notice	Multiply A by B HOLH mules	2B	R U	S, Z, U, V
ed (see timing dia	Divide B by A. If A = 0, then R = B.	2C 611	a new conmand while is allowed in progress is allow	S, Z, U, V, D
CHSD	Change sign of A <sup>5</sup>	2D	R B	S, Z
PTOD NO Sec	Push stack <sup>5</sup>	2E	A* A	S, Z betel
bs yPOPD sisb at	Reading of the stack stack on pribate	2F	ВА	S, Z
ust be realload in	CLR status	00	A B	A eff pniveme

# ment. If more data is popped than the capacity caston

- 1. In the hex code column, SVREQ bit is a 0.
- 2. The stack initially is composed of four 32-bit numbers (A, B, C, D). A is equivalent to Top Of Stack (TOS) and B is Next on Stack (NOS). Upon completion of a command the stack is composed of: the result (R); undefined (U); or the initial contents (A,B,C, or D).
- 3. The stack initially is composed of two 64-bit numbers (A, B). A is equivalent to Top Of Stack (TOS) and B is Next On Stack (NOS). Upon completion of a command the stack is composed of: the result (R); undefined (U); or the initial contents (A, B).
- 4. Any status bit(s) not affected are set to 0. Nomenclature: Sign (S); Zero (Z); Exponent Underflow (U); Exponent Overflow (V); Divide Exception (D).
- 5. If the exponent field of A is zero, R or A\* will be zero.

stack, the total number of syles popped out should be appropriate with the precision — single precision results are 4 bytes and double precision results are 8 bytes. The following procedure must be used for rescing the result from the stack:

Results can be transferred from the stack to the data

A LOW is established on the A<sub>0</sub> input.
 The CS input is made LOW. When WR and RD inputs.

 After appropriate set up time (see timing diagrams), the RD input is made LOW.



Table 3. Execution Times

Command	TOS	NOS	Result anothern	Clock Periods
SADD SSUB SMUL SDIV	3F800000 3F800000 40400000 3F800000	3F800000 3F800000 3FC00000 4000000	4000000 0000000 4090000 3F00000	58 56 198 228
CHSS Z 8	3F800000	_10	BF800000 bas A bbA	GOAS
PTOS	3F800000	-30	Subtract A from 8	16 28
POPS XCHS	3F800000 3F800000	4000000	Multiply A by B	14 26
CHSD PTOD	3FF00000 00000000 3FF00000 00000000	- 0, 0 = 1ne	BFF00000 000000000	24 G 40
S.Z. DOO	3FF00000 00000000	-80	Change sign of A <sup>5</sup> -	26+0
CLR DADD	3FF00000 00000000 3FF00000 0A000000	3FF00000 00000000		578
DSUB A	3FF00000 A0000000	3FF00000 00000000	3FF00000 A0000000	578
DDIV VID	BFF80000 00000000 BFF80000 00000000	3FF80000 00000000 3FF80000 00000000	C0020000 00000000 BFF00000 00000000	1748 × 4560

Note: TOS, NOS and result are in hexadecimal; clock period is in decimal.

# Command Initiation

After properly positioning the required operands in the stack, a command may be issued. The procedure for initiating a command execution is the same as that described above for operand entry, except that the  $A_0$  input is HIGH.

An attempt to issue a new command while the current command execution is in progress is allowed. Under these circumstances, the READY output will not go HIGH until the current command execution is completed.

# Removing the Results

Result from an operation will be available at the TOS. Results can be transferred from the stack to the data bus by reading the stack.

When the stack is read for results, the most significant byte is available first and the least significant byte last.

A result is always of the same precision as the operands that produced it. Thus, when the result is taken from the stack, the total number of bytes popped out should be appropriate with the precision — single precision results are 4 bytes and double precision results are 8 bytes. The following procedure must be used for reading the result from the stack:

- 1. A LOW is established on the Ao input.
- The CS input is made LOW. When WR and RD inputs are both HIGH, the READY output follows the CS input, thus READY will be LOW.
- After appropriate set up time (see timing diagrams), the RD input is made LOW.

- Sometime after this, READY will return HIGH, indicating that the data is available on the DB0-DB7 lines. This data will remain on the DB0-DB7 lines as long as the RD input remains LOW.
- 5. Any time after READY goes HIGH, the RD input can return HIGH to complete the transaction.
- The CS and A<sub>0</sub> inputs can change after appropriate hold time requirements are satisfied (see timing diagram).
- Repeat this procedure until all bytes appropriate for the precision of the result are popped out.

Reading of the stack does not alter its data; it only adjusts the byte pointer. Note data must be removed in even byte multiples to avoid a byte pointer misalignment. If more data is popped than the capacity of the stack, the internal byte pointer will wrap around and older data will be read again, consistent with the LIFO stack.

# Reading Status Register source at villation losses and

The 8232 status register can be read without any regard to whether a command is in progress or not. The only implication that has to be considered is the effect this might have on the END and ERROR outputs discussed in the signal descriptions.

The following procedure must be followed to accomplish status register reading:

- 1. Establish HIGH on the Ao input.
- Establish LOW on the CS input. Whenever WR and RD inputs are HIGH, READY will follow the CS input. Thus, READY will go LOW.
- After appropriate set up time (see timing diagram), RD is made LOW.



- 4. Sometime after the HIGH to LOW transition of RD. READY will become HIGH, indicating that status register contents are available on the DB0-DB7 lines. These lines will contain this information as long as RD is LOW.
- 5. The RD input can be returned HIGH any time after READY goes HIGH. I be sollalinged a not aldiscou
- 6. The Ao input and CS input can change after satisfying appropriate hold time requirements (see timing diagram). The best example of what might be called the 8232's

# Status Register bisup to eareads ent animuon

The 8232 contains an 8-bit status register with the following format:

BUSY	SIGN	ZERO Z	RESERVED	DIVIDE EXCEPTION D	EXPONENT UNDERFLOW	EXPONENT OVERFLOW V	RESERVED
7	6	5	itemana	3	2	int the Le	0

All the bits are initialized to zero upon reset. Also, executing a CLR (Clear Status) command will result in all zero status register bits. A zero in bit 7 indicates that the 8232 is not busy and a new command may be initiated. As soon as a new command is issued, bit 7 becomes 1 to indicate the device is busy and remains 1 until the command execution is complete, at which time it will become 0. As soon as a new command is issued. status register bits 0-6 are cleared to zero. The status bits will be set as required during the command execution. Hence, as long as bit 7 is 1, the remainder of the status register bit indications should not be relied upon unless the ERROR occurs. The following is a detailed status bit description.

- Bit 0 Reserved ob of -(2) lid "vylolid" eff bits (R) lid
- Bit 1 Exponent overflow (V). When 1, this bit indicates that the result exponent is more positive than + 127 (+ 1023). The exponent is "wrapped" into the negative exponent range, skipping the end values.
- Bit 2 Exponent Underflow (U). When 1, this bit indicates that the result exponent is more negative than -126 (-1022). The exponent is "wrapped" into the positive range by the number of underflow bits. skipping -127 (-1023) and +128 (+1024).
- Bit 3 Divide Exception (D). When 1, this bit indicates that an attempt to divide by zero is made. Cleared to zero otherwise.
- Bit 4 Reserved.
- Bit 5 Zero (Z). When 1, this bit indicates that the result returned to TOS after a command is zero. Cleared to zero otherwise.
- Bit 6 Sign (S). When 1, this bit indicates that the result returned to TOS is negative. Cleared to zero otherwise.

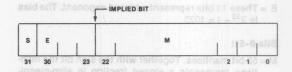
Bit 7 Busy. When 1, this bit indicates the 8232 is in the process of executing a command. It will become zero after the command execution is complete.

All other status register bits are valid when the Busy bit is zero.

# **Data Formats**

The 8232 handles floating-point quantities in two different formats - single precision and double precision. These formats are the same as those used by Intel in other products and those proposed by the IEEE Subcommittee on floating point arithmetic.

The single precision quantities are 32 bits long, as shown below:



# tude notation. There is an implied 1 beyond

Bit 31: I seement to (to tid) it dissifingle from S = Sign of the mantissa. One represents negative and 0 represents positive.

will always be a 1 due to normalization, is

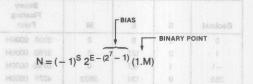
#### Bits 23-30; methi fid beilgmi sint seroteer 9898 edit

E = These 8 bits represent a biased exponent. The bias is 27 - 1 = 127. usnid effT and also lamete efft

#### Bits 0-22:

M = 23-bit mantissa. Together with the sign bit, the mantissa represents a signed fraction in sign-magnitude notation. There is an implied 1 beyond the most significant bit (bit 22) of the mantissa. In other words, the mantissa is assumed to be a 24-bit normalized quantity and the most significant bit, which will always be a 1 due to normalization, is implied. The 8232 restores this implied bit internally before performing arithmetic, normalizes the result and strips the implied bit before returning the results to the external data bus. The binary point is between the implied bit and bit 22 of the mantissa.

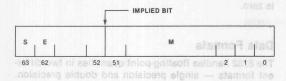
The quantity N represented by the above notation is



Provided E+0 (reserved for 0) or all 1's (illegal). The approximate decimal range for this format is  $\pm 1.17 \times 10^{-38}$  to  $\pm 3.40 \times 10^{38}$ . The format supports 7 significant decimal digits.



A double precision quantity consists of the mantissa sign bit, an 11-bit biased exponent (E), and a 52-bit mantissa (M). The bias for double precision quantities is  $2^{10} - 1$ . The double precision format is illustrated below.



# Bit 63: Vd besu eson) as emas ent era stemon esent

S = Sign of the mantissa. One represents negative and 0 represents positive.

# Bits 52-62:

E = These 11 bits represent a biased exponent. The bias is  $2^{10} - 1 = 1023$ .

#### Bits 0-51:

M = 52-bit mantissa. Together with the sign bit the mantissa represents a signed fraction in sign-magnitude notation. There is an implied 1 beyond the most significant bit (bit 51) of the mantissa. In other words, the mantissa is assumed to be a 53-bit normalized quantity and the most significant bit, which will always be a 1 due to normalization, is implied. The 8232 restores this implied bit internally before performing arithmetic, normalizes the result and strips the implied bit before returning the result to the external data bus. The binary point is between the implied bit and bit 51 of the mantissa.

The quantity N represented by the above notation is

BIAS BINARY POINT 
$$N = (-1)^S 2^{E - (2^{10} - 1)} (1.M)$$

Provided E  $\neq$  0 (reserved for 0) or all 1s (illegal). The approximate decimal range is  $\pm 2.22 \times 10^{-308}$  to  $\pm 1.80 \times 10^{308}$ . The format supports 16 significant decimal digits.

The following are some examples of single precision floating point representations:

Decimal	s	E <sup>ANS</sup>	М	Binary Floating Point
0 1410	0	0	0	0000 0000H
1	0	127	. 0	3F80 0000H
-1	1	127	0	BF80 0000H
255	0	134	.9922	437F 0000H
T MEDELL	0	128	.5708	4049 OFDBH

 $\pm 1.17 \times 10^{-38}$  to  $\pm 3.40 \times 10^{36}$ . The former supports 7

# 4. Sometime after the HGH to LOW trans gnibnoz .

One of the main objectives in choosing the 8232's Intel/ IEEE proposed floating point arithmetic was to provide maximum accuracy with no anomalies. This means that a mathematically unsophisticated user will not be "surprised" by some of the results. It is probably possible for a sophisticated user to obtain reliable results from almost any floating point arithmetic. However, in that case there will be an additional burden on the software.

The best example of what might be called the 8232's "safety factor" is the inclusion of guard bits for rounding. The absence of guard bits leads to the problem demonstrated by the following four-bit multiplication:

$$\begin{array}{c} .1111 \times 2^{0} \\ 1000 \times 2^{1} \\ \hline \text{VARIABLE} & .011111000 \times 2^{1} \\ \end{array}$$

Since the last four bits are lost, the normalized result is:

and the identify function is not valid. In the past this problem has been avoided (hopefully) by relying on excess precision.

Instead the 8232 uses a form of rounding known as "round to even." There are other types of rounding provided for in the proposed IEEE standard, but "round to even," an unbiased rounding scheme, is required. "Round to even" comes into play when a result is exactly halfway between two floating point numbers. In this case the arithmetic produces the "even" number, the one whose last mantissa bit is zero. The 8232 uses three additional bits—the Guard bit (G), the Rounding bit (R), and the "Sticky" bit (S)—to do the rounding. These are bits which hold data shifted out (right) of the accumulator. Rounding is carried out by the following rules, as shown in the following figure, after the result is normalized.

ant olat "b stid wolft G Ac	DIL	menogxe en mun entry	Positive range t Rule
0	0	0	No Round
0000	0	rd ethylb o	Instatte or test
0	1	0	Round Down
0	1	1	(21/31/D/10/01/02/01
1	0	0	Round to Even
the result		n no <sub>t</sub> sini	nerW (Z), when
o. Cleared	mand is zer		Round Up
1	1	1	to zero officerwisi



# **APPLICATIONS INFORMATION**

The diagram in Figure 3 represents the minimum configuration of an 8232 system. The CPU transfers data to and from the 8232 Floating Point Processor using the READY line. The 8232 status is checked using polling by the CPU.

In a high performance configuration (Figure 4), interrupts are used in place of polling. The interrupts are generated for an error condition and to signal the end of execution. Operand transfers are handled by the DMA controller.

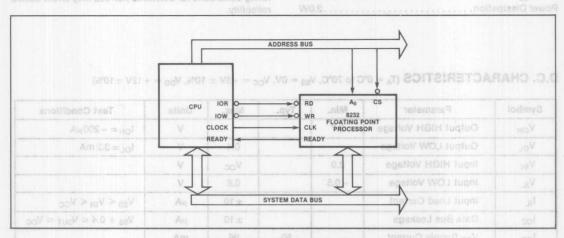


Figure 3. Minimum Configuration Example

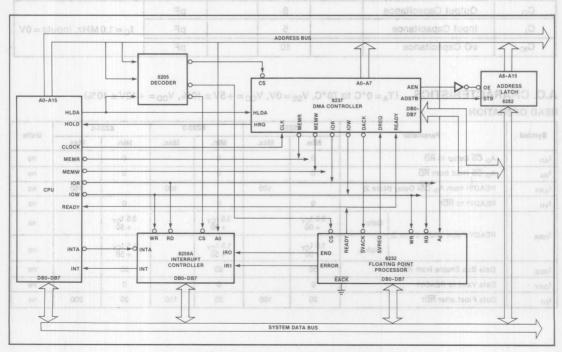


Figure 4. High Performance Configuration Example

# **ABSOLUTE MAXIMUM RATINGS\***

Storage Temperature	65°C to +150°C
Ambient Temperature Under Bias	
V <sub>DD</sub> with Respect to V <sub>SS</sub>	0.5V to +15.0V
V <sub>CC</sub> with Respect to V <sub>SS</sub>	0.5 V to +7.0 V
All Signal Voltages with Respect	
to V <sub>SS</sub>	0.5 V to +7.0 V
Power Dissipation	2.0W

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **D.C. CHARACTERISTICS** ( $T_A = 0^{\circ}C$ to $70^{\circ}C$ , $V_{SS} = 0V$ , $V_{CC} = +5V \pm 10\%$ , $V_{DD} = +12V \pm 10\%$ )

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
V <sub>OH</sub>	Output HIGH Voltage	3.7	(I)	жоож	V	$I_{OH} = -200 \mu A$
V <sub>OL</sub>	Output LOW Voltage		and .	0.4	V	I <sub>OL</sub> = 3.2 mA
V <sub>IH</sub>	Input HIGH Voltage	2.0		V <sub>CC</sub>	V	
V <sub>IL</sub>	Input LOW Voltage	-0.5		0.8	V	
I <sub>IL</sub>	Input Load Current	28	SYSTEM OATA	±10	μΑ	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
loz	Data Bus Leakage			±10	μΑ	$V_{SS} + 0.4 \le V_{OUT} \le V_{CC}$
Icc	V <sub>CC</sub> Supply Current	atlon Exac	50	95	mA	
I <sub>DD</sub>	V <sub>DD</sub> Supply Current		50	95	mA	
Co	Output Capacitance		8		pF	
Cı	Input Capacitance		5		pF	f <sub>C</sub> = 1.0 MHz, Inputs = 0\
CIO	I/O Capacitance		10		pF	

# **A.C. CHARACTERISTICS** $(T_A = 0 \text{ °C to } 70 \text{ °C}, V_{SS} = 0 \text{ V}, V_{CC} = +5 \text{ V} \pm 10 \text{ %}, V_{DD} = +12 \text{ V} \pm 10 \text{ %})$ **READ OPERATION**

Symbol	Parameter		82	32	8232-3		8232-8		Units
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units	
t <sub>AR</sub>	A <sub>0</sub> , CS Setup to RD		0		0		0		ns
t <sub>RA</sub>	A <sub>0</sub> , CS Hold from RD		0		0		0	— О учести	ns
t <sub>ARY</sub>	READY↓ from A <sub>0</sub> , <del>CS</del> ↓ Delay (Note 2)			100		100		150	e ns
t <sub>YR</sub>	READY† to RD†		0		0		0		ns
	READY Pulse Width (Note 3)	Data	3.5 t <sub>CY</sub> + 50		3.5 t <sub>CY</sub> + 50		3.5 t <sub>CY</sub> + 50		ns
terr	READT Fulse Width (Note 3)	1.5 t <sub>CY</sub> + 50		1.5 t <sub>CY</sub> + 50	ACTES STATES	1.5 t <sub>CY</sub> + 50	Carrier	ns	
t <sub>RDE</sub>	Data Bus Enable from RD↓		50		50	CONTROL	50	193	ns
tDRY	Data Valid to READY†	30	0		0		0	1	ns
t <sub>DF</sub>	Data Float after RDt		20	100	20	150	20	200	ns



# A.C. CHARACTERISTICS (Continued)

# WRITE OPERATION

	0	8232		8232-3		8232-8		Units
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
t <sub>AW</sub> A <sub>0</sub> , CS Setup to WR		25 - 4 1 - 400		25	25			ns
t <sub>WA</sub>	A <sub>0</sub> , CS Hold after WR	30		30	X	60 20		ns
t <sub>AWY</sub>	READY↓ from A <sub>0</sub> , CS↓ Delay (Note 2)	TO A STATE OF THE	100	Jan-25	100		150	ns
t <sub>YW</sub>	READY† to WR†	0		0		0		ns
t <sub>RRW</sub>	READY Pulse Width	- tant	t <sub>AW</sub> + 50	- Yest-	t <sub>AW</sub> + 50		t <sub>AW</sub> + 50	ns
t <sub>DW</sub>	Data Setup to WRt	100	1	100		150		ns
twp	Data Hold after WRt	20		20		20		ns

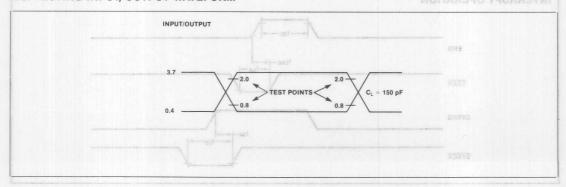
# **OTHER TIMINGS**

	THE RESERVE OF THE PERSON OF T	7/2						
Symbol	Parameter	8232		8232-3		8232-8		Units
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
tcy	Clock Period	250	2500	320	3300	480	5000	ns
t <sub>CPH</sub>	Clock Pulse HIGH Width	100		140		200		ns
t <sub>CPL</sub>	Clock Pulse LOW Width	120		160		240	OPERAL	ns
t <sub>EE</sub>	END Pulse Width (Note 4)	200		300		400		ns
t <sub>EAE</sub>	EACKI to ENDI Delay		150		175	TV as	200	ns
t <sub>AA</sub>	EACK Pulse Width	50		75		100		ns
t <sub>SA</sub>	SVACK+ to SVREQ+ Delay		100		200	e de la companione	300	ns
tss	SVACK Pulse Width	50		75	/	100		ns

#### NOTES:

- 1. Typical values are for T<sub>A</sub> = 25 °C, nominal supply voltages and nominal processing parameters.
- 2. READY is pulled low for both command and data operations.
- Minimum values shown assume no previously entered command is being executed for the data access. If a previously entered command is being
  executed, READY low pulse width is the time to complete execution plus the time shown. Status may be read at any time without exceeding the time
  shown.
- 4. END high pulse width is specified for EACK tied to VSS. Otherwise tEAE applies.

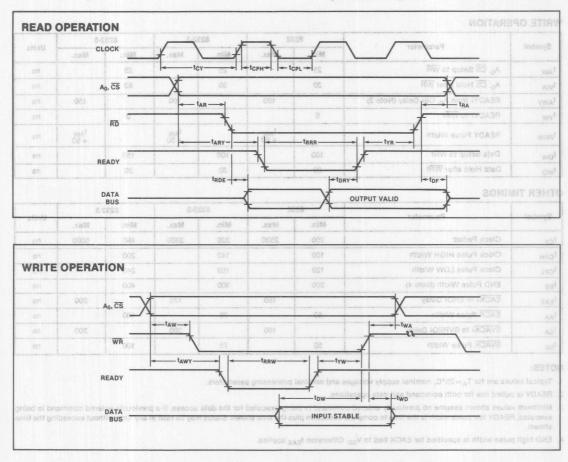
# A.C. TESTING INPUT, OUTPUT WAVEFORM

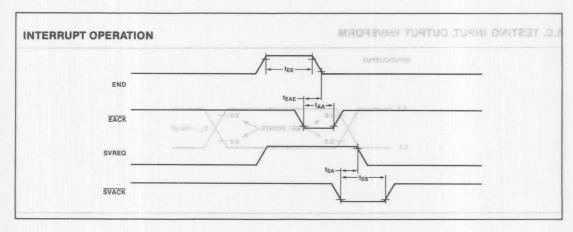




# **WAVEFORMS**

# A.C. CHARACTERISTICS (Continued)







# 8294 DATA ENCRYPTION UNIT

- Certified by National Bureau of Standards
- **80 Byte/Sec Data Conversion Rate**
- 64-Bit Data Encryption Using 56-Bit Key
- DMA Interface
- 3 Interrupt Outputs to Aid in Loading and Unloading Data

- 7-Bit User Output Port
- Single 5V ± 10% Power Supply
- Peripheral to MCS-86<sup>TM</sup>, MCS-85<sup>TM</sup>, MCS-80<sup>TM</sup> and MCS-48<sup>TM</sup> Processors
- Implements Federal Information
   Processing Data Encryption Standard
- **Encrypt and Decrypt Modes Available**

The Intel® 8294 Data Encryption Unit (DEU) is a microprocessor peripheral device designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard. The DEU operates on 64-bit text words using a 56-bit user-specified key to produce 64-bit cipher words. The operation is reversible: if the cipher word is operated upon, the original text word is produced. The algorithm itself is permanently contained in the 8294; however, the 56-bit key is user-defined and may be changed at any time.

The 56-bit key and 64-bit message data are transferred to and from the 8294 in 8-bit bytes by way of the system data bus. A DMA interface and three interrupt outputs are available to minimize software overhead associated with data transfer. Also, by using the DMA interface two or more DEUs may be operated in parallel to achieve effective system conversion rates which are virtually any multiple of 80 bytes/second. The 8294 also has a 7-bit TTL compatible output port for user-specified functions.

Because the 8294 implements the NBS encryption algorithm it can be used in a variety of Electronic Funds Transfer applications as well as other electronic banking and data handling applications where data must be encrypted.

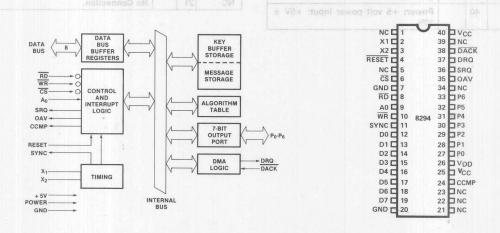


Figure 1. Block Diagram

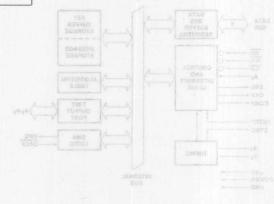
Figure 2. Pin Configuration

# intel

Table 1. Pin Description

Symbol	Pin No.	Туре	Name and Function
NC	1		No Connection.
X1 X2	2 3	1	Crystal: Inputs for crystal, L-C or external timing signal to determine internal oscillator frequency.
RESET	4	- I	Reset: A low signal to this pin resets the 8294.
NC A	5	201	No Connection: No connection or tied high.
CS	6	T	Chip Select: A low signal to this pin enables reading and writing to the 8294.
GND	7	item	<b>Ground:</b> This pin must be tied to ground.
RD	8	I	Read: An active low read strobe at this pin enables the CPU to read data and status from the internal DEU registers.
A <sub>0</sub>	9	1	Address: Address input used by the CPU to select DEU registers during read and write operations.
WR ob	10 2 no	notyp erypt	Write: An active low write strobe at this pin enables the CPU to send data and commands to the DEU.
SYNC	115	onili	Sync: High frequency (Clock ÷ 15) output. Can be used as a strobe for external circuitry.
D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	12 13 14 15 16 17 18 19		Data Bus: Three-state, bi-directional data bus lines used to transfer data between the CPU and the 8294.
GND	20		Ground: This pin must be tied to ground.
V <sub>cc</sub>	40	-	Power: +5 volt power input: +5V ± 10%.

Symbol	Pin No.	Туре	Name and Function
NC	39		No Connection.
DACK	38	1.0E16	DMA Acknowledge: Input signal from the 8257 DMA Controller acknowledg- ing that the requested DMA cycle has been granted.
DRQ (%)	37	0	<b>DMA Request:</b> Output signal to the 8257 DMA Controller requesting a DMA cycle.
SRQ	38	0	Service Request: Interrupt to the CPU indicating that the 8294 is awaiting data or commands at the input buffer. SRQ=1 implies IBF=0.
oav	35	0	Output Available: Interrupt to the CPU indicating that the 8294 has data or status available in its output buffer. OAV=1 implies OBF=1.
NC	34		No Connection.
P6 P5 P4 P3 P2 P1 P0	33 32 31 30 29 28 27	O (DE)	Output Port: User output port lines. Output lines available to the user via a CPU command which can assert selected port lines. These lines have nothing to do with the encryption function. At power-on, each line is in a 1 state.
V <sub>DD</sub>	26	te sh	<b>Power:</b> +5V power input. (+5V ±10%) Low power standby pin.
Vcc	25	eosti	Power: Tied high. und oel A netens
ogla golf	24	m0 m	Conversion Complete: Interrupt to the CPU indicating that the encryption/decryption of an 8-byte block is complete.
NC	23	G. 5 m	No Connection.
NC	22		No Connection.
NC	21		No Connection.



Flaure 2. Pla Configuration

| 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100

Figure 1. Block Diagram



# FUNCTIONAL DESCRIPTION

The data conversion sequence is as follows:

- A Set Mode command is given, enabling the desired as interrupt outputs.
- An Enter New Key command is issued, followed by 8
  data inputs which are retained by the DEU for encryption/decryption. Each byte must have odd parity.
- An Encrypt Data or Decrypt Data command sets the DEU in the desired mode.

After this, data conversions are made by writing 8 data bytes and then reading back 8 converted data bytes. Any of the above commands may be issued between data conversions to change the basic operation of the DEU; e.g., a Decrypt Data command could be issued to change the DEU from encrypt mode to decrypt mode without changing either the key or the interrupt outputs enabled.

# **INTERNAL DEU REGISTERS**

Four internal registers are addressable by the master processor: 2 for input, and 2 for output. The following table describes how these registers are accessed.

RD	WR	CS	A <sub>0</sub>	Register
1	0	0	0	Data input buffer
0	1	0	0	Data output buffer
1	0	0 0	=381	Command input buffer
0	1	0	1	Status output buffer
X	X	1	X	Don't care

The functions of each of these registers are described below.

**Data Input Buffer** — Data written to this register is interpreted in one of three ways, depending on the preceding command sequence.

- 1. Part of a key.
- 2. Data to be encrypted or decrypted.
- 3. A DMA block count.

**Data Output Buffer** — Data read from this register is the output of the encryption/decryption operation.

Command Input Buffer — Commands to the DEU are written into this register. (See command summary below.)

Status Output Buffer — DEU status is available in this register at all times, It is used by the processor for poll-driven command and data transfer operations.

STATUS BIT: FUNCTION: 7 6 5 4 3 2 1 0 X X X KPE CF DEC IBF OBF

OBF Output Buffer Full; OBF = 1 indicates that output from the encryption/decryption function is available in the Data Output Buffer. It is reset when the data is read.

- IBF Input Buffer Full; A write to the Data Input Buffer or to the Command Input Buffer sets IBF = 1. The DEU resets this flag when it has accepted the input byte. Nothing should be written when IBF = 1.
- DEC Decrypt; indicates whether the DEU is in an encrypt or a decrypt mode. DEC=1 implies the decrypt mode. DEC=0 implies the encrypt mode.
- CF Completion Flag; This flag may be used to indicate any or all of three events in the data transfer protocol.
- 1. It may be used in lieu of a counter in the processor routine to flag the end of an 8-byte transfer.
- to eat 12. It must be used to indicate the validity of
  - It may be used in lieu of the CCMP interrupt to indicate the completion of a DMA operation.

KPE Key Parity Error; After a new key has been entered, the DEU uses this flag in conjunction with the CF flag to indicate correct or incorrect parity.

# **COMMAND SUMMARY**

# 1 - Enter New Key

OP CODE:

0	1	0	0	0	0	0	(
---	---	---	---	---	---	---	---

This command is followed by 8 data byte inputs which are retained in the key buffer (RAM) to be used in encrypting and decrypting data. These data bytes must have odd parity represented by the LSB.

# 2 — Encrypt Data

OP CODE:

0	0	1	1	0	0	0	0
us	R		-				9

This command puts the 8294 into the encrypt mode.

#### 3 — Decrypt Data

OP CODE:

0	0	1	0	0	0	0	0
---	---	---	---	---	---	---	---

This command puts the 8294 into the decrypt mode.

# 4 - Set Mode

OP CODE:

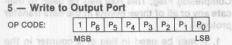
0	0	0	0	A	В	С	D
VIS	В		14,				LSE

# where:

A is the OAV (Output Available) interrupt enable
B is the SRQ (Service Request) interrupt enable
C is the DMA (Direct Memory Access) transfer enable

D is the CCMP (Conversion Complete) interrupt enable

SRQ, or CCMP interrupts respectively. A "1" in bit C will allow DMA transfers. When bit C is set the OAV and SRQ interrupts should also be enabled (bits A,B = 1). Following the command in which bit C, the DMA bit, is set, the 8294 will expect one data byte to specify the number of 8-byte blocks to be converted using DMA.



This command causes the 7 least significant bits of the command byte to be latched as output data on the 8294 output port. The initial output data is 1111111. Use of this port is independent of the encryption/decryption function.

# PROCESSOR/DEU INTERFACE PROTOCOL ENTERING A NEW KEY

The timing sequence for entering a new key is shown in Figure 3. A flowchart showing the CPU software to accommodate this sequence is given in Figure 4.

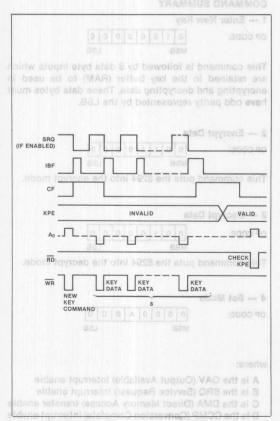


Figure 3. Entering a New Key

input buffer (most significant byte first). After the eighth byte is accepted by the DEU, CF goes true (CF = 1). The CF bit goes false again when KPE is valid. The CPU can then check the KPE flag. If KPE = 1, a parity error has been detected and the DEU has not accepted the key. Each byte is checked for odd parity, where the parity bit is the LSB of each byte.

Since the CF bit is used in this protocol to indicate the validity of the KPE flag, it may not be used to flag the end of the 8 byte key entry. CF = 1 only as long as KPE is invalid. Therefore, the CPU might not detect that CF = 1 and the key entry is complete before KPE becomes valid. Thus, a counter should be used, as in Figure 4, to flag the end of the new key entry. Then, CF is used to indicate a valid KPE flag.

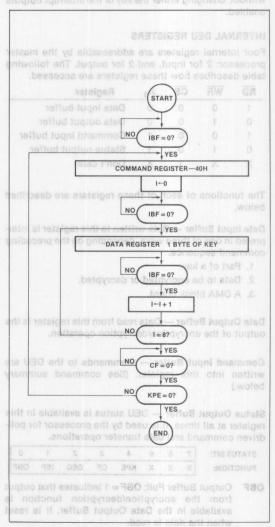


Figure 4. Flowchart for Entering a New Key

decrypting data. The CPU writes 8 data bytes to the DEU's data input buffer for encryption/decryption. CF then goes true (CF = 1) to indicate that the DEU has accepted the 8-byte block. Thus, the CPU may test for IBF = 0 and CF = 1 to terminate the input mode, or it may use a software counter. When the encryption/decryption is complete, the CCMP and OAV interrupts are asserted and the OBF flag is set true (OBF = 1). OAV and OBF are set false again after each of the converted data bytes is read back by the CPU. The CCMP interrupt is set false, and remains false, after the first read. After 8 bytes have been read back by the CPU, CF goes false (CF = 0). Thus, the CPU may test for CF = 0 to terminate the read mode. Also, the CCMP interrupt may be used to initiate a service routine which performs the next series of 8 data reads and 8 data writes. It beldene nismen

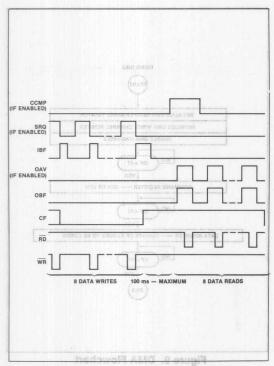


Figure 5. Encrypting/Decrypting Data

SINGLE BYTE COMMANOS

Figure 6 offers two flowcharts outlining the alternative means of implementing the data conversion protocol. Either the CF flag or a software counter may be used to end the read and write modes.

SRQ = 1 implies IBF = 0, OAV = 1 implies OBF = 1. This allows interrupt routines to do data transfers without checking status first. However, the OAV service routine must detect and flag the end of a data conversion.

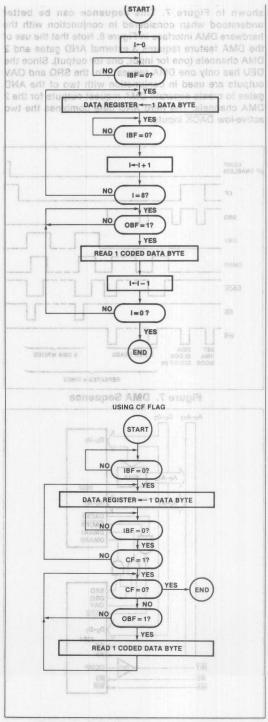


Figure 6. Data Conversion Flowcharts



#### **USING DMA**

The timing sequence for data conversions using DMA is shown in Figure 7. This sequence can be better understood when considered in conjunction with the hardware DMA interface in Figure 8. Note that the use of the DMA feature requires 3 external AND gates and 2 DMA channels (one for input, one for output). Since the DEU has only one DMA request pin, the SRQ and OAV outputs are used in conjunction with two of the AND gates to create separate DMA request outputs for the 2 DMA channels. The third AND gate combines the two active-low DACK inputs.

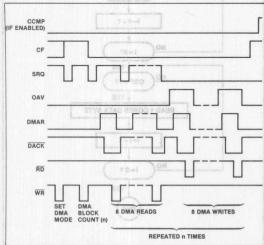


Figure 7. DMA Sequence

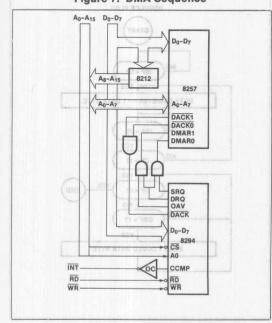


Figure 8. DMA Interface

To initiate a DMA transfer, the CPU must first initialize the two DMA channels as shown in the flowchart in Figure 9. It must then issue a Set Mode command to the DEU enabling the OAV, SRQ, and DMA outputs. The CCMP interrupt may be enabled or disabled, depending on whether that output is desired. Following the Set Mode command, there must be a data byte giving the number of 8-byte blocks of data (n<256) to be converted. The DEU then generates the required number of DMA requests to the 2 DMA channels with no further CPU intervention. When the requested number of blocks has been converted, the DEU will set CF and assert the CCMP interrupt (if enabled). CCMP then goes false again with the next write to the DEU (command or data). Upon completion of the conversion, the DMA mode is disabled and the DEU returns to the encrypt/decrypt mode. The enabled interrupt outputs, however, will remain enabled until another Set Mode command is issued.

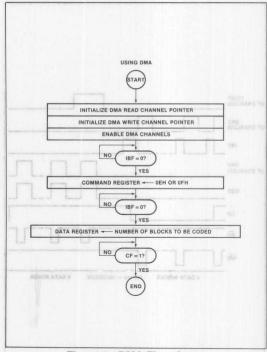


Figure 9. DMA Flowchart

# SINGLE BYTE COMMANDS

Figure 10 shows the timing and protocol for single byte commands. Note that any of the commands is effective as a pacify command in that they may be entered at any time, except during a DMA conversion. The DEU is thus set to a known state. However, if a command is issued out of sequence, an additional protocol is required (Figure 11). The CPU must wait until the command is accepted (IBF = 0). A data read must then be issued to clear anything the preceding command sequence may have left in the Data Output Buffer.





# CPUIDEU INTERFACES

Figures 12 through 15 illustrate four interface configurations used in the CPU/DEU data transfers. In all cases SRQ will be true (if enabled) and IBF will be false when the DEU is ready to accept data or commands.

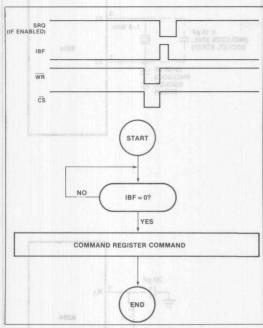


Figure 10. Single Byte Commands

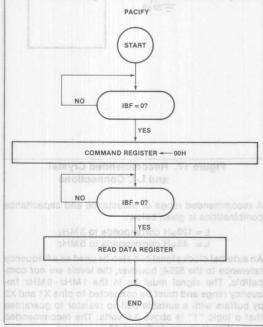


Figure 11. Pacify Protocol

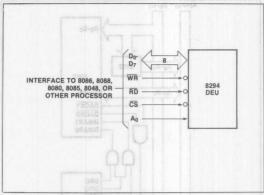


Figure 12. Polling Interface

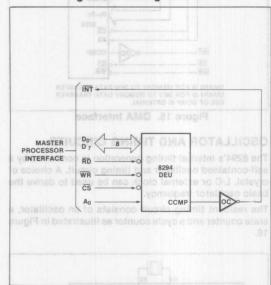


Figure 13. Single Interrupt Interface

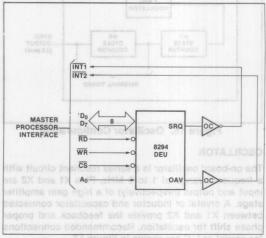


Figure 14. Dual Interrupt Interface

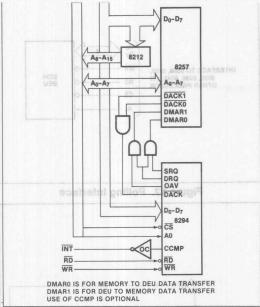


Figure 15. DMA Interface

# OSCILLATOR AND TIMING CIRCUITS

The 8294's internal timing generation is controlled by a self-contained oscillator and timing circuit. A choice of crystal, L-C or external clock can be used to derive the basic oscillator frequency.

The resident timing circuit consists of an oscillator, a state counter and a cycle counter as illustrated in Figure 16.

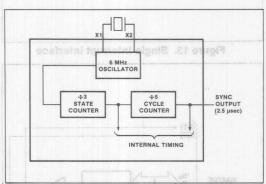


Figure 16. Oscillator Configuration

# **OSCILLATOR**

The on-board oscillator is a series resonant circuit with a frequency range of 1 to 6 MHz. Pins X1 and X2 are input and output (respectively) of a high gain amplifier stage. A crystal or inductor and capacitator connected between X1 and X2 provide the feedback and proper phase shift for oscillation. Recommended connections for crystal or L-C are shown in Figure 17.

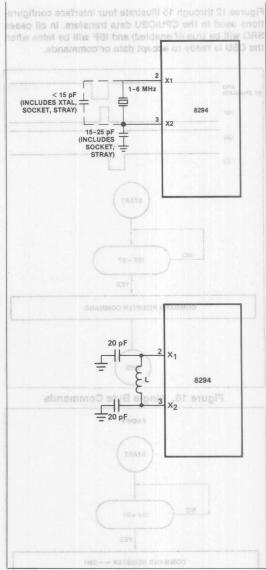


Figure 17. Recommended Crystal and L-C Connections

A recommended range of inductance and capacitance combinations is given below:

L =  $120 \mu$ H corresponds to 3 MHz L =  $45 \mu$ H corresponds to 5 MHz

An external clock signal can also be used as a frequency reference to the 8294; however, the levels are *not* compatible. The signal must be in the 1 MHz-6 MHz frequency range and must be connected to pins X1 and X2 by buffers with a suitable pull-up resistor to guarantee that a logic "1" is above 3.8 volts. The recommended connection is shown in Figure 18.

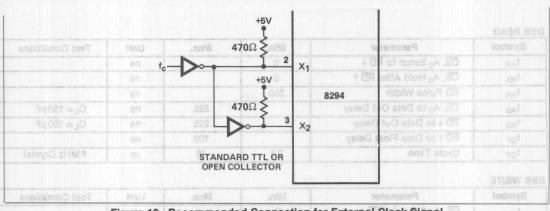


Figure 18. Recommended Connection for External Clock Signal

# **ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias ...... 0°C to 70°C

Storage Temperature ...... -65°C to +150°C

Voltage on Any Pin With
Respect to Ground ...... -0.5V to +7V

Power Dissipation ...... 1.5 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# D.C. AND OPERATING CHARACTERISTICS (TA = 0°C to 70°C, VCC = +5V ± 10%, VSS = 0V)

Symbol	Parameter		Limits		Unit	Test Conditions		
Symbol	200   002	Min.	Тур.	Max.	DAG of 3	Litera Continuit		
V <sub>IL</sub>	Input Low Voltage (AII	-0.5		0.8	ioVinter.	tol Control T.I		
V <sub>IL1</sub>	Input Low Voltage (X <sub>1</sub> , X <sub>2</sub> , RESET)	-0.5		0.6	V			
V <sub>IH</sub>	Input High Voltage (All Except X <sub>1</sub> , X <sub>2</sub> , RESET)	2.2		V <sub>CC</sub>	W V 97	C. TESTING INPUT, OU		
V <sub>IH1</sub>	Input High Voltage (X <sub>1</sub> , X <sub>2</sub> , RESET)	3.8		V <sub>CC</sub>	FLI9NV			
V <sub>OL</sub>	Output Low Voltage (D <sub>0</sub> -D <sub>7</sub> )			0.45	V	I <sub>OL</sub> = 2.0 mA		
V <sub>OL1</sub>	Output Low Voltage (All Other Outputs)		0.0	0.45	V	I <sub>OL</sub> = 1.6 mA		
V <sub>OH</sub>	Output High Voltage (D <sub>0</sub> -D <sub>7</sub> )	2.4	rer <	X	V	$I_{OH} = -400 \mu A$		
V <sub>OH1</sub>	Output High Voltage (All Other Outputs)	2.4	807	-	V 0.45	$I_{OH} = -50 \mu\text{A}$		
IIL	Input Leakage Current (RD, WR, CS, A <sub>0</sub> )			±10	μА	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		
loz	Output Leakage Current (D <sub>0</sub> -D <sub>7</sub> , High Z State)			±10	μА	$V_{SS} + 0.45 \le V_{OUT} \le V_{C}$		
I <sub>DD</sub>	V <sub>DD</sub> Supply Current		5	15	mA			
I <sub>DD</sub> +I <sub>CC</sub>	Total Supply Current		60	125	mA			
lu	Low Input Load Current (Pins 24, 27-38)			0.5	mA	V <sub>IL</sub> = 0.8 V		
I <sub>LI1</sub>	Low Input Load Current (RESET)			0.2	mA	V <sub>IL</sub> = 0.8 V		
I <sub>IH</sub>	Input High Leakage Current (Pins 24, 27-38)			100	μΑ	V <sub>IN</sub> = V <sub>CC</sub>		
CIN	Input Capacitance			10	pF			
C <sub>I/O</sub>	I/O Capacitance			20	pF			



A.C. CHARACTERISTICS ( $T_A = 0$ °C to 70°C,  $V_{CC} = V_{DD} = +5V \pm 10$ %,  $V_{SS} = 0V$ )

# DBB READ

Symbol	Parameter	Min. S 20	Max.	Unit	Test Conditions	
tar	CS, A <sub>0</sub> Setup to RD ↓ 0			ns		
t <sub>RA</sub>	CS, A <sub>0</sub> Hold After RD↑	- Ova-		ns		
t <sub>RR</sub>	RD Pulse Width	250		ns		
t <sub>AD</sub>	CS, A <sub>0</sub> to Data Out Delay	\$ 12011	225	ns	C <sub>L</sub> = 150 pF	
t <sub>RD</sub>	RD ↓ to Data Out Delay	X 8 6-04	225	ns	C <sub>L</sub> = 150 pF	
t <sub>DF</sub>	RD ↑ to Data Float Delay		100	ns		
tcy	Cycle Time	2.5	AGUAT15	μS	6 MHz Crystal	

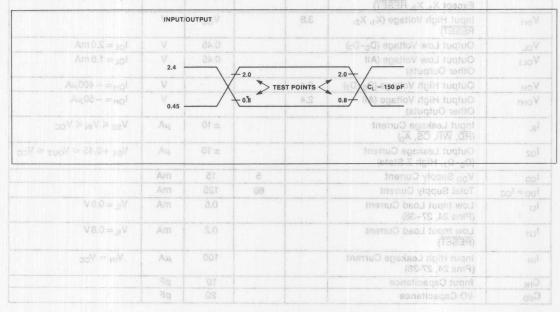
# **DBB WRITE**

Symbol	Symbol         Parameter           t <sub>AW</sub> CS, A₀ Setup to WR ↓		Max.	Unit	Test Conditions
t <sub>AW</sub>			Recommended ConsOction I		
t <sub>WA</sub>	CS, A <sub>0</sub> Hold After WR↑	0		ns	
tww	WR Pulse Width sesson 3:301	OM* 250	*80M	ns	ABSOLUTE MAXIN
t <sub>DW</sub>	Data Setup to WR ↑	150		ns	
t <sub>WD</sub>	Data Hold to WR ↑	0 0.0	01000	ns	molent Lemperatura

#### DMA AND INTERRUPT TIMING

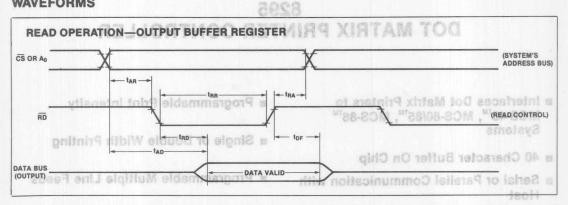
Symbol	Parameter anolitones	Min.	Max.	Unit	Test Conditions
t <sub>ACC</sub>	DACK Setup to Control	0		ns	
tCAC	DACK Hold After Control	TICSOTA = C	ARACTERIS	ns	C. AND OPERA
t <sub>ACD</sub>	DACK to Data Valid	Hell	225	ns	C <sub>L</sub> = 150 pF
tCRQ	Control L.E. to DRQ T.E.	film. Typ.	200	ns	iocini,o.
t <sub>CI</sub>	Control T.E. to Interrupt T.E.	-0.5	t <sub>CY</sub> + 500 (A)	ns wo	V <sub>IL</sub> I Input

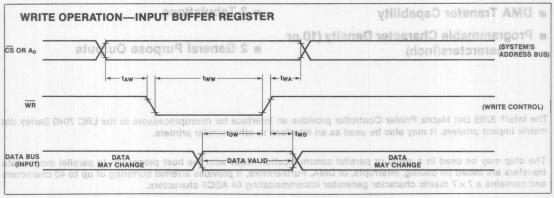
# A.C. TESTING INPUT, OUTPUT WAVEFORM





# **WAVEFORMS**





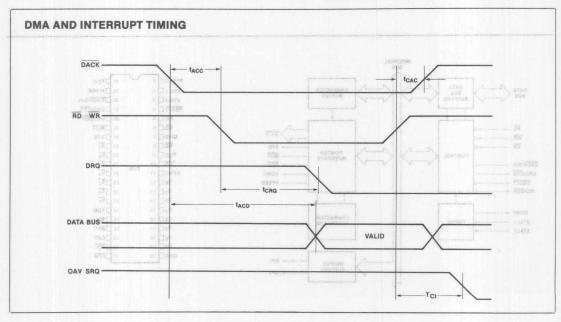


Figure 2. Pin Configuration

Figure 1. Block Diagram

# DOT MATRIX PRINTER CONTROLLER

- Interfaces Dot Matrix Printers to MCS-48<sup>TM</sup>, MCS-80/85<sup>TM</sup>, MCS-86<sup>TM</sup> Systems
- 40 Character Buffer On Chip
- Serial or Parallel Communication with Host
- **DMA Transfer Capability**
- Programmable Character Density (10 or 12 Characters/Inch)

- Programmable Print Intensity
- Single or Double Width Printing
- Programmable Multiple Line Feeds
- 3 Tabulations NAME HOLTAGE OF STREET
- 2 General Purpose Outputs

The Intel® 8295 Dot Matrix Printer Controller provides an interface for microprocessors to the LRC 7040 Series dot matrix impact printers. It may also be used as an interface to other similar printers.

The chip may be used in a serial or parallel communication mode with the host processor. In parallel mode, data transfers are based on polling, interrupts, or DMA. Furthermore, it provides internal buffering of up to 40 characters and contains a  $7 \times 7$  matrix character generator accommodating 64 ASCII characters.

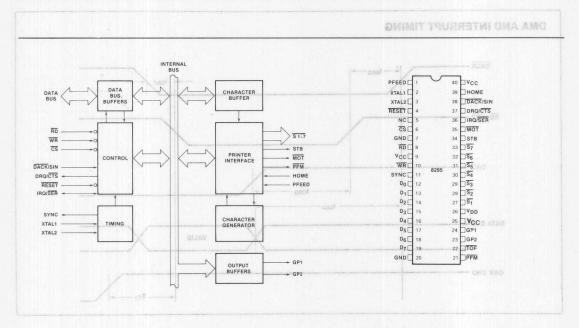


Figure 1. Block Diagram

Figure 2. Pin Configuration



# condition and box 2003 and neewled note Table 1. Pin Description

Symbol	Pin No.	Туре	Name and Function
PFEED	a 10	gulq i	Paper Feed: Paper feed input switch.
XTAL1 XTAL2	2 3	s to	Crystal: Inputs for a crystal to set in- ternal oscillator frequency. For proper operation use 6 MHz crystal.
RESET	4	1	Reset: Reset input, active low. After reset the 8295 will be set for 12 char- acters/inch single width printing solenoid strobe at 320 msec.
NC	5	polityl	No Connection: No connection or tied high.
CS	6	1	Chip Select: Chip select input used to enable the RD and WR inputs except during DMA.
GND MOI		deun dmu	Ground: This pin must be tied to ground.
eed o DR crivated.	s ai s	ugni i	Read: Read input which enables the master CPU to read data and status In the serial mode this pin must be tied to V <sub>CC</sub> .
V <sub>CC</sub>	9	Star	Power: +5 volt power input: +5V ± 10%.
WR		by (a an Tai	Write: Write input which enables the master CPU to write data and commands to the 8295. In the serial mode this pin must be tied to V <sub>SS</sub> .
SYNC	11	0	Sync: 2.5 μs clock output. Can be used as a strobe for external circuitry
D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	12 13 14 15 16 17 18 19	I/O	Data Bus: Three-state bidirectional data bus buffer lines used to interface the 8295 to the host processor in the parallel mode. In the serial mode $D_0$ — $D_2$ sets up the baud rate.
GND	20		<b>Ground:</b> This pin must be tied to ground.
V <sub>CC</sub>	40	T-20	Power: +5 volt power input: +5 ± 10%.

0		
		X
	1	

Symbol	Pin No.	Туре	Name and Function
HOME	39	gille gille gilly is	Home: Home input switch, used by the 8295 to detect that the print head is in the home position.
DACK/SIN	38	ar <b>l</b> ich harad	DMA Acknowledge/Serial Input: In the parallel mode used as DMA ac knowledgment; in the serial mode used as input for data.
DRQ/CTS	37 29ni	O soligh ad bru	DMA Request/Clear to Send: In the parallel mode used as DMA reques output pin to indicate to the 8257 tha a DMA transfer is requested; in the serial mode used as clear-to-send signal.
IRQ/SER		n.O e abo pin te	Interrupt Request/Serial Mode: Ir parallel mode it is an interrupt request input to the master CPU; ir serial mode it should be strapped to Vss.
MOT	35	0	Motor: Main motor drive, active low
STB	34	0	Solenoid Strobe: Solenoid strobe output. Used to determine duration o solenoids activation.
S <sub>7</sub>   S <sub>6</sub>   S <sub>5</sub>   S <sub>4</sub>   S <sub>3</sub>   S <sub>2</sub>   S <sub>1</sub>	33 32 31 30 29 28 27	o di line	Solenoid: Solenoid drive outputs active low.  12
V <sub>DD</sub>	26	sharts ts at	Power: +5V power input (+5V ± 10%). Low power standby pin.
Vcc	25	11 19	Power: Tied high.
GP1 GP2	24 23	0	General Purpose: General purpose output pins.
TOF	22	perl.	<b>Top of Form:</b> Top of form input, used to sense top of form signal for type I printer.
PFM	21	0	Paper Feed Motor Drive: Paper feed motor drive, active low.



# **FUNCTIONAL DESCRIPTION**

The 8295 interfaces microcomputers to the LRC 7040 Series dot matrix impact printers, and to other similar printers. It provides internal buffering of up to 40 characters. Printing begins automatically when the buffer is full or when a carriage return character is received. It provides a modified 7x7 matrix character generator. The character set includes 64 ASCII characters.

Communication between the 8295 and the host processor can be implemented in either a serial or parallel mode. The parallel mode allows for character transfers into the buffer via DMA cycles. The serial mode features selectable data rates from 110 to 4800 baud.

The 8295 also offers two general purpose output pins which can be set or cleared by the host processor. They can be used with various printers to implement such functions as ribbon color selection, enabling form release solenoid, and reverse document feed.

# COMMAND SUMMARY

COMMINIA	IND GOIMMAITI
Hex Code	Description
one oo rese	Set GP1. This command brings the GP1 pin to a logic high state. After power on it is automatically set high.
01	Set GP2. Same as the above but for GP2.
02	Clear GP1. Sets GP1 pin to logic low state, inverse of command 00.
03	Clear GP2. Same as above but for GP2. Inverse command 01.
04	Software Reset. This is a pacify command. This command is not effective immediately after commands requiring a parameter, as the Reset command will be interpreted as a parameter.
05	Print 10 characters/in. density.
06	Print 12 characters/in. density.
_ v07 y yus	Print double width characters. This command prints characters at twice the normal width, that is, at either 17 or 20 characters per line.
08 besu sugari Tod of the	Enable DMA mode; must be followed by two bytes specifying the number of data characters to be fetched. Least significant byte accepted first.

Hex Code	Description
09	Tab character.
0A	Line feed.
OB ed	Multiple Line Feed; must be followed by a byte specifying the number of line feeds.
0C	Top of Form. Enables the line feed output until the Top of Form input is activated.
OD	Carriage Return. Signifies end of a line and enables the printer to start printing.
0E	Set Tab #1, followed by tab position byte.
0F	Set Tab #2, followed by tab position byte Should be greater than Tab #1.
10	Set Tab #3, followed by tab position byte. Should be greater than Tab #2.
land-petible end not recease of ni recease o	Print Head Home on Right. On some printers the print head home position is on the right. This command would enable normal left to right printing with such printers.
12	Set Strobe Width; must be followed by strobe width selection byte. This command adjusts the duration of the strobe activa-

# PROGRAMMABLE PRINTING OPTIONS

# CHARACTER DENSITY

The character density is programmable at 10 or 12 characters/inch (32 or 40 characters/line). The 8295 is automatically set to 12 characters/inch at power-up. Invoking the Print Double-Width command halves the character density (5 or 6 characters/inch). The 10 char/in or 12 char/in command must be re-issued to cancel the Double-Width mode. Different character density modes may not be mixed within a single line of printing.

#### **PRINT INTENSITY**

The intensity of the printed characters is determined by the amount of time during which the solenoid is on. This on-time is programmable via the Set Strobe-Width command. A byte following this command sets the solenoid on-time according to Table 2. Note that only the three least significant bits of this byte are important.

Table 2. Solenoid On-Time

D7—D3	D2	D1	D0	Solenoid On (microsec)
х	0	0	0	200
X	0	0	1	240
×	0	1	0	280
X	0	1	1	320
X	1	0	0	360
X	1	0	1	400
X	1	1	0	440
×	1	1	1	480

# **TABULATIONS**

Up to three tabulation positions may be specified with the 8295. The column position of each tabulation is selected by issuing the Set Tab commands, each fol-



lowed by a byte specifying the column. The tab positions will then remain valid until new Set Tab commands are issued.

Sending a tab character (09H) will automatically fill the character buffer with blanks up to the next tab position. The character sent immediately after the tab character will thus be stored and printed at that position.

# **CPU TO 8295 INTERFACE**

Communication between the CPU and the 8295 may take place in either a serial or parallel mode. However, the selection of modes is inherent in the system hardware; it is not software programmable. Thus, the two modes cannot be mixed in a single 8295 application.

# PARALLEL INTERFACE

Two internal registers on the 8295 are addressable by the CPU: one for input, one for output. The following table describes how these registers are accessed.

RD	WR	CS	Register & war
1	0	0	Input Data Register
0	odio	0	Output Status Register

Input Data Register—Data written to this register is interpreted in one of two ways, depending on how the data is coded.

- 1. A command to be executed (0XH or 1XH).
- A character to be stored in the character buffer for printing (2XH, 3XH, 4XH, or 5XH). See the character set. Table 2.

Output Status Register—8295 status is available in this register at all times.

STATUS BIT:	7	6	5	4	3	2	-1	0
FUNCTION:	X	X	PA	DE	X	х	IBF	X

PA—Parameter Required; PA = 1 indicates that a command requiring a parameter has been received. After the necessary parameters have been received by the 8295, the PA flag is cleared.

**DE**—DMA Enabled; DE = 1 whenever the 8295 is in DMA mode. Upon completion of the required DMA transfers, the DE flag is cleared.

IBF—Input Buffer Full; IBF = 1 whenever data is written to the Input Data Register. No data should be written to the 8295 when IBF = 1.

A flow chart describing communication with the 8295 is shown in Figure 3.

The interrupt request output (IRQ, Pin 36) is available on the 8295 for interrupt driven systems. This output is asserted true whenever the 8295 is ready to receive data.

To improve bus efficiency and CPU overhead, data may be transferred from main memory to the 8295 via DMA cycles. Sending the Enable DMA command (08H) activates the DMA channel of the 8295. This command must be followed by two bytes specifying the length of the data string to be transferred (least significant byte first). The 8295 will then assert the required DMA requests to

the 8257 DMA controller without further CPU intervention. Figure 4 shows a block diagram of the 8295 in DMA mode.

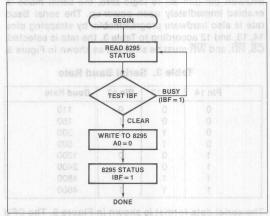


Figure 3. Host to 8295 Protocol Flowchart

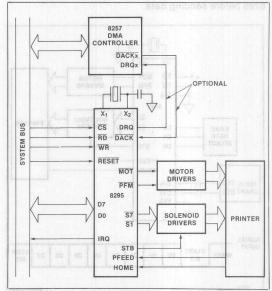


Figure 4. Parallel System Interface

Data transferred in the DMA mode may be either commands or characters or a mixture of both. The procedure is as follows:

- Set up the 8257 DMA controller channel by sending a starting address and a block length.
- Set up the 8295 by issuing the "Enable DMA" command (08H) followed by two bytes specifying the block length (least significant byte first).

The DMA enabled flag (DE) will be true until the assigned data transfer is completed. Upon completion of the transfer, the flag is cleared and the interrupt request (IRQ) signal is asserted. The 8295 then returns to the non-DMA mode of operation.



#### SERIAL INTERFACE Monthly relicatings AMG VSSB entr

The 8295 may be hardware programmed to operate in a serial mode of communication. By connecting the IRQ/SER pin (pin 36) to logic zero, the serial mode is enabled immediately upon power-up. The serial Baud rate is also hardware programmable; by strapping pins 14, 13, and 12 according to Table 3, the rate is selected. CS, RD, and WR must be strapped as shown in Figure 5.

**Table 3. Serial Baud Rate** 

Pin 14	Pin 13	Pin 12	Baud Rate
0	0	0	110
0	0 =	a.io 1	150
0	1 1 7 7	0	300
0	1	0 = 10	600
1	0	0	1200
1	0	UTATE SESS	2400
1	1	0	4800
1	1	1	4800

The serial data format is shown in Figure 5. The CPU should wait for a clear to send signal (CTS) from the 8295 before sending data.

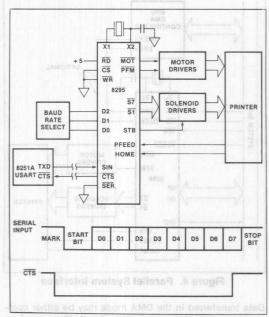


Figure 5. Serial Interface to UART (8251A)

# 8295 TO PRINTER INTERFACE

The strobe output signal of the 8295 determines the duration of the solenoid outputs, which hold the data to the printer. These solenoid outputs cannot drive the printer solenoids directly. They should be buffered through solenoid drivers as shown in Figure 6. Recommended solenoid and motor driver circuits may be found in the printer manufacturer's interface guide.

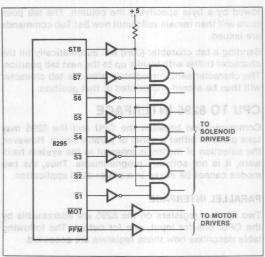


Figure 6. 8295 To Printer Solenoid Interface

# OSCILLATOR AND TIMING CIRCUITS

The 8295's internal timing generation is controlled by a self-contained oscillator and timing circuit. A 6 MHz crystal is used to derive the basic oscillator frequency. The resident timing circuit consists of an oscillator, a state counter and a cycle counter as illustrated in Figure 7. The recommended crystal connection is shown in Figure 8.

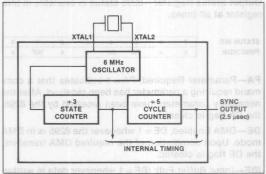


Figure 7. Oscillator Configuration

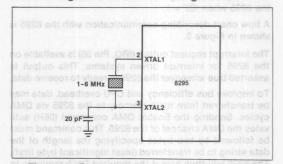


Figure 8. Recommended Crystal Connection

20	space		30		0		40	@	50	P
21			31		1		41	Α	51	DEB DEAD
22	"Fost Con	tinti	32	.xsW	2	.niM	42	Bramasa		lodmR3
23	#	an	33		3	0	43	tup to Pa	53	S
24	\$		34		4		44	U	34	T
25	%		35		5		45	1 Of Eleft A blo	55	AFÜ
26	&	an	36		6	250	46	F rijbiW		FIRM
2790 081	0 ,	ns	37		7		47	Data OP Delay	ot oA 57	W
20	1   0	an	38	225	8		48 49	ata Out Delay	58	X
2A	*	en.	3A	100	i		5A	ata Float Delay		90 <b>Ž</b>
2B	+	SII.	3B	15	;		4B	K e	nIT o 5B	lcy
2C	,	-	3C		<	material state of the same	4C	L	5C	
2D			3D		=		4D	M	5D	]
2E			3E		>		4E	N	5E	<b>↑</b>
2F	1		3F		?		4F	0	5F	-
										THE STATE OF THE

# **ABSOLUTE MAXIMUM RATINGS\***

Power Dissipation......1.5 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# D.C. AND OPERATING CHARACTERISTICS ( $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$ , $V_{CC} = V_{DD} = +5\text{V} \pm 10\%$ , $V_{SS} = 0\text{V}$ )

Symbol	) facT	Parameter	TT	Limits		Unit	Test Conditions	
Symbol	Parameter		Min.	Тур.	Max.	land of ou	102 80A0 t	
V <sub>IL</sub>		Low Voltage (All t X <sub>1</sub> , X <sub>2</sub> , RESET)	-0.5	0	0.8	d After Oc	CAC DAOK HO	
V <sub>IL1</sub>	Input	Low Voltage (X <sub>1</sub> , X <sub>2</sub> ,	-0.5		0.6	V	tago DAOK to DR	
V <sub>IH</sub>		High Voltage (All t X <sub>1</sub> , X <sub>2</sub> , RESET)	2.2		V <sub>CC</sub>	V		
V <sub>IH1</sub>	Input RESE	High Voltage (X <sub>1</sub> , X <sub>2</sub> ,	3.8		V <sub>CC</sub>	V	MO THOM OMITORY	
VoL	Outpu	t Low Voltage (D <sub>0</sub> -D <sub>7</sub> )			0.45	V	I <sub>OL</sub> = 2.0 mA	
V <sub>OL1</sub>		t Low Voltage (All Outputs)			0.45	o TUV	I <sub>OL</sub> = 1.6 mA	
V <sub>OH</sub>	Outpu	t High Voltage (D <sub>0</sub> -D <sub>7</sub> )	2.4			V	$I_{OH} = -400  \mu A$	
V <sub>OH1</sub>		t High Voltage (All Outputs)	2.4	0.5	4/-	- V	$I_{OH} = -50 \mu\text{A}$	
I <sub>IL</sub>		Leakage Current VR, CS, A <sub>0</sub> )	> avvion	E37 <	±10	μА	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	
I <sub>OZ</sub>		t Leakage Current 7, High Z State)			±10	μА	$V_{SS} + 0.45 \le V_{OUT} \le V_{C}$	
I <sub>DD</sub>	V <sub>DD</sub> S	upply Current		5	15	mA		
I <sub>DD</sub> +I <sub>CC</sub>	Total S	Supply Current		60	125	mA		
l <sub>Ll</sub>		nput Load Current 24, 27-38)			0.5	mA	V <sub>IL</sub> = 0.8 V	
I <sub>LI1</sub>	Low Ir	nput Load Current T)			0.2	mA	V <sub>IL</sub> = 0.8 V	
I <sub>IH</sub>	Input I (Pins 2	High Leakage Current 22, 38)			100	μΑ	V <sub>IN</sub> = V <sub>CC</sub>	
CIN	Input	Capacitance			10	pF		
C <sub>I/O</sub>	I/O Ca	pacitance			20	pF		

Print Char.



A.C. CHARACTERISTICS ( $T_A = 0^{\circ}C$  to  $70^{\circ}C$ ,  $V_{CC} = V_{DD} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ ) A HETO ARAMO 3038

Hex Code Print Char. Hex Code Print Char. Hex Code

#### **DBB READ**

Print Char.

Symbol	Se Parameter	Min.	Max.	Unit	Test Conditions
tar	CS, A <sub>0</sub> Setup to RD ↓	0 AS		ns	# E3
tRA	CS, A <sub>0</sub> Hold After RD ↑	0 45		ns	% 35
t <sub>RR</sub>	RD Pulse Width	aa 250	1	ns ns	8 89
t <sub>AD</sub>	CS, A <sub>0</sub> to Data Out Delay	47	225	ns	C <sub>L</sub> = 150 pF
t <sub>RD</sub>	RD ↓ to Data Out Delay	Oh.	225	ns	C <sub>L</sub> = 150 pF
tDF	RD to Data Float Delay	Aa	100	ns	- A
tcy	Cycle Time	84 2.5	15	μS	+ 8

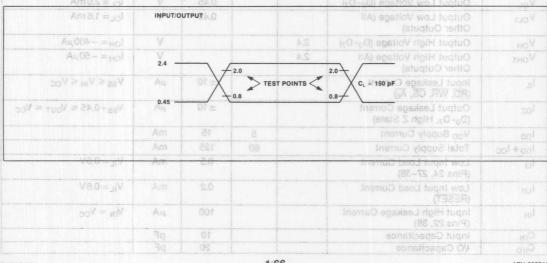
#### **DBB WRITE**

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
taw	CS, A <sub>0</sub> Setup to WR ↓	move o	COMIT	ns	MARI STUJUGGA
netion Awb pere	CS, A <sub>0</sub> Hold After WR ↑	0 device		ns	
vod two tibno	WR Pulse Width 15 solveb str	10 not 250 0°07	ot 0°0	.asins sbrit	Ambient Temperature
t <sub>DW</sub>	Data Setup to WR ↑	150 0°08	+ of "68	ns	Storage Temperature.
t <sub>WD</sub>	Data Hold to WR 1	onites 0	+3/3.0	ns	Personal Any Plat VV

#### D.C. AND OPERATING CHARACTERISTICS (TA = 0°C to 70°C, VCC = Vbp DMA AND INTERRUPT TIMING

Symbol	Parameter		Min.		Max.	of Unit	Test	Conditions
tACC	DACK Setup to Contr	ol	-446. 0	.5115///		ns		
tcac	DACK Hold After Con	trol	0	6.0-	1	ns	166043	JI.A
tCRQ	WR to DRQ Cleared	8.0		8.0-	200	ns, ns	humal	
t <sub>ACD</sub>	DACK to Data Valid				225	ns	CL	= 150 pF
	V	Vcc		2.2		igh Voltage (A X <sub>1</sub> , X <sub>2</sub> , RESET		HIV

## A.C. TESTING INPUT, OUTPUT WAVEFORM



1-66

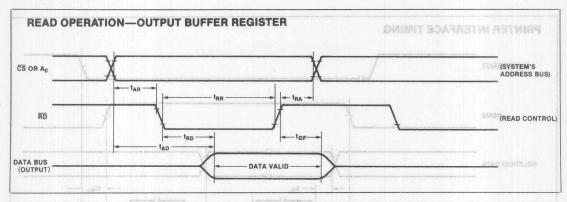
AFN-00231C

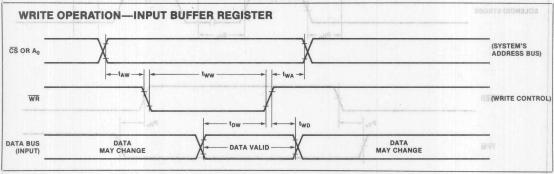


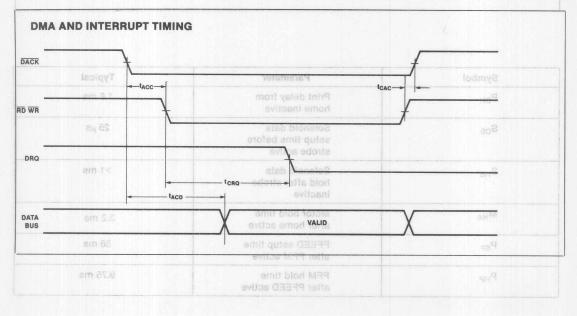


## **WAVEFORMS**

## WAVEFORMS (Continued)





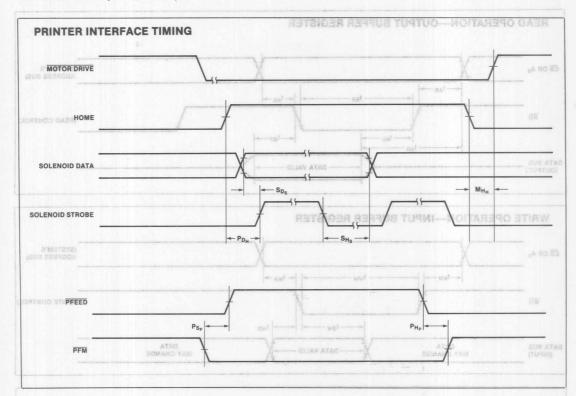






## **WAVEFORMS (Continued)**





## DMA AND INTERRUPT TIMING

Symbol	Parameter	Typical
P <sub>DH</sub>	Print delay from home inactive	1.8 ms
S <sub>DS</sub>	Solenoid data setup time before strobe active	25 μs
S <sub>HS</sub>	Solenoid data hold after strobe inactive	>1 ms
M <sub>HA</sub>	Motor hold time after home active	3.2 ms AYAD aug
P <sub>SP</sub>	PFEED setup time after PFM active	58 ms
P <sub>HP</sub>	PFM hold time after PFEED active	9.75 ms



# **Memory Controllers**

## 8202A DYNAMIC RAM CONTROLLER

- a Provides All Signals Necessary to Control 2104A, 2117, or 2118 Bynamic Memories
- AGENT COMPANIES OF TOTAL AROUND THE THE TARGET AND A VOICE AND A V
- 8065A, IAPX 88, and IAPX 86 Family Microprocessors
- a Decodes CPU Status for Advanced Read Capability
- Provides System Acknowledge and Transfer Acknowledge Signers
- a Internal Clock Capability with the 8202A-1

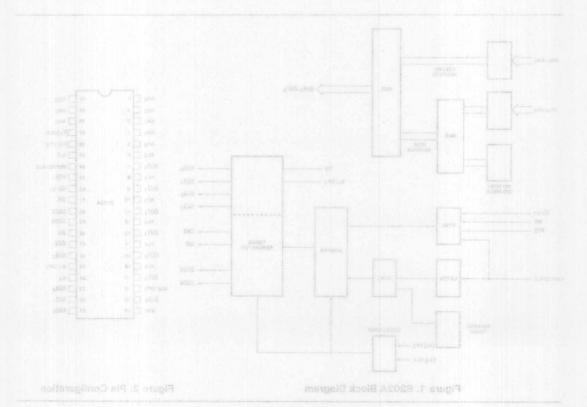
a Directly Addresses and Drives Up to 64K Bytes Without External Drivers

a Provides Address Multiplexing and

Provides a Refresh Timer and a Refresh Counter

B Refresh Cycles Way be Internally or Externally Requested

The Intel® 8202A is a Dynamic Ram System Controller designed to provide all algorith recessary to use 2104A, 2117, or 2118 Dynamic RAMs in microcomputer systems. The 8202A provides multiplexed addresses and address strobes, as well as refresh/access arbitration. The 8202A-1 supports an internal crystal oscillator.





# 8202A DYNAMIC RAM CONTROLLER

- Provides All Signals Necessary to Control 2104A, 2117, or 2118 Dynamic Memories
- Directly Addresses and Drives Up to 64K Bytes Without External Drivers
- Provides Address Multiplexing and Strobes
- Provides a Refresh Timer and a Refresh Counter
- Refresh Cycles May be Internally or Externally Requested

- Provides Transparent Refresh Capability
- Fully Compatible with Intel® 8080A, 8085A, iAPX 88, and iAPX 86 Family Microprocessors
- Decodes CPU Status for Advanced Read Capability
- Provides System Acknowledge and Transfer Acknowledge Signals
- Internal Clock Capability with the 8202A-1

The Intel® 8202A is a Dynamic Ram System Controller designed to provide all signals necessary to use 2104A, 2117, or 2118 Dynamic RAMs in microcomputer systems. The 8202A provides multiplexed addresses and address strobes, as well as refresh/access arbitration. The 8202A-1 supports an internal crystal oscillator.

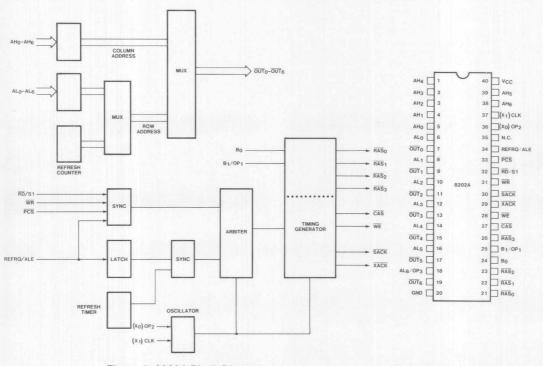


Figure 1. 8202A Block Diagram

Figure 2. Pin Configuration



Table 1. Pin Descriptions

Symbol	Pin No.	Туре	Name and Function
ALO	6	1	Address Low: CPU address in
AL <sub>1</sub>	8	e atitue e	puts used to generate memory
AL <sub>2</sub>	10	author s	row address.
AL <sub>3</sub>	12	leant a	AL6/OP3 used to select 4h
AL4	14	to ord	RAM mode.
AL5	16	dateo 2	injunction with the RAS and City
AL6/OP3	18	the given	R pirnanyls art vd basu seable
vo ethway	baar	a to he	fresh cycles. During the first p
AH <sub>O</sub>	5	ajTUO-	Address High: CPU address in
AH <sub>1</sub>	4	1	puts used to generate memory
AH <sub>2</sub>	3	1	column address.
AH3	2	duos de	mate a refresh cycle. the refre
AH <sub>4</sub>		belovo	
AH <sub>5</sub>	39	1	
-	38	i	sali (CAS inactive, RAS active)
AH <sub>6</sub>	36	UNIVERSITY OF	THE PROPERTY OF THE PARTY OF TH
ВО	24	T	Bank Select Inputs: Used to
B <sub>1</sub> /OP <sub>1</sub>	25	T	gate the appropriate RAS <sub>0</sub>
			RAS3 output for a memory cy
	A 3281	MG 10 9	cle. B <sub>1</sub> /OP <sub>1</sub> option used to se
			lect the Advanced Read Mode.
PCS	33	1	Protected Chip Select: Used to
	6-4		enable the memory read and
			write inputs. Once a cycle is
	Digni F	W bas	started, it will not abort even i
	V 10 I	BET YK	PCS goes inactive before cycle
	risen r	en awol	completion.
WR	31	1 AS	Memory Write Request.
RD/S1	32	dryss	Memory Read Request: S
and suite	n Hw	relide	function used in Advanced Read
		Mandre	
niod not .	plests	iony re	mode selected by OP <sub>1</sub> (pin 25)
REFRQ/	34	Tess.	External Refresh Request: ALE
ALE	super	refresh	function used in Advanced Read
			mode, selected by OP <sub>1</sub> (pin 25)
OUTO	7	0	Output of the Multiplexer
OUT <sub>1</sub>	9	0	These outputs are designed to
OUT <sub>2</sub>	11	0	drive the addresses of the Dy
OUT <sub>3</sub>	13	0	CONTRACT FORMAL STATE
	1000		namic RAM array. For 4K RAM
OUT <sub>4</sub>	15	0	operation, OUT <sub>6</sub> is designed to
OUT <sub>5</sub>	17	0	drive the 2104A CS input. (Note
OUT <sub>6</sub>	19	0	that the OUT <sub>0-6</sub> pins do not re
	and the	Office of	quire inverters or drivers fo
OUT OVER	Bur to	NUNE R	proper operation.
WE	28	0	Write Enable: Drives the Write
	21 1/24	- di ci	Enable inputs of the Dynamic
.031613	ELIQI	entr at n	RAM array.
CAS	27	0	Column Address Strobe: This
		11013	output is used to latch the Col
		bold be	umn Address into the Dynamic

Symbol	Pin No.	Туре	Name and Function
RAS <sub>0</sub> RAS <sub>1</sub> RAS <sub>2</sub> RAS <sub>3</sub>	21 22 23 26	0 0 0	Row Address Strobe: Used to latch the Row Address into the bank of dynamic RAMs, selected by the 8202A Bank Selections (B <sub>0</sub> , B <sub>1</sub> /OP <sub>1</sub> ).
XACK on FW bo		111111111111111111111111111111111111111	Transfer Acknowledge: This output is a strobe indicating valid data during a read cycle or data written during a write cycle.  XACK can be used to latch valid data from the RAM array.
SACK  TRANS (196  -91 (199	its. Ri PRO i mem: prog	eupon i BiR erib etheven il eloyo n H339	a memory access cycle. It can be used as an advanced trans- fer acknowledge to eliminate
(X <sub>0</sub> ) OP <sub>2</sub> (X <sub>1</sub> ) CLK	36 37	I/O o I/O	Oscillator Inputs: These inputs are designed for a quartz crystal to control the frequency of the oscillator. If $X_0/OP_2$ is connected to a $1K\Omega$ resistor pulled to $+12V$ then $X_1/CLK$ becomes a TTL input for an external clock.
N.C.	35	es" and	Reserved for future use.
VCC	40	Reidi A	Power Supply:+5V.
GND	20		Ground.

NOTE: Crystal mode for the 8202A-1 only.

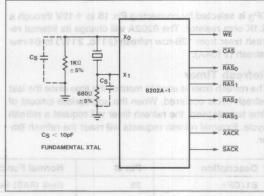


Figure 3. Crystal Operation for the 8202A-1



### **Functional Description**

The 8202A provides a complete dynamic RAM controller for microprocessor systems as well as expansion memory boards. All of the necessary control signals are provided for 2104A, 2117, and 2118 dynamic RAM's.

All 8202A timing is generated from a single reference clock. This clock is provided via an external oscillator or an on chip crystal oscillator. All output signal transitions are synchronous with respect to this clock reference, except for the CPU handshake signals SACK and XACK (trailing edge).

CPU memory requests normally use the RD and WR inputs. The advanced READ mode allows ALE and S1 to be used in place of the RD input.

Failsafe refresh is provided via an internal refresh timer which generates internal refresh requests. Refresh requests can also be generated via the REFRQ input.

An on-chip synchronizer/arbiter prevents memory and refresh requests from affecting a cycle in progress. The READ, WRITE, and external REFRESH requests may be asynchronous to the 8202A clock; on-chip logic will synchronize the requests, and the arbiter will decide if the requests should be delayed, pending completion of a cycle in progress.

#### Option Selection

The 8202A has three strapping options. When  $OP_1$  is selected (16K mode only), pin 32 changes from a  $\overline{RD}$  input to an S1 input, and pin 34 changes from a REFREQ input to an ALE input. See "Refresh Cycles" and "Read Cycles" for more detail.  $OP_1$  is selected by tying pin 25 to  $\pm$ 12V though a 5.1K ohm resistor.

When  $OP_2$  is selected, by connecting pin 36 to  $\pm 12V$  through a 1K ohm resistor, pin 37 changes from a crystal input (X<sub>1</sub>) to the CLK input for an external TTL clock.

OP<sub>3</sub> is selected by connecting Pin 18 to +12V through a 5.1K ohm resistor. The 8202A will change its internal refresh timer from 128-row refresh (2118, 2117) to 64-row refresh (2104A).

#### **Refresh Timer**

The refresh timer is used to monitor the time since the last refresh cycle occurred. When the appropriate amount of time has elapsed, the refresh timer will request a refresh cycle. External refresh requests will reset the refresh timer.

#### **Refresh Counter**

The refresh counter is used to sequentially refresh all of the memory's rows. The 8-bit counter is incremented after every refresh cycle.

## **Address Multiplexer**

The address multiplexer takes the address inputs and the refresh counter outputs, and gates them onto the address outputs at the appropriate time. The address outputs, in conjunction with the RAS and CAS outputs, determine the address used by the dynamic RAMs for read, write, and refresh cycles. During the first part of a read or write cycle, ALO-AL6 are gated to OUTO-OUT6, then AHO-AH6 are gated to the address outputs.

During a refresh cycle, the refresh counter is gated onto the address outputs. All refresh cycles are RAS-only refresh (CAS inactive, RAS active).

To minimize buffer delay, the information on the address outputs is inverted from that on the address inputs.

OUT<sub>0</sub>-OUT<sub>6</sub> do not need inverters or buffers unless additional drive is required.

## Synchronizer/Arbiter

The 8202A has three inputs, REFRQ/ALE (pin 34), RD (pin 32) and WR (pin 31). The RD and WR inputs allow an external CPU to request a memory read or write cycle, respectively. The REFRQ/ALE allows refresh requests to be requested external to the 8202A.

All three of these inputs may be asynchronous with respect to the 8202A's clock. The arbiter will resolve conflicts between refresh and memory requests, for both pending cycles and cycles in progress. Read and write requests will be given priority over refresh requests.

#### **System Operation**

The 8202A is always in one of the following states:

- a) IDLE
- b) TEST Cycle
- c) REFRESH Cycle
- d) READ Cycle
- e) WRITE Cycle

The 8202A is normally in the IDLE state. Whenever one of the other cycles is requested, the 8202A will leave the IDLE state to perform the desired cycle. If no other cycles are pending, the 8202A will return to the IDLE state.

Description	Pin #	Normal Function	Option Function
B1/OP1	25	Bank (RAS) Select Simenya odli o	Advanced-Read Mode
X <sub>0</sub> /OP <sub>2</sub>	of main 36 G fatey	Crystal Oscillator (8202A-1)	External Oscillator
AL6/OP3	18	Address Input	64-ROW Refresh

Figure 4. 8202A Option Selection



#### Test Cycle Him hemsongo el metava rossecondorolm A

The TEST Cycle is used to check operation of several 8202A internal functions. TEST cycles are requested by activating the RD and WR inputs, independent of PCS. The TEST Cycle will reset the refresh address counter and perform a WRITE Cycle. The TEST Cycle should not be used in normal system operation, since it would affect the dynamic RAM refresh.

## Refresh Cycles ,emit easons been lienevo erit etaluo

The 8202A has two ways of providing dynamic RAM refresh; a "atiny-visa" amoreo ellernon ASOSB erit cont2 emit ent vd atugni stab MARI erit te eldste ed jaum stab erit

- 1) Internal (failsafe) refresh misulant switch 2500 2AO
- en 2) External (hidden) refresh and ton each metave ent

Both types of 8202A refresh cycles activate all of the RAS outputs, while CAS, WE, SACK, and XACK remain inactive.

Internal refresh is generated by the on-chip refresh timer. The timer uses the 8202A clock to ensure that refresh of all rows of the dynamic RAM occurs every 2 milliseconds. If REFRQ is inactive, the refresh timer will request a refresh cycle every 10-16 microseconds.

External refresh is requested via the REFRQ input (pin 34). External refresh control is not available when the Advanced-Read mode is selected. External refresh requests are latched, then synchronized to the 8202A clock.

The arbiter will allow the refresh request to start a refresh cycle only if the 8202A is not in the middle of a cycle.

Simultaneous memory request and external refresh request will result in the memory request being honored first. This 8202A characteristic can be used to "hide" refresh cycles during system operation. A circuit similar to Figure 5 can be used to decode the CPU's instruction fetch status to generate an external refresh request. The refresh request is latched while the 8202A performs the instruction fetch; the refresh cycle will start immediately after the memory cycle is completed, even if the RD input has not gone inactive. If the CPU's instruction decode time is long enough, the 8202A can complete the refresh cycle before the next memory request is generated.

Certain system configurations require complete external refresh requests. If external refresh is requested faster than the minimum internal refresh timer (tREF), then, in effect, all refresh cycles will be caused by the external refresh request, and the internal refresh timer will never generate a refresh request.

Figure 7. Read Access Time

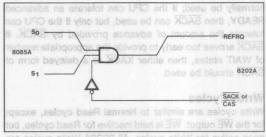


Figure 5. Hidden Refresh

## **Read Cycles**

The 8202A can accept two different types of memory Read requests:

- 1) Normal Read, via the RD input
- 2) Advanced Read, using the S1 and ALE inputs

The user can select the desired Read request configuration via the B1/OP1 hardware strapping option on pin 25.

	Normal Read	Advanced Read
Pin 25	B1 input	+12 Volt Option
Pin 32	RD input	S1 input
Pin 34	REFRQ input	ALE input
# RAM banks	4 (RAS 0-3)	2 (RAS 2-3)
Ext. Refresh	Yes	No

Figure 6. 8202A Read Options

Normal Reads are requested by activating the RD input, and keeping it active until the 8202A responds with an XACK pulse. The RD input can go inactive as soon as the command hold time (tCHS) is met.

Advanced Read cycles are requested by pulsing ALE while S1 is active; if S1 is inactive (low) ALE is ignored. Advanced Read timing is similiar to Normal Read timing, except the falling edge of ALE is used as the cycle start reference.

If a Read cycle is requested while a refresh cycle is in progress, then the 8202A will set the internal delayed-SACK latch. When the Read cycle is eventually started, the 8202A will delay the active SACK transition until XACK goes active, as shown in the AC timing diagrams. This delay was designed to compensate for the CPU's READY setup and hold times. The delayed–SACK latch is cleared after every READ cycle.

Based on system requirements, either SACK or XACK can be used to generate the CPU READY signal. XACK will



normally be used; if the CPU can tolerate an advanced READY, then SACK can be used, but only if the CPU can tolerate the amount of advance provided by SACK. If SACK arrives too early to provide the appropriate number of WAIT states, then either XACK or a delayed form of SACK should be used.

#### Write Cycles

Write cycles are similiar to Normal Read cycles, except for the WE output. WE is held inactive for Read cycles, but goes active for Write cycles. All 8202A Write cycles are "early-write" cycles; WE goes active before CAS goes active by an amount of time sufficient to keep the dynamic RAM output buffers turned off.

### **General System Considerations**

All memory requests (Normal Reads, Advanced Reads, Writes) are qualified by the PCS input. PCS should be stable, either active or inactive, prior to the leading edge of RD, WR, or ALE. Systems which use battery backup should pullup PCS to prevent erroneous memory requests, and should also pullup WR to keep the 8202A out of its test mode.

In order to minimize propagation delay, the 8202A uses an inverting address multiplexer without latches. The system must provide adequate address setup and hold times to guarantee RAS and CAS setup and hold times for the RAM. The 8202A tad AC parameter should be used for this system calculation.

The B0-B1 inputs are similar to the address inputs in that they are not latched. B0 and B1 should not be changed during a memory cycle, since they directly control which RAS output is activated.

The 8202A uses a two-stage synchronizer for the memory request inputs (RD, WR, ALE), and a separate two stage synchronizer for the external refresh input (REFRQ). As with any synchronizer, there is always a finite probability of metastable states inducing system errors. The 8202A synchronizer was designed to have a system error rate less than 1 memory cycle every three years based on the full operating range of the 8202A.

the 8202A will delay the active SACK transition until XACK goes active, as shown in the AC fiming diagrams. This delay was designed to compensate for the CPU's READY setup and hold times. The delayed–SACK letch is cleared

Based on system requirements, either SACK or XACK can be used to generate the OPU READY signal. XACK will

A microprocessor system is concerned with the time data is valid after  $\overline{\text{RD}}$  goes low. See Figure 7. In order to calculate memory read access times, the dynamic RAM's A.C. specifications must be examined, especially the RAS-access time (tRAC) and the CAS-access time (tCAC). Most configurations will be CAS-access limited; i.e., the data from the RAM will be stable t<sub>CC,max</sub> (8202A) + tCAC (RAM) after a memory read cycle is started. Be sure to add any delays (due to buffers, data latches, etc.) to calculate the overall read access time.

Since the 8202A normally performs "early-write" cycles, the data must be stable at the RAM data inputs by the time  $\overline{\text{CAS}}$  goes active, including the RAM's data setup time. If the system does not normally guarantee sufficient write data setup, you must either delay the  $\overline{\text{WR}}$  input signal or delay the 8202A  $\overline{\text{WE}}$  output.

Delaying the WR input will delay all 8202A timing, including the READY handshake signals, SACK and XACK, which may increase the number of WAIT states generated by the CPU.

If the WE output is externally delayed beyond the CAS active transition, then the RAM will use the falling edge of WE to strobe the write data into the RAM. This WE transition should not occur too late during the CAS active transition, or else the WE to CAS requirements of the RAM will not be met.

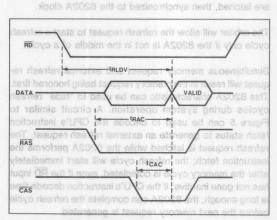


Figure 7. Read Access Time

refresh requests. If external refresh is requested faster than the minimum internal refresh timer (type), then, in effect, all refresh cycles will be caused by the external re-

fresh request, and the internal refresh timer will never



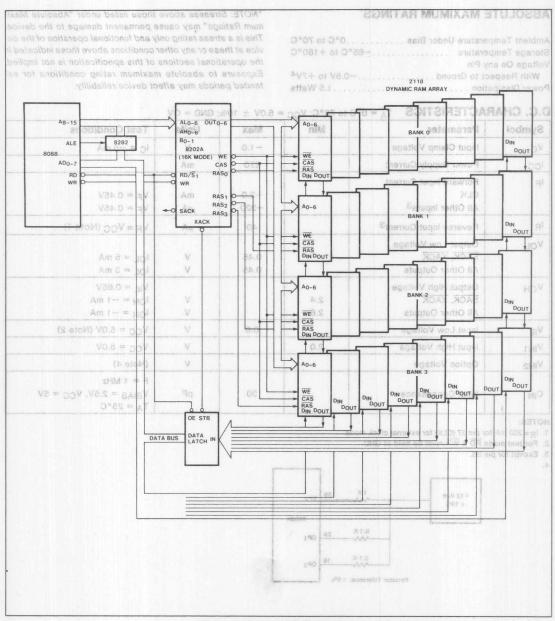


Figure 8. Typical 8088 System



### **ABSOLUTE MAXIMUM RATINGS'**

 \*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. CHARACTERISTICS TA = 0°C to 70°C; VCC = 5.0V ± 10%; GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
VC HOD	Input Clamp Voltage		-1.0	Noo2A	$I_C = -5 \text{ mA}$
Icc	Power Supply Current	2AB	270	mA	\$-0QA
lF	Forward Input Current CLK All Other Inputs <sup>3</sup>	a-oa A	-2.0 -320	mA μA	V <sub>F</sub> = 0.45V V <sub>F</sub> = 0.45V
IR will	Reverse Input Current <sup>3</sup>		40	μΑ Ι	VR = VCC (Note 1)
VOL	Output Low Voltage SACK, XACK All Other Outputs	ZAS 4 ZAS AR TUO O DINO	0.45 0.45	v v	I <sub>OL</sub> = 5 mA I <sub>OL</sub> = 3 mA
VOH	Output High Voltage SACK, XACK All Other Outputs	2.4		V V	$V_{IL} = 0.65V$ $I_{OH} = -1 \text{ mA}$ $I_{OH} = -1 \text{ mA}$
VIL	Input Low Voltage	TOO DW DOOT	0.8	V	V <sub>CC</sub> = 5.0V (Note 2)
VIH1	Input High Voltage	2.0		V	V <sub>CC</sub> = 5.0V
V <sub>IH2</sub>	Option Voltage	8-04 K		V	(Note 4)
CIN	Input Capacitance	WF CAS Date	30	pF	F = 1 MHz V <sub>BIAS</sub> = 2.5V, V <sub>CC</sub> = 5V T <sub>A</sub> = 25°C

#### NOTES

- 1. IR = 200 mA for pin 37 (CLK) for external clock mode.
- 2. For test mode RD & WR must be held at GND.
- 3. Except for pin 36.

4.

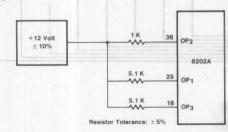


Figure 8. Typical 8086 System

Normal Read or Write Cycle



## A.C. CHARACTERISTICS

 $T_A = 0$ °C to 70°C,  $V_{CC} = 5V \pm 10\%$ 

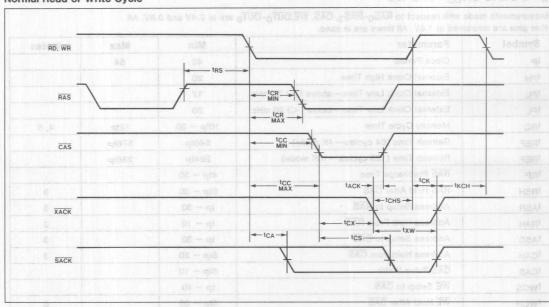
Measurements made with respect to  $\overline{RAS}_0$ - $\overline{RAS}_3$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{OUT}_0$ - $\overline{OUT}_6$  are at 2.4V and 0.8V. All other pins are measured at 1.5V. All times are in nsec.

Symbol	Parameter	Min	Max	Notes
tp -	Clock Period	40	54	
tpH	External Clock High Time	20		
tpL	External Clock Low Time—above (>) 20 mHz	17	1 1 1 1	BAR
tpL	External Clock Low Time—below (<) 20 mHz	20		
tRC	Memory Cycle Time	10tp - 30	12tp	4, 5
tREF	Refresh Time (64 cycles—4K mode)	548tp	576tp	242
tREF	Refresh Time (128 cycles—16K mode)	264tp	288tp	
tRP	RAS Precharge Time	4tp - 30		
tRSH	RAS Hold After CAS	5tp - 30	<b>原料加州为洲</b> 区	3
tASR	Address Setup to RAS	tp - 30		я <sub>бах</sub> 3
†RAH	Address Hold From RAS	tp - 10		3
tASC	Address Setup to CAS	tp - 30		3
†CAH	Address Hold from CAS	5tp - 20		3
tCAS	CAS Pulse Width	5tp - 10		
twcs	WE Setup to CAS	tp - 40		
twch	WE Hold After CAS	5tp - 35		8
tRS	RD, WR, ALE, REFRQ delay from RAS	5tp	Mode	nead bear
MRP RD, WR setup to RAS		0		5
†RMS	REFRQ setup to RD, WR	2tp		
tRMP	REFRQ setup to RAS	2tp		5
tpcs	PCS Setup to RD, WR, ALE	20		
tAL	S1 Setup to ALE	15		
tLA	S1 Hold from ALE	30		
tCR	RD, WR, ALE to RAS Delay	tp + 30	2tp + 70	2
tcc	RD, WR, ALE to CAS Delay	3tp + 25	4tp + 85	2
tsc	CMD Setup to Clock	15	1	1
tMRS	RD, WR setup to REFRQ	5	1	CAR
tCA	RD, WR, ALE to SACK Delay		2tp + 47	2
tcx	CAS to XACK Delay	5tp - 25	5tp + 20	
tcs	CAS to SACK Delay	5tp - 25	5tp + 40	2
tACK	XACK to CAS Setup	10		
txw	XACK Pulse Width	tp - 25		7
tck	SACK, XACK turn-off Delay		35	
tKCH	CMD Inactive Hold after SACK, XACK	10		
tLL	REFRQ Pulse Width	20		-
tCHS	CMD Hold Time	30		SACK
tRFR	REFRQ to RAS Delay		4tp + 100	6
tww	WR to WE Delay	0	50	8
tAD	CPU Address Delay	0	40	3

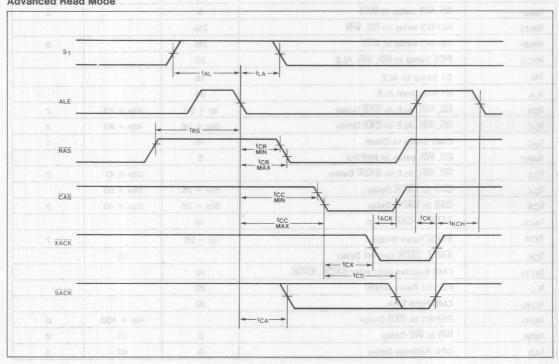


WAVEFORMS

### **Normal Read or Write Cycle**



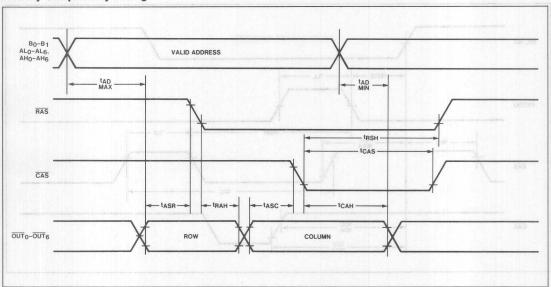
### **Advanced Read Mode**



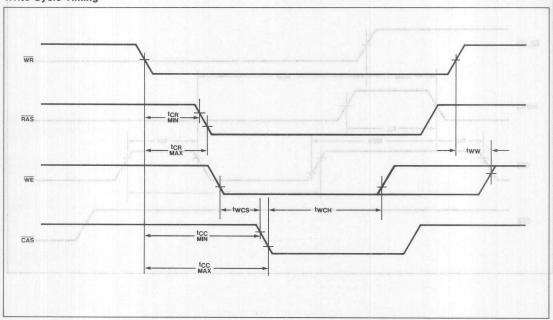


## **WAVEFORMS** (cont'd)

## **Memory Compatibility Timing**



## **Write Cycle Timing**

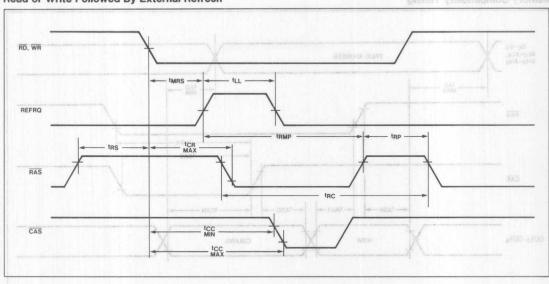


WAVEFORMS (cont'd)

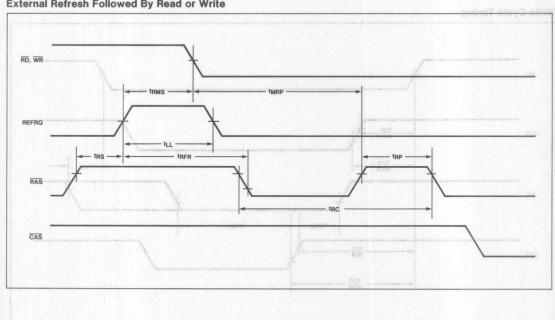


## WAVEFORMS (cont'd)

## Read or Write Followed By External Refresh



## **External Refresh Followed By Read or Write**



Clock And System Timing represents the design of the control of th

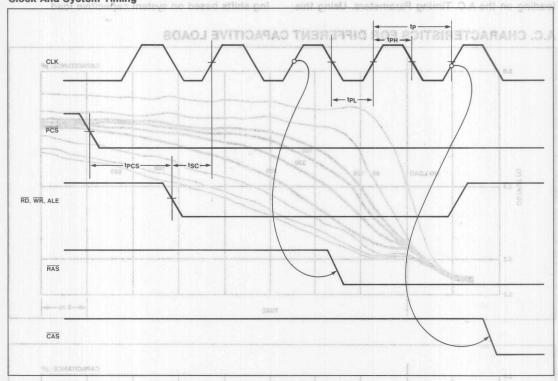
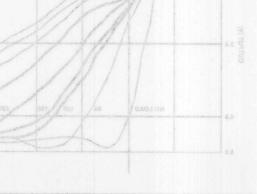


Table 2 8202A Output Test Loading.

Load	ing.
Pin	Test Load
SACK, XACK	C <sub>L</sub> = 30 pF
OUT <sub>0</sub> -OUT <sub>6</sub>	C <sub>L</sub> = 160 pF
RAS <sub>0</sub> -RAS <sub>3</sub>	C <sub>L</sub> = 60 pF
WE	C <sub>L</sub> = 224 pF
CAS	C <sub>I</sub> = 320 pF

#### NOTEC

- t<sub>SC</sub> is a reference point only. ALE, RD, WR, and REFRQ inputs do not have to be externally synchronized to 8202A clock.
- If t<sub>RS</sub> min and t<sub>MRS</sub> min are met then, t<sub>CA</sub>, t<sub>CR</sub>, and t<sub>CC</sub> are valid, otherwise t<sub>CS</sub> is valid.
- †ASR, †RAH, †ASC, †CAH, and †RSH depend upon B0-B1 and CPU address remaining stable throughout the memory cycle. The address inputs are not latched by the 8202A.
- 4. For back-to-back refresh cycles, tRC max = 13tp
- t<sub>RC</sub> max is valid only if t<sub>RMP</sub> min is met (READ, WRITE followed by REFRESH) or t<sub>MRP</sub> min is met (REFRESH followed by READ, WRITE).
- 6. tRFR is valid only if tRS min and tRMS min are met.
- 7. t<sub>XW</sub> min applies when RD, WR has already gone high. Otherwise XACK follows RD. WR.
- WE goes high according to twch or tww, whichever occurs first.



Use the Test Load as the base capacitance for estimating filming shifts for extent critical liming parameters.

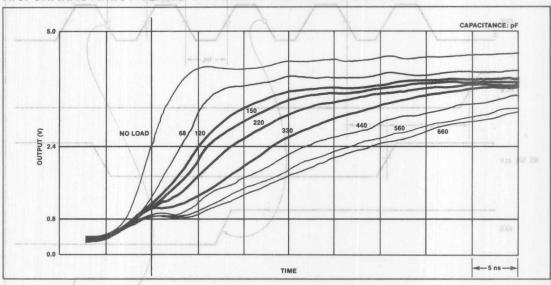


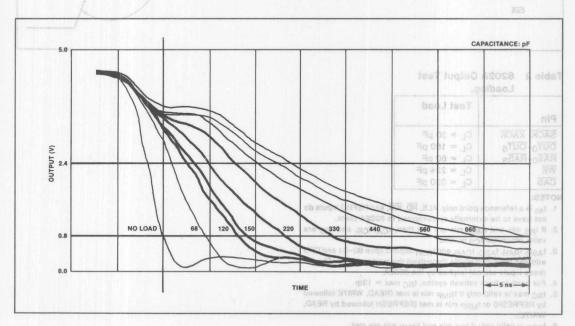


The typical rising and falling characteristic curves can be used to determine the effects of capacitive loading on the A.C. Timing Parameters. Using this

design tool in conjunction with the timing waveforms, the designer can determine typical timing shifts based on system capacitive load.

## A.C. CHARACTERISTICS FOR DIFFERENT CAPACITIVE LOADS





#### NOTE:

Use the Test Load as the base capacitance for estimating timing shifts for system critical timing parameters.

#### TYPICAL CONDITIONS:

 $T_A = 25^{\circ}C$  Pins not under test are loaded with Test Load  $V_{CC} = +5V$  capacitance.  $t_p = 50 \text{ ns}$ 



Example: Find the effect on t<sub>CR</sub> and t<sub>CC</sub> using 64 22. From the waveform diagrams, we determine that 2118 Dynamic RAMs configured in 4 banks.

- 1. Determine the typical RAS and CAS capacitance:
  From the data sheet RAS = 4 pF and CAS = 4 pF.

  ∴ RAS load = 64 pF + board capacitance.
  CAS load = 256 pF + board capacitance.
  Assume 2 pF/in (trace length) for board capacitance.
- m Decodes CPU Status for Advanced Read Capability in 16K mode
- Provides System Acknowledge and Transfer Acknowledge Signals
- m Refresh Cycles May be Internally or Externally Requested (For Transparent Refresh)
- g Internal Series Damping Resistors on All

- From the waveform diagrams, we determine that the falling edge timing is needed for t<sub>CR</sub> and t<sub>CC</sub>.
   Next find the curve that best approximates the test load; i.e., 68 pF for RAS and 330 pF for CAS.
- 3. If we use 72 pF for RAS loading, then the t<sub>CR</sub> (max.) spec should be increased by *about* 1 ns. Similarly if we use 288 pF for CAS, then t<sub>CC</sub> (min.) and (max.) should decrease about 1 ns.
- m Directly Addresses and Drives Up to 64
  Devices Without External Drivers
- m Provides Address Multiplexing and Strobes
- E Provides a Refresh Timer and a Refresh Counter
  - m Provides Refresh/Access Arbitration
  - a External or Internal Clock Capability

The Intel® 8203 is a Dynamic Ram System Controller designed to provide all signals necessary to use 2164, 2118, 2117, or 2104A Dynamic RAMs in microcomputer systems. The 8203 provides multiplexed addresses and address strobes, refresh/access arbitration. Refresh cycles can be started internally or externally.

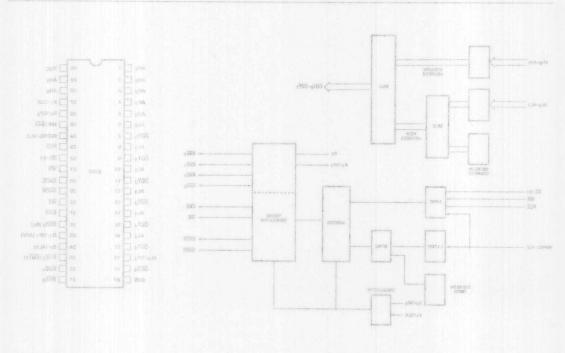


Figure 2. Pin Configuration

Flaure 1, 8203 Block Diagram

## end sets mixorque teed and 64K DYNAMIC RAM CONTROLLER

- Provides All Signals Necessary to Control 64K (2164), 16K (2117, 2118) and 4K (2104A) Dynamic Memories
- Directly Addresses and Drives Up to 64
  Devices Without External Drivers
- Provides Address Multiplexing and Strobes
- Provides a Refresh Timer and a Refresh Counter
- Provides Refresh / Access Arbitration
- **External or Internal Clock Capability**

- Fully Compatible with Intel® 8080A, 8085A, iAPX 88, and iAPX 86 Family Microprocessors
- Decodes CPU Status for Advanced Read Capability in 16K mode
- Provides System Acknowledge and Transfer Acknowledge Signals
- Refresh Cycles May be Internally or Externally Requested (For Transparent Refresh)
- Internal Series Damping Resistors on All Outputs

The Intel® 8203 is a Dynamic Ram System Controller designed to provide all signals necessary to use 2164, 2118, 2117, or 2104A Dynamic RAMs in microcomputer systems. The 8203 provides multiplexed addresses and address strobes, refresh logic, refresh/access arbitration. Refresh cycles can be started internally or externally.

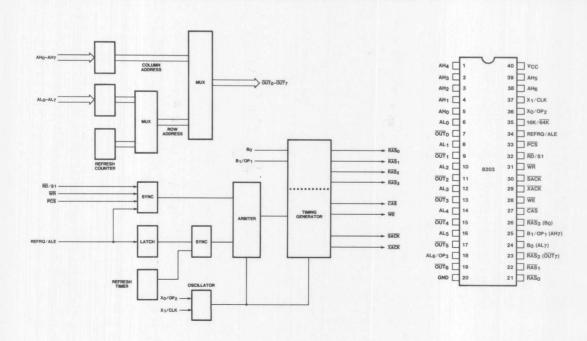


Figure 1. 8203 Block Diagram

Figure 2. Pin Configuration



anolice les noits Table 1. Pin Descriptions

Symbol	Pin No.	Туре	Name and Function
AL <sub>0</sub> AL <sub>1</sub> AL <sub>2</sub> AL <sub>3</sub> AL <sub>4</sub> AL <sub>5</sub> AL <sub>6</sub> /OP <sub>3</sub>	6 8 10 12 14 16 18	bns "a iniya ya I I pnitoer I (r X) d	Address Low: CPU address inputs used to generate memory row address. AL6/OP3 used to select 4K RAM mode.
AH <sub>0</sub> AH <sub>1</sub> AH <sub>2</sub> AH <sub>3</sub> AH <sub>4</sub> AH <sub>5</sub> AH <sub>6</sub>	5 4 3 2 1 39 38	pin 18 <sup>1</sup> ) chande 34, 21 4	Address High: CPU address in puts used to generate memory column address.
B <sub>0</sub> /AL <sub>7</sub> B <sub>1</sub> /OP <sub>1</sub> / AH <sub>7</sub>	25,0 upon leasin	differ the dos on the service sis will sequen	gate the appropriate RAS output
PCS	33 	G48	Protected Chip Select: Used to enable the memory read and write inputs. Once a cycle is started, it will not abort even it PCS goes inactive before cycle completion.
WR	31	T.A.	Memory Write Request.
RD/S1309 (p8) 10	Selek	t <b>r</b> bA nsd 8 eboW	Memory Read Request: St function used in Advanced Read mode selected by OP <sub>1</sub> (pin 25)
REFRQ/ ALE	34	0	External Refresh Request: ALE function used in Advanced Read mode, selected by OP <sub>1</sub> (pin 25).
OUT <sub>0</sub> OUT <sub>1</sub> OUT <sub>2</sub> OUT <sub>3</sub> OUT <sub>4</sub> OUT <sub>5</sub> OUT <sub>6</sub>	7 9 11 13 15 17 19	0 0 0 0 0 0 0	Output of the Multiplexer. These outputs are designed to drive the addresses of the Dynamic RAM array. (Note that the OUT <sub>0-7</sub> pins do not require inverters or drivers for proper operation.
WE	28	0 68	Write Enable: Drives the Write Enable inputs of the Dynamic RAM array.
CAS	27 sbc	Nead M	Column Address Strobe: This output is used to latch the Column Address into the Dynamic RAM array.

Symbol	Pin No.	Туре	Name and Function
RAS <sub>0</sub> RAS <sub>1</sub> RAS <sub>2</sub> / OUT <sub>7</sub> RAS <sub>3</sub> /B <sub>0</sub>	21 22 23 26	O O O coss	Row Address Strobe: Used to latch the Row Address into the bank of dynamic RAMs, selected by the 8203 Bank Select pins (B <sub>0</sub> , B <sub>1</sub> /OP <sub>1</sub> ). In 64K mode, only RAS <sub>0</sub> and RAS <sub>1</sub> are available; pin 23 operates as OUT <sub>7</sub> and pin 26 operates as the B <sub>0</sub> bank select input.
XACK			id data during a read cycle of data written during a write cycle
SACK 9 6	ALE mit te	awolle o	wait states. (Note: If a memory access request is made during a refresh cycle, SACK is delayed
X <sub>0</sub> /OP <sub>2</sub> X <sub>1</sub> /CLK The second of the second	iq ni upen l si qiri: eb iliv	retidus	Oscillator Inputs: These inputs are designed for a quartz crysta to control the frequency of the oscillator. If $X_0/OP_2$ is directly pulled up to $V_{CC}$ or if $X_0/OP_2$ is connected to a $1K\Omega$ resistor pulled to $+12V$ then $X_1/CLK$ becomes a TTL input for an external clock.
16K/64K		noi sit alor t ere ts	Mode Select: This input selects 16K mode (2117, 2118) or 64K mode (2164). Pins 23-26 change function based on the mode of operation.
VCC 30	40	of to er	Power Supply: +5V.
GND	20	sqmoo	Ground. 8058 erf ,abom and

## Functional Description Public 2AR own and to lea

The 8203 provides a complete dynamic RAM controller for microprocessor systems as well as expansion memory boards. All of the necessary control signals are provided for 2164, 2118, 2117, and 2104A dynamic RAM's.

The 8203 has three modes, one for 4K dynamic RAM's, one for 16K's and one for 64K's, controlled by pin 35 and pin 18.



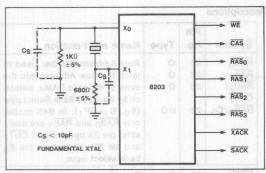


Figure 3. Crystal Operation

All 8203 timing is generated from a single reference clock. This clock is provided via an external oscillator or an on-chip crystal oscillator. All output signal transitions are synchronous with respect to this clock reference, except for the CPU handshake signals SACK and XACK.

CPU memory requests normally use the  $\overline{RD}$  and  $\overline{WR}$  inputs. The Advanced-Read mode allows ALE and S1 to be used in place of the  $\overline{RD}$  input.

Failsafe refresh is provided via an internal timer which generates refresh requests. Refresh requests can also be generated via the REFRQ input.

An on-chip synchronizer/arbiter prevents memory and refresh requests from affecting a cycle in progress. The READ, WRITE, and external REFRESH requests may be asynchronous to the 8203 clock; on-chip logic will synchronize the requests, and the arbiter will decide if the requests should be delayed, pending completion of a cycle in progress.

#### 16K/64K Option Selection

Pin 35 is a strap input that controls the two 8203 modes. Figure 4 shows the four pins that are multiplexed. In 16K mode (pin 35 tied to V<sub>CC</sub> or left open), the 8203 has two Bank Select inputs to select one of four RAS outputs. In this mode, the 8203 is exactly compatible with the Intel 8202A Dynamic RAM Controller. In 64K mode (pin 35 tied to GND), there is only one Bank Select input (pin 26) to select the two RAS outputs. More than two banks of 64K dynamic RAM's can be used with external logic.

#### **Other Option Selections**

The 8203 has three strapping options. When  $OP_1$  is selected (16K mode only), pin 32 changes from a  $\overline{RD}$  input to an S1 input, and pin 34 changes from a REFRQ input to an ALE input. See "Refresh Cycles" and "Read Cycles" for more detail.  $OP_1$  is selected by tying pin 25 to  $\pm$ 12V through a 5.1K ohm resistor.

When  $OP_2$  is selected, by connecting pin 36 to  $V_{CC}$ , pin 37 changes from a crystal input (X<sub>1</sub>) to the CLK input for an external TTL clock.

OP3 is selected by connecting pin 18 to +12V through a 5.1K ohm resistor, the 8203 will change its internal refresh timer from 128-row refresh (2164, 2118, 2117) to 64-row refresh (2104A).

#### **Refresh Timer**

The refresh timer is used to monitor the time since the last refresh cycle occurred. When the appropriate amount of time has elapsed, the refresh timer will request a refresh cycle. External refresh requests will reset the refresh timer.

#### **Refresh Counter**

The refresh counter is used to sequentially refresh all of the memory's rows. The 8-bit counter is incremented after every refresh cycle.

Pin #	16K Function	64K Function
23	RAS <sub>2</sub>	Address Output (OUT <sub>7</sub> )
24	Bank Select (B <sub>0</sub> )	Address Input (AL <sub>7</sub> )
25	Bank Select (B <sub>1</sub> )	Address Input (AH <sub>7</sub> )
26	RAS <sub>3</sub>	Bank Select (B <sub>0</sub> )

Figure 4. 16K/64K Mode Selection

Inputs			abon	Outputs			
na v obsti	Bo	B <sub>1</sub>	RAS <sub>0</sub>	RAS <sub>1</sub>	RAS <sub>2</sub>	RAS <sub>3</sub>	
r bengis	0	0	0	10	1	100	
16K	0	ola en	a tra	0	11	100	
Mode	(1) ve	0	1.1	10	0	100	
	1on o	atrice y	110	10	<b>31</b>	0 0	
64K	0	ovith to t	0	10	TI.	SELVO	
Mode	1		100910	0	8.7	aTUO	

Figure 5. Bank Selection

Description	Pin #	Normal Function	Option Function
B1/OP1(16K only)/AH7	25	Bank (RAS) Select	Advanced-Read Mode
X <sub>0</sub> /OP <sub>2</sub>	36	Internal (Crystal) Oscillator	External Oscillator
AL <sub>6</sub> /OP <sub>3</sub>	18	Address Input	64-Row Refresh

Figure 6. 8203 Option Selection



## Address Multiplexer and material latenage

The address multiplexer takes the address inputs and the refresh counter outputs, and gates them onto the address outputs at the appropriate time. The address outputs, in conjunction with the  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  outputs, determine the address used by the dynamic RAMs for read, write, and refresh cycles. During the first part of a read or write cycle, AL<sub>O</sub>-AL<sub>7</sub> are gated to  $\overline{\text{OUT}}_0-\overline{\text{OUT}}_7$ , then AH<sub>O</sub>-AH<sub>7</sub> are gated to the address outputs.

During a refresh cycle, the refresh counter is gated onto the address outputs. All refresh cycles are RAS-only refresh (CAS inactive, RAS active).

To minimize buffer delay, the information on the address outputs is inverted from that on the address inputs,

OUT<sub>0</sub>-OUT<sub>7</sub> do not need inverters or buffers unless additional drive is required.

## Synchronizer/Arbiter

The 8203 has three inputs, REFRQ/ALE (pin 34),  $\overline{RD}$  (pin 32) and  $\overline{WR}$  (pin 31). The  $\overline{RD}$  and  $\overline{WR}$  inputs allow an external CPU to request a memory read or write cycle, respectively. The REFRQ/ALE allows refresh requests to be requested external to the 8203.

All three of these inputs may be asynchronous with respect to the 8203's clock. The arbiter will resolve conflicts between refresh and memory requests, for both pending cycles and cycles in progress. Read and write requests will be given priority over refresh requests.

#### System Operation

The 8203 is always in one of the following states:

- a) IDLE
- b) TEST Cycle
- c) REFRESH Cycle
- d) READ Cycle in MARI only to second address and form at a body
- e) WRITE Cycle

The 8203 is normally in the IDLE state. Whenever one of the other cycles is requested, the 8203 will leave the IDLE state to perform the desired cycle. If no other cycles are pending, the 8203 will return to the IDLE state.

#### **Test Cycle**

The TEST Cycle is used to check operation of several 8203 internal functions. TEST cycles are requested by activating the  $\overline{PCS}$ ,  $\overline{RD}$  and  $\overline{WR}$  inputs. The TEST Cycle will reset the refresh address counter and perform a WRITE Cycle. The TEST Cycle should not be used in normal system operation, since it would affect the dynamic RAM refresh.

#### **Refresh Cycles**

The 8203 has two ways of providing dynamic RAM refresh:

- 1) Internal (failsafe) refresh
- 2) External (hidden) refresh had become the

Both types of 8203 refresh cycles activate all of the  $\overline{RAS}$  outputs, while  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{SACK}$ , and  $\overline{XACK}$  remain inactive.

Internal refresh is generated by the on-chip refresh timer. The timer uses the 8203 clock to ensure that refresh of all rows of the dynamic RAM occurs every 2 milliseconds (128 cycles) or every 4 milliseconds (256 cycles). If REFRQ is inactive, the refresh timer will request a refresh cycle every 10-16 microseconds.

External refresh is requested via the REFRQ input (pin 34). External refresh control is not available when the Advanced-Read mode is selected. External refresh requests are latched, then synchronized to the 8203 clock.

The arbiter will allow the refresh request to start a refresh cycle only if the 8203 is not in the middle of a cycle.

Simultaneous memory request and external refresh request will result in the memory request being honored first. This 8203 characteristic can be used to "hide" refresh cycles during system operation. A circuit similar to Figure 7 can be used to decode the CPU's instruction fetch status to generate an external refresh request. The refresh request is latched while the 8203 performs the instruction fetch; the refresh cycle will start immediately after the memory cycle is completed, even if the  $\overline{\rm RD}$  input has not gone inactive. If the CPU's instruction decode time is long enough, the 8203 can complete the refresh cycle before the next memory request is generated.

Certain system configurations require complete external refresh requests. If external refresh is requested faster than the minimum internal refresh timer (tREF), then, in effect, all refresh cycles will be caused by the external refresh request, and the internal refresh timer will never generate a refresh request.

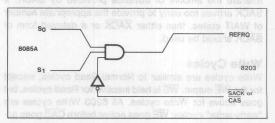


Figure 7. Hidden Refresh



### **Read Cycles**

The 8203 can accept two different types of memory Read requests:

- 1) Normal Read, via the RD input sells?) lement (f
- Advanced Read, using the S1 and ALE inputs (16K mode only)

The user can select the desired Read request configuration via the B1/OP1 hardware strapping option on pin 25.

s to deeden tadt s	Normal Read	Advanced Read
Pin 25	B1 input	+12 Volt Option
Pin 32	RD input	S1 input
Pin 34	REFRQ input	ALE input
# RAM banks	4 (RAS 0-3)	2 (RAS 2-3)
Ext. Refresh	Yes	No

Figure 8. 8203 Read Options

Normal Reads are requested by activating the  $\overline{\text{RD}}$  input, and keeping it active until the 8203 responds with an  $\overline{\text{XACK}}$  pulse. The  $\overline{\text{RD}}$  input can go inactive as soon as the command hold time (tCHS) is met.

Advanced Read cycles are requested by pulsing ALE while S1 is active; if S1 is inactive (low) ALE is ignored. Advanced Read timing is similiar to Normal Read timing, except the falling edge of ALE is used as the cycle start reference.

If a Read cycle is requested while a refresh cycle is in progress, then the 8203 will set the internal delayed-SACK latch. When the Read cycle is eventually started, the 8203 will delay the active SACK transition until XACK goes active, as shown in the AC timing diagrams. This delay was designed to compensate for the CPU's READY setup and hold times. The delayed–SACK latch is cleared after every READ cycle.

Based on system requirements, either SACK or XACK can be used to generate the CPU READY signal. XACK will normally be used; if the CPU can tolerate an advanced READY, then SACK can be used, but only if the CPU can tolerate the amount of advance provided by SACK. If SACK arrives too early to provide the appropriate number of WAIT states, then either XACK or a delayed form of SACK should be used.

#### Write Cycles

Write cycles are similiar to Normal Read cycles, except for the  $\overline{WE}$  output.  $\overline{WE}$  is held inactive for Read cycles, but goes active for Write cycles. All 8203 Write cycles are "early-write" cycles;  $\overline{WE}$  goes active before  $\overline{CAS}$  goes active by an amount of time sufficient to keep the dynamic RAM output buffers turned off.

## General System Considerations

All memory requests (Normal Reads, Advanced Reads, Writes) are qualified by the PCS input. PCS should be stable, either active or inactive, prior to the leading edge of RD, WR, or ALE. Systems which use battery backup should pullup PCS to prevent erroneous memory requests.

In order to minimize propagation delay, the 8203 uses an inverting address multiplexer without latches. The system must provide adequate address setup and hold times to guarantee RAS and CAS setup and hold times for the RAM. The tAD AC parameter should be used for this system calculation.

The B<sub>0</sub>-B<sub>1</sub> inputs are similiar to the address inputs in that they are not latched. B<sub>0</sub> and B<sub>1</sub> should not be changed during a memory cycle, since they directly control which RAS output is activated.

The 8203 uses a two-stage synchronizer for the memory request inputs (RD, WR, ALE), and a separate two stage synchronizer for the external refresh input (REFRQ). As with any synchronizer, there is always a finite probability of metastable states inducing system errors. The 8203 synchronizer was designed to have a system error rate less than 1 memory cycle every three years based on the full operating range of the 8203.

A microprocessor system is concerned when the data is valid after  $\overline{\text{RD}}$  goes low. See Figure 9. In order to calculate memory read access times, the dynamic RAM's A.C. specifications must be examined, especially the RAS-access time (tRAC) and the CAS-access time (tCAC). Most configurations will be CAS-access limited; i.e., the data from the RAM will be stable tcc,max (8203) + tCAC (RAM) after a memory read cycle is started. Be sure to add any delays (due to buffers, data latches, etc.) to calculate the overall read access time.

Since the 8203 normally performs "early-write" cycles, the data must be stable at the RAM data inputs by the time  $\overline{\text{CAS}}$  goes active, including the RAM's data setup time. If the system does not normally guarantee sufficient write data setup, you must either delay the  $\overline{\text{WR}}$  input signal or delay the 8203  $\overline{\text{WE}}$  output.

Delaying the  $\overline{\text{WR}}$  input will delay all 8203 timing, including the READY handshake signals,  $\overline{\text{SACK}}$  and  $\overline{\text{XACK}}$ , which may increase the number of WAIT states generated by the CPU.

If the WE output is externally delayed beyond the CAS active transition, then the RAM will use the falling edge of WE to strobe the write data into the RAM. This WE transition should not occur too late during the CAS active transition, or else the WE to CAS requirements of the RAM will not be met



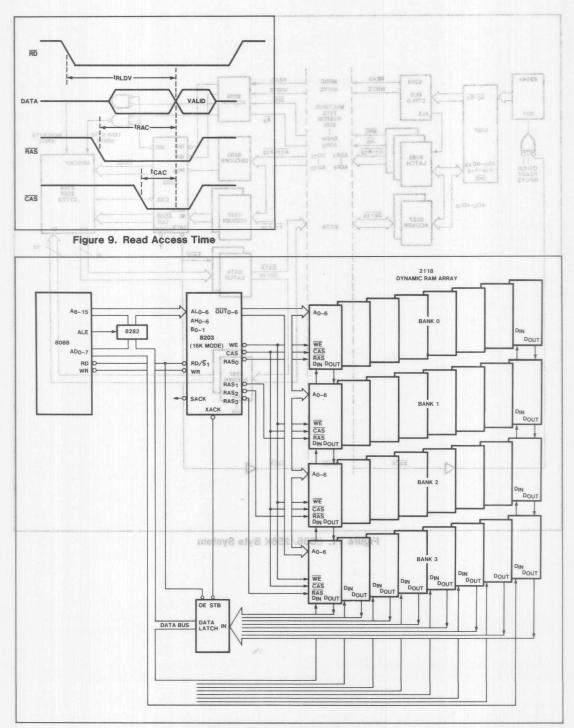
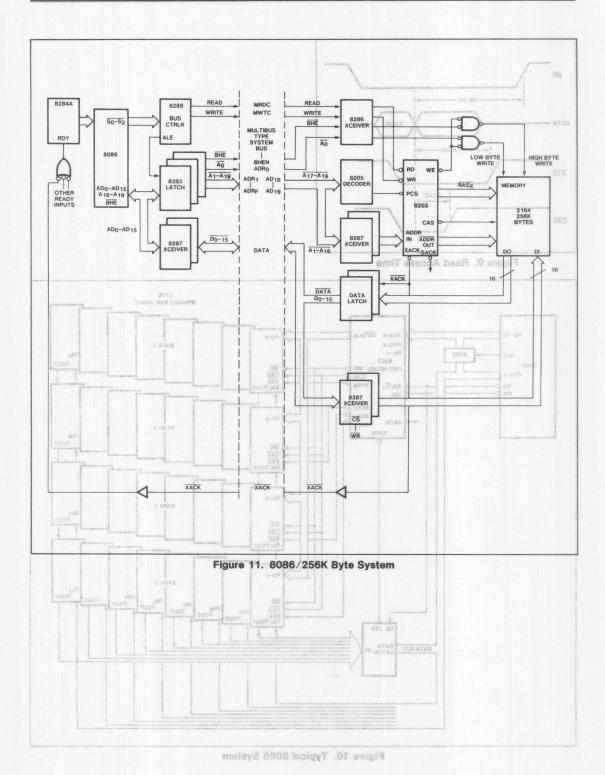


Figure 10. Typical 8088 System







#### **ABSOLUTE MAXIMUM RATINGS'**

Voltage On any Pin With Respect to Ground ..... -0.5V to +7V4 

\*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

External Clock High Time

S1 Setup to ALE

S i Hold from ALE

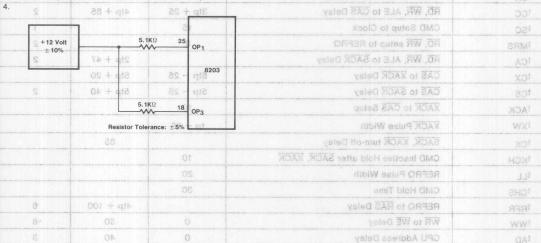
RD, WR, ALE to RAS Delay

AP

## D.C. CHARACTERISTICS TA = 0°C to 70°C; VCC = 5.0V ± 10% (5.0V ± 5% for 8203-3); GND = 0V

Symbol	Parameter	20	MinsHm 0	s (≥Maxed-	emiTUnits/teet	Test Conditions	jqt
V <sub>C</sub> 8.4	Input Clamp Volta	ge 08 - q101		-1.0	ydle Ti <b>v</b> e	IC = -5 mA	inc
Icc	Power Supply Cur	rent 91843		(9270 H)-	aelovmAd) em	Refresh T	1981
l <sub>F</sub>	Forward Input Cur	rent 91M3S		(8	me (128 cycle	Refresh T	1981
	CLK	4tp - 30		-2.0	narge Ame	V <sub>F</sub> = 0.45V	981
8	All Other Inputs <sup>3</sup>	5tp - 30		-320	Alter Aus	V <sub>F</sub> = 0.45V	наят
l <sub>R</sub> ε	Reverse Input Cur	rent308 - a		40	EAFµAt quie	V <sub>R</sub> = V <sub>CC</sub> (Note 1)	RSA
VOL 8	Output Low Volta	ge 01 - q			Iold From RAS	Address F	HAR!
8	SACK, XACK	06 - qt		0.45	stup toVCAS	IOL = 5 mA	tasc
8	All Other Outputs	00 - 018		0.45	BAD Word blod	IOL = 3 mA	HADI
VOH	Output High Volta	ge 01 - g/6			Width	V <sub>IL</sub> = 0.65 V	toas
	SACK, XACK All Other Outputs	DA - 61	2.4		to CAS	$I_{OH} = -1 \text{ mA}$ $I_{OH} = -1 \text{ mA}$	twes
V <sub>IL</sub> 8	Input Low Voltage	85 - qt8		0.8	trer CAS	V <sub>CC</sub> = 5.0V (Note 2)	IWCH
VIH1	Input High Voltage		2.0	VCC	LE, REPHO del	V <sub>CC</sub> = 5.0V	287
V <sub>IH2</sub>	Option Voltage	913		VCC	OWN CO of our	(Note 3)	SMB <sub>1</sub>
CIN 3	Input Capacitance	210		30	etup to RAS pF o to RD, WR, A	VDIAC = 25V VCC =	

<sup>3.</sup> Except for pin 36 in XTAL mode.



<sup>1.</sup> IR = 200 mA for pin 37 (CLK) for external clock mode.

<sup>2.</sup> For test mode RD & WR must be held at GND. tp + 30



## A.C. CHARACTERISTICS

 $T_A$  = 0°C to 70°C;  $V_{CC}$  = 5V  $\pm$  10% (5.0V  $\pm$  5% for 8203-3); GND = 0V

Measurements made with respect to RAS<sub>0</sub>-RAS<sub>3</sub>, CAS, WE, OUT<sub>0</sub>-OUT<sub>6</sub> are at 2.4V and 0.8V. All other pins are measured at 1.5V. All times are in nsec.

Symbol	Parameter subschape to absolute retended to AVV+ c	va.o-Min	to GroxaM	Notes /
tp	Clock Period	40	54	wer Dissipat
tpH	External Clock High Time	20		
tpL VO = GV	External Clock Low Time—above (>) 20 mHz	TA = 71°C to 70	CLEURICS	C. CHARI
tpL anoifib	External Clock Low Time—below (≤) 20 mHz	20	Parameter	lodmyê
tRC	Memory Cycle Time	10tp - 30	attoV c12tp) tugni	4, 5
tREF	Refresh Time (64 cycles—4K mode)	548tp 1097	576tp	33
tref	Refresh Time (128 cycles)	264tp	288tp	
tRP	RAS Precharge Time	4tp - 30	OLK	
trsh	RAS Hold After CAS	5tp - 30	All Other Inputs <sup>3</sup>	3
tASR (f atol)	Address Setup to RAS	tp - 30 mer	Reverse Input Cur	3 8
†RAH	Address Hold From RAS	tp - 10	Output Low Volter	3 10
tASC	Address Setup to CAS	tp - 30	SACK XACK	3
†CAH	Address Hold from CAS	5tp - 20	All Other Outputs	3
tCAS	CAS Pulse Width	5tp - 10	Output High Volta	140
twcs	WE Setup to CAS	tp - 40	ACACK, XACAC	
twch	WE Hold After CAS	5tp - 35		8
tRS	RD, WR, ALE, REFRQ delay from RAS	5tp	15 clio s ec - 2ndiii	2, 6
tMRP	RD, WR setup to RAS	0	Sauda učiri rodu.	5
tRMS	REFRQ setup to RD, WR	2tp	Option voltage	6 514
<sup>t</sup> RMP	REFRQ setup to RAS	2tp		5
tPCS	PCS Setup to RD, WR, ALE	20	Communique de qui	911
†AL	S1 Setup to ALE	15		1763:
tLA	S1 Hold from ALE	30 30 50 5 180	pvn 37 (CLK) for exter	1g = 200 mA for
tCR	RD, WR, ALE to RAS Delay	tp + 30	2tp + 70	nig tot 2esxill
tcc	RD, WR, ALE to CAS Delay	3tp + 25	4tp + 85	2
tsc	CMD Setup to Clock	15	91	11
tMRS	RD, WR setup to REFRQ	5 5 5	8.8	Boy St+ 2
tCA .	RD, WR, ALE to SACK Delay		2tp + 47	2
tcx	CAS to XACK Delay	5tp - 25	5tp + 20	
tcs	CAS to SACK Delay	5tp - 25	5tp + 40	2
†ACK	XACK to CAS Setup	10	5.0	
txw	XACK Pulse Width	tp - 25	select notation?	
tck	SACK, XACK turn-off Delay		35	
tKCH	CMD Inactive Hold after SACK, XACK	10		Trees of
tLL	REFRQ Pulse Width	20		
tCHS	CMD Hold Time	30		
trer	REFRQ to RAS Delay		4tp + 100	6
tww	WR to WE Delay	0	50	8
†AD	CPU Address Delay	0	40	3

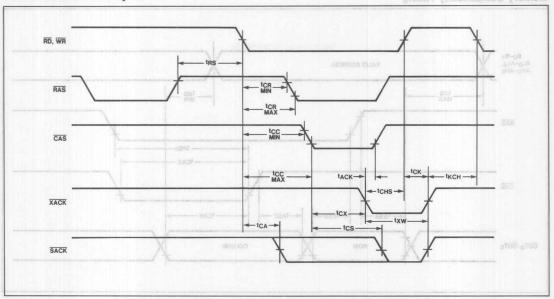
WAVEFORMS (cont'd)

Write Cycle Timing

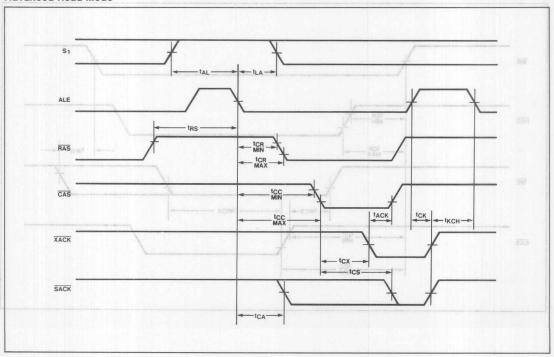


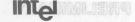
## **WAVEFORMS**

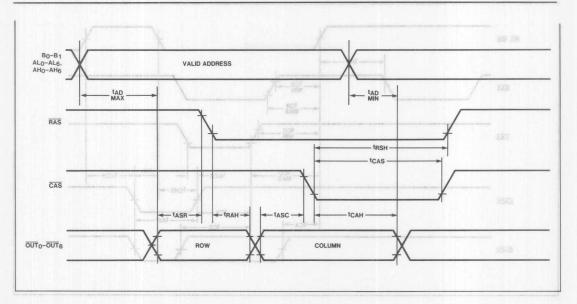
## **Normal Read or Write Cycle**



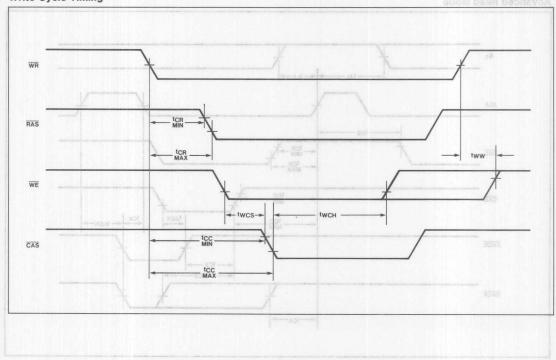
#### **Advanced Read Mode**

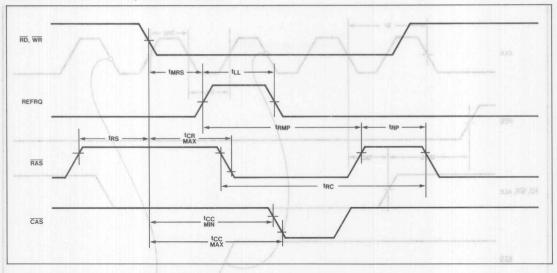




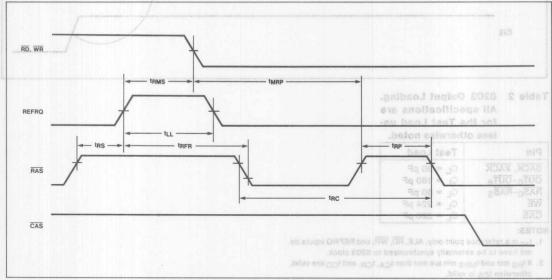


## Write Cycle Timing





#### External Refresh Followed By Read or Write



- 6. tgsp is valid only if the mix and trans min are that. 7. txyy min applies when RD, WR has already gone high. Otherwise
- 8. WE goes high according to twoy or tww. whichever occurs

#### WAVEFORMS (cont'd)



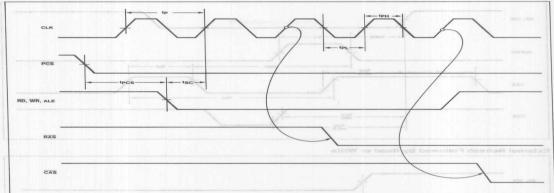


Table 2 8203 Output Loading. All specifications are for the Test Load unless otherwise noted.

Pin	Test Load		
SACK, XACK	CL = 30 pF CL = 160 pF		
RASO-RAS3	CL = 60 pF CL = 224 pF		
CAS	CL = 320 pF		

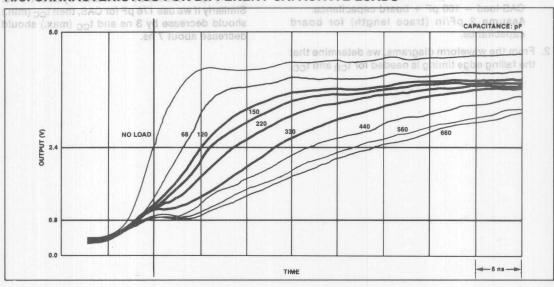
- 1. tac is a reference point only. ALE, RD, WR, and REFRQ inputs do not have to be externally synchronized to 8203 clock.
- 2. If t<sub>RS</sub> min and t<sub>MRS</sub> min are met then t<sub>CA</sub>, t<sub>CR</sub>, and t<sub>CC</sub> are valid, otherwise tos is valid.
- tASR, tRAH, tASC, tCAH, and tRSH depend upon B0-B1 and CPU address remaining stable throughout the memory cycle. The address inputs are not latched by the 8203.
- 4. For back-to-back refresh cycles, tRC max = 13tp
- 5. tBC max is valid only if tBMP min is met (READ, WRITE followed by REFRESH) or tMRP min is met (REFRESH followed by READ,
- t<sub>民民</sub> is valid only if t<sub>RS</sub> min and t<sub>RMS</sub> min are met.
   t<sub>XW</sub> min applies when RD, WR has already gone high. Otherwise XACK follows RD, WR.
- 8. WE goes high according to tWCH or tww. whichever occurs

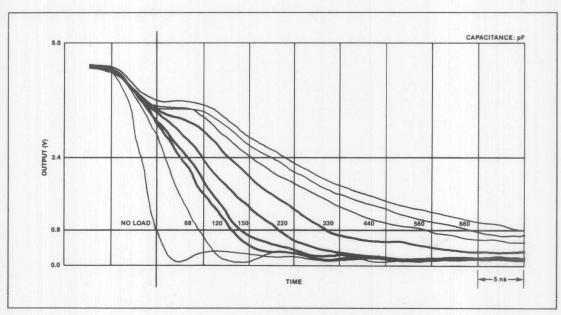


intel

The typical rising and falling characteristic curves can be used to determine the effects of capacitive loading on the A.C. Timing Parameters. Using this design tool in conjunction with the timing waveforms, the designer can determine typical timing shifts based on system capacitive load.

# A.C. CHARACTERISTICS FOR DIFFERENT CAPACITIVE LOADS of + Re 28 book and the control of the contr





#### NOTE

Use the Test Load as the base capacitance for estimating timing shifts for system critical timing parameters.

#### **TYPICAL CONDITIONS:**

 $T_{A} = 25^{\circ}C$   $V_{CC} = +5V$   $t_{p} = 50 \text{ ns}$ 

Pins not under test are loaded with Test Load capacitance.



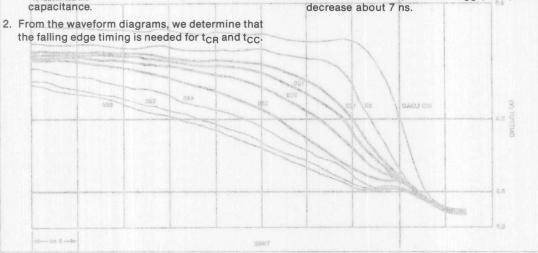


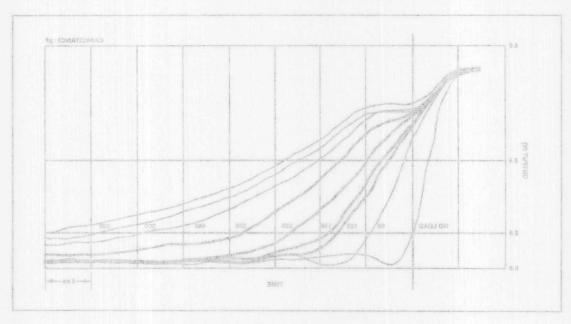
Example: Find the effect on t<sub>CR</sub> and t<sub>CC</sub> using 32 2164 Dynamic RAMs configured in 2 banks.

1. Determine the typical RAS and CAS capacitance: From the data sheet RAS = 5 pF and CAS = 5 pF. CAS load = 160 pF + board capacitance. Assume 2 pF/in (trace length) for board

Next find the curve that best approximates the evil test load; i.e., 68 pF for RAS and 330 pF for CAS.

3. If we use 88 pF for RAS loading, then t<sub>CR</sub> (min.) spec should be increased by about 1 ns, and ton .: RAS load = 80 pF + board capacitance. AGAD IM (max.) spec should be increased by about 2 ns. Similarly if we use 176 pF for CAS, then t<sub>CC</sub> (min.) should decrease by 3 ns and t<sub>CC</sub> (max.) should





 $t_0 = 50 \text{ rm}$ 

shifts for system critical timing parameters.

- Detects and Corrects All Single Bit
- Detects All Double Bit and Most **Multiple Bit Errors**
- 52 ns Maximum for Detection; 67 ns **Maximum for Correction (16 Bit** System) it is TOROT is In (matry)
- Expandable to Handle 80 Bit Memories

is active, it causes the 8206 to output all zeros at DOn.15

Syndrome Outputs for Error Logging

- Separate Input and Output Errors ugni esent c'3028 evate nt beau ete a dia o meteys tid Busses-No Timing Strobes Required
  - Supports Reads With and Without Correction, Writes, Partial (Byte) Writes, and Read-Modify-Writes
  - HMOS Technology for Low Power
  - 68 Pin Leadless JEDEC Package
  - Single +5V Supply

The HMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each 8206 handles 8 or 16 data bits and up to 8 check bits. 8206's can be cascaded to provide correction and detection for up to 80 bits of data. Other 8206 features include the ability to handle byte writes, memory initialization, and error logging.

with the proper write check bits on CBO.

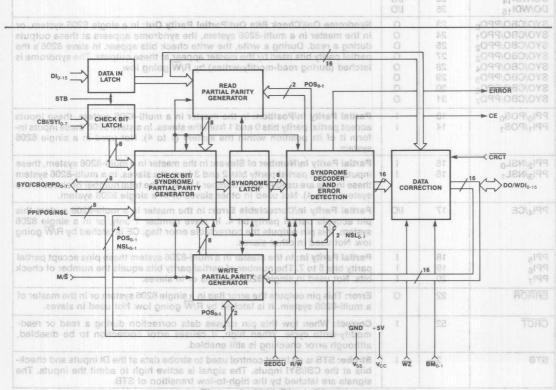


Figure 1. 8206 Block Diagram



Table 1. Pin Description

Symbol	Pin No.	Туре	Name and Function
DI <sub>0-15</sub>	1, 68-61, 59-53	T	Data In: These inputs accept a 16 bit data word from RAM for error detection and/or correction.
CBI/SYI <sub>0</sub> CBI/SYI <sub>1</sub> CBI/SYI <sub>2</sub> CBI/SYI <sub>3</sub>	5 6 6 7 8	ne luc simit :	Check Bits In/Syndrome In: In a single 8206 system, or in the master in a multi-8206 system, these inputs accept the check bits (5 to 8) from the RAM. In a single 8206 16 bit system, CBI <sub>0-5</sub> are used. In slave 8206's these inputs accept the syndrome from the master, with the syndrome latched by R/W going low.
CBI/SYI <sub>4</sub> CBI/SYI <sub>5</sub> CBI/SYI <sub>6</sub>	10 11	eethii eethii	Multiple Bit Errors Correction, 1
CBI/SYI7	12	-pagen	52 ns Maximum for Detection; 67 ns Writes, and
DO/WDI <sub>0</sub> DO/WDI <sub>1</sub> DO/WDI <sub>2</sub> DO/WDI <sub>3</sub> DO/WDI <sub>4</sub> DO/WDI <sub>5</sub> DO/WDI <sub>6</sub> DO/WDI <sub>7</sub>	51 50 49 48 47 46 45 44	1/0 1/0 1/0 1/0 1/0 1/0 1/0	<b>Data Out/Write Data In:</b> In a read cycle, data accepted by $Dl_{0-15}$ appears at these outputs corrected if $\overline{CRCT}$ is low, or uncorrected if $\overline{CRCT}$ is high. The $\overline{BN}$ inputs must be high to enable the output buffers during the read cycle. In a write cycle, data to be written into the RAM is accepted by these inputs for computing the write check bits. In a partial-write cycle, the byte not to be modified appears at either $DO_{0-7}$ if $\overline{BM_0}$ is high, or $DO_{8-15}$ if $\overline{BM_1}$ is high, for writing to the RAM. When $\overline{WZ}$ is active, it causes the 8206 to output all zeros at $DO_{0-15}$ with the proper write check bits on CBO.
DO/WDI <sub>8</sub>	11 42 ivo	10 1/0	e HMOS 8206 Error Detection and Correction Unit is a high-speed device
DO/WDI <sub>9</sub> DO/WDI <sub>10</sub>	41	1/0	rrection for memory systems (static and dynamic) requiring high reliab
DO/WDI11	39	1/0	ndles 8 or 16 data bits and up to 8 check bits. 8206's can be cascaded to pr
DO/WDI <sub>12</sub>	38 m	.al/O	to 80 bits of data. Other 8206 features include the ability to handle byte
DO/WDI <sub>13</sub> DO/WDI <sub>14</sub>	37 36	1/0	or logging.
DO/WDI <sub>14</sub> DO/WDI <sub>15</sub>	35	1/0	
SYO/CBO/PPO	23	0	Syndrome Out/Check Bits Out/Partial Parity Out: In a single 8206 system, o
SYO/CBO/PPO1	24	0	in the master in a multi-8206 system, the syndrome appears at these output
SYO/CBO/PPO2	25	0	during a read. During a write, the write check bits appear. In slave 8206's th
SYO/CBO/PPO3	27	0	partial parity bits used by the master appear at these outputs. The syndrome i
SYO/CBO/PPO <sub>4</sub> SYO/CBO/PPO <sub>5</sub>	28	0	latched (during read-modify-writes) by R/W going low.
SYO/CBO/PPO6	30	O	READ A POSS.
SYO/CBO/PPO7	31	0	BT8
PPI <sub>0</sub> /POS <sub>0</sub> PPI <sub>1</sub> /POS <sub>1</sub>	13 14		Partial Parity In/Position: In the master in a multi-8206 system, these input accept partial parity bits 0 and 1 from the slaves. In a slave 8206 these inputs in form it of its position within the system (1 to 4). Not used in a single 820 system.
PPI <sub>2</sub> /NSL <sub>0</sub>	15	1	Partial Parity In/Number of Slaves: In the master in a multi-8206 system, these
PPI <sub>3</sub> /NSL <sub>1</sub>	16	IRROD K	inputs accept partial parity bits 2 and 3 from the slaves. In a multi-8206 system these inputs are used in slave number 1 to tell it the total number of slaves in the system (1 to 4). Not used in other slaves or in a single 8206 system.
PPI <sub>4</sub> /CE	17	I/O	Partial Parity In/Correctable Error: In the master in a multi-8206 system thi
			pin accepts partial parity bit 4. In slave number 1 only, or in a single 820 system, this pin outputs the correctable error flag. CE is latched by R/W going low. Not used in other slaves.
PPI <sub>5</sub>	18	1	Partial Parity In: In the master in a multi-8206 system these pins accept partia
PPI <sub>6</sub>	19	1	parity bits 5 to 7. The number of partial parity bits equals the number of chec
PPI <sub>7</sub>	20	1	bits. Not used in single 8206 systems or in slaves.
ERROR	22	0	<b>Error:</b> This pin outputs the error flag in a single 8206 system or in the master o a multi-8206 system. It is latched by R/W going low. Not used in slaves.
CRCT	52	1,	Correct: When low this pin causes data correction during a read or read- modify-write cycle. When high, it causes error correction to be disabled although error checking is still enabled.
STB	2,43	À .	Strobe: STB is an input control used to strobe data at the DI inputs and check bits at the CBI/SYI inputs. The signal is active high to admit the inputs. The signals are latched by the high-to-low transition of STB.



Table 1	1. Pin	Description	(Continued)

Symbol	Pin No.	Туре	Name and Function	
d to be ove 0MB 1MB 1 1 The 8206 men word, using the	33 to a 32 to	portion bits fo	Byte Marks: When high, the Data Out pins are enabled for a read cycle. W low, the Data Out buffers are tristated for a write cycle. $\overline{BM}_0$ controls DO while $\overline{BM}_1$ controls DO <sub>8-15</sub> . In partial (byte) writes, the byte mark input is for the new byte to be written.	
new byte Want the memory.		ned wri	Read/Write: When high this pin causes the 8206 to perform detection an correction (if CRCT is low). When low, it causes the 8206 to generate check bit On the high-to-low transition the syndrome is latched internally for reamodify-write cycles.	
WZ 33	34 JOYO 3T	IAM-A	Write Zero: When low this input overrides the $\overline{BM}_{0-1}$ and $R/\overline{W}$ inputs to cause the 8206 to output all zeros at $DO_{0-15}$ with the corresponding check bits a $CBO_{0-7}$ . Used for memory initialization.	
M/S	or the 8206	ne dis ti	Master/Slave: Input tells the 8206 whether it is a master (high) or a slave (low	
SEDCU ber ain	mcEnory. T	embr in	Single EDC Unit: Input tells the master whether it is operating as a single 8206 (low) or as the master in a multi-8206 system (high). Not used in slaves.	
Vccelonad ai n	s c 06 ectio	riT lesi	Power Supply: +5V netsement of it asso bns (OS9) tugtuo ythis listra	
V <sub>SS</sub>	26, 43	rodify-v	Ground The master 6205 then generates and returns the executin bnurgh	
C. T. I.	HISTORY IN		indrome to the slaves (SYO) for correction of the	

# THROW and OF Outputs to determine it a correctable

The 8206 Error Detection and Correction Unit provides greater memory system reliability through its ability to detect and correct memory errors. It is a single chip device that can detect and correct all single bit errors and detect all double bit and some higher multiple bit errors. Some other odd multiple bit errors (e.g., 5 bits in error) are interpreted as single bit errors, and the CE flag is raised. While some even multiple bit errors (e.g., 4 bits in error) are interpreted as no error, most are detected as double bit errors. This error handling is a function of the number of check bits used by the 8206 (see Figure 2) and the specific Hamming code used. Errors in check bits are not distinguished from errors in a word.

For more information on error correction codes, see Intel Application Notes AP-46 and AP-73.

A single 8206 handles 8 or 16 bits of data, and up to 5 8206's can be cascaded in order to handle data paths of 80 bits. For a single 8206 8 bit system, the DI<sub>8-15</sub>, DO/WDI<sub>8-15</sub> and  $\overline{BM}_1$  inputs are grounded. See the Multi-Chip systems section for information on 24-80 bit systems.

The 8206 has a "flow through" architecture. It supports two kinds of error correction architecture: 1) Flow-through, or correct-always; and 2) Parallel, or check-only. There are two separate 16-pin busses.

DATA WORD BITS	
6206 outputs is signiff- mode the 6286 issues an	ntly shorteged. In this
nich can then perform one nen the curr 10 cycle for	several of lone: lengt
truction, perpen a diag-	rection, ratart the in
32	stic routine, etc. 7
eight bits ir04ength and	syndrome 7 ord, five to
formation about the exis- error, is made84 silable to	ntaining all necessary in
oins. Error logação may be	system at the SYO o-7
g the syndrome and the	complished by latchin smory add 8 ss of the w
72	8
80	RITE CYBLE

Figure 2. Number of Check Bits Used by 8206

one to accept data from the RAM (DI) and the other to deliver corrected data to the system bus (DO/WDI). The logic is entirely combinatorial during a read cycle. This is in contrast to an architecture with only one bus, with bidirectional bus drivers that must first read the data and then be turned around to output the corrected data. The latter architecture typically requires additional hardware (latches and/or transceivers) and may be slower in a system due to timing skews of control signals.



#### **READ CYCLE**

With the R/W pin high, data is received from the RAM outputs into the DI pins where it is optionally latched by the STB signal. Check bits are generated from the data bits and compared to the check bits read from the RAM into the CBI pins. If an error is detected the ERROR flag is activated and the correctable error flag (CE) is used to inform the system whether the error was correctable or not. With the BM inputs high, the word appears corrected at the DO pins if the error was correctable, or unmodified if the error was uncorrectable.

If more than one 8206 is being used, then the check bits are read by the master. The slaves generate a partial parity output (PPO) and pass it to the master. The master 8206 then generates and returns the syndrome to the slaves (SYO) for correction of the data.

The 8206 may alternatively be used in a "check-only" mode with the CRCT pin left high. With the correction facility turned off, the propagation delay from memory outputs to 8206 outputs is significantly shortened. In this mode the 8206 issues an ERROR flag to the CPU, which can then perform one of several options: lengthen the current cycle for correction, restart the instruction, perform a diagnostic routine, etc.

A syndrome word, five to eight bits in length and containing all necessary information about the existence and location of an error, is made available to the system at the SYO<sub>0-7</sub> pins. Error logging may be accomplished by latching the syndrome and the memory address of the word in error.

#### WRITE CYCLE

For a full write, in which an entire word is written to memory, the data is written directly to the RAM, bypassing the 8206. The same data enters the 8206 through the WDI pins where check bits are generated. The Byte Mark inputs must be low to tristate the DO drivers. The check bits, 5 to 8 in number, are then written to the RAM through the CBO pins for storage along with the data word. In a multi-chip system, the master writes the check bits using partial parity information from the slaves.

In a partial write, part of the data word is overwritten, and part is retained in memory. This is accomplished by performing a read-modify-write cycle. The complete old word is read into the 8206 and corrected,

with the syndrome internally latched by R/W going low. Only that part of the word not to be modified is output onto the DO pins, as controlled by the Byte Mark inputs. That portion of the word to be overwritten is supplied by the system bus. The 8206 then calculates check bits for the new word, using the byte from the previous read and the new byte from the system bus, and writes them to the memory.

### **READ-MODIFY-WRITE CYCLES**

On the high-to-low

Upon detection of an error the 8206 may be used to correct the bit in error in memory. This reduces the probability of getting multiple-bit errors in subsequent read cycles. This correction is handled by executing read-modify-write cycles.

The read-modify-write cycle is controlled by the R/W input. After (during) the read cycle, the system dynamic RAM controller or CPU examines the 8206 ERROR and CE outputs to determine if a correctable error occurred. If it did, the dynamic RAM controller or CPU forces R/W low, telling the 8206 to latch the generated syndrome and drive the corrected check bits onto the CBO outputs. The corrected data is available on the DO pins. The DRAM controller then writes the corrected data and corresponding check bits into memory.

The 8206 may be used to perform read-modify-writes in one or two RAM cycles. If it is done in two cycles, the 8206 latches are used to hold the data and check bits from the read cycle to be used in the following write cycle. The Intel 8207 Advanced Dynamic RAM controller allows read-modify-write cycles in one memory cycle. See the System Environment section.

#### INITIALIZATION

A memory system operating with ECC requires some form of initialization at system power-up in order to set valid data and check bit information in memory. The 8206 supports memory initialization by the write zero function. By activating the  $\overline{WZ}$  pin, the 8206 will write a data pattern of zeros and the associated check bits in the current write cycle. By thus writing to all memory at power-up, a controller can set memory to valid data and check bits. Massive memory failure, as signified by both data and check bits all ones or zeros, will be detected as an uncorrectable error.



#### **MULTI-CHIP SYSTEMS**

A single 8206 handles 8 or 16 bits of data and 5 or 6 check bits, respectively. Up to 5 8206's can be cascaded for 80 bit memories with 8 check bits.

When cascaded, one 8206 operates as a master, and all others as slaves. As an example, during a read cycle in a 32 bit system with one master and one slave, the slave calculates parity on its portion of the word—"partial parity"—and presents it to the master through the PPO pins. The master combines the partial parity from the slave with the parity it calculated from its own portion of the word to generate

the syndrome. The syndrome is then returned by the master to the slave for error correction. In systems of data and 5 or 6 with more than one slave the above description continues to apply, except that the partial parity outputs of the slaves must be XOR'd externally. Figure 3 shows the necessary external logic for multi-chip systems. Write and read-modify-write cycles are carried out analogously. See the System Operation section for multi-chip wiring diagrams.

There are several pins used to define whether the 8206 will operate as a master or a slave. Tables 2 and 3 illustrate how these pins are tied.

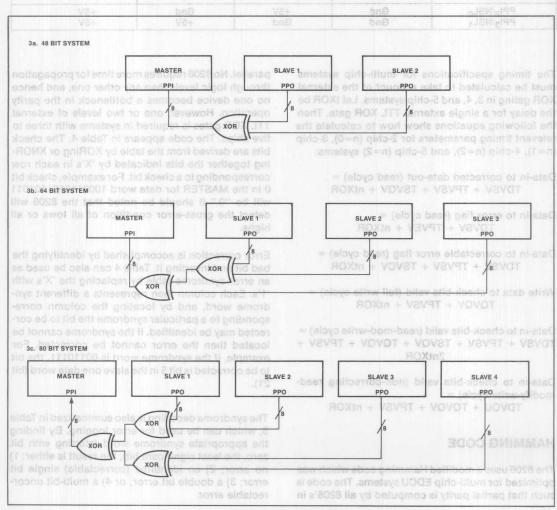


Figure 3. External Logic For Multi-Chip Systems



Table 2.	Master/Slave	Pin	<b>Assignments</b>
----------	--------------	-----	--------------------

Pin No.	eb Pin Name vala	Master	Slave 1	Slave 2	Slave 3	Slave 4
arity outputs	I is M/Sedi ted to	oxe N+5Vs of se	mit Gnd-aso s	d neo Gnd S8 a	of all Gnd toea	Gnd
erura Ville	SEDCU OX ad	laum +5Vala eri	+5V	+5V 9 4	+5V	+5V
13	PPI <sub>0</sub> /POS <sub>0</sub>	PPI and	Gnd	+5V	Gnd	+5V
14	PPI <sub>1</sub> /POS <sub>1</sub>	PPI	Gnd	Gnd	+5V	+5V
15	PPI <sub>2</sub> /NSL <sub>0</sub>	PPI	r, and · sys	HERM +5V Bels	+5V	80808+5V
38 16 STO	PPI3/NSL1	snobbblue mo	read . riec	onin+5Volqma	xe na+5V zeva	2 28 8+5V

\*See Table 3.

ter through the PPO pins. The master combines the DRI and There are several pins used to define whether the bar through the PPO partial partity from the slave. Tables 2 and 1 and 1

Dell 915	suid asaut won sia.	<b>Number of Slaves</b>	ab or niow aus to u	
Pin	1	2	3	4
PPI <sub>2</sub> /NSL <sub>0</sub>	Gnd	+5V	Gnd	+5V
PPI <sub>3</sub> /NSL <sub>1</sub>	Gnd	Gnd	+5V	+5V

The timing specifications for multi-chip systems must be calculated to take account of the external XOR gating in 3, 4, and 5-chip systems. Let tXOR be the delay for a single external TTL XOR gate. Then the following equations show how to calculate the relevant timing parameters for 2-chip (n=0), 3-chip (n=1), 4-chip (n=2), and 5-chip (n=2) systems:

Data-in to corrected data-out (read cycle) = TDVSV + TPVSV + TSVQV + ntXOR

Data-in to error flag (read cycle) = TDVSV + TPVEV + ntXOR

Data-in to correctable error flag (read cycle) = TDVSV + TPVSV + TSVCV + ntXOR

Write data to check-bits valid (full write cycle) = TQVQV + TPVSV + ntXOR

Data-in to check-bits valid (read-mod-write cycle) = TDVSV + TPVSV + TSVQV + TQVQV + TPVSV + 2ntXOR

Data-in to check-bits valid (non-correcting readmodify-write cycle) =

TDVQU + TQVQV + TPVSV + ntXOR

### **HAMMING CODE**

The 8206 uses a modified Hamming code which was optimized for multi-chip EDCU systems. The code is such that partial parity is computed by all 8206's in

parallel. No 8206 requires more time for propagation through logic levels than any other one, and hence no one device becomes a bottleneck in the parity operation. However, one or two levels of external TTL XOR gates is required in systems with three to five chips. The code appears in Table 4. The check bits are derived from the table by XORing or XNORing together the bits indicated by 'X's in each row corresponding to a check bit. For example, check bit 0 in the MASTER for data word 1000110110110111 will be "0." It should be noted that the 8206 will detect the gross-error condition of all lows or all highs.

Error correction is accomplished by identifying the bad bit and inverting it. Table 4 can also be used as an error syndrome table by replacing the 'X's with '1's. Each column then represents a different syndrome word, and by locating the column corresponding to a particular syndrome the bit to be corrected may be identified. If the syndrome cannot be located then the error cannot be corrected. For example, if the syndrome word is 00110111, the bit to be corrected is bit 5 in the slave one data word (bit 21).

The syndrome decoding is also summarized in Table 5, which can be used for error logging. By finding the appropriate syndrome word (starting with bit zero, the least significant bit), the result is either: 1) no error; 2) an identified (correctable) single bit error; 3) a double bit error; or 4) a multi-bit uncorrectable error.

Figure 3. External Logic For Multi-Chip Systems

### Table 4. Modified Hamming Code Check Bit Generation

Check bits are generated by XOR'ing (except for the CB0 and CB1 data bits, which are XNOR'ed in the Master) the data bits in the rows corresponding to the check bits. Note there are 6 check bits in a 16-bit system, 7 in a 32-bit system, and 8 in 48-or-more-bit systems.

SYTE NU	JMBER				0	25.00							1					OPERATION				2				22 18			3							4				0			- 5	7 6	3 111	
BIT NU	MBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7			1	2	3	4 5	6	7	0	1	2 3	3 4	5	6	7	0	1	2 :	3	4 5	6	7	0	1	2	3	4	5	6
	CB0 =	Х	х	-	X	-	x	х	-	х	0.	-	х	-	X	-	-	XNOR	-	X	х	X	- >	X	-	2	х	х -	-	×	-	-	x	x	-	x	- )	( )	-	x	-	-	х	-	x	-
38.113.43	CB1 =	X	-	X	-	-	X	-	X	-	X	/m.	X	X	-	X	-	XNOR	X	X	X	-	- )	( -	X	X	X	C	0	0-	C-	X	X	+ 0	X	. K	- )	(	X	0	X		X	X	-	X
CHECK	CB2 =	- 0	X	X	-	X	-	X	X	-	3-1	X	-	X	-	-	X	XOR	-	X	X	X	- )	X	X	100	-	x )	( -	-	-	-	-	X	X	-	χ .	. >	X	-	-	X	-	X	-	-
	CB3 =	X	X	X	X	X	-	-	-	X	X	X	-	-		-	-	XOR	X	X		13	x .	×	X	X	-	- 0	( X	0	0-	-	X	X	X	X	X	17	C.	X	X	X	-		- 03	
BITS	CB4 =	1-1	-	-	X	X	X	X	X	-	-	-	-	-	X	X	X	XOR	X	X	-	~	x )	X	X		-		· X	-	X	-	-	-	-	X	x )	( )	X	-	-	-	-	-	X	X
	CB5 =	-	-	-	-	-	-	-	-	X	Х	X	х	X	X	X	X	XOR	-	-	-	X	x )	X	X		-	10		X	X	X	X	X	X	X	X	()	X	-	65	d		50	-	-
	CB6 =	-	-	-/	-	-	1-	1	-	-	-	-	-	_	L	-	-	XOR	-	-	-	20	20 .	500	-3	X	Х	X X	( X	X	X	X	X	X	X	X	x )	( )	X	-	-	-	-	-	-	-
	CB7 =	-	-	-		-	-	-	-	-	-	-	-	-		-	-	XOR	-	-	-	1	10	8	-	1	-	10	63-1	4	97	0	2 4	- 2	- 0	- 9	- 6	0	17	X	X	X	X	X.	X	X
DATA	DITC	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1		1	1	1	1	2 2	2	2	2	2	2 2	2 2	2	3	3	3	3	3	3	3 3	3 3	3	4	4	4	4	4	4	4
DATA	0113	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5		6	7	8	9	0 1	2	3	4	5	6	8	9	0	1	2	3	4	5	6	7 8	9	0	1	2	3	4	5	6

16 BIT OR MASTER

SLAVE #1

SLAVE #2

BYTE N	JMBER				(	6							- 1	7	7						. 1	3								9				OPERATION
BIT NU	MBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	OF EMATION
	CB0 =	х	-	X	-	х	X	-	-	x	I	x	X	-	-	х	-	-	х	x	X	-	X	х	-	-5	X	X	10		x		21	XOR
	CB1 =	-	X	X	-	-	-	X	X	X	X	X	2	-	-	X	-	-	X	X	X	1_	X	х	х	-	-	X	X	-	-	-	-	XOR
CHECK	CB2 =	-	X	X	X	-	X	X	-	-	X	X	-	-	X		-	x		-	X	-	x	X	-	-0	X	X	140	-	X	845	X	XOR
	CB3 =	X	2	X	-	-	X	X	-	X	X	-	_	X	X	-	-	-	X	X	X	X	-	1	x	X	X	1	-	x	_	-		XOR
BITS	CB4 =	-	-	-	X	X	X	X	X	-	-	-	-	-	X	X	X	-	X	X	-3	20	-	X	x	X	X	X	9 -	3 -5	2 -	X	3-1	XOR
	CB5 =	-	-	-	-	-	-	-	-	X	X	Х	X	X	X	X	X	x	_	X	X	X	X	0	x	-	-	1	x	_	-	1	X	XOR
	CB6 =	х	X	X	X	X	X	X	X	-	-	-	-	_	-	-	-	X	X	-	-0	X	X	X	x	-	_	-	_	x	L	X	-	XOR
1-4	CB7 =	-	-	-	-	-	-	-	-	X	X	х	х	X	X	X	X	-	-	-	-8	T	-	9	3	X	X	X	X	X	X	X	X	XOR -
DATA	DITC	4	4	5	5	5	5	5	5	5	5	5	5	6	6	6	6	6	6	6	6	6	6	7	7	7	7	7	7	7	7	7	7	
DATA	BIIS	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	77007

SLAVE #3

SLAVE #4

AFN-01966A

1-104



Table 5. Sy	ndrome	Decoding
-------------	--------	----------

				0 0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
,	Syndr			1 0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	Bi			2 0	0	0	0	1	1	1	1	0	0	0	0	1	20	1	1
7	6	5	4	3 0	0	0	0	0	0	0	0	P 18	1	1	1	× 100	1	1	1
0	0	0	0	N	CB0	CB1	D	CB2	D	D	18	CB3	D	D	× 0	D	1	2	D
0	0	0	1	CB4	D	D	5	D	6	.7	D	D	' 3'	16	D	4	D	D	517m
0	0	1	0	CB5	D	D	11	D	19	12	D	D	. 8	9	D	10	D	D	67
0	0	1	1	D	13	14	D	15	D	D	21	20	×D	$\times$ D	66	D	22	23	Do
0	1	0	0	CB6	D	D	25	D	26	49	D	D	48	24	× D	27	D	D	50
0	1	0	18	D.	52	55	D.	51	D	D	70	28	× D	×D	65	Del	53	54	D
0	1	1	0	XXDO	29	31	D	64	D	D	69	68	×D	×D	32	D	33	34	D
0	1	1	1	30	D	D	37	D	38	39	D	D	35	× 71	, D	36	D	D	U
1	0	0	0	CB7	D	D	43	D	77	44	D	D	40	41	× D	42	D	D	EU0
1	0	0	1	D	45	46	D	47	D	D	74	72	× Ď	D	×U	D	73	U	D
1	0	1	0	D	59	75	D	79	D	D	58	60	D	D	56	D	U	57	D
1	0	1	1	63	D	D	62	D	U	U	D	D	Û	U	D	61	D	D	U
1	1	0	0	D	Ü	U	Do	U	D	D	U	76	D	D	Ú	D	U	U	0 D
1	1	0	1	78	D	D	U	D	U	U	D	D	Ü	Ú	D	U	D	D	U
1	191	1	0	U	D	D	U	D	U	U	D	D	U	Ü	D	U	<sub>O</sub> D	D	U
1	11	1	1	D.	U	U	D	U	D	D	U	U	D	D	Ü	D	U	U	D

N = No Error ××××××××

CBX = Error in Check Bit X × X = Error in Data Bit X × X

D = Double Bit Error

U = Uncorrectable Multi-Bit Error

### SYSTEM ENVIRONMENT

The 8206 interface to a typical 32 bit memory system is illustrated in Figure 4. For larger systems, the partial parity bits from slaves two to four must be

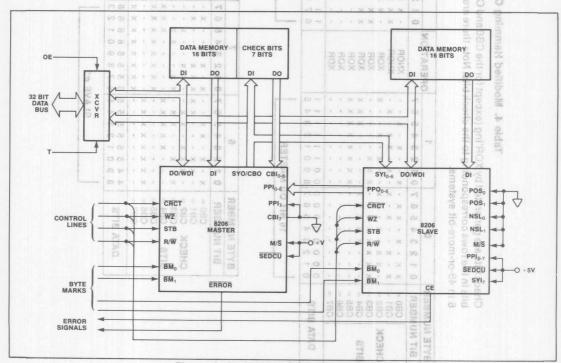


Figure 4. 32-Bit 8206 System Interface



XOR'ed externally, which calls for one level of XOR gating for three 8206's and two levels for four or five 8206's.

to the check bits memory held inactive, and then performing ordinary reads. The

The 8206 is designed for direct connection to the Intel 8207 Advanced Dynamic RAM Controller, due to be sampled in the first quarter of 1982. The 8207 has the ability to perform dual port memory control,

and Figure 5 illustrates a highly integrated dual port RAM implementation using the 8206 and 8207. The 8206/8207 combination permits such features as automatic scrubbing (correcting errors in memory during refresh), extending RAS and CAS timings for Read-Modify-Writes in single memory cycles, and automatic memory initialization upon reset. Together these two chips provide a complete dual-port, error-corrected dynamic RAM subsystem.

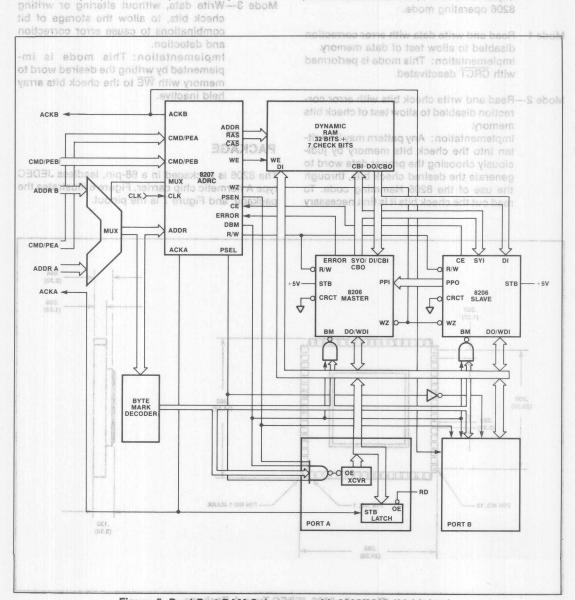


Figure 5. Dual Port RAM Subsystem with 8206/8207 (32-bit bus)



#### MEMORY BOARD TESTING aviil a stupi if bris

The 8206 lends itself to straightforward memory board testing with a minimum of hardware overhead. The following is a description of four common test modes and their implementation.

- Mode 0—Read and write with error correction.
  Implementation: This mode is the normal 8206 operating mode.
- Mode 1—Read and write data with error correction disabled to allow test of data memory.

  Implementation: This mode is performed with CRCT deactivated.

Mode 2-Read and write check bits with error cor-

rection disabled to allow test of check bits memory.

Implementation: Any pattern may be written into the check bits memory by judiciously choosing the proper data word to generate the desired check bits, through the use of the 8206 Hamming code. To

read out the check bits it is first necessary

to fill the data memory with all zeros, which may be done by activating WZ and incrementing memory addresses with WE to the check bits memory held inactive, and then performing ordinary reads. The check bits will then appear directly at the SYO outputs, with bits CB0 and CB1 inverted.

Mode 3—Write data, without altering or writing check bits, to allow the storage of bit combinations to cause error correction and detection.

Implementation: This mode is im-

Implementation: This mode is implemented by writing the desired word to memory with WE to the check bits array held inactive.

### PACKAGE

The 8206 is packaged in a 68-pin, leadless JEDEC type A hermetic chip carrier. Figure 6 illustrates the package, and Figure 7 is the pinout.

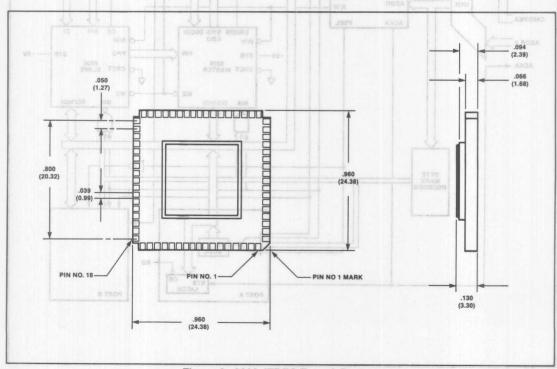


Figure 6. 8206 JEDEC Type A Package



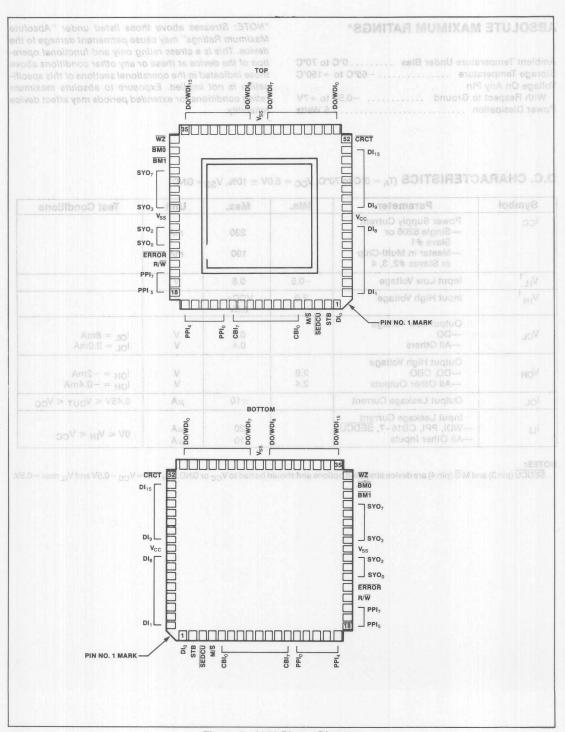


Figure 7. 8206 Pinout Diagram



### **ABSOLUTE MAXIMUM RATINGS\***

 \*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### D.C. CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5.0V ± 10%, VSS = GND)

Symbol	Parameter -	Min.	Max.	Unit	Test Conditions
lcc	Power Supply Current —Single 8206 or Slave #1 —Master in Multi-Chip or Slaves #2, 3, 4		230 190	mA mA	3
V <sub>IL</sub> <sup>1</sup>	Input Low Voltage	-0.5	0.8	V	
V <sub>IH</sub> <sup>1</sup>	Input High Voltage	2.0	VCC+ 0.5V	V	
V <sub>OL</sub>	Output Low Voltage —DO —All Others	C 20 20 20 20 20 20 20 20 20 20 20 20 20	0.4 0.4	V	I <sub>OL</sub> = 8mA I <sub>OL</sub> = 2.0mA
V <sub>OH</sub>	Output High Voltage —DO, CBO —All Other Outputs	2.6 2.4		V	I <sub>OH</sub> = -2mA I <sub>OH</sub> = -0.4mA
loL	Output Leakage Current		±10	μΑ	0.45V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>
ILI	Input Leakage Current —WDI, PPI, CB16-7, SEDCU —All Other Inputs	V.	20 10	μA μA	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>

#### NOTES

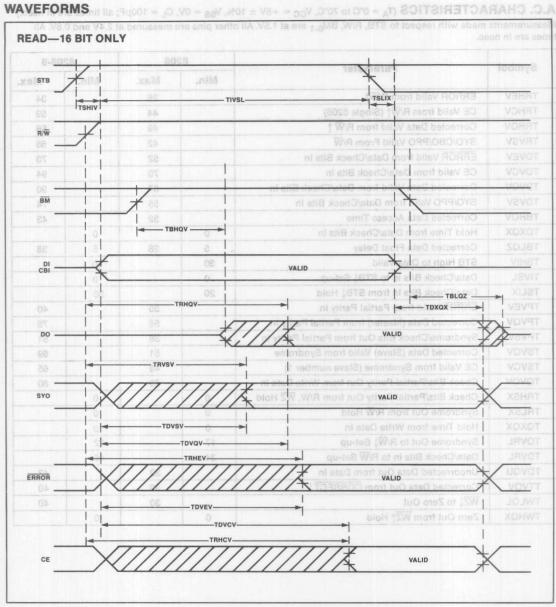
1. SEDCU (pin 3) and M/S (pin 4) are device strapping options and should be tied to  $V_{CC}$  or GND.  $V_{IH}$  min =  $V_{CC}$  -0.5V and  $V_{IL}$  max = 0.5V.



**A.C. CHARACTERISTICS** ( $T_A = 0^{\circ}C$  to  $70^{\circ}C$ ,  $V_{CC} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $C_L = 100pF$ ; all times are in nsec.) Measurements made with respect to STB, R/W,  $\overline{BM}_{0-1}$  are at 1.5V. All other pins are measured at 2.4V and 0.8V. All times are in nsec.

Cumbal	Parameter	82	206	82	06-8
Symbol	Parameter	Min.	Max.	Min.	Max
TRHEV	ERROR Valid from R/W↑	107	25		34
TRHCV	CE Valid from R/W↑ (Single 8206)		44	Virial	59
TRHQV	Corrected Data Valid from R/W ↑		49	M	66
TRVSV	SYO/CBO/PPO Valid From R/W		42	1	- 56
TDVEV	ERROR Valid from Data/Check Bits In		52		70
TDVCV	CE Valid from Data/Check Bits In		70		94
TDVQV	Corrected Data Valid from Data/Check Bits In		67		90
TDVSV	SYO/PPO Valid from Data/Check Bits In		55		74
TBHQV	Corrected Data Access Time		32		43
TDXQX	Hold Time from Data/Check Bits In	0	1537ps	0	
TBLQZ	Corrected Data Float Delay	5	28	5	38
TSHIV	STB High to Data Valid	30		40	10
TIVSL	Data/Check Bits In to STB↓ Set-up	0		0	
TSLIX	Data/Check Bits In from STB↓ Hold	20		30	
TPVEV	ERROR Valid from Partial Parity In	VCIG	30		40
TPVQV	Corrected Data (Master) from Partial Parity In	N.	56		76
TPVSV	Syndrome/Check Bits Out from Partial Parity In	35	38		51
TSVQV	Corrected Data (Slave) Valid from Syndrome		51		69
TSVCV	CE Valid from Syndrome (Slave number 1)		48		65
TQVQV	Check Bits/Partial Parity Out from Write Data In	7777	59		80
TRHSX	Check Bits/Partial Parity Out from R/W, WZ Hold	0		0	048
TRLSX	Syndrome Out from R/W Hold	0		0	
TQXQX	Hold Time from Write Data In	0	revat	0	
TQVRL	Syndrome Out to R/W  ↓ Set-up	17-7070		22	
TDVRL	Data/Check Bits In to R/W Set-up	34		46	
TDVQU	Uncorrected Data Out from Data In	11111	32	Val	43
TTVQV	Corrected Data Out from CORRECT↓	7777	30		40
TWLQL	WZ↓ to Zero Out		30		40
TWHQX	Zero Out from WZ↑ Hold	0		0	

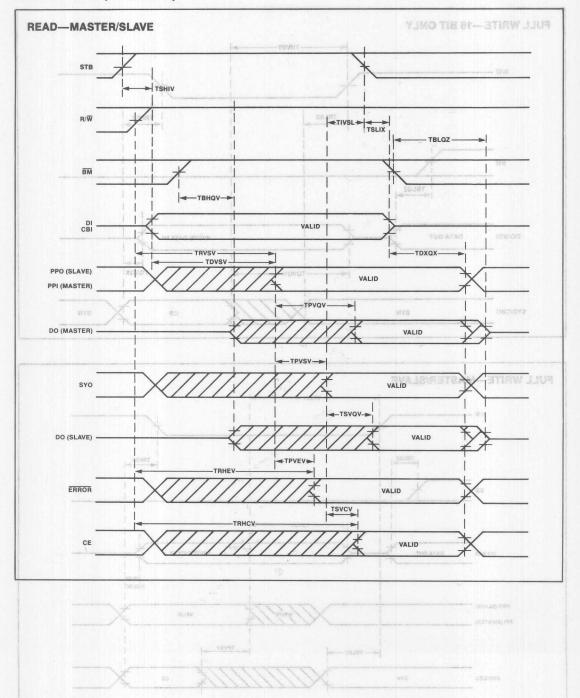




WAVEFORMS (Continued)



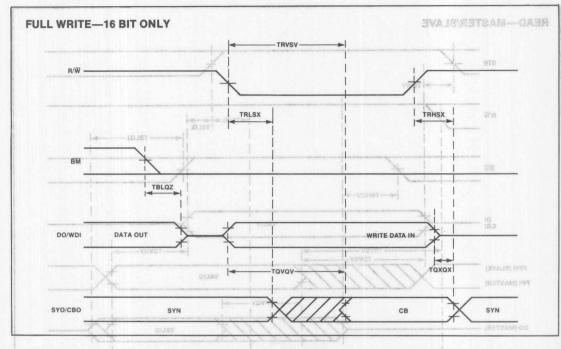
### **WAVEFORMS (Continued)**

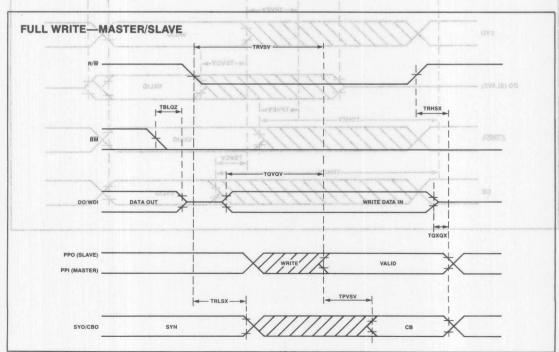


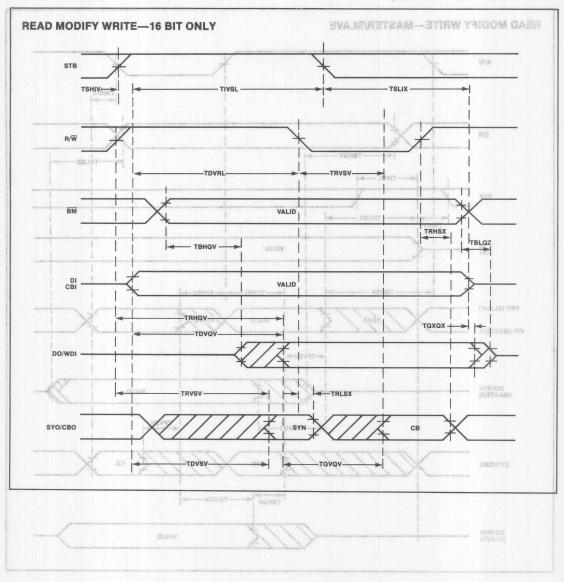


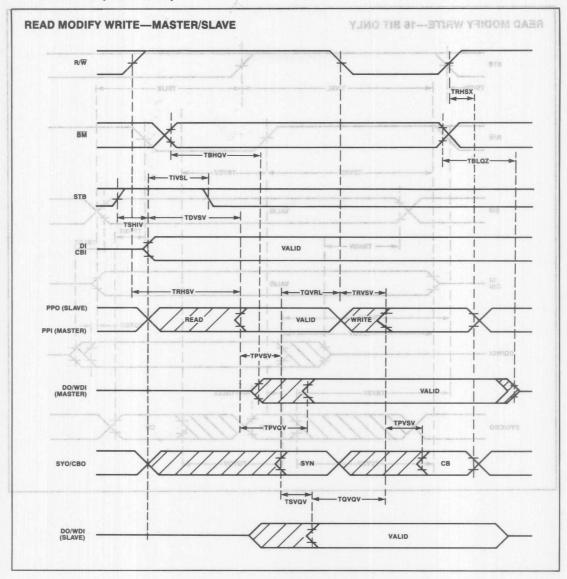
### **WAVEFORMS (Continued)**

### WAVEFORMS (Continued)



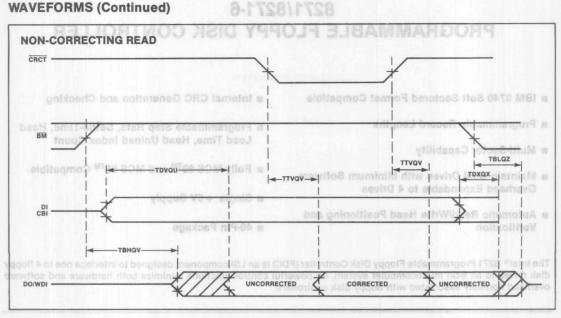


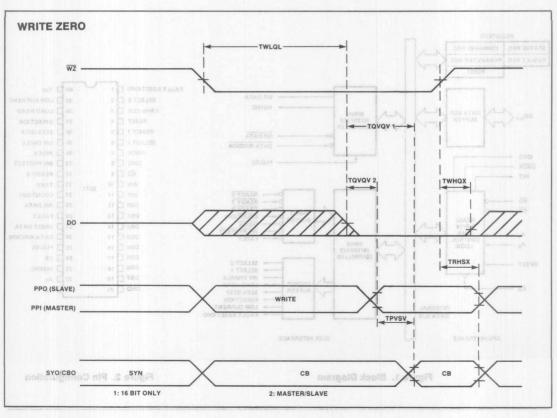






### **WAVEFORMS (Continued)**









## 8271/8271-6 PROGRAMMABLE FLOPPY DISK CONTROLLER

- IBM 3740 Soft Sectored Format Compatible
- Programmable Record Lengths
- m Multi-Sector Capability
- Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives
- Automatic Read/Write Head Positioning and Verification

- Internal CRC Generation and Checking
- Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count
- Fully MCS-80<sup>TM</sup> and MCS-85<sup>TM</sup> Compatible
- Single +5V Supply
- 40-Pin Package

The Intel® 8271 Programmable Floppy Disk Controller (FDC) is an LSI component designed to interface one to 4 floppy disk drives to an 8-bit microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk controllers.

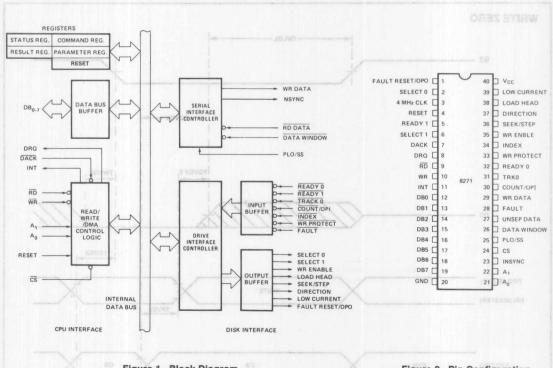


Figure 1. Block Diagram

Figure 2. Pin Configuration





Table 1. Pin Description

Symbol	Pin No.	Туре	Name and Function					
V <sub>CC</sub>	40	providir esult of	+5V Supply.					
GND	20	atri lost	Ground.					
Clock	3	emmos (	Clock: A square wave clock.					
Reset ass assignment of the second of the se	rais. If an nais can i	WA sign	Reset: A high signal on the reset input forces the 8271 to an idle state. The 8271 remains idle until a command is issued by the CPU. The output signals of the drive interface are forced inactive (LOW). Reset must be active for 10 or more clock cycles.					
CS tamot	24 priwolio	opnate has the t	Chip Select: The I/O Read and I/O Write inputs are enabled by the chip select signal.					
DB <sub>7</sub> -DB <sub>0</sub>	19-12	1/0	Data Bus: The Data Bus lines are bidirectional, three-state lines (8080 data bus compatible).					
WR SVIROUS	10	ī	Write: The Write signal used to signal the cont logic that a transfer of d from the data bus to the 82 is required.					
RD dhut etiu etiupet s		l mmands arametes	Read: The Read signal is used to signal the control logic that a transfer of data from the 8271 to the data bus is required.					
INT	11	0	Interrupt: The interrupt signal indicates that the 8271 requires service.					
A <sub>1</sub> -A <sub>0</sub>	22-21	ì	Address Line: These two lines are CPU Interface Reg- ister select lines.					
DRQ	8 coup entry	O (qque of	Data Request: The DMA request signal is used to request a transfer of data between the 8271 and memory.					
DACK		as a god	Data Acknowledge: The DMA acknowledge signal notifies the 8271 that a DMA cycle has been granted. For non-DMA transfers, this signal should be driven in the manner of a "Chip Select."					
Select 1- 6 O Select 0 2			Selected Drive: These lines are used to specify the selected drive. These lines are set by the command byte.					

Symbol	Pin No.	Туре	Name and Function
This pin is use a type of dai		Singl to sp separ	Fault Reset: The optional fault reset output line is used to reset an error condition which is latched by the drive. If this line is not used for a fault reset it can be used as an optional output line. This line is set with the write special register command.
Write Enable	35	o o o	Write Enable: This signal enables the drive write logic.
Seek/Step	36 189 WG		Seek/Step: This multi- function line is used during drive seeks.
Direction  The state of the sta	high wi high! high! by deb rollor		Direction: The direction line specifies the seek direction. A high level on this pin steps the R/W head toward the spindle (step-in), a low level steps the head away from the spindle (step-out).
Load Head	38	0	Load Head: The load head line causes the drive to load the Read/Write head against the diskette.
Low Current	39	поп	Low Current: This line notifies the drive that track 43 or greater is selected.
Ready 1, Ready 0	5 32		Ready 1: These two lines indicate that the specified drive is ready.
Fault natural	vonnii		Fault: This line is used by the drive to specify a file unsafe condition.
Count/OPI and include axioest bed to the conditions to conditions and retries	satible rdling the Of I with i	and har relieves sociated OC aup	Count/OPI: If the optional seek/direction/count seek mode is selected, the count pin receives pulses to step the R/W head to the desired track. Otherwise, this line can be used as an optional input.
Write Protect	33	ead/wri	Write Protect: This signal specifies that the diskette inserted is write protected.
TRKO meni b	rack		Track Zero: This signal indicates when the R/W head is positioned over track zero.
Index	34	sk directived the ted, no	Index: The index signal gives an indication of the relative position of the diskette.



Table 1	Din	Description	(Continued)

Symbol 5	Pin No.	Туре	Name and Function
PLO/SS		toute to res which	Phase-Locked Oscillator/ Single Shot: This pin is used to specify the type of data separator used.
Write Data	29	el enil	Write Data: Composite write data.
Unseparated Data	27 dana yadzas	esistW edene	Unseparated Data: This input is the unseparated data and clocks.
Data Window	26	Speki function drive to	Data Window: This is a data window established by a single-shot or phase-locked oscillator data separator.
INSYNC Negation of the state of the work of the work from the state of	e 23 e en vel en vir	A high the H spind steps spind	Input Synchronization: This line is high when 8271 has attained input data synchronization, by detecting 2 bytes of zeros followed by an expected Address Mark. It will stay high until the end of the ID or data field.

#### **FUNCTIONAL DESCRIPTION**

#### General

The 8271 Floppy Disk Controller (FDC) interfaces either two single or one dual floppy drive to an eight bit microprocessor and is fully compatible with Intel's new high performance MCS-85 microcomputer system. With minimum external circuitry, this innovative controller supports most standard, commonly-available flexible disk drives including the mini-floppy.

The 8271 FDC supports a comprehensive soft sectored format which is IBM 3740 compatible and includes provision for the designating and handling of bad tracks. It is a high level controller that relieves the CPU (and user) of many of the control tasks associated with implementing a floppy disk interface. The FDC supports a variety of high level instructions which allow the user to store and retrieve data on a floppy disk without dealing with the low level details of disk operation.

In addition to the standard read/write commands, a scan command is supported. The scan command allows the user program to specify a data pattern and instructs the FDC to search for that pattern on a track. Any application that is required to search the disk for information (such as point of sale price lookup, disk directory search, etc.), may use the scan command to reduce the CPU overhead. Once the scan operation is initiated, no CPU intervention is required.

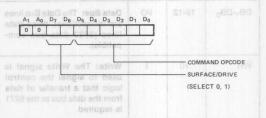
### **CPU Interface Description**

This interface minimizes CPU involvement by supporting a set of high level commands and both DMA and non-DMA type data transfers and by providing hierarchical status information regarding the result of command execution.

The CPU utilizes the control interface (see the Block diagram) to specify the FDC commands and to determine the result of an executed command. This interface is supported by five Registers which are addressed by the CPU via the A<sub>1</sub>, A<sub>0</sub>,  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  signals. If an 8080 based system is used, the  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  signals can be driven by the 8228's  $\overline{\text{I/OR}}$  and  $\overline{\text{I/OW}}$  signals. The registers are defined as follows:

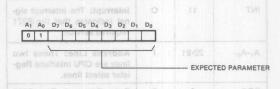
#### **Command Register**

The CPU loads an appropriate command into the Command Register which has the following format:



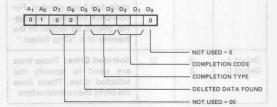
#### Parameter Register

Accepts parameters of commands that require further description; up to five parameters may be required, example:



### Result Register

The Result Register is used to supply the outcome of FDC command execution (such as a good/bad completion) to the CPU. The standard Result byte format is:



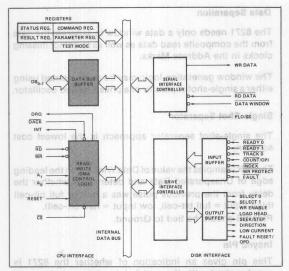
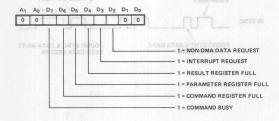


Figure 3. 8271 Block Diagram Showing CPU Interface Functions

#### Status Register

Reflects the state of the FDC.



#### **Reset Register**

Allows the 8271 to be reset by the program. Reset must be active for 11 or more chip clocks.

#### INT (Interrupt Line)

Another element of the control interface is the Interrupt line (INT). This line is used to signal the CPU that an FDC operation has been completed. It remains active until the result register is read.

#### **DMA Operation**

The 8271 can transfer data in either DMA or non DMA mode. The data transfer rate of a floppy disk drive is high enough (one byte every 32 µsec) to justify DMA transfer. In DMA mode the elements of the DMA interface are:

#### **DRQ:** DMA Request:

The DMA request signal is used to request a transfer of data between the 8271 and memory.

## DACK: DMA Acknowledge: 18001 Hosti Inemus ent bas

The DMA acknowledge signal notifies the 8271 that a DMA cycle has been granted.

### RD, WR: Read, Write sh sosheint svind side DDG edT

The read and write signals are used to specify the direction of the data transfer.

DMA transfers require the use of a DMA controller such as the Intel®8257. The function of the DMA controller is to provide sequential addresses and timing for the transfer at a starting address determined by the CPU. Counting of data block lengths is performed by the FDC.

To request a DMA transfer, the FDC raises DRQ. DACK and RD enable DMA data onto the bus (independently of CHIP SELECT). DACK and WR transfer DMA data to the FDC. If a data transfer request (read or write) is not serviced within 31  $\mu$ sec, the command is cancelled, a late DMA status is set, and an interrupt is generated. In DMA mode, an interrupt is generated at the completion of the data block transfer.

When configured to transfer data in non-DMA mode, the CPU must pass data to the FDC in response to the non-DMA data requests indicated by the status word. The data is passed to and from the chip by asserting the DACK and the RD or WR signals. Chip select should be inactive (HIGH).

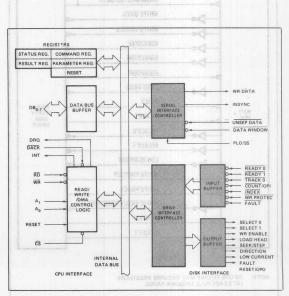


Figure 4. 8271 Block Diagram Showing Disk Interface

DRO: DMA Request:





#### **Disk Drive Interface**

The 8271 disk drive interface supports the high level command structure described in the Command Description section. The 8271 maintains the location of bad tracks and the current track location for two drives. However, with minor software support, this interface can support four drives by expanding the two drive select lines (select 0, select 1) with the addition of minimal support hardware.

The FDC Disk Drive Interface has the following major functions, and beau are signals attracted to seen and

#### **READ FUNCTIONS**

Utilize the user supplied data window to obtain the clock and data patterns from the unseparated read data.

Establish byte synchronization abbs latinsupse ebivorq

Compute and verify the ID and data field CRCs. 1818 8 18

#### WRITE FUNCTIONS

Encode composite write data. steb AMG eldane OR bns

Compute the ID and data field CRCs and append them to theirerespective fields. Issuper retenant stab s 11 .00 CONTROL FUNCTIONS and page 15 minting beginner

To request a DMA transfer, the

Generate the programmed step rate, head load time, head settling time, head unload delay, and monitor drive functions. When configured to transfer data in non-DM

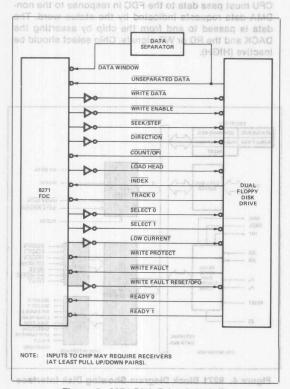


Figure 5. 8271 Disk Drive Interface

#### **Data Separation**

The 8271 needs only a data window to separate the data from the composite read data as well as to detect missing clocks in the Address Marks.

The window generation logic may be implemented using either a single-shot separator or a phase-locked oscillator.

#### Single-Shot Separator

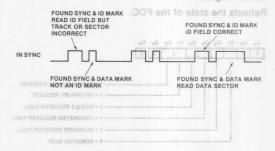
The single-shot separator approach is the lowest cost solution.

The FDC samples the value of Data Window on the leading edge of Unseparated Data and determines whether the delay from the previous pulse was a half or full bit-cell (high input = full bit-cell, low input = half bit-cell).

PLO/SS should be tied to Ground.

#### Insync Pin

This pin gives an indication of whether the 8271 is synchronized with the serial data stream during read operations. This pin can be used with a phase-locked oscillator for soft and hard locking.



Allows the 8271 to be reset by the program. Reset must be active for 11 or more chip clocks.

Another element of the control interface is the interrupt line (INT). This line is used to signal the CPU that an FDC operation has been completed. It remains active until the

The 8271 can transfer data in either DMA or non DMA In DMA mode the elements of the DMA interface are:



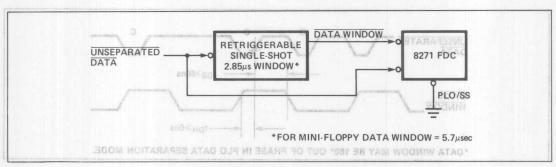
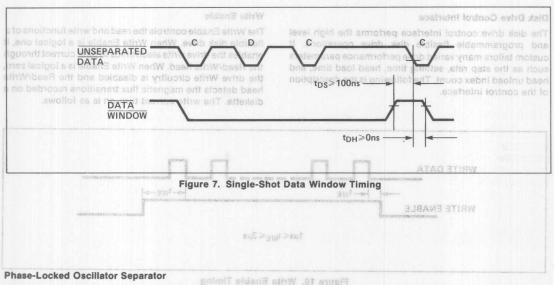


Figure 6. Single-Shot Data Separator Block Diagram



#### **Phase-Locked Oscillator Separator**

The FDC samples the value of Data Window on the leading edge of Unseparated Data and determines whether the pulse represents a Clock or Data Pulse.

Insync may be used to provide soft and hard locking control for the phase-locked oscillator.

PLO/SS should be tied to Vcc (+5V).

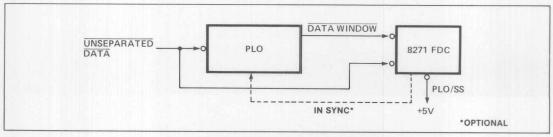


Figure 8. PLO Data Separator Block Diagram



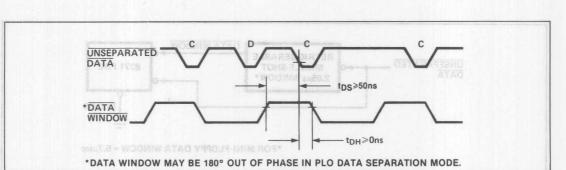


Figure 9. PLO Data Window Timing

#### Disk Drive Control Interface

The disk drive control interface performs the high level and programmable flexible disk drive operations. It custom tailors many varied drive performance parameters such as the step rate, settling time, head load time, and head unload index count. The following is the description of the control interface.

#### Write Enable

The Write Enable controls the read and write functions of a flexible disk drive. When Write Enable is a logical one, it enables the drive write electronics to pass current through the Read/Write head. When Write Enable is a logical zero, the drive Write circuitry is disabled and the Read/Write head detects the magnetic flux transitions recorded on a diskette. The write current turn-on is as follows.

edge of Unseparated Data and determines whether the

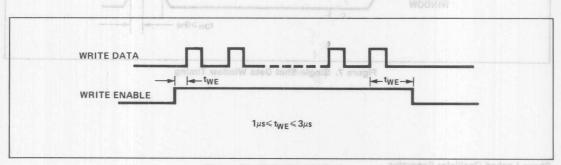
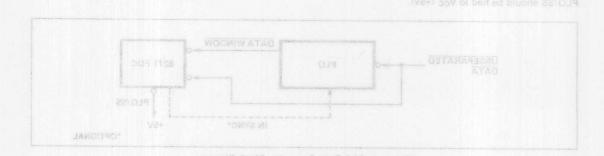


Figure 10. Write Enable Timing pnibool bash bas the ebivorg of besu ed yam anyani gnibsel an nor



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l<sub>9</sub>ini

#### Seek Control

Seek Control is accomplished by Seek/Step, Direction, and Count pins and can be implemented two ways to provide maximum flexibility in the subsystem design. One instance is when the programmed step rate is not equal to zero. In this case, the 8271 uses the Seek/Step and Direction pins (the Seek/Step pin becomes a Step pin). Programmable Step timing parameters are shown.

Another instance is when the programmable step rate is equal to zero, in which case the 8271 holds the seek line high until the appropriate number of user-supplied step pulses have been counted on the count input pin.

The Direction pin is a control level indicating the direction in which the R/W head is stepped. A logic high level on this line moves the head toward the spindle (step-in). A logic low level moves the head away from the spindle (step-out).

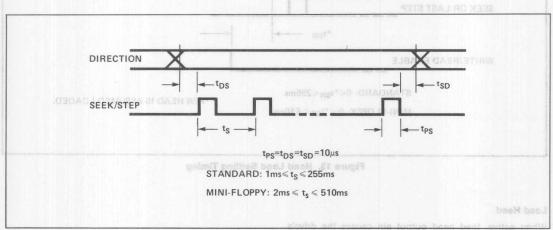


Figure 11. Seek Timing effectable and no behalf of oil band ethylogen

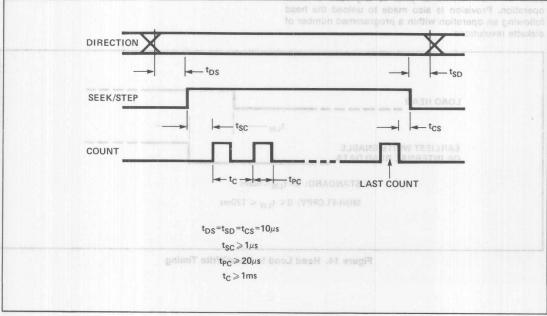


Figure 12. Seek/Step/Count Timing

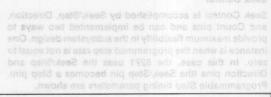




#### Head Seek Settling Time Toutness at his notices Q and

The 8271 allows the head settling time to be programmed from 0 to 255ms, in increments of 1ms.

The head settling time is defined as the interval of time from completion of the last step to the time when reading or writing on the diskette is possible (R/W Enable). The R/W head is assumed loaded.



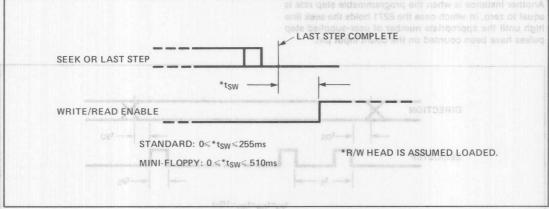


Figure 13. Head Load Settling Timing

#### Load Head

When active, load head output pin causes the drive's read/write head to be loaded on the diskette. When the head is initially loaded, there is a programmed delay (0 to 60ms in 4ms increments) prior to any read or write operation. Provision is also made to unload the head following an operation within a programmed number of diskette revolutions.

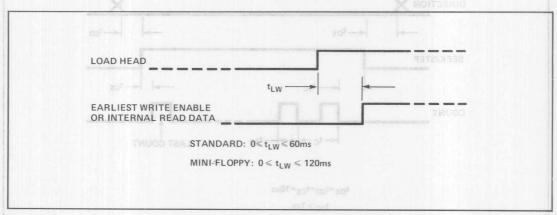


Figure 14. Head Load to Read/Write Timing

The Index input is used to determine "Sector not found" status and to initiate format track/read ID commands and head unload Index and Count operations.

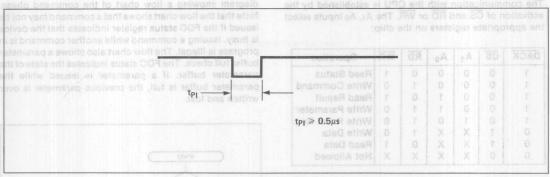


Figure 15. Index Timing and to beaugmos at nottatego DOR and

#### Track 0

This input pin indicates that the diskette is at track 0. During any seek operation, the stepping out of the actuator ceases when the track 0 pin becomes active.

#### Select 1, 0

Only one drive may be selected at a time. The Input/Output pins that must be externally qualified with Select 0 and Select 1 are:

Unseparated Data
Data Window
Write Enable
Seek/Step
Count/Optional Input
Load Head
Track 0
Low Current
Write Protect
Write Fault
Fault Reset/Optional Output
Index

When a new set of select bits is specified by a new command or the FDC finishes the index count before head unload, the following pins will be set to the 0 state:

Write Enable (35)
Seek/Step (36)
Direction (37)
Load Head (38)
Low Head Current (39)

The select pins will be set to the state specified by the command or both are set to zero following the index count before head unload.

### Low Current emoting at saving bnammoo ent pninub

This output pin is active whenever the physical track location of the selected drive is greater than 43. Generally

this signal is used to enable compensation for the lower velocities encountered while recording on the inner tracks.

### Write Protect MRAD OF MWG STI MO STITUS SHIT SAAHR MOFTUDSKS

The 8271 will not write to a disk when this input pin is active and will interrupt the CPU if a Write attempt is made. Operations which check Write Protect are aborted if the Write Protect line is active.

This signal normally originates from a sensor which detects the presence or absence of the Write Protect hole in the diskette jacket.

#### Write Fault and Write Fault Reset

The Write Fault input is normally latched by the drive and indicates any condition which could endanger data integrity. The 8271 interrupts the CPU anytime Write Fault is detected during an operation and immediately resets the Write Enable, Seek/Step, Direction, and Low Current signals. The write fault condition can be cleared by using the write fault reset pin. If the drive being used does not support write fault, then this pin should be connected to  $\rm V_{CC}$  through a pull-up resistor.

#### Ready 1, 0

These two pins indicate the functional status of the disk drives. Whenever an operation is attempted on a drive which is not ready, an interrupt is generated. The interface continually monitors this input during an operation and if a Not Ready condition occurs, immediately terminates the operation. Note that the 8271 latches the Not Ready condition and it can only be reset by the execution of a Read Drive Status command. For drives that do not support a ready signal, either one can be derived with a one shot and the index pulse, or the ready inputs can be grounded and Ready determined through some software means.



# The Command Phase

As an 8080 peripheral device, the 8271 accepts commands from the CPU, executes them and provides a RESULT back to the 8080 CPU at the end of command execution. The communication with the CPU is established by the activation of  $\overline{CS}$  and  $\overline{RD}$  or  $\overline{WR}$ . The A<sub>1</sub>, A<sub>0</sub> inputs select the appropriate registers on the chip:

PRINCIPLES OF OPERATION

DACK	CS	A <sub>1</sub>	Ao	RD	WR	Operation
1	0	0	0	0	1	Read Status
1	0	0	0	1	0	Write Command
1	0	0	1	0	1	Read Result
1	0	0	1	1	0	Write Parameter
1	0	1	0	1	0	Write Reset Reg
0	1	X	X	1	0	Write Data
0	1	X	X	0	1	Read Data
0	0	X	X	X	X	Not Allowed

The FDC operation is composed of the following sequence of events.

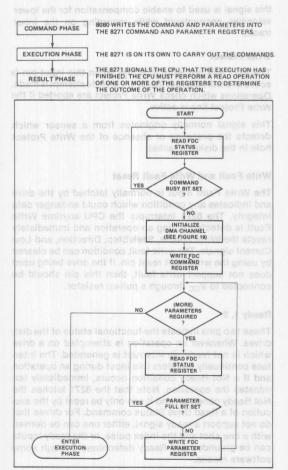


Figure 16. Passing the Command and Parameters to the 8271

The software writes a command to the command register. As a function of the command issued, from zero to five parameters are written to the parameter register. Refer to diagram showing a flow chart of the command phase. Note that the flow chart shows that a command may not be issued if the FDC status register indicates that the device is busy. Issuing a command while another command is in progress is illegal. The flow chart also shows a parameter buffer full check. The FDC status indicates the state of the parameter buffer. If a parameter is issued while the parameter buffer is full, the previous parameter is over written and lost.

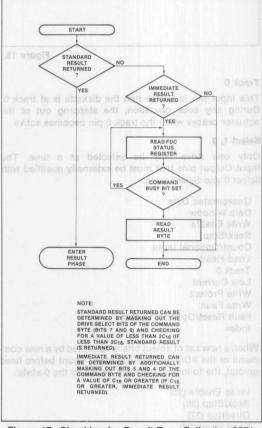


Figure 17. Checking for Result Type Following 8271 Command and Parameters

## The Execution Phase

During the execution phase the operation specified during the command phase is performed. During this phase, there is no CPU involvement if the system utilizes DMA for the data transfers. The execution phase of each command is discussed within the detailed command descriptions. The following table summarizes many of the basic execution phase characteristics.

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#### EXECUTION PHASE BASIC CHARACTERISTICS

The following table summarizes the various commands with corresponding execution phase characteristics.

al tellud fluser ent mi stab ent. U Table 2. Execution Phase Basic Characteristics

completed a command	FDC Phas	edi 121s vino b3sv	4 837	5	6	7	8
commands	Deleted Data	oth Head 1 on Read		Seek	Seek Check	Result	Completion Interrupt
SCAN DATA	SKIP	LOAD /	<x 18="" t<="" td="" ™=""><td>YES</td><td>YES</td><td>YES</td><td>YES</td></x>	YES	YES	YES	YES
SCAN DATA AND			x	YES	YES	YES	YES
DEL DATA eleigmop of			68)				
WRITE DATA	is cxared	id LOAD noiser/o	/ 1	YES	YES	YES	YES
WRITE DEL DATA	×	LOAD	1 / 3	YES	YES	YES	YES
READ DATA	SKIP	LOAD TOM S /S	×	YES	YES	YES	YES
READ DATA AND			X	YES	YES	YES	YES
DEL DATATOM STEEDER			·				
READ ID	x	LOAD	x	YES	NO	YES	YES
VERIFY DATA AND	XFER	LOAD	x	YES	YES	YES	YES
DEL DATA		30 bres F ed 6:					lusoR 6ttT
FORMAT TRACK	X	LOAD 🗸	edit/o U9;	YES	NO	YES	YES
SEEK	X	LOAD y	ed <b>x</b> am as	YES	noil NO b	namYES ent	to eYES
READ DRIVE STATUS	X COLOR	After reading the Sta Result Register for n	x	NO	NO	NOTE 5	Vd DNO
SPECIFY		- x	×	NO	NO	NO	NO
RESET			x	NO	NO	NO	NO
R SP REGISTERS	Minas X and	This byte format lax to look up error rou	×	NO	NO	NOTE 6	NO
W SP REGISTERS		rXsult byte farmat is	x	NO	NO	NO	SONOS
Note: 1. "x" → DON'T CARE	2. " $$ " $\rightarrow$ chec	ck 3. "-" $\rightarrow$ No change 4.	"y" → Check at en	d of operatio	n 5. See "REA	D DRIVE STATE	JS" command.
6. See "READ SPECIA	L REGISTER"	command.	RW	80		O L A	

Explanation of the execution phase characteristics table.

#### 1. Deleted Data Processing

If deleted data is encountered during an operation that is marked skip in the table, the deleted data record is not transferred into memory, but the record is counted. For example, if the command and parameters specify a read of five records and one of the records was written with a deleted data mark, four records are transferred to memory. The deleted data flag is set in the result byte. However, if the operation is marked transfer, all data is transferred to memory regardless of the type of data mark.

#### 2. Head

The Head column in the table specifies whether the Read/Write head will be loaded or not. If the table specifies load, the head is loaded after it is positioned over the track. The head loaded by a command remains loaded until the user specified number of index pulses have occurred.

Bits 4 and 3: Completion Type

#### 3. Ready

The Ready column indicates if the ready line (Ready 1, Ready 0) associated with the selected drive is checked. A not ready state is latched by the 8271 until the user executes a read status command.

#### 4. Write Protect

The operations that are marked check Write Protect are immediately aborted if Write Protect line is active at the beginning of an operation.

#### 5. Seek

Many of the 8271 commands cause a seek to the desired track. A current track register is maintained for each drive or surface.

#### 6. Seek Check

Operations that perform Seek Check verify that selected data in the ID field is correct before the 8271 accesses the data field.

register. Whenever the FDC is busy processing a

Bit 6: Command Full





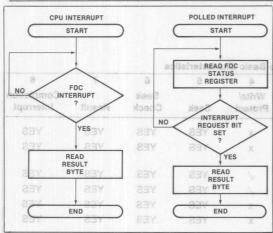


Figure 18. Getting the Result

#### The Result Phase

During the Result Phase, the FDC notifies the CPU of the outcome of the command execution. This phase may be initiated by: a stow

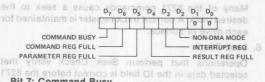
- 1. The successful completion of an operation.
- 2. An error detected during an operation.

#### PROGRAMMING

A <sub>1</sub>	A <sub>0</sub>	CS RD	CS WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg
1	0	_	Reset Reg
1	1	_	Write Protect

#### STATUS REGISTER

#### **FDC Status**



#### Bit 7: Command Busy

The command busy bit is set on writing to the command register. Whenever the FDC is busy processing a command, the command busy bit is set to a one. This bit is set to zero after the command is completed.

accesses the data field.

#### Bit 6: Command Full

The command full bit is set on writing to the command buffer and cleared when the FDC begins processing the command.

#### Bit 5: Parameter Full

This bit indicates the state of the parameter buffer. This bit is set when a parameter is written to the FDC and reset after the FDC has accepted the parameter.

#### Bit 4: Result Full TOARAND DISAS BRAMS MOTTUDENS

This bit indicates the state of the result buffer. It is valid only after Command Busy bit is low. This bit is set when the FDC finishes a command and is reset after the result byte is read by the CPU. The data in the result buffer is valid only after the FDC has completed a command. Reading the result buffer while a command is in progress yields no useful information.

#### **Bit 3: Interrupt Request**

This bit reflects the state of the FDC INT pin. It is set when FDC requests attention as a result of the completion of an operation or failure to complete an intended operation. This bit is cleared by reading the result register. GAOJ

#### Bit 2: Non-DMA Data Request

When the FDC is utilized without a DMA controller, this bit is used to indicate FDC data requests. Note that in the non-DMA mode, an interrupt is generated (interrupt request bit is set) with each data byte written to or read from the diskette.

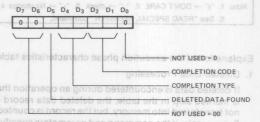
#### Bits 1 and 0:

Not used (zero returned).

After reading the Status Register, the CPU then reads the Result Register for more information.

#### THE RESULT REGISTER

This byte format facilitates the use of an address table to look up error routines and messages. The standard result byte format is:



## read of five records and one of the recor: 8 that T

#### Not used (zero returned). I sham also betsleb a ritiw

## to memory. The deleted data flag is set in the

Deleted Data Found: This bit is set when deleted data is encountered during a transaction.

### Bits 4 and 3: Completion Type

The completion type field provides general information regarding the outcome of an operation.

The completion type field provides general information regarding the outcome of an operation.

Comm	letion		1B000 SVBIT
	pe	Event	3. Ready
0	0 1 408	Good Completion - No E	The Report
0	perser	System Error - recoverab	
0.128	by the	operator intervention prob	ably required
1	1	Command/Drive Error — e error or drive hardware fa	

Load Bad Tracks





#### Bits 2 and 1: Completion Code

The completion code field provides more detailed information about the completion type (See Table).

				0
Completion	Completion		0	PARI
Туре	Code	Event BAD TRACK NO	0	PAR
00	00	Good Completic Scan Not Met	on/	PAR
00	01	Scan Met Equal		RAS
00	10	Scan Met Not E	qua	1
00	11			
O1 ENDE	face 200° bad to	Clock Error		nsie"
01 Hack 10	mace tone bad	Late DMA		
01	10	ID CRC Error		aram
dress)10	1 (Philipsi Ac	Data CRC Error	HOE	ti bai
10	00	Drive Not Ready	/	
tracks 0nd our	bad noti men	Write Protect	1005	n el l
10	noi10:lisiti		ind	if fine
10	11	Write Fault		
11	00	Sector Not Four	nd.	SEEK
11	01	ADPLIANTED	WU	71 THE
		sevom bnammos		
11 3080	r verifting the	ading the head o		ioritiv

It is important to note the hierarchical structure of the result byte. In very simple systems where only a GO-NO GO result is required, the user may simply branch on a zero result (a zero result is a good completion). The next level of complexity is at the completion type interface. The completion type supplies enough information so that the software may distinguish between fatal and non-fatal errors. If a completion type 01 occurs, ten retries should be performed before the error is considered unrecoverable.

The Completion Type/Completion Code interface supplies the greatest detail about each type of completion. This interface is used when detailed information about the transaction completion is required.

specify commands selectable by the first parameter

2. An in-progress command is aborted.

specified by the systems software. Prior to initiating 0.118

Not used (zero returned). of basemass notizings evib

Definition	st Parameter Specify Type noitherpretation that the seek on
Successful Completion/ Scan Not Met	The diskette operation specified was completed without error. If scan operation was specified, the pattern scanned was not found on the track addressed.
Ne track 00 signal is detected.	The data pattern specified with the scan command was found on the track
ignal is not detalled to Metalled Steps, and error status is returned.	The data pattern specified with the scan command was found with the collection of the track addressed, but the equality was not met.
rorral solution the read/write hear terd is used to position the read/write hear thead position is unknown (such as after	During a diskette read operation, a clock bit was missing (dropped). Note that this function is disabled when reading any of the ID address marks (which contain lists) missing clock pulses). If this error occurs, the operation is terminated immediately and an interrupt is generated.
Late DMA	During either a diskette read or write operation, the data channel did not respond within the allotted time interval to prevent data from being overwritten or lost. This error immediately terminates the operation and generates an interrupt.
r ID Field CRC Error J38 18 283 828 828 828 828 828 828 828 828 82	The CRC word (two bytes) derived from the data read in an ID field did not match the CRC word written in the ID field when the track was formatted. If this error occurs, the associated diskette operation is prevented and no data is transferred.
Data Field CRC Error	During a diskette read operation, the CRC word derived from the data field read did not match the data field CRC word previously written. If this error occurs, the data read from the sector should be considered invalid.
is used to interrogate the drive status on the result register will hold the fina	Drive not powered up     Diskette not loaded     Non-existent drive addressed     Drive went not ready during an operation
Write Protect	A diskette write operation was specified on a write protected diskette. The intended write operation is prevented and no data is written on the diskette.
Track 00 Not Found  Write Fault  Write Fault  Sector Not Found  Sector Not Found  AND	increments its track address register (stepping the drive to the next track) and again compares the track addresses. If the track addresses still do not match, the



#### INITIALIZATION

#### Reset Command day ametava alomia view nl jetvo flucen

	A <sub>1</sub>	Ao	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub> 2	D <sub>0</sub>
PAR:	1	0	0	0	0	0	0	0	0.84	1 प्राव
PAR:	1	0	0	0	0	0	0	0	0	0

Function: The Reset command emulates the action of the reset pin. It is issued by outputting a one followed by a zero to the Reset register.

- 1. The drive control signals are forced low.
- 2. An in-progress command is aborted.
- 3. The FDC status register flags are cleared.
- 4. The FDC enters an idle state until the next command is

Reset must be active for 10 or more clock cycles.

#### SPECIFY COMMAND

Many of the interface characteristics of the FDC are specified by the systems software. Prior to initiating any drive operation command, the software must execute the three specify commands. There are two types of specify commands selectable by the first parameter issued.

#### First Parameter Specify Type

0DH	Initialization
10H	Load bad Tracks Surface '0'
18 <sub>H</sub>	Load bad Tracks Surface '1'

The Specify command is used prior to performing any diskette operation (including formatting of a diskette) to define the drive's inherent operating characteristics and also is used following a formatting operation or installation of another diskette to define the locations of bad tracks. Since the Specify command only loads internal registers within the 8271 and does not involve an actual diskette operation, command processing is limited to only Command Phase. Note that once the operating characteristics and bad tracks have been specified for a given drive and diskette, redefining these values need only be done if a diskette with unique bad tracks is to be used or if the system is powered down.

#### initialization:

A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	Do
0	0	0	0	1	1	0	1	0	1
0	.1	0	0	0	0	1	-1	0	1
0	1	STEP	RATE*					bas	tdres
0	1	HEAD	SETTL	ING TIM	E*	non sted o	opera s clea	ny an rode i	noi
0	1					HE	AD LOA	D TIME*	
	0 0 0 0	0 0 0 0 1 0 1 0 1	0 0 0 0 0 0 0 0 1 0 0 1 STEP 0 1 HEAD 0 1 INDE	0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 STEP RATE* 0 1 HEAD SETTL	0 0 0 0 1 0 1 0 0 0 0 1 STEP RATE* 0 1 HEAD SETTLING TIM	0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 1 0 1 0 0 0 1 1 1 0 1 STEP RATE* 0 1 HEAD SETTLING TIME* 0 1 INDEX CNT BEFORE HEAD LOA	0 0 0 0 1 1 0 0 1 0 0 1 0 0 0 1 1 0 0 1 STEP RATE* 0 1 HEAD SETTLING TIME* 0 1 INDEX CNT BEFORE HEAD LOAD TIME*

\*Note: Mini-floppy parameters are doubled.

Parameter 0 — 0DH = Select Specify Initialization.

Parameter 1 — D<sub>7</sub>-D<sub>0</sub> = Step Rate (0-255ms in 1ms steps). Parameter 2 — D<sub>7</sub>-D<sub>0</sub> = Head Settling Time (0-255ms in 1 ms steps). {0 – 510ms in 2ms steps} () = standard,

{} = mini

Parameter 3 — D7-D4 = Index Count — Specifies the number of Revolutions (0-14) which are to occur before the FDC automatically unloads the R/W head. If 15 is specified, the head remains loaded.

 $D_3$ - $D_0$  = Head Load Time (0-60ms in steps of 4ms). {0 - 120ms in 8ms steps} () = standard, {} = mini

#### **Load Bad Tracks**

tailed	A <sub>1</sub>	A <sub>0</sub>	D7	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D	Do
CMD:	0	0	0	00	te qu	100	0	0045	000	main
PAR:	0	1	0	0	0	in had	1/0	0	0	0
PAR:	0	19-19	BAD	TRACK	NO. 1	SDD			adi	
PAR:	0	18101	BAD	TRACK	VO. 2	00	line:		00	
PAR:	0	1	CURF	RENT TR	ACK	10	Made		00	
1	sup:	Not	Met	net e		01			90	

Parameter 0: 10<sub>H</sub> = Load Surface zero bad tracks 18<sub>H</sub> = Load Surface one bad track

Parameter 1:000 000 00

Bad track address number 1 (Physical Address).

It is recommended to program both bad tracks and current track to FF<sub>H</sub> during initialization.

### SEEK COMMAND

The seek command moves the head to the specified track without loading the head or verifying the track.

The seek operation uses the specified bad tracks to compute the physical track address. This feature insures that the seek operation positions the head over the correct track

When a seek to track zero is specified, the FDC steps the head until the track 00 signal is detected.

If the track 00 signal is not detected within (FF)<sub>H</sub> steps, a track 0 not found error status is returned.

A seek to track zero is used to position the read/write head when the current head position is unknown (such as after a power up).

	A	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
CMD:	0	0	SEL 1	SEL 0	1	0	980	0	0	1
PAR:	0	1	TRAC	K ADD	RESS 0	255				

Seek operations are not verified. A subsequent read or write operation must be performed to determine if the correct track is located.

#### **READ DRIVE STATUS COMMAND**

This command is used to interrogate the drive status. Upon completion the result register will hold the final drive status.

0	301	0	SEL 1	SEL 0	1	0	1	1.	0	
			-				-		_	-
men.										
RESI	111	T. F4	CH BIT	INDIC	ATESCI	IRREN	TSTAT	E OF I	UPLIT PI	NIS
RESI A1		T: EA	ACH BIT	INDIC D <sub>6</sub>	ATES CI	URREN'	T STAT	E OF II	NPUT PII	NS.
									D <sub>1</sub>	0

\*Note the two ready bits are zero latching. Therefore, to clear the drive not ready condition, assuming the drive is ready, and to detect it via software, one must issue this command twice.





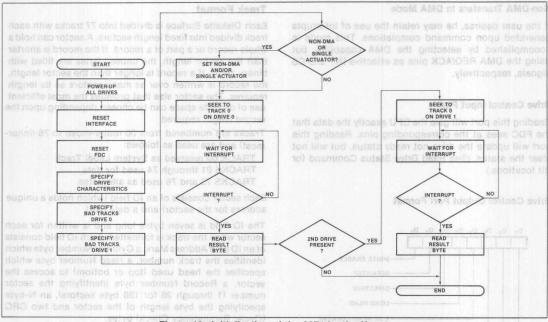


Figure 19. Initialization of the 8271 by the User

### Read/Write Special Registers 201 8 110 nothing one ableit

This command is used to access special registers within the 8271. but offers of the second is so that the seco

ther	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub> no
CMD:	0	0	SEL 1	SEL 0	сом	MAND	OPCOD	elone	ini ett	diske
PAR:	0	valse	REGI	STER AD	DRESS		lam	1 180	Form	588

Command code:

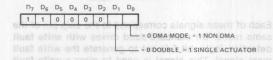
3DH Read Special Register and paled 50 your difference of paled 50 your difference of the pale

For both commands, the first parameter is the register address; for Write commands a second parameter specifies data to be written. Only the Read Special Register command supplies a result.

Table 4. Special Registers

Description 21010ea 81	Register Address in Hex	Comment
Scan Sector Number	06	See Scan Description
Scan MSB of Count	14	See Scan Description
Scan LSB of Count	13	See Scan Description
Surface 0 Current Track	12	emaining sectors
Surface 1 Current Track	1A Daniah	scation of these is
Mode Register	17 of all dis to st	See Mode Register Description
Drive Control Output Port	The second second	See Drive Output Port Description
Drive Control Input Port	22	See Drive Input Port Description
Surface 0 Bad Track 1	10	ddress Marks
Surface 0 Bad Track 2	. 11	
Surface 1 Bad Track 1	18	ers smarks are
Surface 1 Bad Track 2	19	which are used to

#### Mode Register Write Parameter Format



#### Bits 6 & 7 evinb besie inim nO evinb ent ninthy not solbrid

Must be one. Total evid and tho to no must of beau ed had

## Bits 5-2 on retaigns and gnithw of roing been ad beum ref

(Not used). Must be set to zero. 191 and to select and avea

#### \*Bit 1

Double/Single Actuator: Selects single or double actuator mode. If the single actuator mode is selected, the FDC assumes that the physical track location of both disks is always the same. This mode facilitates control of a drive which has a single actuator mechanism to move two heads.

surfaces) of the disligite. On double-sided disligites, the

### corresponding top and bottom tracks are referred to fill\*

Data Transfer Mode: This bit selects the data transfer mode. If this bit is a zero, the FDC operates in the DMA mode (DMA Request/ACK). If this bit is a one, the FDC operates in non-DMA mode. When the FDC is operating in DMA mode, interrupts are generated at the completion of commands. If the non-DMA mode is selected, the FDC generates an interrupt for every data byte transferred.

diskettel, an index pulse is generated to indicate the

1-132 AFN-00223B

<sup>\*</sup>Bits 0 and 1 are initialized to zero. On a find a set initialized to zero.



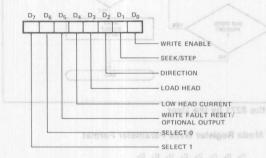
#### Non-DMA Transfers in DMA Mode

If the user desires, he may retain the use of interrupts generated upon command completions. This mode is accomplished by selecting the DMA capability, but using the DMA REQ/ACK pins as effective INT and CS signals, respectively.

#### **Drive Control Input Port**

Reading this port will give the CPU exactly the data that the FDC sees at the corresponding pins. Reading this port will update the drive not ready status, but will not clear the status. (See Read Drive Status Command for Bit locations.)

#### **Drive Control Output Port Format**



Each of these signals correspond to the chip pin of the same name. On standard-sized drives with write fault detection logic, bit 5 is set to generate the write fault reset signal. This signal is used to clear a write fault indication within the drive. On mini-sized drives, this bit can be used to turn on or off the drive motor prior to initiating a drive operation. A time delay after turn on may be necessary for the drive to come up to speed. The register must be read prior to writing the register in order to save the states of the remaining bits. When the register is subsequently written to modify bit 5, the remaining bits must be restored to their previous states.

# IBM DISKETTE GENERAL FORMAT

The IBM Flexible Diskette used for data storage and retrieval is organized into concentric circular paths or TRACKS. There are 77 tracks on either one or both sides (surfaces) of the diskette. On double-sided diskettes, the corresponding top and bottom tracks are referred to as a CYLINDER. Each track is further divided into fixed length sections or SECTORS. The number of sectors per track—26, 15 or 8—is determined when a track is formatted and is dependent on the sector length—128, 256 or 512 bytes respectively—specified.

All tracks on the diskette are referenced to a physical index mark (a small hole in the diskette). Each time the hole passes a photodetector cell (one revolution of the diskette), an Index pulse is generated to indicate the logical beginning of a track. This index pulse is used to initiate a track formatting operation.

#### **Track Format**

Each Diskette Surface is divided into 77 tracks with each track divided into fixed length sectors. A sector can hold a whole record or a part of a record. If the record is shorter than the sector length, the unused bytes are filled with binary zeros. If a record is longer than the sector length, the record is written over as many sectors as its length requires. The sector size that provides the most efficient use of diskette space can be chosen depending upon the record length required.

Tracks are numbered from 00 (outer-most) to 76 (inner-most) and are used as follows:

TRACK 00 reserved as System Label Track TRACKS 01 through 74 used for data TRACKS 75 and 76 used as alternates.

Each sector consists of an ID field (which holds a unique address for the sector) and a data field.

The ID field is seven bytes long and is written for each sector when the track is formatted. Each ID field consists of an ID field Address Mark, a Cylinder Number byte which identifies the track number, a Head Number byte which specifies the head used (top or bottom) to access the sector, a Record Number byte identifying the sector number (1 through 26 for 128 byte sectors), an N-byte specifying the byte length of the sector and two CRC (Cyclic Redundancy Check) bytes.

The Gaps separating the index mark and the ID and data fields are written on a track when it is formatted. These gaps provide both an interval for switching the drive electronics from reading or writing and compensation for rotational speed and other diskette-to-diskette and drive-to-drive manufacturing tolerances to ensure that data written on a diskette by one system can be read by another (diskette interchangeability).

#### **IBM Format Implementation Summary**

#### **Track Format**

The disk has 77 tracks, numbered physically from 00 to 76, with track 00 being the outermost track. There are logically 75 data tracks and two alternate tracks. Any two tracks may be initialized as bad tracks. The data tracks are numbered logically in sequence from 00 to 74, skipping over bad tracks (alternate tracks replace bad tracks). Note: In IBM format track 00 cannot be a bad track.

#### **Sector Format**

Each track is divided into 26, 15, or 8 sectors of 128, 256, or 512 bytes length respectively. The first sector is numbered 01, and is physically the first sector after the physical index mark. The logical sequence of the remaining sectors may be nonsequential physically. The location of these is determined at initialization by CPU software.

Each sector consists of an ID field and a data field. All fields are separated by gaps. The beginning of each field is indicated by 6 bytes of (00)<sub>H</sub> followed by a one byte address mark.

#### **Address Marks**

Address Marks are unique bit patterns one byte in length which are used to identify the beginning of ID and Data fields. Address Mark bytes are unique from all other data



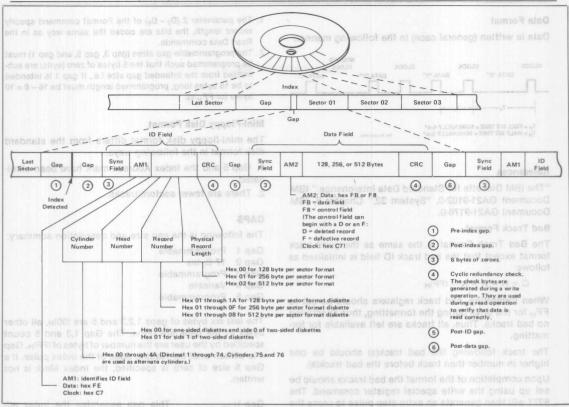


Figure 20. Track Format

bytes in that certain bit cells do not contain a clock bit (all other data bytes have clock bits in every bit cell.) There are four different types of Address Marks used. Each of these is used to identify different types of fields.

### Index Address Mark nem stab entr

The Index Address Mark is located at the beginning of each track and is a fixed number of bytes in front of the first record.

#### **ID Address Mark**

The ID Address Mark byte is located at the beginning of each ID field on the diskette.

### Data Address Mark

The Data Address Mark byte is located at the beginning of each non-deleted Data Field on the diskette.

#### **Deleted Data Address Mark**

The Deleted Data Address Mark byte is located at the beginning of each deleted Data Field on the diskette.

Address Mark Summary	Clock Pattern	Data Pattern
Index Address Mark	D7	FC
ID Address Mark	C7	FE
Data Address Mark	C7	FB
Deleted Data Address Mark	C7	F8
Bad Track ID Address Mark	C7	FE

#### **ID** Field

MARK	С	H	R	N	CRC	CRC
------	---	---	---	---	-----	-----

C = Cylinder (Track) Address, 00-74

H = Head Address

R = Record (Sector) Address, 01-26

N = Record (Sector) Length, 00-02

Note: Sector Length =  $128 \times 2^{N}$  bytes

CRC = 16 Bit CRC Character (See Below)

### Data Field

MARK	DATA	CRC	ODO
INICALLY	DAIA	UNL	CRC

Data is 128, 256, or 512 bytes long.

Note: All marks, data, ID characters and CRC characters are recorded and read most significant bit first.

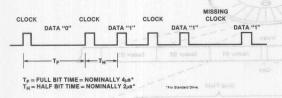
## CRC Characters bos 1758 and most elamiple sham

The 16-bit CRC character is generated using the generator polynominal X16 + X12 + X5 + 1, normally initialized to (FF) $_{\rm H}$ . It is generated from all characters (except the CRC in the ID or data field), including the data (not the clocks) in the address mark. It is recorded and read most significant bit first.



#### **Data Format**

Data is written (general case) in the following manner:



"The IBM Diskette for Standard Data Interchange," IBM Document GA21-9182-0. "System 32," Chapter 8, IBM Document GA21-9176-0.

### Bad Track Format

The Bad Track Format is the same as the good track format except that the bad track ID field is initialized as follows:

$$C = H = R = N = (FF)_H$$

When formatting, bad track registers should be set to FFH for the drive during the formatting, thus specifying no bad tracks. Thus, all tracks are left available for formatting.

The track following the bad track(s) should be one higher in number than track before the bad track(s).

Upon completion of the format the bad tracks should be set up using the write special register command. The 8271 will then generate an extra step pulse to cross the bad track, locating a new track that now happens to be an extra track out.

#### **Format Track**

	1164	711									
			Format Command								
	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
CMD:	0	0	SEL 1	SEL 0	1	0	0	0	bnlly	) 1 <sub>m</sub>	
PAR:	0	1	TRA	TRACK ADDRESS							
PAR:	0	1	GAP 3 SIZE MINUS 6 6 A (101062) 610068							A =	
PAR:	0	1	RECO	RECORD LENGTH NO. OF SECTORS/TRACK							
PAR:	0	1	GAP	GAP 5 SIZE MINUS 6							
PAR:	0	1	GAP	1 SIZE	MINUS	6	JANJ	3165 0	21	377	

The format command can be used to initialize a disk track compatible with the IBM 3740 format. A Shugart "IBM Type" mini-floppy format may also be generated.

The Format command can be used to initialize a diskette, one track at a time. When format command is used, the program must supply ID fields for each sector on the track. During command execution, the supplied ID fields (track head sector addresses and the sector length) are written sequentially on the diskette. The ID address marks originate from the 8271 and are written automatically as the first byte of each ID field. The CRC character is written in the last two bytes of the ID field and is derived from the data written in the first five bytes. During the formatting operation, the data field of each sector is filled with data pattern (E5)H. The CRC, derived from the data pattern is also appended to the last byte.

- 1. The parameter 2 (D7 D5) of the Format command specify record length, the bits are coded the same way as in the Read Data commands.
- 2. The programmable gap sizes (gap 3, gap 5, and gap 1) must be programmed such that the 6 bytes of zero (sync) are subtracted from the intended gap size i.e., if gap 1 is intended to be 16 bytes long, programmed length must be 16-6=10bytes (of FFH's).

### Mini-Floppy Disk Format

The mini-floppy disk format differs from the standard disk format in the following ways:

- 1. Gap 5 and the Index Address mark have been eliminated.
- 2. There are fewer sectors/tracks.

#### **GAPS**

The following is the gap size and description summary:

Gap 1 Programmable Gap 2 17 Bytes Gap 3 Programmable Gap 4 Variable Gap 5 Programmable

The last six bytes of gaps 1,2,3 and 5 are (00)H, all other bytes in the gaps are (FF)H. The Gap 1,3 and 5 count specified by the user are the number of bytes of (FF)H. Gap 4 is written until the leading edge of the index pulse. If a Gap 5 size of zero is specified, the Index Mark is not written.

Gap 1: N bytes FF's

This gap separates the index address mark of the index pulse from 6 bytes 0's for sync the first ID mark. It is used to protect the first ID field from a write on the last physical sector of the current track.

Gap 2: 11 bytes FF's

This gap separates the ID field from the data mark and field such that 6 bytes 0's for sync during a write only the data field and to most all solved will be changed even if the write gate turns on early, due to drive speed changes.

Gap 3:

This gap separates a data area from N bytes FF's the next ID field. It is used so that 6 bytes 0's for sync during drive speed changes the next ID mark will not be overwritten, thus causing loss of data.

Gap 4: FF's only

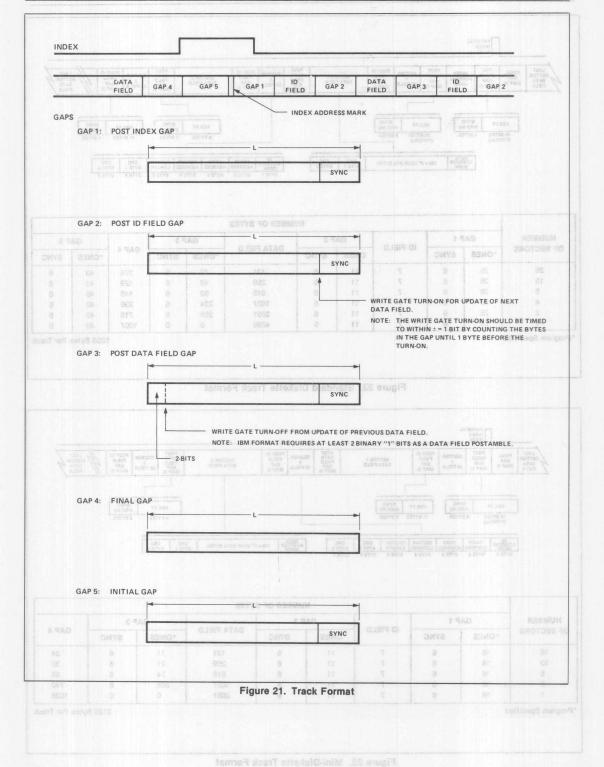
This gap fills out the rest of the disk and is used for slack during formatting. During drive speed variations and is betseen at all this gap will shrink or grow if the disk is re-formatted.

Gap 5: N bytes FF's

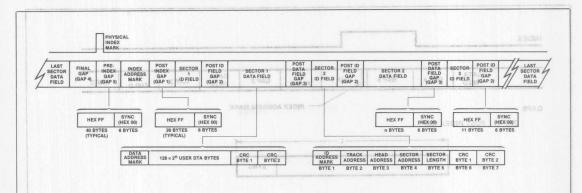
This gap separates the last sector from the Index Address mark and 6 bytes 0's for sync is used to assure that the index address mark is not destroyed by writing on the last physical data sector on the track.

The number of FF bytes is programmable for gaps 1, 3 and 5.







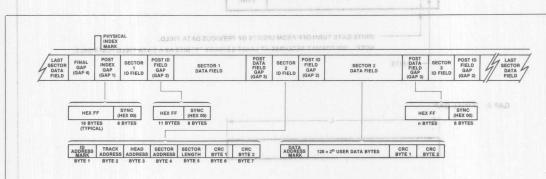


					NUMBER OF BYTES 4AD CLERED GAP 4S 9AD								
NUMBER OF SECTORS	GAP 1			GAP 2		DATA FIELD	GAP 3			GAP 5			
	*ONES	SYNC	ID FIELD	ONES	SYNC	DATA FIELD	*ONES	SYNC	GAP 4	*ONES	SYNC		
26	26	6	7	11	6	131	27	6	275	40	6		
15	26	6	7	11	6	259	48	6	129	40	6		
8	26	6	7	11	6	515	90	6	146	40	6		
4 70(3)	26 409	HO 6HO-M	RUT ST70 STIRL	11	6	1027	224	6	236	40	6		
2	26	6	DATA FIFED.	11	6	2051	255	6	719	40	6		
LD BE TIMED	26	UT BEAD B	TOTE: PIE WRIT	11	6	4099	0	0	1007	40	6		

\*Program Specified RC454 STY6 I JITHU 4AD SHT MI

5208 Bytes Per Track

Figure 22. Standard Diskette Track Format



				N	UMBER OF	BYTES	-		
NUMBER	GA	P 1	GAP 2			GAP 3			
OF SECTORS	*ONES	SYNC	ID FIELD	ONES	SYNC	DATA FIELD	*ONES	SYNC	GAP 4
18	16	6	7	11	6	131	11	6	24
10	16	6	7	11	6	259	21	6	30
5	16	6	7	11	6	515	74	6	88
2	16	6	7	11	6 Tre	1027	255	6	740
1	16	6	7	ok Format	6	2051	0	0	1028

\*Program Specified

3125 Bytes Per Track

Figure 23. Mini-Diskette Track Format

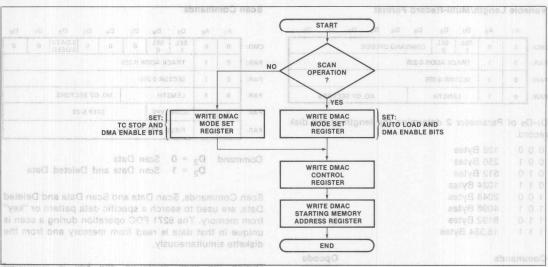


Figure 24. User DMA Channel Initialization Flowchart

#### Read ID Command entitle barages of bluow year etyd

	A <sub>1</sub>	Ao	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	Do
MD:	0 0	0	SEL	SEL 0	8:001	eyt is	et()	10 M	babu	lan
AR:	8901	TUPIT	TRAC	TRACK ADDRESS 1890 SVE STOLLES TO 190 MI						
AR:	0	ulae.	0	0	0	0	0	0	0	0
AR:	(Oast	a 11	NUME	EROFI	DFIELD	os .	e arti	ti o	nime.	min

The Read ID command transfers the specified number of ID fields into memory (beginning with the first ID field after Index). The CRC character is checked but not transferred.

These fields are entered into memory in the order in which they are physically located on the disk, with the first field being the one starting at the index pulse.

#### **Data Processing Commands**

All the routine Read/Write commands examine specific drive status lines before beginning execution, perform an implicit seek to the track address and load the drive's read/write head. Regardless of the type of command (i.e., read, write or verify), the 8271 first reads the ID field(s) to verify that the correct track has been located (see sector not found completion code) and also to locate the addressed sector. When a transfer is complete (or cannot be completed), the 8271 sets the interrupt request bit in the status register and provides an indication of the outcome of the operation in the result register.

If a CRC error is detected during a multisector transfer, processing is terminated with the sector in error. The address of the failing sector number can be determined by examining the Scan Sector Number register using the Read Special Register command.

Full power of the multisector read/write commands can be realized by doing DMA transfer using Intel® 8257 DMA Controller, For example, in a 128 byte per sector multisector write command, the entire data block (containing 128 bytes times the number of sectors) can be located in a disk memory buffer. Upon completion of the command phase, the 8271 begins execution by accessing the desired track, verifying the ID field, and locating the data field of the first record to be written. The 8271 then DMA-accesses the first sector and starts counting and writing one byte at a time until all 128 bytes are written. It then locates the data field of the next sector and repeats the procedure until all the specified sectors have been written. Upon completion of the execution phase the 8271 enters into the result phase and interrupts the CPU for availability of status and completion results. Note that all read/write commands, single or multisector are executed without CPU intervention.

Note, execution of multi-sector operations are faster if the sectors are *not* interleaved. To be detailed by the sectors are not interleaved.

#### 128 Byte Single Record Format

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
CMD:	0	0	SEL 1	SEL 0	COMM	AND O	PCODE			noita		
PAR:	0	hee:	TRAC	TRACK ADDR 0-255								
PAR:	0 5	sin :	SECT	OR 0-2	5590хв						iei	
Noor	0 01	hapi	21 150	a cons	03 210	175 W	373770 d	100. 10	di Bido	(Verlor	124	

Commands	Opcode
READ DATA	12
READ DATA AND DELETED DATA	16
WRITE DATA	OA
WRITE DELETED DATA	0E
VERIFY DATA AND DELETED DATA	1E





#### Variable Length/Multi-Record Format

	A <sub>1</sub>	Ao	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
CMD:	0	0	SEL 1	SEL 0	COM	/AND	OPCODE	1	
PAR:	0	1	TRA	CK ADE	OR 0-25	5			-
PAR:	0	1	SECT	OR 0-2	55			MOITAREY T	0
PAR:	0 .	1	LI	ENGTH			NO. OF S	ECTORS	

D<sub>7</sub>-D<sub>5</sub> of Parameter 2 determine the length of the disk

000	128 Bytes
0 0 1	256 Bytes
0 1 0	512 Bytes
0 1 1	1024 Bytes
1 0 0	2048 Bytes
1 0 1	4096 Bytes
1 1 0	8192 Bytes
1 1 1	16,384 Bytes

Commands	Opcode
READ DATA	well nells 13 iff
READ DATA AND DELETED DATA	17
WRITE DATA	0B
WRITE DELETED DATA	
VERIFY DATA AND DELETED DATA	D griob yd1Fexili
SCAN DATA TYOURS IN SIGMS	00
SCAN DATA AND DELETED DATA	04

## Read Commands Dexe enged ITS8 art seeing braining

## Function 1000 state bas iotoes lent ent sessoon-AMO

The read command transfers data from a specified disk record or group of records to memory. The operation of this command is outlined in execution phase table.

## Write Commands or no felamos and curate to villosliava

Write Data, Write Deleted Data.

#### Function

The write command transfers data from memory to a specified disk record or group of records.

#### **Verify Command**

Verify Data and Deleted Data.

#### Function

The verify command is identical to the read data and deleted data command except that the data is not transferred to memory. This command is used to check that a record or a group of records has been written correctly by verifying the CRC character.

#### Scan Commands

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
CMD:	0	0	SEL 1	SEL 0	0	0	0	S.DATA S.DELD	0	0
PAR:	0	1	TRA	CK ADD	R 0-255	5				
PAR:	0	1	SEC1	OR 0-2	55					
PAR:	0	1	LENG	STH		NO.	OF SE	CTORS		
PAR:	0	ลาโลด	SCAN	TYPE		S	TEP SI	ZE		
PAR:	0	015	FIEL	D LENG	тн (к	(Y)				

Command  $D_2 = 0$  Scan Data

D<sub>2</sub> = 1 Scan Data and Deleted Data

Scan Commands, Scan Data and Scan Data and Deleted Data, are used to search a specific data pattern or "key" from memory. The 8271 FDC operation during a scan is unique in that data is read from memory and from the diskette simultaneously.

During the scan operation, the key is compared repetitively (using the 8257 DMA Controller in auto load mode) with the data read from the diskette (e.g., an eight byte key would be compared with the first eight bytes (1-8) read from the diskette, the second eight bytes (9-16), the third eight bytes (17-24), etc.). The scan operation is concluded when the key is located or when the specified number of sectors have been searched without locating the key. When concluded, the 8271 FDC requests an interrupt. The program must then read the result register to determine if the scan was successful (if the key was located). If successful, several of the FDC's special registers can be examined (read special registers command) to determine more specific information relating to the scan (i.e., the sector number in which the key was located, and the number of bytes within the sector that were not compared when the key was located).

The 8271 does not do a sliding scan, it does a fixed block linear search. This means the key in memory is compared to an equal length block in a sector; when these blocks meet the scan conditions the scan will stop. Otherwise, the scan continues until all the sectors specified have been searched.

The following factors regarding key length must be considered when establishing a key in memory.

1. When searching multiple sectors, the length of the key must be evenly divisible into the sector length to prevent the key from being split at subsequent sector boundaries. Since the character FF<sub>H</sub> is not compared, the key in memory can be padded to the required length using this character. For example, if the actual pattern compared on the diskette is twelve characters in length, the field length should be sixteen and four bytes of FF<sub>H</sub>



loini

would be appended to the key. Consequently, the last block of sixteen bytes compared within the first sector would end at the sector boundary and the first byte of the next sector would be compared with the first byte of the key. Splitting data over sector boundarys will not work properly since the FDC expects the start of key at each sector boundary.

2. Since the first byte of the key is compared with the first byte of the sector, when the pattern does not begin with the first byte of the sector, the key must be offset using the character FF16. For example, if the first byte of a nine byte pattern begins on the fifth byte of the sector, four bytes of FF16 are prefixed to the key (and three bytes of FF16 are appended to the key to meet the length requirement) so that the first actual comparison begins on the fifth byte.

The Scan Commands require five parameters:

#### Parameter 0, Track Address

Specifies the track number containing the sectors to be scanned. Legal values range from  $00_{\rm H}$  to  $4C_{\rm H}$  (0 to 76) for a standard diskette and from  $00_{\rm H}$  to  $22_{\rm H}$  (0 to 34) for a mini-sized diskette.

#### Parameter 1, Sector Address

Specifies the first sector to be scanned. The number of sectors scanned is specified in parameter 2, and the order in which sectors are scanned is specified in parameter 3.

#### Parameter 2. Sector Length/Number of Sectors

The sector length field (bits 7-5) specifies the number of data bytes allocated to each sector (see parameter 2, routine read and write commands for field interpretation). The number of sectors field (bits 4-0) specifies the number of sectors to be scanned. The number specified ranges from one sector to the physical number of sectors on the track

#### Parameter 3

D<sub>7</sub>-D<sub>6</sub>: Indicate scan type

00-EQ Scan for each character within the field length (key) equal to the corresponding character within the disk sector. The scan stops after the first equal condition is met.

01-GEQ Scan for each character within the disk sector greater than or equal to the corresponding character within the field length (key). The scan stops after the first greater than or equal condition is met.

10-LEQ Scan for each character within the disk sector less than or equal to the corresponding character within the field length (key). The scan stops after the first less than or equal condition is met.

D<sub>5</sub>-D<sub>0</sub>: Step Size: The Step Size field specifies the offset to the next sector in a multisector scan. In this case, the next sector address is generated by adding the Step Size to the current sector address.

### Parameter 4, Field Length

8271/8271-6

Specifies the number of bytes to be compared (length of key). While the range of legal values is from 1 to 255, the field length specified should be evenly divisible into the sector length to prevent the key from being split at sector boundaries, if the multisector scan commands are used.

### **Scan Command Results**

More detailed information about the completion of Scan Commands may be obtained by executing Read Special Register commands.

## Read Special Register - ritorial biast mumikam jostA maos

Parameter Results

- Of The sector <u>number</u> of the sector in which the specified scan data pattern was located.
- MSB Count The number of 128 byte blocks remaining to be compared in the current sector when the scan data pattern was located. This register is decremented with each 128 byte block read.
- be compared in the current sector when the scan data pattern is located. This register is initialized to 128 and is decremented with each byte compared.

Upon a scan met condition, the equation below can be used to determine the last byte in the located pattern.

Pointer = sector length - ((Register 14H)\*128 + (Register 13H))





first byte of the key. Splitting data over sector bound-

arys will not work properly since the FDC expects the

## 8271 Scan Command Example dose 101 nsp2 OBJ-01

Assume there are only 2 records on track 0 with the following data:

Record 01: 01 02 03 04 05 06 07 08 000....00 Record 02: 01 02 AA 55 00 00 00 00 ......00

Command	Field [1] Length	Starting Sector #	# of Sectors	Key <sup>[2]</sup>	Completion Code <sup>[3]</sup>	Spec R06		risters <sup>[4]</sup>	Comment On S
* SCAN EQ	2	enbbs rot	urrent sed 1	01,02	SME	01	0 4	127D	Met in first field
SCAN EQ	2	1	1	02,03	SNM	X	X	X	Not met
SCAN EQ	2	1	.1	FF <sup>[5]</sup> ,05	SNM	X	X	X	Not met with don't care
* SCAN EQ	2	1 1111	Field Len	FF <sup>[5]</sup> ,06	SME	01	0	123D	Met with don't care
* SCAN EQ	qm 2) ed	of sative to	19021111	AA,55	SME	02	0	125D	Met in Record 02
* SCAN EQ	2 830	lav 2ggl h	e ra <b>r</b> ige d	01,02	SME	02	0	127D	Starting sector ≠ 1
* SCAN EQ	ib v41eve	hould be	s belfioed	05,06,07,08	SME	01	0	121D	Field, Key length = 4
* SCAN GEQ	med mo	t the key f	nevery of	05.06.07.08	SME	01	0	121D	GEQ-SME TOO TESS OF
* SCAN GEQ	4	sector sci	Hum adf	05,04,07,08	SMNE	01	0	121D	GEQ-SMNE
* SCAN GEQ	4	1	2	00,03,AA,44 <sup>[6]</sup>	SNM	X	X	X 88	GEQ-SNM
* SCAN LEQ	4	1	1	01,03,FF,04	SMNE	01	0	125D	LEQ-SMNE
* SCAN LEQ	4	1 0	luas it be	01,02,FF,04	SME	01	010.00	125D	LEQ-SME
nestion of Scan	mon arit	tuoris noi	tempotoi l		34) for a		to 22		standard diskette and

#### NOTES

- Field Length Each record is partitioned into a number of fields equal to the record size divided by the field length.

  Note that the record size should be evenly divisable by the field length to insure proper operation of multi record scan. Also, maximum field length = 256 bytes.
- 2. Key The key is a string of bytes located in the user system memory. The key length should equal the field length.

  By programming the 8257 DMA Controller into the auto load mode, the key will be recursively read in by the chip (once per field).
- Completion Code Shows how Scan command was met or not met.
   SNM SCAN Not Met 0 0 (also Good Complete)
   SME SCAN Met Equal 0 1
   SMNE SCAN Met Not Equal 1 0
- 4. Special Registers

R06 — This register contains the record number where the scan was met.
R14 — This register contains the MSB count and is decremented every 128 characters.

Length ( $\ell$ ) (D7-D5 of PAR 2)	Record Size	R14 = $2\ell$ - 1 at minimum reference flower of the (Initialize at Beginning of Record)
000 Mon, th 100 ustion be last byte 010 he locati 110	200 Dylos	ter first equal condition is met.  1 Upon to each character within the disk so: 2 used the correspond used to the correspond used to the correspond used the correspond used to the correspond
gister 14H)* (33 • (Register	sector (digth - ((Re	g character within the field langth (ke).  Pointer  s scan stops after the first greater than or

- R13 This register contains a modulo 128 LSB count which is initialized to 128 at beginning of each record. This count is decremented after each character is compared except for the last character in a pattern match situation.
- 5. The OFF<sub>H</sub> character in the key is treated as a don't care character position.
- 6. The Scan comparison is done on a byte by byte basis. That is, byte 1 of each field is compared to byte 1 of the key, byte 2 of each field is compared to byte 2 of the key, etc.





#### **ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias .....0°C to 70°C¹
Storage Temperature .....-65°C to +150°C
Voltage on Any Pin with
Respect to Ground ....-0.5V to +7V
Power Dissipation ......1 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. CHARACTERISTICS (V<sub>CC</sub> = +5.0V ±5%

8721 and 8271-8:  $T_A = 0$  °C to 70 °C; 8271-6:  $T_A = 0$  °C to 50 °C)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	- 0.5	0.8	V	A
VIHamblit	Input High Voltage	2.0	$(V_{CC} + 0.5)$	V	- Llociny
V <sub>OLD</sub>	Output Low Voltage (Data Bus)	r-Burst Mod	0.45	AN MAIL DI	I <sub>OL</sub> = 2.0 mA
V <sub>OLI</sub>	Output Low Voltage (Interface Pins)		0.5	V	I <sub>OL</sub> = 1.6 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	$I_{OH} = -220  \mu A$
IIL	Input Load Current Section		± 10	μΑ	V <sub>IN</sub> = V <sub>CC</sub> to 0V
loz	Off-State Output Current		± 10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> to 0V
Icc	V <sub>CC</sub> Supply Current		180	mA	Fasty Reset

## CAPACITANCE (TA = 25°C; VCC = GND = 0V)

Symbol	Parameter	Min.	Тур.	Max.	Unit	bolto Test Conditions
CIN	Input Capacitance	126		10	pF	t <sub>c</sub> = 1 MHz pH xoolO Hot
CI/O	I/O Capacitance	50	nd Data	20 bets	pF	Unmeasured Pins Returned to GND

NOTE: 1. Ambient temperature under bias for 8271-6 is 0°C to 50°C.

## A.C. CHARACTERISTICS (V<sub>CC</sub> = +5.0V ±5%)

(8271 and 8271-8:  $T_A = 0^{\circ}C$  to 70°C; 8271-6:  $T_A = 0^{\circ}C$  to 50°C)

#### READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t <sub>AC</sub>	Select Setup to RD	0		ns	Note 2
t <sub>CA</sub>	Select Hold from RD	0		ns	Note 2
t <sub>RR</sub>	RD Pulse Width	250	600	ns	25
t <sub>AD</sub>	Data Delay from Address		250	ns	Note 2
t <sub>RD</sub>	Data Delay from RD		150	ns	C <sub>L</sub> = 150 pF, Note 2
t <sub>DF</sub>	Output Float Delay	20	100	ns	C <sub>L</sub> = 20 pF for Minimum; 150 pF for Maximum
t <sub>DC</sub>	DACK Setup to RD OLLOW, O	25		ns	O DIBOLA RUR VRO DIVA
t <sub>CD</sub>	DACK Hold from RD	25		ns	
t <sub>KD</sub>	Data Delay from DACK		250	ns	





## A.C. CHARACTERISTICS (Continued)

device. This is a stress rating only and functional opera-

## tion of the device at these or any other content and the

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t <sub>AC</sub>	Select Setup to WRAXA not anothibned gritten VV	- 00V8.	)	ns -	Respect to Ground
t <sub>CA</sub>	Select Hold from WR	0		ns	nonequality
t <sub>ww</sub>	WR Pulse Width	250		ns	
t <sub>DW</sub>	Data Setup to WR	150		ns	
t <sub>WD</sub>	Data Hold from WR	0		ns	aconocomo an action of
t <sub>DC</sub>	DACK Setup to WR	25	Demonstra	ns	OHOTHA LOWER N
t <sub>CD</sub>	DACK Hold from WR	25	F 821103-7-22	ns	
amoltik	Min. Max. Unit Test Conc		reler	msie9	

#### DMA

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
tca	Request Hold from WR or RD (for Non-Burst Mode)	(au8	150	ns	oro Ontont Low

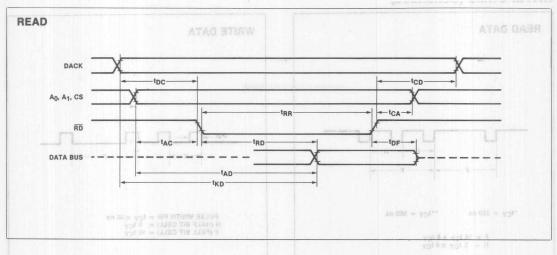
OTHER TI	MINGS		2.4				A HERR	1 indino	111
Symbol	snV As	Parameter			8271	/8271-6		Input Lo	
Symbol	IoV Aq	Parameter			Min.	Max.	Unit	Test Conditions	
t <sub>RSTW</sub>	Reset Pulse Width	180			10	tnert	t <sub>CY</sub>	V <sub>CC</sub> Sup	0
t <sub>r</sub>	Input Signal Rise Time	е				20	ns		
t <sub>f</sub>	Input Signal Fall Time	)				20	ns		
t <sub>RSTS</sub>	Reset to First IOWR			IV0 = I	2	V::0	t <sub>CY</sub>	NTANCE O	3
t <sub>CY</sub>	Clock Period				250	00		Note 3	
t <sub>CL</sub> and	Clock Low Period	JinU	ляМ.	Typ.	110			of Parent	di
t <sub>CH</sub>	Clock High Period	Pg	10		125	8	ns	Input Cap	1
tos	Data Window Setup to	o Unseparat	ed Clock a	and Data	50		ns	WO Capaci	0
t <sub>DH</sub>	Data Window Hold fro	m Unsepara	ted Clock	and Data	0	es for 821	ns	Ambient temperature	1

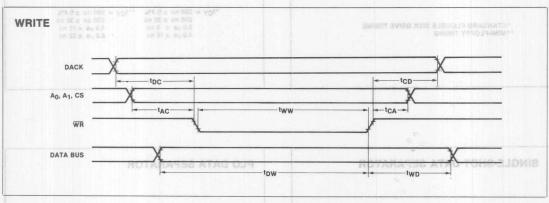
#### NOTES:

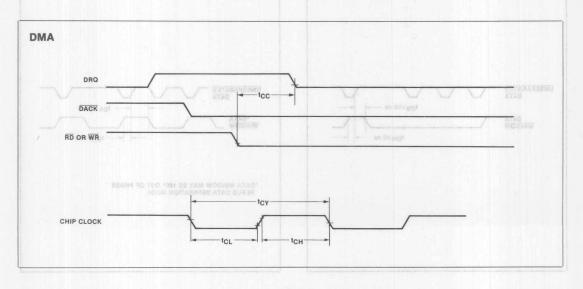
- 1. All timing measurements are made at the reference voltages unless otherwise specified: Input "1" at 2.0V, "0" at 0.8V Output "1" at 2.0V, "0" at 0.8V
- 2. t<sub>AD</sub>, t<sub>RD</sub>, t<sub>AC</sub>, and t<sub>CA</sub> are not concurrent specs.
- 3. Standard Floppy:  $t_{CY} = 250 \text{ ns} \pm 0.4\%$  Mini-Floppy:  $t_{CY} = 500 \text{ ns} \pm 0.4\%$  Mini-Floppy:  $t_{CY} = 500 \text{ ns} \pm 0.4\%$ (8271 and 8271-8: TA = 0°C to 70°C; 8271-6: TA = 0°C to 50°C)

#### A.C. TESTING INPUT, OUTPUT WAVEFORM

## A.C. TESTING LOAD CIRCUIT 2.0 DEVICE Data Delar TEST POINTS < + CLO stad Output Fiedt Delay A C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1. AND 0.45V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC 1. AND 0.8V FOR A LOGIC 0. CL INCLUDES JIG CAPACITANCE

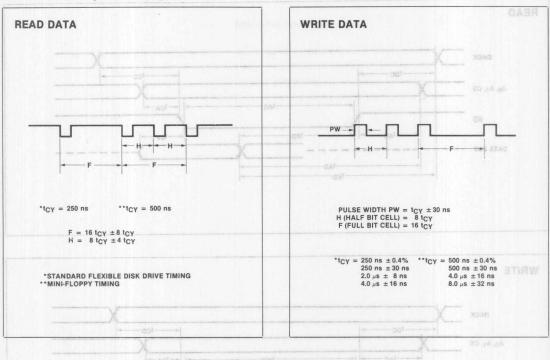


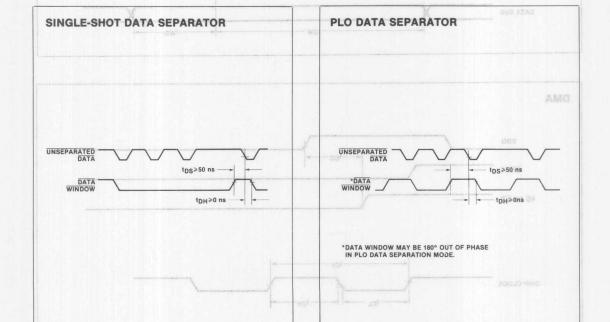
















Name and Function

## 8272

8272

# SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer
   Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette

- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most
   Microprocessors Including 8080A, 8085A, 8086 and 8088
- Single-Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40-Pin Plastic Dual-in-Line Package

The 8272 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The 8272 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Drive Interface.

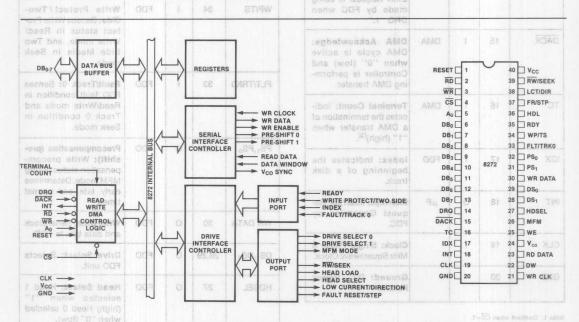


Figure 1. 8272 Internal Block Diagram

Figure 2. Pin Configuration



Table 1. Pin Description

Symbol	Pin No.	Туре	Connec- tion To	Name and Function	au	Symbol	Pin No.	Туре	Connec- tion To	Name and Function
RST	1	1	μР	Reset: Places FDC in	2 1	V <sub>CC</sub>	40	Past 1		D.C. Power: +5V
AMO-	Nor	o Ah	ia ni e	idle state. Resets output lines to FDD to ''0'' (low).		RW/SEEK	39	0	FDD .	Read Write / SEEK When "1" (high) Seek mode selected and
RD of q	2 U no	l(1) suot	μP	Read: Control signal for transfer of data from		ingths:			eta0	when "0" (low) Read Write mode selected.
				FDC to Data Bus, when "0" (low).		LCT/DIR	38	0	FDD	Low Current/Direction Lowers Write current
WR ,A08	3 08 g	inge ingir s	Philopalic and and and and	Write: Control signal for transfer of data to FDC via Data Bus, when "0" (low).		ransfer	sck T		nd Mu Ploppy	on inner tracks in Read/Write mode, de- termines direction head will step in Seek mode.
<del>CS</del>		Cloc ar Su	<sub>E</sub> μP[[	Chip Select: IC selected when "0" (low), allowing RD and WR to be enabled.		FR/STP	hsqm	, Co	Fields	Fault Reset/Step: Re- sets fault FF in FDD in Read/Write mode, pro- vides step pulses to
Ao	5	<b>[</b> [1]	μΡ	Data/Status Register		bseA :	mi mi MeG i	ersQ Biw	Sasis, lemona	move head to another cylinder in Seek mode.
J. 64 L. 64 L. 1				Select: Selects Data Reg ( $A_0 = 1$ ) or Status Reg ( $A_0 = 0$ ) content be sent to Data Bus.		HDL	36	0	FDD	Head Load: Command which causes read/write head in FDD to contact
ninchatai	6 10	1/0[1]	ontage t	ns will unlo ent anistor	ion del	(O) Chip, wh	llar (FI	Contra	Disk I	diskette.
DB <sub>0</sub> -DB <sub>7</sub>		100 88	μP	Data Bus: Bidirectional 8-Bit Data Bus.	1	RDY ibula	1		1300370-0000	Ready: Indicates FDE is ready to send or re
DRQ	14	0	DMA	Data DMA Request: DMA Request is being	nting				urdens a	ceive data. om selfons
				made by FDC when DRQ "1."		WP/TS	34	ŀ	FDD	Write Protect / Two- Side: Senses Write Pro-
DACK	15	1	DMA	DMA Acknowledge: DMA cycle is active when "0" (low) and				7		tect status in Read Write mode, and Two Side Media in Seel mode.
		\$ D 9	103A H	Controller is performing DMA transfer.		FLT/TRK0	33	T	FDD	Fault/Track 0: Senses
TC <sup>41 ent e E e e</sup> e e e e e e e e e e e e e e e	16	100	DMA	Terminal Count: Indicates the termination of a DMA transfer when "1" (high) <sup>[2]</sup> .	LOCK STA SABLE SABLE MIET O	DHW - IN DHO	SERIAL			FDD fault condition in Read/Write mode and Track 0 condition in Seek mode.
IDX 089 C S	17	1 Da	FDD	Index: Indicates the beginning of a disk track.	HIFT 1 DATA WINDOW YNC	PS <sub>1</sub> ,PS <sub>0</sub>	31,32	0	FDD	Precompensation (pre- shift): Write precom- pensation status during MFM mode. Determines
INT PRO S	18	0	μP	Interrupt: Interrupt Request Generated by	100	1961 <u>                                     </u>				early, late, and norma times.
MARI CI O	10	***	DAG GI	FDC.		WR DATA	30 aviac	0	FDD	Write Data: Serial clock and data bits to FDD.
AYAG GR	19		\$41 4/2	Clock: Single Phase 8 MHz Squarewave Clock.	YUS	DS <sub>1</sub> ,DS <sub>0</sub>	28,29	0	FDD	Drive Select: Selects FDD unit.
GND ***	20	es Do	NO .	Ground: D.C. Power Return.		HDSEL	27	0	FDD	Head Select: Head 1 selected when "1" (high) Head 0 selected

Note 2: TC must be activated to terminate the Execution Phase of any command.

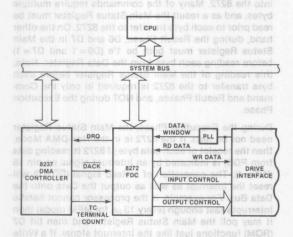


mod trienallib & galfupexe to elde Table 1. Pin Description (Continued) suits 2 ent neewled glidenoitals and the signals RD, WR, and An is shown bel

Symbol	Pin No.	Туре	Connec- tion To	Name and Function						
MFM	26	0	PLL (2928	MFM Mode: MFM mode when "1," FM mode when "0."						
WE PART AW	25	100.00	FDD	Write Enable: Enable write data into FDD.						
operation	24		neglen ras instru ther com	VCO Sync: Inhibits VCO in PLL when "0" (low), enables VCO when "1."						
RD DATA	23	ale r ssor.	econo en	Read Data: Read data from FDD, containing clock and data bits.						

Pin No.	Туре	Connec- tion To	Name and Function
22	Regilat Negal Negal	PLL 0	Data Window: Generated by PLL, and used to sample data from FDD.
		-	Write Clock: Write data rate to FDD FM = 500 kHz, MFM = 1 MHz, with
nto Dai		0	a pulse width of 250 ns for both FM and MFM.
eter ar	Regi	n Status	Must be enabled for all operations, both Read
	No. 22 s 21 sQ mo	No. Type  22 F	No. Type tion To

## 8272 SYSTEM BLOCK DIAGRAM



bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available

Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to
Scan High or Equal	Track 0)
Scan Low or Equal	Sense Interrupt Status
Specify	Sense Drive Status

#### **FEATURES**

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The 8272 offers many additional features such as multiple sector transfers in both read and write modes with a single command, and full IBM compatibility in both single (FM) and double density (MFM) modes.

# DESCRIPTION THE DAMA CONTROL OF THE STATE OF

Hand-shaking signals are provided in the 8272 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the 8237. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor for every transfer of a data byte between the CPU and the 8272. In the DMA mode, the processor need only load a command into the FDC and all data transfers occur under control of the 8272 and DMA controller.

There are 15 separate commands which the 8272 will execute. Each of these commands require multiple 8-bit

#### 8272 REGISTERS — CPU INTERFACE

The 8272 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after execution of a command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and 8272.



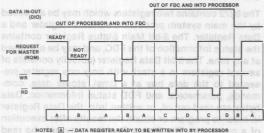
The relationship between the Status/Data registers and the signals RD, WR, and Ao is shown below.

A <sub>0</sub>	RD	WR	FUNCTION
0	0 obniv a	1 1 19	Read Main Status Register
0	and the same	0	Illegal
0	0	0 50	Illegal
1 hw	0	0	Illegal ne sur par
<b>1</b> M	00 o a a	fB1 1	Read from Data Register
110	visied wick	0	Write into Data Register

The bits in the Main Status Register are defined as

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB <sub>0</sub>	FDD 0 Busy	D <sub>0</sub> B	FDD number 0 is in the Seek mode.
DB <sub>1</sub>	FDD 1 Busy	D <sub>1</sub> B	FDD number 1 is in the Seek mode.
DB <sub>2</sub>	FDD 2 Busy	D <sub>2</sub> B	FDD number 2 is in the Seek mode.
DB <sub>3</sub>	FDD 3 Busy	D <sub>3</sub> B	FDD number 3 is in the Seek mode.
DB <sub>4</sub>	FDC Busy	СВ	A read or write command is in process.
DB <sub>5</sub> als O	Non-DMA mode	NDM	The FDC is in the non-DMA mode. This bit is set only during the execution phase in non-DMA mode. Transition to "0" state indicates execution phase has ended.
DB <sub>6</sub> Butter 2 for	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB7 of I le been bi s emit bi the user. I the sebo	Request for Master	ROM PROPERTY OF THE PROPERTY O	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus.



DATA REGISTER NOT READY TO BE WRITTEN INTO BY PROCESSO - DATA REGISTER READY FOR NEXT DATA BYTE TO BE READ BY THE

D - DATA REGISTER NOT READY FOR NEXT DATA BYTE TO BE READ BY

STATUS REGISTER TIMING

The 8272 is capable of executing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the 8272 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information

required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it

was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping in-

formation are made available to

the processor.

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the 8272. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the 8272. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1)before reading each byte from the Data Register. Note. this reading of the Main Status Register before each byte transfer to the 8272 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the 8272 is in the Non-DMA Mode, then the receipt of each data byte (if 8272 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal (RD = 0) will reset the Interrupt as well as output the Data onto the Data Bus. For example, if the processor cannot handle Interrupts fast enough (every 13 µs for MFM mode) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write

Command is in process then the WR signal performs the reset to the Interrupt signal.

If the 8272 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The 8272 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a  $\overline{DACK} = 0$  (DMA Acknowledge) and a  $\overline{RD} = 0$ (Read signal). When the DMA Acknowledge signal goes low (DACK = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a WR signal will appear instead of RD. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has seven bytes of

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data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The 8272 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The 8272 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the 8272 to form the Command Phase, and are read out of the 8272 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the 8272 the Execution Phase automatically starts. In a similar fashion, when

the last byte of data is read out in the Result Phase, the command is automatically ended and the 8272 is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to pin 16 (TC = 1). This is a convenient means of ensuring that the processor may always get the 8272's attention even if the disk system hangs up in an abnormal manner.

#### **POLLING FEATURE OF THE 8272**

After the Specify command has been sent to the 8272, the Drive Select Lines DS0 and DS1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the 8272 polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the 8272 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the 8272 occurs continuously between instructions, thus notifying the processor which drives are on or off line.

Table 2. 8272 Command Set

mand	100 YE	13)	-		D	ATA	BUS				- 1 2 1						DAT	BU	S			R	
PHASE	R/W	D <sub>7</sub>	De	5 D	5 1	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	REMARKS	PHASE	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	REMARKS	
mend manual	CITTOTO CITTOTO	38	-			REA	D D	ATA			- 1	WRITE DATA								- B			
Command	W	МТ	MF	M SI	K	0	0	1	1	0	Command Codes	Command	W	MT	MFM	0	0	0	MAP	0	1	Command Codes	
	W	0	0	0	)	0	0	HDS	DS1	DS0		sebe0 s	W	0	0	0	0	0	HDS	DS1	DS0	Command W   I	
	W				-	_ 0					Sector ID information		W		02G H							Sector ID information	
	W	1	0.000			_ H			W	V	prior to Command	100	W	(a)				4				prior to Command	
	W	-						0		-	execution	pitedar	W			_		R	-		-	execution	
	W	1									Recuban		W	10	-	-	E	TC	10			- 2	
	W												W					PL					
	W			HITA		DT	L	10.30				ns 816		de.			_ D					noducex8	
Execution	cusebres	51									Data transfer	Execution	ya anis	100								Data transfer	
Execution	es ausi	0									between the FDD											between the main-	
											and main-system	notisition	itus In er Con	90								system and FDD	
Result	R										Status information	Result	R				C.	τ ο				Status information	
nesuit	R	T				ST	1				after Command	nesuit	R									after Command	
	R					ST	2_				execution	Gl bril .sz	R									execution	
	R					_ C						on sas no										8	
	R	01	-					0.0	0	0	Sector ID information after command		R	B 73							-	Sector ID information	
	R	-		- 10	1	_ H	-	4		1770		ecution	R	-		-	JAUG	R	0.0	-	274	after Command execution	
	n		373.2						-1	M.	execution		-					-		900			
				-	100	70	2000	ED D	200			89300.0	1			-	RITE	ELE	11.	-	1100.	W   W   M	
Command	W	March 1975						1		0	Command Codes	Command	W		MFM		0	1	0	0	1	Command Codes	
	W	0	0	0	)	0	0	HDS	DS1	DS0	1 100	Disamont	W	0	0	0	0	0	HDS	DS1	DS0	T W	
	W	-		-	1391	_ C	_	HDS		-	Sector ID information		W	9				0_				Sector ID information	
	W	-				H					prior to Command		W	-		_						prior to Command	
	W	-	-	-	-	_ H	-		-		execution		W	-		-		7		-	_	execution	
	W												W				-	OT	0		-	W	
		al.	1	J. Lie-		GF	L	d.	0	.8	Commend W		W				G	PL				+ 1 7 1	
	W									-		belea	1000				_ D	TL _				Execution	
Execution											Data transfer	Execution	disawi	06.								Data transfer	
Execution		11									between the FDD	Execution	elam b	da.								between the FDD	
	ed the	11-1-1									and main-system	documento	ni austa	-								and main-system	
Result	R	10				ST	0				Status information	Result	R	1			S	ΤΟ.				Status information	
1100011	R	401				ST	1		al lane		after Command	Hosait	B				S	1	8			after Command	
	R					ST	2 _				execution		R				_ 5	Γ2				execution	
	R					C						ecchagn ptal	R					0				A	
								linva			Sector ID information	bnami										Sector ID information	
								-			after Command		R	90		-						after Command	
	H	-				_ N	_				execution		R	-	-		-	A	-	200	1	execution	

Note: 1. Symbols used in this table are described at the end of this section.

- 2. An = 1 for all operations.
- 3. X = Don't care, usually made to equal binary 0

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## and place and fill the passes at a Table 2. 8272 Command Set (Continued) was the second fluxed of the place and the second fluxed of th

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS	PHASE	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub> D	1 D <sub>0</sub>	REMARKS
H HIQ V	18	READ A TRACK	ompe yours	SCAN LOW OR EQUAL					Apu salán masa				
Command	w	0 MFM SK 0 0 0 1 0	Command Codes	Command	W	MT	MFM	SK	aiqu	1	0 (	1	Command Codes
neve r	W	0 0 0 0 0 HDS DS1 DS0	processor in	esteria	W	0	0	0	0	0	HDS D	31 DS0	Pro - 8279 - com
rer	W	termionde de c' du abned me	Sector ID information	Main	W	-65 11	23 621	Jun	(		OF GAL	(6) [1]	Sector ID informatio
	W	н	prior to Command	by the	Wse	80	D VE	m.		1	penoi.	nam.	prior Command
	W	R	execution	pisters	W	a min	18	UNI	704	3-	onli	enili 1	execution
	W	EOT	POLLING	entr gr	W	aid	alla	FR. I		TC	0 12.18	bds	STO. STI. STR
	W	GPL		yllutes	W	-		121	G	PL_			d sault Phase to
the 8275	W	des deed as often simmos ytto	After the Spe		W	10 1	0110	635		TP _	324x 1	1411, 101	
Usellar	ofus	ect Lines DS0 and DS1 will	Data transfer	Execution	and	dame							Data compared
Execution	abna		between the FDD	autara	ent	101							between the FDD
llog STS	8 art		and main-system.										and main-system
			FDC reads all of	Desuit	R				0.	- 0			Ctatus information
line fror	Vibse		cylinders contents from index hole to	Result	R	375	10 01	110	S	1	en are	WAY S	Status information after Command
ensa) el	sta		EOT	ent ni	R	90	1.30	Tu	S	2	eis b	AS . 8	execution
8272 wi	erit	por opening or_closing) then	o a of oub vi	ant ni	R	rite	THE	100		_	111000	taun	needs threat
Result	R	ST 0	Status information		R	40	bas	100 10		- 1	5 41 4	A PET	Sector ID information after Command
10.169	R	IDEAL SUISIC ST1 W. JOUTISM	after Command	net pe	R	100	Dire			· _	1 121 1	1911	execution
Dash to	R	Supplied Str. 2 Current Series	execution	ee bai	tithe	270	CHILI	1111	111111	2000	TVO 18	HIG B	- CACCULION
d enti y	R	ndicated. The molling of the	Sector ID information	HuseR	10.1	oner	ninc	SCA	N HIC	SH O	R EQUA	hoda	uence. No fore
ructions	B		after Command	Command	W	MT	MFM	SK	1 .	11	ndil A	hitu	Command Codes
	R	N N	execution	0012 111	W	0					HDS DS		ommond Dise
		READ ID		LOUING	W	STU	21	20	anı	07	11198	81 3	Sector ID information
Command	w	0 MFM 0 0 1 0 1 0	Commands	when	W	185	181	mia	<u> </u>		starts	VHISO	prior Command
Command	W	0 0 0 0 0 HDS DS1 DS0	Commands		W	-				- 8			execution
	**	0 0 0 0 0 HDS DS1 DS0			W	-	-	-		TC		-	
Execution			The first correct ID		W			_		PL _			
LXCCUTION			information on the	-	W					TP _			
			Cylinder is stored in		100								
			Data Register	Execution									Data compared
Result	R	ST 0	Status information	2. 8272	sld	100							between the FDD and main-system
nesuit	R	ST 1	after Command	N. 7 40 St. 440	0310	100							and main-system
	R	ST 2	execution	Result	R			0.00		0 _			Status information
	R	C S ATAG			R	-			\$1	1	300		after Command
	R	IN GO PO GO HO GO GO GO	Sector ID information	RKS	R	-100	40	-01	_ S	2 _	-0 -0	-07	execution
	R	N	during Execution Phase		R	-		-			24 27		Sector ID informatio
	n	ATAG STREW	rilase		R				ATA	-	379		after Command
mabo 3 t	nemma.	FORMAT A TRACK	Command W M	Codes	R	001	0	7		19	0 218	MRM	execution
Command	W	0 MFM 0 0 1 1 0 1	Command Codes	7-7-7		-	000	i da	RECA	LIBE	RATE	0	0   W
information	W	0 0 0 0 0 HDS DS1 DS0	Li wi	Command	W	10	0	0	0	0			To
baarama	W	10 N H	Bytes/Sector	Command	V-360 NO	0	0	0	0	0	1	1 1	Command Codes
	W	SC GPL	Sectors/Cylinder	Execution	W	10	U	U	U	0	0 D	S1 DS0	- W. L
	W	D 103	Gap 3 Filler Byte	Execution		1 1							Head retracted to Track 0
			L W I			1				100			Truck o
Execution			FDC formats an					SENS	EINT	ERRI	UPT STA	TUS	W
1816	nent et		entire cylinder	Command	W	0	0	0	0	1	0 0	0 0	Command Codes
Result	R	ST 0	Status information	Result	R	10			\$1	0 _			Status information a
	R	ST 1	after Command	maraya	R	1	-		_ PC	N _			the end of each seel
noitemo	R	ST 2	execution	neissymol	of east	8							operation about the
bnama	R	C 7 TO	In this case, the ID	bnami	100 10	B					2		FDC
	R	R	information has no						S	PECI	FY		
oitemotni	R	N H	meaning	Command	W	0	0	0	0	0	0 1	1	Command Codes
onomi	103 10	to H		baum	W						ни		- A - O - O - O - O - O - O - O - O - O
. 1	GITTION	SCAN EQUAL	3	1 9	W	0	_ HL1	Γ		19	110	ND	- R
Command	W	MT MFM SK 1 0 0 0 1	Command Codes			1		22.00	IOF -	DU			2
Sebo0 B	W	0 0 0 0 0 HDS DS1 DS0	W business	gatura t	1000000		-	SEN	ISE D	HIVE	STATUS	•	
	W	C	Sector ID information	Command	W	0	0	0	0	0	1 (	0	Command Codes
oltamolok	W	B D	prior to Command execution	rolling motors	W	0	0	0	0	0	HDS DS	1 DS0	1 00
bnamme	W	R U	evacation	Result	R	10			_ ST	3	TITLE		Status information
	W	EOT F	39		dispos	10							about FDD
	W	GPL	- W							EEK			W
THE STATE OF	W	STP O	-1 10	C	141	Ι.	0	_		23.7	-		In the land
Execution			Data compared	Command	W	0	0	0	0		1 1		Command Codes
1011	1017-01		between the FDD		W	0	0	0			HDS DS	51 DS0	
the FDD	STORY		and main-system	1918	W		-		_ NO	N _			noitucexa
Result	R	ST A	Status information	Execution		la l							Head is positioned
Hesuit	R	ST 0 ST 1	after Command	nost-									over proper Cylinder
bname	R	ST 2 TA	execution	hnami		10							on Diskette
1	R	C TR	81 9	1	ollupe	Xe			181	VALI	ID.		
and the same of th	R	H D	Sector ID information						-	-			77 6
intomutuc	R	R H	after Command	Command	W	8		In	valid	Code	es		Invalid Command
bneme	R	N SI	execution	bnemr		9 .							Codes (NoOp - FDC
				1		15							goes into Standby State)
				Result	R	Non			CT	0	son elegal		ST 0 = 80
				. TOOUTE	1.1	1-		-	_ 01	0 _			
													da 101 - (16) c





**Table 3. Command Mnemonics** 

SYMBOL	NAME	DESCRIPTION
A <sub>0</sub>	Address Line 0	$A_0$ controls selection of Main Status Register ( $A_0 = 0$ ) or Data Register ( $A_0 = 1$ ).
C	Cylinder Number	C stands for the current selected Cylinder track number 0 through 76 of the medium.
D	Data OM OM	D stands for the data pattern which is going to be written into a Sector.
D <sub>7</sub> -D <sub>0</sub>	Data Bus	8-bit Data Bus where D <sub>7</sub> is the most significant bit, and D <sub>0</sub> is the least significant bit.
DS0, DS1	Drive Select	DS stands for a selected drive number 0 or 1.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT 10	End of Track	EOT stands for the final Sector number of a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync Field).
Н	Head Address	H stands for head number 0 or 1, as specified in ID field.
HDS	Head Select	HDS stands for a selected head number 0 or 1 (H = HDS in all command words).
HLT :	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MFM	FM or MFM Mode	If MF is low, FM mode is selected and if it is high, MFM mode is selected.
MT	Multi-Track	be performed (a cylinder under both HD0
N	Number	N stands for the number of data bytes written in a Sector.

COMMAND DESCRIPTION
---------------------

During the Command Phase, the Main Status Register must be polled by the CPU before each byte is written into the Data Register. The DIO (DB6) and RQM (DB7) bits in the Main Status Register must be in the "0" and "1" states respectively, before each byte of the command may be written into the 8272. The beginning of the execution phase for any of these commands will cause DIO and RQM to switch to "1" and "0" states respectively.

#### After writing data into the current sectoATAC CARR

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR)

SYMBOL	NAME	DESCRIPTION
NCN 39	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
Ranij	Record yed steb e	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC mad	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip gainsom	SK stands for Skip Deleted Data Address Mark.
SRT Daga en	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). The same Stepping Rate applies to all drives (F=1 ms, E=2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0\!=\!0$ ). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP polibolit i itaa OG (doleh t	ole twice withou "R"), then the F	During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.

compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-bybyte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 4 below shows the Transfer Capacity.

expend has notices note to bleit OI and ab Table 4. Transfer Capacity

Multi-Track	MFM/FM MFM	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
er 1 00 a	S Rogis	00 ps	(128) (26) = 3,328 (256) (26) = 6,656	26 at Side 0 or 26 at Side 1
respecti	br0s 0	o) te <sup>00</sup> a ba	(128) (52) = 6,656 (256) (52) = 13,312	26 at Side 1
opeosies or obna		02 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(256) (15) = 3,840 (512) (15) = 7,680	15 at Side 0 or 15 at Side 1
sad filata 1	R sol of	10 01 9 m s 02	(256) (30) = 7,680 (512) (30) = 15,360	15 at Side 1
0 00 F0ag	bnii10	02 03	(512) (8) = 4,096 (1024) (8) = 8,192	8 at Side 0 or 8 at Side 1
1 1	esta)(sta	Q 0 02 QM	(512) (16) = 8,192 (1024) (16) = 16,384	8 at Side 1



The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to 0FFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every  $27~\mu s$  in the FM Mode, and every  $13~\mu s$  in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 5 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 5. ID Information When Processor
Terminates Command

AT 100	A) reseig	Final Sector Transferred to		ID Information at Result Phase					
МТ	EOT	Processor	C	H	R	N			
81	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R+1	NC			
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	C+1	NC	R=01	NC			
o tor a	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC.	R+1	NC			
to red	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C+1	NC	R=01	NC			
VGO	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R+1	NC			
	08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	NC	LSB	R=01	NC			
ori) r (8 e)lis e	0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R+1	NC			
11,50	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C+1 aboM	LSB	R=01	NC			

Notes: 1. NC (No Change): The same value as the one at the beginning of command

LSB (Least Significant Bit): The least significant bit of H is complemented.

#### WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same; refer to the Read Data Command for details:

- Transfer Capacity
- · EN (End of Cylinder) Flag
- ND (No Data) Flag

- Head Unload Time Interval () 918 and heatile mental.
- . ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 us in the FM mode. and every 15 us in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command.

#### sector 20, then the Scan Com ATAC CETTING

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

# READ DELETED DATA all ni tee pall (nun tevo) Ao

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

which is the current head position w XXART A DASH This command is similar to READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this against PCN, and when NCN = PCN, then chammoo is

This command terminates when EOT number of sectors have been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

#### **READ ID**

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the IN-DEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high) and the command is terminated.

whole sector of data is compared, if the conditions are

# FORMAT A TRACK and at number of the sector number o

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected. Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the 8272 for each sector on the track. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R+1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes if the FDC encounters a Delete.notination.

Table 6 shows the relationship between N. SC. and GPL for various sector sizes: and no notose tast ent as not

Table 6. Sector Size Relationships

FORMAT	SECTOR SIZE	N	sc	GPL <sup>1</sup>	GPL <sup>2</sup>	REMARKS
FM Mode	128 bytes/Sector 256 512	00 01 02	1A <sub>(16)</sub> 0F <sub>(16)</sub> 08	07(16) OE(16) 1B(16)	1B(16) 2A(16) 3A(16)	IBM Diskette 1 IBM Diskette 2
FM Mode	1024 bytes/Sector 2048 4096	03 04 05	04 02 01	=	_	
MFM Mode	256 512 1024 2048 4096 8192	01 02 03 04 05 06	1A(16) 0F(16) 08 04 02 01	OE(16) 1B(16) 35(16)	36(16) 54(16) 74(16)	IBM Diskette 20

- Note: 1. Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.
  - 2. Suggested values of GPL in format command

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order to show that a I



#### SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of D<sub>FDD</sub> = D<sub>Processor</sub>, D<sub>FDD</sub> ≤ D<sub>Processor</sub>, or D<sub>FDD</sub> ≥ D<sub>Processor</sub>. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R+STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high). the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 7 shows the status of bits SH and SN under various conditions of SCAN.

Table 7. Scan Status Codes

	STATUS R	EGISTER 2	COMMENTS	
COMMAND	BIT 2 = SN	BIT 3 = SH		
corld tures, who	0	BRY MOFE	D <sub>FDD</sub> = D <sub>Processor</sub>	
Scan Equal	Janean e	100 1011 36	DFDD # DProcessor	
FDB at the end	0	wiends of t	D <sub>FDD</sub> = D <sub>Processor</sub>	
Scan Low or Equal	0	0	D <sub>FDD</sub> < D <sub>Processor</sub>	
den ma em ei	50 c4 1 5	0 1	D <sub>FDD</sub> < D <sub>Processor</sub> D <sub>FDD</sub> ≰ D <sub>Processor</sub>	
O BIU BBIRNINI	0	DO LA COLO	D <sub>FDD</sub> = D <sub>Processor</sub>	
Scan High or Equal	818 0 3 51	8 7 0 0 0	D <sub>FDD</sub> > D <sub>Processor</sub>	
ennie YOARR	to Inches	0	D <sub>FDD</sub> > D <sub>Processor</sub> D <sub>FDD</sub> ≱ D <sub>Processor</sub>	

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK=0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK=1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK=1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors STP=01, or alternate sectors STP=02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP=02, MT=0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27  $\mu$ s (FM Mode) or 13  $\mu$ s (MFM Mode). If an Overrun occurs the FDC terminates the command.

### read all the data in the sector and set the Chiffso In Status Register 2 to a 1 (high), and then termin/ABB/s

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and performs the following operation if there is a difference:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated.



#### RECALIBRATE

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIP-MENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

#### **SENSE INTERRUPT STATUS**

An Interrupt signal is generated by the FDC for one of the following reasons:

- 1. Upon entering the Result Phase of:
  - a. Read Data Command
  - b. Read a Track Command
  - c. Read ID Command
  - d. Read Deleted Data Command
  - e. Write Data Command
  - f. Format a Cylinder Command
  - g. Write Deleted Data Command
  - h. Scan Commands
- 2. Ready Line of FDD changes state
- 3. End of Seek or Recalibrate Command
- 4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Table 8. Seek, Interrupt Codes

SEEK END	INTERR	UPT CODE	YH I Bauti PY		
BIT 5	BIT 6	BIT 7	CAUSE		
o dicate the cotected signal		This bit is	Ready Line changed state, either polarity		
1 icate the statu rom the FDD.	DD. 0	fromone I	Normal Termination of Seek or Recalibrate Command		
icate tits statu from the FDD icate the statu	isingia 0 st	anT out to	Abnormal Termination of Seek or Recalibrate Command		

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

#### SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . . . FE = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

#### SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

### INVALID tes al gall eint rebnity

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the 8272 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the 8272 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find a 80H indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

NO.	NAME	SYMBOL	THE PERSON NAMED IN COLUMN TO PARTY.
		STATUS	S REGISTER 0
D <sub>7</sub>	Interrupt Code	IC	D <sub>7</sub> =0 and D <sub>6</sub> =0 Normal Termination of Command, (NT). Command was completed and properly executed.
D <sub>6</sub>	d Unload*T outlon Phat te head un 16 to 240 n	IUT (Hea I the Exe	D <sub>7</sub> =0 and D <sub>8</sub> =1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
ni e orc		is, 02 = 3 ma) defii ulaes. Tr roremen	D <sub>7</sub> = 1 and D <sub>6</sub> = 0 Invalid Command issue, (IC). Command which was issued was never started.
	ead Load a ed Load el beration et 254 me i	e HLT (H n the Ha Wildte o rom 2 to	$D_7$ = 1 and $D_6$ = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D <sub>5</sub>	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D <sub>4</sub>	Equipment Check	me <sup>Oa</sup> ndi sa sas re sal time	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recali- brate Command) then this flag is set.
D <sub>3</sub>	Not Ready	NR Bilego At Lai tid en nertw br	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D <sub>2</sub>	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D <sub>1</sub>	Unit Select 1	US 1	These flags are used to indicate a
D <sub>0</sub>	Unit Select 0	US 0	Drive Unit Number at Interrupt
		STATUS	REGISTER 1
D <sub>7</sub>	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D <sub>6</sub>	tenos si do	to the F	Not used. This bit is always 0 (low).
D <sub>5</sub>	Data Error	of DE O	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D <sub>4</sub>	Over Run	OR OR OR OTS	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D <sub>3</sub>	a butt tind a	gister U	Not used. This bit always 0 (low).
	No Data		During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
	to use this FDC in a s		During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

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iste	Schecks the	TATUS R	EGISTER 1 (CONT.)
D <sub>1</sub>		WA ignal re in Statt in Statt	detecte e write protect signal from
D <sub>0</sub>	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set
	I I TE Commas READY signasons spelles	mmand LIBRA of the nand, a	If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
		STATU	S REGISTER 2
D <sub>7</sub>			Not used. This bit is always 0 (low).
D <sub>6</sub>	Control Mark	СМ	During executing the READ DATA of SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D <sub>5</sub>	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D <sub>4</sub>	Wrong Cylinder	WC 5	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D <sub>3</sub>	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D <sub>2</sub>	Scan Not Satisfied	SN sn al	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D <sub>1</sub>	Bad Cylinder	BC upinu e	This bit is related with the ND bit, and when the content of C on the medium is different from that store in the IDR and the content of C is FF, then this flag is set.
D <sub>0</sub>	Missing Address Mark in Data Field	MD	When data is read from the medium if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
	0.000.000	STATU	JS REGISTER 3
D <sub>7</sub>	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D <sub>6</sub>	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D <sub>5</sub>	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D <sub>4</sub>		/OTron Seek c	This bit is used to indicate the status of the Track 0 signal from the FDD.
D <sub>3</sub>	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD
D <sub>2</sub>	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D <sub>1</sub>	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD
D <sub>0</sub>	Unit Select 0	US 0	This bit is used to indicate the statu of the Unit Select 0 signal to the FDD

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### **ABSOLUTE MAXIMUM RATINGS\***

Operating Temperature	10°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	0.5 to +7 Volts
All Input Voltages	-0.5 to $+7$ Volts
Supply Voltage V <sub>CC</sub>	0.5 to +7 Volts
Power Dissipation	1 Watt

\*T\_ = 25°C

NOTICE: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Wilto Cypla

## D.C. CHARACTERISTICS $(T_A = 0^{\circ}C \text{ to } +70^{\circ}C, V_{CC} = +5V \pm 5\%)$

	en an Parameter	L	imits		Test wat
Symbol		Min.	Max.	Unit mont b	
V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	VF monty	Med Tist Dela
V <sub>IH</sub> ,	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	Variable	Med 170
V <sub>IL</sub>	(CLK & WR CLK)	-0.5	0.65	Violari si	NO CIRC YOUR
V <sub>IH</sub> and 8	(CLK & WR CLK)	2.4	V <sub>CC</sub> + 0.5	V 4GE	DROI DROI 10
V <sub>OL</sub>	Output Low Voltage		0.45	V To to KI	I <sub>OL</sub> = 2.0 mA
V <sub>OH</sub>	Output High Voltage	2.4	V <sub>CC</sub>	V	$I_{OH} = -200  \mu A$
MFM= OO	V <sub>CC</sub> Supply Current	1.012	150	mA	(O NOW YOU
I <sub>IL</sub>	Input Load Current (All Input Pins)	962	10 -10	μΑ μΑ	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = 0V
I <sub>LOH</sub>	High Level Output Leakage Current		10 yeled on	A White Au to Wo	V <sub>OUT</sub> =V <sub>CC</sub>
I <sub>LOL</sub> = Main	Low Level Output Leakage Current		-10	μΑ 100R of quies	NAME OF THE PARTY

## **CAPACITANCE** $(T_A = 25^{\circ}C, f_C = 1 \text{ MHz}, V_{CC} = 0V)$

	Parameter	Lin	nits	Unit Quied A	Test Conditions
Symbol		Min.	Max.		
C <sub>IN(Φ)</sub>	CIN(Φ) Clock Input Capacitance		20	19818 pFot gute8	All Pins Except
C <sub>IN</sub> Input Capacitance			10	(qast.pFt most bio	Pin Under Test Tied to AC
Cout	Output Capacitance		20	pF <sub>amil</sub> alo	Ground

3, tog wide min. Is for distance drive units, in the page of same unit, tog can be ranged from time to 16 ma with 8 littly clock period, and 2 ms to 32 ms





# A.C. CHARACTERISTICS (T<sub>A</sub> = 0°C to 70°C; V<sub>CC</sub> = +5.0V ± 5%)

Symbol	negray cause permanent of	ameter	1777	0°881+	O Min.	Max.	Unit	Test Conditions
	Clock High Period	e. Imsises device at		+7 Volts	125		ns	Note 4 CV Jugni III
tRST	Deser Midfil	+7 Volts Indicated in		01 8.014		tcy	Supply Voltage Vo	
Read Cycle								lower Dissipation
	Select Setup to RD↓				0		ns	
	Select Hold from RDt				0		ns	T <sub>A</sub> =25°C
	RD Pulse Width				250		ns	
	Data Delay from RD↓					200	ns	
t <sub>DF</sub>	Output Float Delay				20	100	ns	
Write Cycle								
t <sub>AW</sub>	Select Setup to WRI Select Hold from WRt		V <sub>GC</sub> =		0	TICS	ns ns	C. CHARACT
tww	WR Pulse Width		etimita		250		ns	
	Data Setup to WRt				150		ns	
two	Data Hold from WRt	.xsW			5 1919	Paran	ns	Symbol
Interrupts								
	INT Delay from RDt			.0-	/oltage	500	ns	V <sub>aL</sub> ,
t <sub>WI</sub>	INT Delay from WRt				Voltage	500	ns	HIV
DMA			U.3s		O PROVIDE	Might A	NOT TO SERVICE	, HI Y
	DRQ Cycle Period		-0.5		13	HW & X	шиs	V <sub>II</sub> .
	DACK+ to DRQ+				-	200	ns	
nun					800	HAN 'S X	ns	8 MHz clock
LICEAN	DRQt to WRI				250 epsiloV	12 10	ns	8 MHz clock 8 MHz clock
Haller	DRQT to RDT or WRT						μS	6 MHZ CIOCK
FDD Interface	HO! Y			TYP 1	epstloV r	put Hig	TUO	ROA
twcy	WCK Cycle Time			2 or 4 1 or 2	Current	Supply	μS	MFM = 0 Note 2
twch	WCK High Time			250	100	350	ns	
ton	Pre-Shift Delay from WCK†				20	100	ns	nd nd
t <sub>CD</sub>	WDA Delay from WCK†				20	100	ns	
twpp	Write Data Width	. 01			t <sub>WCH</sub> - 50	leve I	ns	Rod
***	WET to WCKT or WEL to WCKL De	lay			20	100	ns	
twwcy	Window Cycle Time			2	2110/111	o alles	μS	MFM = 0
UT= +0.45V	oV Au	0.5		1_	Torotto	Java L	<u>un  </u>	MFM = 1
	Window Setup to RDD†				15 718111	O epsa	ns	
IIDAA	Window Hold from RDD↓				15	-	ns	
tRDD	RDD Active Time (HIGH)				40	1	ns	
FDD SEEK/ DIRECTION/				/0 = <sub>DO</sub> V	$f_{\rm c}=1$ MHz.	= 25°C	(T) Ξ	APACITANC
STEP								1
tus isem	US <sub>0.1</sub> Setup to RW/SEEK†	atlmi			12		μS	
t <sub>SD</sub> enotition of	RW/SEEK Setup to LCT/DIR				6.8	Pari	μS	Symbol
t <sub>DS</sub>	RW/SEEK Hold from LCT/DIR				30		μS	
001	LCT/DIR Setup to FR/STEP1				: Capacitano	ok input	μS	maQ.
	LCT/DIR Hold from FR/STEP				24		μS	8 MHz cloc
	DS <sub>0,1</sub> Hold from FR/Step↓			-	95 na)10	H Capa	μS	City
STP	STEP Active Time (High) STEP Cycle Time			5	9033 1106	so hia	μS	Note 3 1000
	FAULT RESET Active Time (High)				8	10	μS	Note 3
	INDEX Pulse Width			625		10	μS	

## NOTES:

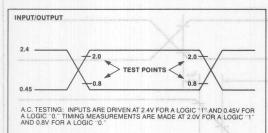
- 1. Typical values for  $T_A = 25\,^{\circ}\text{C}$  and nominal supply voltage.
- 2. The former values are used for standard floppy and the latter values are used for mini-floppies.
- 3.  $t_{SC} = 33 \mu s$  min. is for different drive units. In the case of same unit,  $t_{SC}$  can be ranged from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.
- 4. From 2.0V↑to +2.0V↓.

1-159

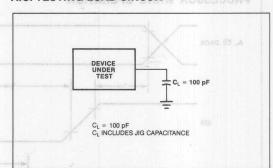




## A.C. TESTING INPUT, OUTPUT WAVEFORM

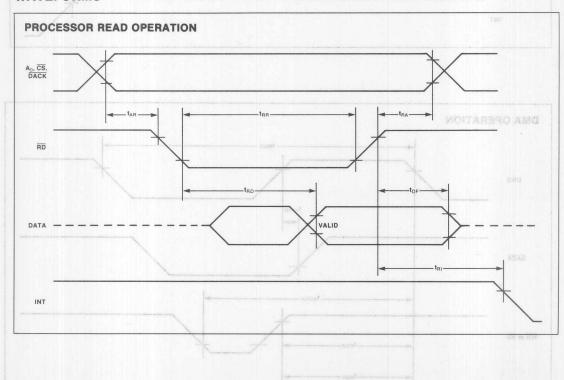


## A.C. TESTING LOAD CIRCUIT



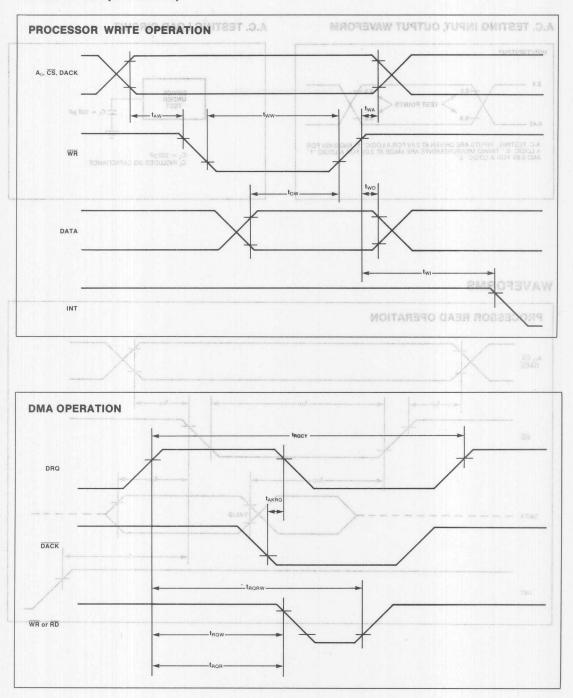
WAVEFORMS (Continued)

## **WAVEFORMS**







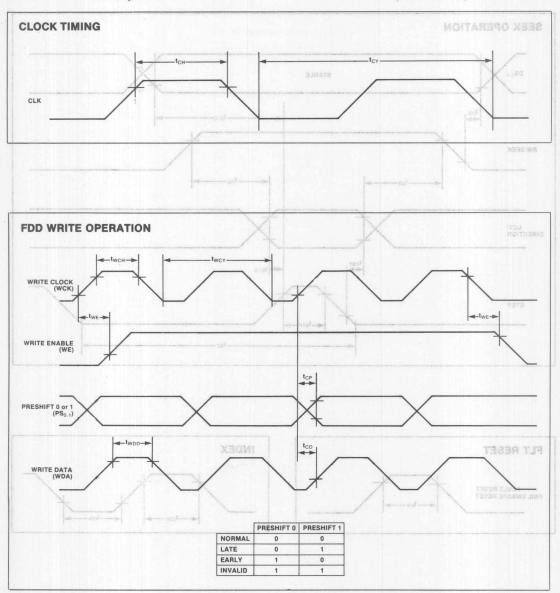






AFN-01259B

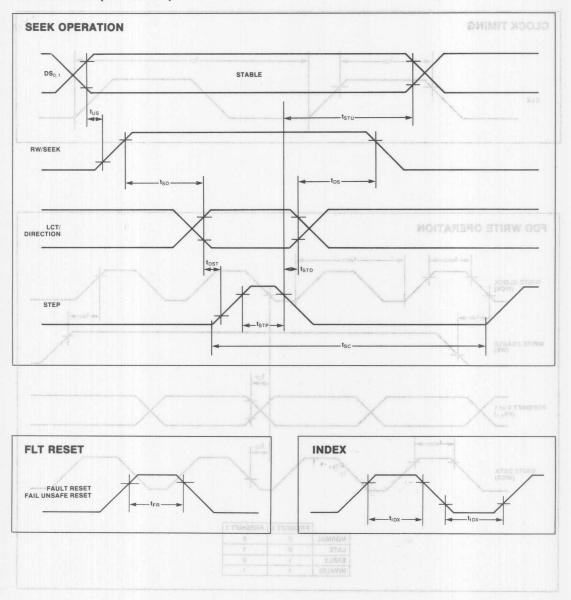
## **WAVEFORMS** (Continued)





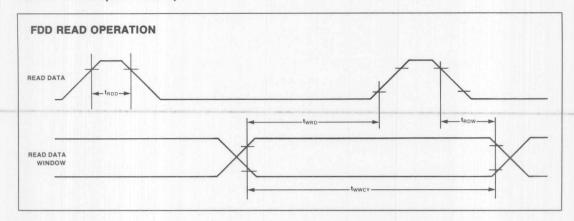


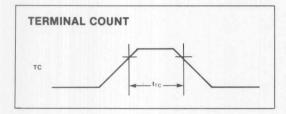
## **WAVEFORMS (Continued)**

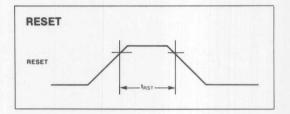




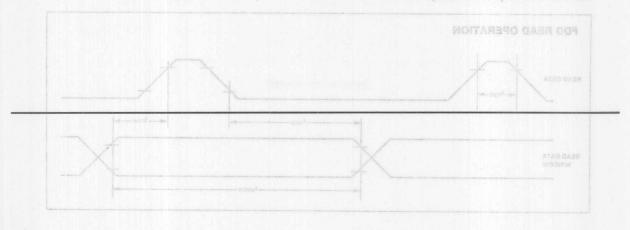
# WAVEFORMS (Continued) 0150111111111000 6160

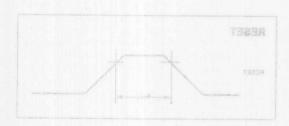






# Data Communications







## PROGRAMMABLE COMMUNICATION INTERFACE

- Synchronous and Asynchronous Operation
- Synchronous 5–8 Bit Characters;
  Internal or External Character
  Synchronization; Automatic Sync
  Insertion
- Asynchronous 5–8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling
- Synchronous Baud Rate—DC to 64K Baud

- Asynchronous Baud Rate—DC to 19.2K Baud
- Full-Duplex, Double-Buffered
  Transmitter and Receiver
- Error Detection—Parity, Overrun and Framing
- Compatible with an Extended Range of Intel Microprocessors
- 28-Pin DIP Package antercoon At 258 on T
- All Inputs and Outputs are TTL box 1858 Compatible
- Single +5V Supply
- Single TTL Clock 1970 elduck and A1538

The Intel® 8251A is the enhanced version of the industry standard, Intel 8251 Universal Synchronous/ Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's microprocessor families such as MCS-68, 80, 85, and iAPX-86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using N-channel silicon gate technology.

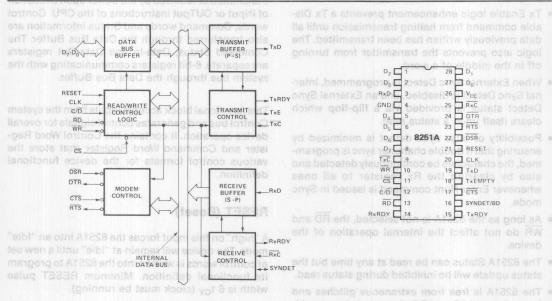


Figure 1. Block Diagram

Figure 2. Pin Configuration



#### **FEATURES AND ENHANCEMENTS**

The 8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.

Vicque +5V Supply

- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the RD and WR do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous Baud rate from DC to 64K.

#### **FUNCTIONAL DESCRIPTION**

#### General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed for a wide range of Intel microcomputers such as 8048, 8080, 8085, 8086 and 8088. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support most serial data techniques in use, including IBM "bi-sync."

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

#### **Data Bus Buffer**

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-In and Data-Out registers are separate, 8-bit registers communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

## **RESET (Reset)**

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6  $t_{\rm CY}$  (clock must be running).

A command reset operation also puts the device into the "Idle" state.

Figure 1. Block Diagram



## CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

## WR (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

## RD (Read)

A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.

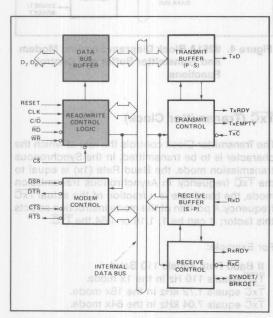


Figure 3. 8251A Block Diagram Showing Data
Bus Buffer and Read/Write Logic
Functions

	C/D	RD	WR	CS	
113	0	0	1	0	8251A DATA → DATA BUS
	0	1010	0	0	DATA BUS → 8251A DATA
	1110	0	DIMON	0	STATUS ⇒ DATA BUS
	101 er	1 1	0,5	0	DATA BUS ⇒ CONTROL
	X	olo bis	allor	0	DATA BUS ⇒ 3-STATE
	X	X	X	1	DATA BUS ⇒ 3-STATE

## C/D (Control/Data)

This input, in conjunction with the WR and RD inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.

1 = CONTROL/STATUS; 0 = DATA.

## CS (Chip Select) dene gnied dogu notezimenent

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When  $\overline{CS}$  is high, the Data Bus is in the float state and  $\overline{RD}$  and  $\overline{WR}$  have no effect on the chip.

#### **Modem Control**

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

## DSR (Data Set Ready)

The DSR input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The DSR input is normally used to test modem conditions such as Data Set Ready.

### DTR (Data Terminal Ready)

The DTR output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The DTR output signal is normally used for modem control such as Data Terminal Ready.

## RTS (Request to Send)

The RTS output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The RTS output signal is normally used for modem control such as Request to Send.

## CTS (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or CTS off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down.

C/D (Control/Data)



#### **Transmitter Buffer**

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of TxC. The transmitter will begin transmission upon being enabled if  $\overline{\text{CTS}} = 0$ . The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable or  $\overline{\text{CTS}}$  is off or the transmitter is empty.

## Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

# TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of WR when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data Input Register.

## TxE (Transmitter Empty)

When the 8251A has no characters to send, the TxEMPTY output will go "high." It resets upon receiving a character from the CPU if the transmitter is enabled. TxEMPTY remains low when the transmitter is disabled even if it is actually empty. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplex operational mode.

In the Synchronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers." TXEMPTY does not go low when the SYNC characters are being shifted out.

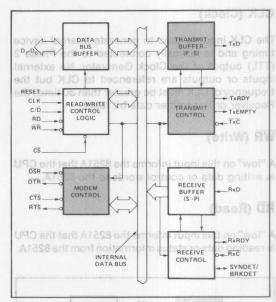


Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

## TxC (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the TxC frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual TxC frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the TxC.

#### For Example:

If Baud Rate equals 110 Baud,

TxC equals 110 Hz in the 1x mode.

TxC equals 1.72 kHz in the 16x mode.

TxC equals 7.04 kHz in the 64x mode.

The falling edge of  $\overline{\text{TxC}}$  shifts the serial data out of the 8251A.

#### Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of  $\overline{\text{RxC}}$ .



# intel

## Receiver Control MOITAREGO GELHATEG

This functional block manages all receiver-related activities which consists of the following features.

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition." Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

Parity error detection sets the corresponding status bit. ed. D. ArdS8 edition represents a same

The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

## RxRDY (Receiver Ready) on a notion transform

This output indicates that the 8251A contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

RxEnable, when off, holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

## RxC (Receiver Clock) 100 OMY2) TEGMY2

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of RxC. In Asynchronous Mode, the Baud Rate is a fraction of the actual RxC frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 the RxC.

SYNC character in the Receive mode. If seeme SYNC

Baud Rate equals 300 Baud, if

RxC equals 300 Hz in the 1x mode;

RxC equals 4800 Hz in the 16x mode;

RxC equals 19.2 kHz in the 64x mode.

Baud Rate equals 2400 Baud, if

RxC equals 2400 Hz in the 1x mode;

RxC equals 38.4 kHz in the 16x mode;

RxC equals 153.6 kHz in the 64x mode.

Data is sampled into the 8251A on the rising edge of  $\overline{\text{RxC}}$ .

NOTE: In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both TxC and RxC will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

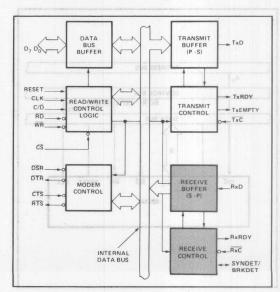


Figure 5. 8251A Block Diagram Showing
Receiver Buffer and Control Functions



# SYNDET (SYNC Detect/ of Taylogo R) OXA BRKDET Break Detect)

This pin is used in Synchronous Mode for SYN-DET and may be used as either input or output, programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bisync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

The Receiver Clock controls the rate at which the

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251A to start assembling data characters on the rising edge of the next RxC. Once in SYNC, the "high" input signal can be removed. When External SYNC Detect is programmed, Internal SYNC Detect is disabled.

## **BREAK (Async Mode Only)**

This output will go high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

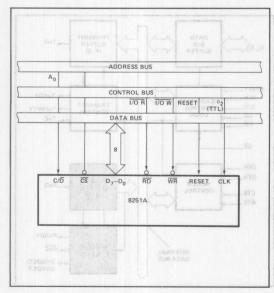


Figure 6. 8251A Interface to 8080 Standard
System Bus

## DETAILED OPERATION DESCRIPTION

# General polyolios of the following

The complete functional definition of the 8251A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251A. On the other hand, the 8251A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The 8251A cannot begin transmission until the Tx Enable (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send (CTS) input. The TxD output will be held in the marking state upon Reset.

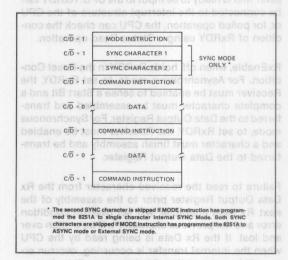


Figure 7. Typical Data Block





## Programming the 8251A of augmontance

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

- 1. Mode Instruction as and epivorg for secon USO
- 2. Command Instruction T A 238 and enoted and

# Mode Instruction Www (about released Divine

This instruction defines the general operational characteristics of the 8251A. It must follow a Reset operation (internal or external). Once the Mode Instruction has been written into the 8251A by the CPU, SYNC characters or Command Instructions may be written.

#### Command Instruction

This instruction defines a word that is used to control the actual operation of the 8251A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation (see Figure 7). The Mode Instruction must be written immediately following a Reset operation, prior to using the 8251A for data communication.

All control words written into the 8251A after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251A at any time in the data block during the operation of the 8251A. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251A back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

# To abbum and to bestant if divining ent to album and Mode Instruction Definition and stab tast and

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components, one Asynchronous and the other Synchronous, sharing

the same package. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

## Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of TxC at a rate equal to 1, 1/16, or 1/64 that of the TxC, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A the TxD output reamins "high" (marking) unless a Break (continuously low) has been programmed.

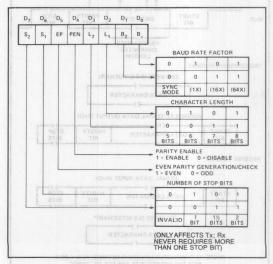


Figure 8. Mode Instruction Format,
Asynchronous Mode

# l<sub>g</sub>ini

#### Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16X or 64X mode only). If a low is detected again, it is a valid START bit. and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of RxC. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the receiver reguires only one stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the 8251A.

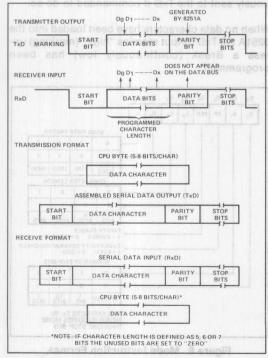
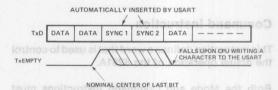


Figure 9. Asynchronous Mode

#### Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251A which usually is a SYNC character. When the CTS line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of TxC. Data is shifted out at the same rate as the TxC.

Once transmission has started, the data stream at the TxD output must continue at the  $\overline{\text{TxC}}$  rate. If the CPU does not provide the 8251A with a data character before the 8251A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the 8251A.



#### Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of RxC. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the 8251A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USARTends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit. "offining noticurtent should

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the 8251A out of the HUNT mode. The high level can be removed after one RXC cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.



letni

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in Hunt, regardless of whether the Receiver is enabled or not.

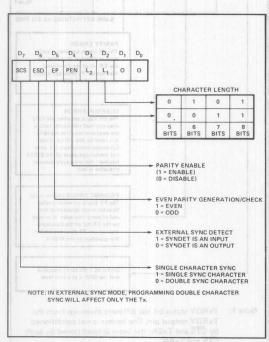


Figure 10. Mode Instruction Format,
Synchronous Mode

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one," thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. Note that the SYNDET F/F is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the 8251A to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary. - 00 January

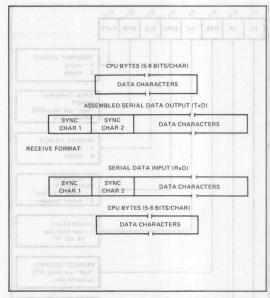


Figure 11. Data Format, Synchronous Mode

#### **COMMAND INSTRUCTION DEFINITION**

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the sync characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" (C/D = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.

#### Note: Internal Reset on Power-up

When power is first applied, the 8251A may come up in the Mode, Sync character or Command format. To guarantee that the device is in the Command Instruction format before the Reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with  $C/\bar{D}=1$  configures sync operation and writes two dummy 00H sync characters. An Internal Reset command (40H) may then be issued to return the device to the "Idle" state.





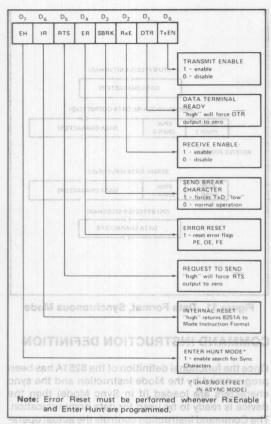


Figure 12. Command Instruction Format

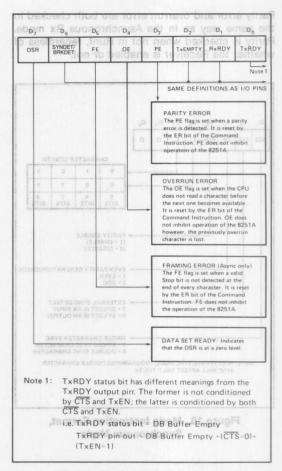
#### STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (Status update is inhibited during status read.)

A normal "read" command is issued by the CPU with  $C/\overline{D}=1$  to accomplish this function,

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.



The CPU tamed bean Reatless (1914) This will also HUNT mode it synchronization is lost. This will also

#### APPLICATIONS OF THE 8251A

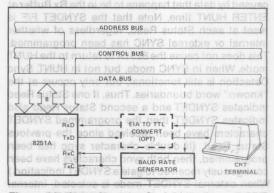


Figure 14. Asynchronous Serial Interface to CRT Terminal, DC—9600 Baud in the last less than the serial Interface to CRT Terminal, DC—9600 Baud in the last less than the last less than





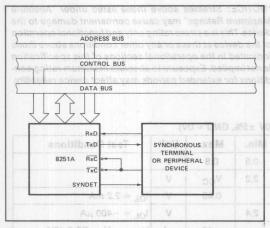


Figure 15. Synchronous Interface to Terminal or Peripheral Device

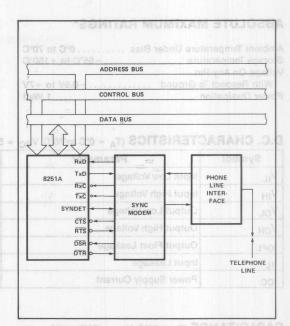


Figure 17. Synchronous Interface to Telephone Lines

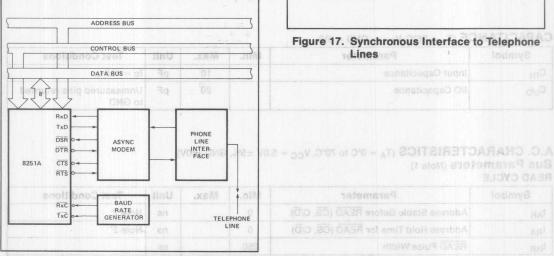


Figure 16. Asynchronous Interface to Telephone Lines

	Address Stable Before READ (CS, C/D Address Hold Time for READ (CS, C/D	
rajer		
	Address Hold Time for	
	Data Dalay from READ	

	.niss			Test Conditions					
			en						
Address Hold Time for WRITE	0								
			ns						
Recovery Time Batween WRITES				ote 4					





#### **ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bi	as0°C to 70°C
Storage Temperature	
Voltage On Any Pin	ADDRESS BU
With Respect To Ground	0.5V to +7V
Power Dissipation	14 JORTHOO 1 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# D.C. CHARACTERISTICS ( $T_A = 0$ °C to 70°C, $V_{CC} = 5.0V \pm 5$ %, GND = 0V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V <sub>IL</sub> зионч	Input Low Voltage	-0.5	0.8	HAIRV SO	→ SXA Arasa
V <sub>IH</sub>	Input High Voltage	2.2	Vcc	٧	T3GHY8
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 2.2 mA
Vон	Output High Voltage	2.4		V	$I_{OL} = -400 \mu\text{A}$
OFL	Output Float Leakage	no ter	±10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> TO 0.45V
II вмониател	Input Leakage		±10	μΑΘ	VIN = VCC TO 0.45V
lcc	Power Supply Current	processor	100	mA	All Outputs = High

#### CAPACITANCE (TA = 25°C, VCC = GND = 0V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
CIN	Input Capacitance		10	pF	fc = 1MHz
C <sub>I/O</sub>	I/O Capacitance		20	pF	Unmeasured pins returned to GND

# A.C. CHARACTERISTICS ( $T_A = 0^{\circ}C$ to $70^{\circ}C$ , $V_{CC} = 5.0V \pm 5\%$ , GND = 0V) Bus Parameters (Note 1) READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t <sub>AR</sub>	Address Stable Before $\overline{\text{READ}}$ ( $\overline{\text{CS}}$ , $\text{C/}\overline{\text{D}}$ )	0	8137	ns	Note 2
t <sub>RA</sub>	Address Hold Time for $\overline{\text{READ}}$ ( $\overline{\text{CS}}$ , $\overline{\text{C/D}}$ )	0		ns	Note 2
t <sub>RR</sub>	READ Pulse Width	250		ns	
t <sub>RD</sub>	Data Delay from READ	enor	200	ns	3, Cc= 150 pF(aA .81 enugl
t <sub>DF</sub>	READ to Data Floating	10	100	ns	Lines

#### WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Test Condtions
t <sub>AW</sub>	Address Stable Before WRITE	0		ns	
twa	Address Hold Time for WRITE	0		ns	
tww	WRITE Pulse Width	250		ns	
t <sub>DW</sub>	Data Set-Up Time for WRITE	150		ns	
twD	Data Hold Time for WRITE	20		ns	
t <sub>RV</sub>	Recovery Time Between WRITES	6		tcy	Note 4





A.C. CHARACTERISTICS (Continued)

## A.C. CHARACTERISTICS (Continued)

#### OTHER TIMINGS

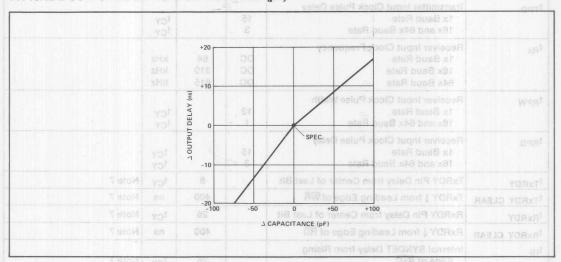
Symbol	Parameter abbA & barab	Min	Max.	Unit	Test Conditions
tcYad amiT visv	Clock Period	320	1350	ns	Notes 5, 6
t <sub>o</sub>	Clock High Pulse Width a show auchour	140	t <sub>CY</sub> -90	a nso	Writes for Asynchronous M
t̄g xill xill xill xill xill xill xill xil	Clock Low Pulse Width	90	Pollot eni e	ns	<ol> <li>Ine IXC and RXC frequent towl:</li> </ol>
t <sub>R</sub> , t <sub>F</sub>	Clock Rise and Fall Time	.5 tcy).	20 1	ns	For 16x and 64x Baud Rah
t <sub>DTx</sub>	TxD Delay from Falling Edge of TxC	1 28 clock	um, dysie im délay o	μs	<ol> <li>Reset False Wall = 0 top</li> <li>Status update can have a </li> </ol>
f <sub>Tx</sub>	Transmitter Input Clock Frequency 1x Baud Rate 16x Baud Rate 64x Baud Rate	DC DC DC	64 310 615	kHz kHz kHz	
<sup>t</sup> TPW	12	unagan.	t <sub>CY</sub>	A ING THATHA A LANGUE	
<sup>t</sup> TPD	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	15 3		t <sub>CY</sub>	A1 01 01 01 01 01 01 01 01 01 01 01 01 01
f <sub>Rx</sub> Receiver Input Clock Frequency 1x Baud Rate 16x Baud Rate 64x Baud Rate			64 310 615	kHz kHz kHz	
<sup>t</sup> RPW	Receiver Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	12	DEFVA (us)	t <sub>CY</sub>	
<sup>t</sup> RPD	Receiver Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	15 3	2 7 OALBA	t <sub>CY</sub>	
<sup>t</sup> TxRDY	TxRDY Pin Delay from Center of Last Bit	1	8	tcy	Note 7
TxRDY CLEAR	TxRDY ↓ from Leading Edge of WR		400	ns	Note 7
<sup>t</sup> RxRDY	RxRDY Pin Delay from Center of Last Bit	08-	26	tcy	Note 7
TRXRDY CLEAR	RxRDY ↓ from Leading Edge of RD		400	ns	Note 7
<sup>t</sup> ıs	Internal SYNDET Delay from Rising Edge of RxC		26	tcy	Note 7
t <sub>ES</sub>	External SYNDET Set-Up Time After Rising Edge of RxC	18	AVEFORE	tcy	Note 7
<sup>t</sup> TxEMPTY	TxEMPTY Delay from Center of Last Bit	20		tcy	Note 7
twc	Control Delay from Rising Edge of WRITE (TxEn, DTR, RTS)	8		tcy	Note 7 TUSTUOITUSMI
tca	Control to READ Set-Up Time (DSR, CTS)	20		tcy	Note 7

# A.C. CHARACTERISTICS (Continued)

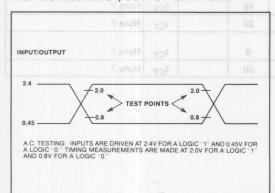
- 1. AC timings measured  $V_{OH}=2.0\,V_{OL}=2.0,V_{OL}=0.8$ , and with load circuit of Figure 1. 2. Chip Select (CS) and Command/Data (C/D) are considered as Addresses.
- 3. Assumes that Address is valid before Rp. 4. This recovery time is for Mode Initialization only. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 tcy and for Synchronous Mode is 16 tcy.
- The TxC and RxC frequencies have the following limitations with respect to CLK: For 1x Baud Rate, f<sub>Tx</sub> or f<sub>Rx</sub> ≤ 1/(30 tcy):

- For 16x and 64x Baud Rate,  $f_{Tx}$  or  $f_{Rx} \le 1/(4.5 \, t_{CY})$ . 6. Reset Pulse Width = 6  $t_{CY}$  minimum; System Clock must be running during Reset.
- 7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

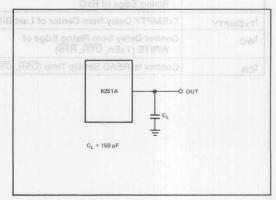
#### TYPICAL A OUTPUT DELAY VS. A CAPACITANCE (pF)



#### A.C. TESTING INPUT, OUTPUT WAVEFORM



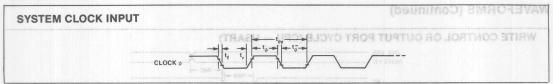
#### A.C. TESTING LOAD CIRCUIT

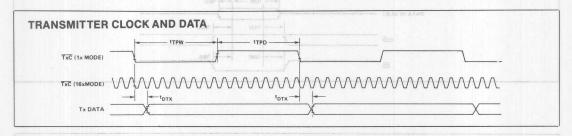


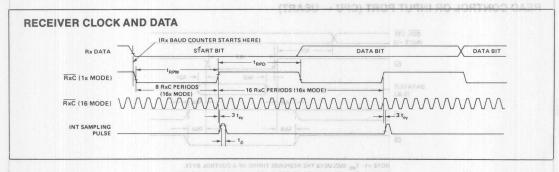


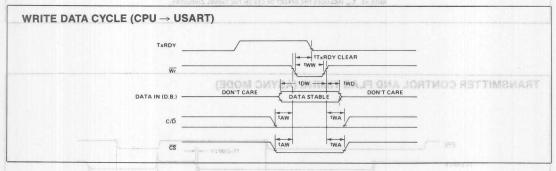


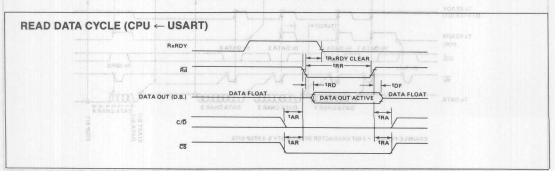
#### **WAVEFORMS**







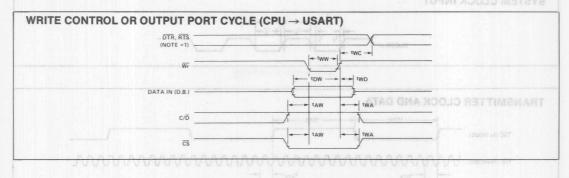


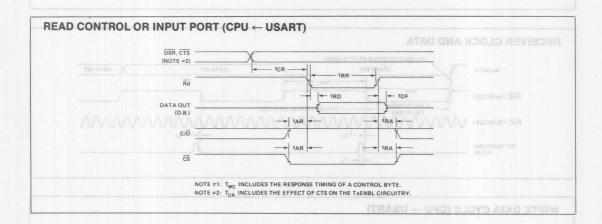


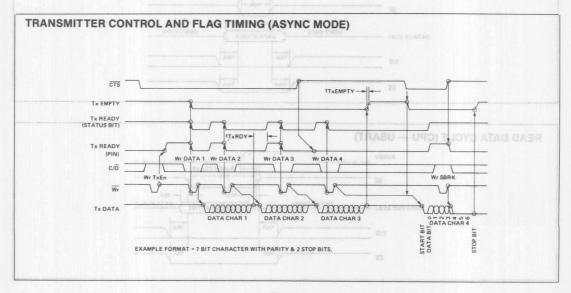




#### **WAVEFORMS (Continued)**

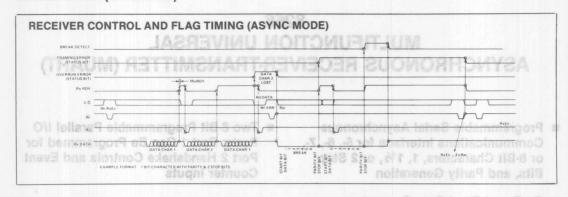


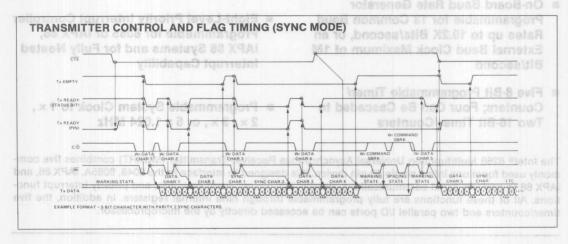


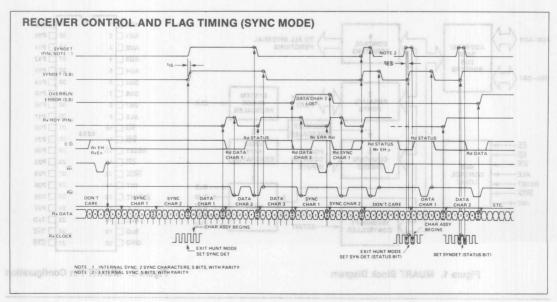




#### **WAVEFORMS (Continued)**







# RECEIVER CONTROL AND FLAG TIMING (AS 628) DEL **MULTIFUNCTION UNIVERSAL** ASYNCHRONOUS RECEIVER-TRANSMITTER (MUART)

- Programmable Serial Asynchronous Communications Interface for 5-, 6-, 7-, or 8-Bit Characters, 1, 11/2, or 2 Stop Bits, and Parity Generation
- Two 8-Bit Programmable Parallel I/O Ports; Port 1 Can Be Programmed for Port 2 Handshake Controls and Event **Counter Inputs**
- On-Board Baud Rate Generator **Programmable for 13 Common Baud** Rates up to 19.2K Bits/second, or an **External Baud Clock Maximum of 1M** Bit/second
- Eight-Level Priority Interrupt Controller Programmable for 8085 or iAPX 86, iAPX 88 Systems and for Fully Nested **Interrupt Capability**
- Five 8-Bit Programmable Timer/ Counters; Four Can Be Cascaded to Two 16-Bit Timer/Counters
- Programmable System Clock to 1 × , 2 x , 3 x , or 5 x 1.024 MHz

The Intel® 8256 Multifunction Universal Asynchronous Receiver-Transmitter (MUART) combines five commonly used functions into a single 40-pin device. It is designed to interface to the 8048, 8085A, iAPX 86, and iAPX 88 to perform serial communications, parallel I/O, timing, event counting, and priority interrupt functions. All of these functions are fully programmable through nine internal registers. In addition, the five timer/counters and two parallel I/O ports can be accessed directly by the microprocessor.

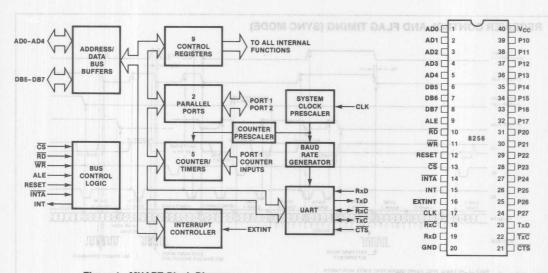


Figure 1. MUART Block Diagram

Figure 2. MUART Pin Configuration



Table 1. Pin Description

Symbol	Pin No.	Туре	Name and Function		
AD0-AD4 DB5-DB7	1-5 6-8	1/0	Address/Data: Three-State Address/Data lines which interface with the CPU lowe 8-bit address/data bus. The 5-bit address is latched on the falling edge of ALE. In 8048 and 8085 mode, AD0-AD3 are used		
	paeup	out fro	AD4 are used in oood and bood mode		
	12	the rest of the	written into or read from the control		
ALE	9	1	Address Latch Enable: Latches the Saddress lines on AD0-AD4 and CS or the falling edge.		
beau e	10°00 8 & A c	MTIES FOA FOA BO	Read Control: When this signal is low the previously selected register is enabled onto the data bus.		
WR 30	FA1ta	Stillis o add	Write Control: When this signal is low the value on the data bus is placed into the previously selected register.		
RESET	12 ga	en Ball St IN	Pulse provided by the CPU to initialize the system. The MUART remains "idle until it is reprogrammed by the CPU.		
CS asiden	13 bas to	junei	Chip Select: A low on this signal enables the MUART. It is latched with the address on the falling edge of ALE and RD and WR have no effect unless. CS was latched low during the ALI cycle.		
ni-alse of	A sarute	iel to	Interrupt Acknowledge: If the MUAR has been enabled to respond to interrupts, it puts an RST on the bus for the 8085 or a vector for the 8086. The bit in the interrupt register is reset when the interrupt is placed onto the bus.		
INT	15	0	Interrupt: A high signals the CPU that the MUART needs service.		
EXTINT	16 i-Maend auist8	A LEA 13. A I 11 tine	External Interrupt: A high on this pin signals that an external device requests service. EXTINT must be held high until		
CLK	17	Ikine I maj si	INTA or read interrupt occurs.  System Clock: This input provides at accurate timing source for the MUART It must be 1×, 2×, 3×, or 5× 1.024 MHz and is used by the baud rate generator and real time clocks.		
RxC	18	OVI	Receive Clock: If baud rate 0 is selected, this input clocks bits into RxL on the rising edge. If a baud rate from 1-0F <sub>16</sub> is selected, this output will provide a rising edge at the center each received data bit. This output remains high during start, stop, and		
RxD	1-dgld /	tive.	Parity bits.  Receive Data: Serial data input from the		
I Illay n	ransitio	Wol	modem or terminal to the MUART.  Ground: Power supply and logic ground		
GND	20	PS	reference.		

	Symbol	Pin No.	Туре	Name and Function
	V <sub>CC</sub>	40	PS	Power: +5V POWER supply.
	P17-P10	32-39 1000 fqu	nounc	Parallel I/O Port 1: Each pin can be programmed as an input or an output to perform general purpose I/O functions for the CPU under software control. In addition to general I/O, I/O Port 1 can be programmed to a variety of special functions for handshake control, counter inputs, and special communications functions.
不 明 然 田 於	P27-P20		I/O IA OI ISON	Parallel I/O Port 2: Each nibble (4 bits) of this port can be either an input or an output. Also, this port can be used as a bidirectional 8-bit port using handshake lines in Port 1.
	iorQxTrm receiv	23 ) ent pr	n.O no	<b>Transmit Data:</b> This output carries the serial data to the terminal or modem from the MUART.
	an DXT is a contact of the contact o	sd by a purpor liby char O func	enera lividur oial i	Transmit Clock: If the baud rate is 0, this input clocks data out of the transmitter on the falling edge. If a baud rate of 1 or 2 is selected, this input permits the user to provide a 32× or 64× clock which is used for the receiver and transmitter. If the baud rate is 3-0F <sub>16</sub> , the internal transmitter clock is output. If 1½ stop bits are selected and characters are continuously transmitted, the internal baud rate generator will be reset at the end of the stop bits and the clock will have a small positive spike instead of a half clock. A high-to-low transition occurs at the beginning of each bit and a low-to-high transition at the center of each bit.
Hill	k. Four two 18-b imers ca	s teritis polo me or bab	eau syst casca bit o	Clear to Send: This input enables the serial transmitter. If $\overline{\text{CTS}}$ is low, any character in the transmitter buffer will be sent. A single negative-going pulse causes the transmission of a single previously loaded character out of the transmitter buffer. If this pulse occurs when the buffer is empty or during the transmission of a character up to 0.5 of the first stop bit, it will be ignored. If a baud rate from 1-0F <sub>16</sub> is selected, $\overline{\text{CTS}}$ must be low for at least 1/32 of a bit, or it will be ignored.
16 16 18 18 18 18 18 18 18 18 18 18 18 18 18	ot priority ns on ti mal inte particul s or mo d 8088/1	interrur functio ane exte i for a ntrolfer 1085 an	ormal and c and c user port i	An eight-level priority intervolon/figured for fully nested or n Seven of the eight interrupts a MUART (counter/timers, UART) rupt is provided which can be function or for chaining intervolons with direct interrupt with direct interrupt with direct interrupt v



#### **FUNCTIONAL DESCRIPTION**

The 8256 Multi-Function Universal Asynchronous Receiver-Transmitter (MUART) combines five commonly used functions onto a single 40-pin device. The MUART performs asynchronous serial communications, parallel I/O, timing, event counting, and interrupt control.

#### Serial Communications

The serial communications portion of the MUART contains a full-duplex asynchronous receiver-transmitter (UART). A programmable baud rate generator is included on the MUART to permit a variety of operating speeds without external components. The UART can be programmed by the CPU for a variety of character sizes, parity generation and detection, error detection, and start/stop bit handling. The receiver checks the start and stop bits in the center of the bit, and a break halts the reception of data. The transmitter can send breaks and can be controlled by an external enable pin.

#### Parallel I/O

The MUART includes 16 bits of general purpose parallel I/O. Eight bits (Port 1) can be individually changed from input to output or used for special I/O functions. The other eight bits (Port 2) can be used as nibbles (4 bits) or as bytes. These eight bits also include a handshaking capability using two pins on Port 1.

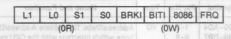
#### Counter/Timers

There are five 8-bit counter/timers on the MUART. The timers can be programmed to use either a 1kHz or 16kHz clock generated from the system clock. Four of the 8-bit counter/timers can be cascaded to two 16-bit counter/timers, and one of the 8-bit counter/timers can be reset to its initial value by an external signal.

#### Interrupts

An eight-level priority interrupt controller can be configured for fully nested or normal interrupt priority. Seven of the eight interrupts service functions on the MUART (counter/timers, UART), and one external interrupt is provided which can be used for a particular function or for chaining interrupt controllers or more MUARTs. The MUART will support 8085 and 8086/88 systems with direct interrupt vectoring, or the MUART can be polled to determine the cause of the interrupt.

#### **Command Register 1**



#### FRQ — Timer Frequency Select

This bit selects between two frequencies for the five timers. If FRQ = 0, the timer input frequency is  $16\,\text{kHz}$  (62.5  $\mu$ s). If FRQ = 1, the timer input frequency is  $1\,\text{kHz}$  (1 ms). The selected clock frequency is shared by all the counter/timers enabled for timing; thus, all timers must run with the same time base.

#### 8086 - 8086 Mode Enable

This bit selects between 8048/8085 mode and 8086/8088 mode. In 8085 mode (8086 = 0), A0 to A3 are used to address the internal registers, and an RST instruction is generated in response to the first  $\overline{\text{INTA}}$ . In 8086 mode (8086 = 1), A1 to A4 are used to address the internal registers, and A0 is used as an extra chip select (A0 must equal zero to be enabled). The response to  $\overline{\text{INTA}}$  is for 8086 interrupts where the first  $\overline{\text{INTA}}$  is ignored, and an interrupt vector (40<sub>16</sub> to 47<sub>16</sub>) is placed on the bus in response to the second  $\overline{\text{INTA}}$ .

#### BITI - Interrupt on Bit Change

This bit disables the Timer 2 interrupt and enables an interrupt when a low-to-high transition occurs on pin 7 of Port 1 (pin 32).

#### BRKI - Break-in Detect Enable

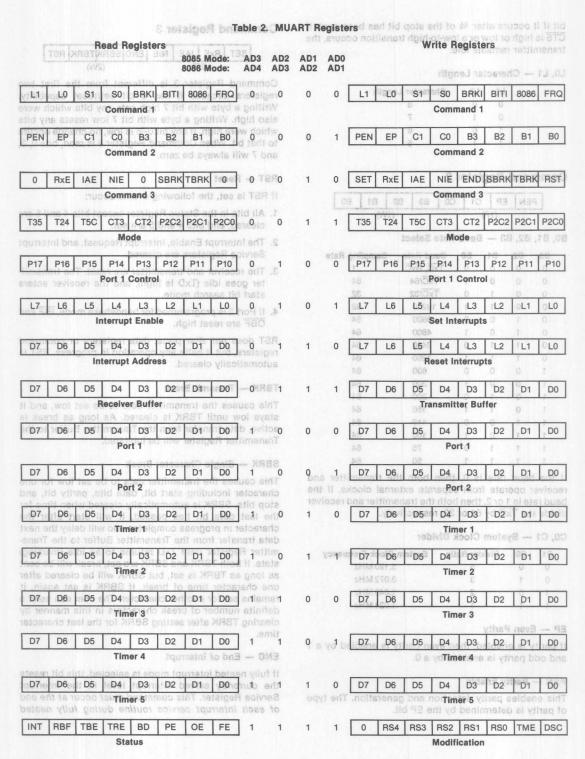
This bit enables the break-in detect feature. A break-in is detected when pin 6 of Port 1 (pin 33) is low during the first stop bit of a transmitted character. This could be used to detect a break-in condition by connecting the serial transmission line to pin 33. A break-in detect is OR-ed with break detect in bit 3 of the Status Register. If  $\overline{\text{RxC}}$  and  $\overline{\text{TxC}}$  are used for the serial bit rates, break-in cannot be detected.

#### S0, S1 - Stop Bit Length

ength

If 0.75 stop bits is selected,  $\overline{\text{CTS}}$  becomes edge sensitive rather than level sensitive. A high-to-low transition of  $\overline{\text{CTS}}$  immediately initiates the transmission of the next character. A high-to-low transition will be ignored if the transmit buffer is empty, or if it occurs before 0.75 of the first stop bit. It will shorten the stop



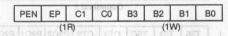


bit if it occurs after 34 of the stop bit has been sent. If Command Register 3 CTS is high or low or a low-to-high transition occurs, the transmitter remains idle.

#### L0. L1 - Character Length

L1a	LO	Character	Length	1
0	0	8	<u> </u>	
0	1	7		
 1.1	0	6	100	
1	1	5		

#### **Command Register 2**



#### B0. B1. B2. B3 - Baud Rate Select

В3	B2	B1	В0	<b>Baud Rate</b>	Sa	mpling	Rate
010	0	0	0	TxC, RxC	01.4	1	
0	0	0	Cpstn	TxC/64		64	
0	0	1	0	TxC/32		32	
0.0	0	5.1	8.1	19200		32	
0	1	0	0	9600		64	
0	1	0	1	4800		64	
0.0	1	2.1	0	2400		64	
0	1	1	1	1200	(continues or	64	
1	0	0	0	600		64	
001	0	0	.1	300		64	
1	0	1	0	200	U/1.2	64	
1	0	1	18 707	150		64	
1	-1-	0	0	110		- 64	
901	1	0	91	100		64	
1	1	1	0	75		64	
1_	1	1	1	50		64	
			mark &				

If the baud rate is 0, then both the transmitter and receiver operate from separate external clocks. If the baud rate is 1 or 2, then both the transmitter and receiver divide the TxC by 64 or 32, respectively.

#### C0, C1 - System Clock Divider

C1	CO	Divider Ratio	System Clock Frequency
0	0	5	5.120 MHz
0	1	3	3.072 MHz
1	0	2	2.048 MHz
1041	-1	20 1 20 1 50	1.024 MHz

#### EP - Even Parity

If parity is enabled, then even parity is enabled by a 1 and odd parity is enabled by a 0.

#### PEN - Parity Enable

This enables parity detection and generation. The type of parity is determined by the EP bit.

	_		_	-	1	-		
	SET	RxE	IAE	NIE	END	SBRK	TBRK	RST
3.0	1.0	(2	R)			(2)	W)	

Command Register 3 is different from the first two registers because it has a bit set/reset capability. Writing a byte with bit 7 high sets any bits which were also high. Writing a byte with bit 7 low resets any bits which were high. If any bit 0-6 is low, no change occurs to that bit. When Command Register 3 is read, bits 0, 3, and 7 will always be zero.

#### RST - Reset DIRETDIRES O JAM LAN LOVE

If RST is set, the following events occur:

- 1. All bits in the Status Register except bits 4 and 5 are cleared, and bits 4 and 5 are set.
- 2. The Interrupt Enable, Interrupt Request, and Interrupt Service Registers are cleared.
- 3. The receiver and transmitter are reset. The transmitter goes idle (TxD is high), and the receiver enters start bit search mode.
- 4. If Port 2 is programmed for handshake mode, IBF and OBF are reset high.

RST does not alter ports, data registers or command registers, but it halts any operation in progress. RST is automatically cleared.

#### TBRK — Transmit Break

This causes the transmitter data to be set low, and it stays low until TBRK is cleared. As long as break is active, data transfer from the Transmitter Buffer to the Transmitter Register will be inhibited.

#### SBRK - Single Character Break

This causes the transmitter data to be set low for one character including start bit, data bits, parity bit, and stop bits. SBRK is automatically cleared when time for the last data bit has passed. It will start after the character in progress completes and will delay the next data transfer from the Transmitter Buffer to the Transmitter Register until TxD returns to an idle (marking) state. If both TBRK and SBRK are set, break will be sent as long as TBRK is set, but SBRK will be cleared after one character time of break. If SBRK is set again, it remains set for another character. The user can send a definite number of break characters in this manner by clearing TBRK after setting SBRK for the last character

#### END — End of Interrupt

If fully nested interrupt mode is selected, this bit resets the currently served interrupt level in the Interrupt Service Register. This command must occur at the end of each interrupt service routine during fully nested



interrupt mode. END is automatically cleared when the Interrupt Service Register (internal) is cleared. See the NIE description for more information on nested interrupt servicing. END is ignored if nested interrupts are not enabled.

# NIE - Nested Interrupt Enable

This bit enables fully nested interrupts. In this mode, the service routine for a lower priority interrupt can be interrupted by a request from a higher priority task.

In fully nested interrupt mode, INTA or reading the Interrupt Address Register resets the highest priority interrupt bit in the Interrupt Register (internal), sets the corresponding bit in the Interrupt Service Register (internal), and resets INT. If an interrupt of higher priority than the currently served interrupt is requested or the END bit is set while another interrupt request is pending, the INT line will go high again. If an interrupt service routine is interrupted by an interrupt of higher priority, two or more bits in the Interrupt Service Register will be set.

If NIE is low, interrupt priority is used only when two interrupts occur at the same time. INT will be high as long as the CPU has not responded to all the interrupts in the Interrupt Register.

#### IAE - Interrupt Acknowledge Enable

This bit enables an automatic response to INTA. The particular response is determined by the 8086 bit in Command Register 1.

#### RxE — Receiver Enable

This bit enables the serial receiver. The Receiver Buffer and all receiver status information will be disabled except for the break detect status.

# SET — Bit Set/Reset

If this bit is high during a write to Command Register 3, then any bit marked by a high will be set. If this bit is low, then any bit marked by a high will be cleared.

#### **Mode Register**

T35	T24	T5C	СТЗ	CT2	P2C2	P2C1	P2C0
	(3	R)			(3)	W)	
						an L	777

#### P2C2, P2C1, P2C0 — Port 2 Control

			Writinoistan 2 sets the datain
P2C2			Mode of the Upper of policower
ed Oalu	P002p	0.80	de nibble di ste input stote input
0.0	ento o	contents	nibble of input and output
0	1	0	nibble output input
0	1	1	nibble output output
1	0	0	byte handshake input
1	0	1	byte handshake output
1	1	0	DO NOT USE
1	1	1	test

If test mode is selected and BRG of Port 1 Control Register is set, then the output from the internal baud rate generator is placed on pin 4 of Port 1 (pin 35).

# CT2. CT3 — Counter/Timer Mode

If CT2 or CT3 are high, then counter/timer 2 or 3 respectively is configured as an event counter on pin 2 or 3 respectively of Port 1 (pins 37 or 36). The event counter decrements the count by one on each low-to-high transition of the external input. If CT2 or CT3 is low, then the respective counter/timer is configured as a timer and the Port 1 pins are used for parallel I/O.

#### T5C - Timer 5 Control

If T5C is set, then Timer 5 can be preset and started by an external signal. Writing to the Timer 5 Register loads the Timer 5 Save Register and stops the timer. A high-to-low transition on pin 5 of Port 1 (pin 34) loads the timer with the saved value and starts the timer. The next high-to-low transition on pin 5 retriggers the timer by reloading it with the initial value and continues timing.

When the timer reaches zero it issues an interrupt request, disables its interrupt level and continues counting. A subsequent high-to-low transition on pin 5 resets Timer 5 to its initial value. For another timer interrupt, the Timer 5 interrupt enable bit must be set again.

#### T35, T24 — Cascade Timers Mggl sirth nedt it retained

These two bits cascade Timers 3 and 5 or 2 and 4. Timers 2 and 3 are the lower bytes, while Timers 4 and 5 are the upper bytes. If T5C is set, then both Timers 3 and 5 can be preset and started by an external pulse. When a high-to-low transition occurs, Timer 5 is preset to its saved value, but Timer 3 is always preset to all ones. If either CT2 or CT3 is set, then the corresponding timer pair is a 16-bit event counter.

#### **Port 1 Control Register**

act. I	100	ert 1	201	501	750	Lan I	501
P17	P16	P15	P14	P13	P12	P11	P10
	(4	R)			(4)	W)	

Receiver and Transmitter

Each bit in the Port 1 Control Register configures the direction of the corresponding pin. If the bit is high, the pin is an output, and if it is low the pin is an input. Every Port 1 pin has another function which is controlled by other registers. If that special function is disabled, the pin functions as a general I/O pin as specified by this register. The special functions for each pin are described below.

# Port 10, 11 - Handshake Control

If byte handshake control is enabled for Port 2 by the Mode Register, then Port 10 is programmed as STB/ACK handshake control input and Port 11 is programmed as IBF/OBF handshake control output.

If byte handshake mode is enabled for output on Port 2, OBF indicates that a character has been loaded into the



Port 2 output buffer. When an external device reads the data, it acknowledges this operation by driving ACK low.

OBF is set low by writing to Port 2 and is reset high by ACK.

If byte handshake mode is enabled for input on Port 2, STB is an input to the MUART to latch the data into Port 2. After the data is latched, IBF is driven low. IBF is reset high when Port 2 is read.

#### Port 12, 13 - Counter 2, 3 Input

If Timer 2 or Timer 3 is programmed as an event counter by the mode register, then Port 12 or 13 is the counter input for Event Counter 2 or 3, respectively.

#### Port 14 — Baud Rate Generator Output Clock

If test mode is enabled by the Mode Register and Command Register 2 baud rate select is greater than 2, then Port 14 is an output from the internal baud rate generator.

# Port 15 — Timer 5 Trigger Visitini entrally it pubsoles

If T5C is set in the Mode Register enabling a retriggerable timer, then Port 15 is the input which starts and reloads Timer 5.

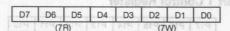
# Port 16 - Break-in Detect

If break-in detect is enabled by BRKI in Command Register 1, then this input is used to sense a break-in. If Port 16 is low while the serial transmitter is sending the last stop bit, then a break-in condition is signaled.

#### Port 17 — Port Interrupt Source

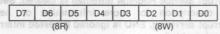
If BITI in Command Register 1 is set, then a low-to-high transition on Port 17 generates an interrupt request on priority level 1.

#### **Receiver and Transmitter Buffer**



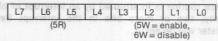
Both the transmitter and the receiver in the MUART are fully double buffered. The Receiver Buffer full flag is cleared when the character is read. If the character is not read before the next character's first stop bit, then an overrun error is generated. Bytes written to the Transmitter Buffer are held until the Transmitter Register (internal) is empty. If the Transmitter Register is empty, the byte is transferred immediately and the Transmitter Buffer empty flag is set. If a serial character length is less than 8 bits, then the unused most significant bits are set to zero on a read and are ignored on a write.

#### Port Aw bersels vilselfametus al OVE sbom touvietel



Writing to Port 1 sets the data in the Port 1 output latch. Writing to an input pin does not affect the pin, but the data is stored and will be output if the direction of the pin is changed later. If the pin is used as a control signal, the pin will not be affected, but the data is stored. Reading Port 1 transfers the data in Port 1 onto the data bus. Reading an output pin or a control pin puts the data in the output latch (not the control signal) onto the data bus.

#### Interrupt Enable Register

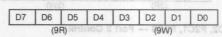


priority than the currently served interrupt is requested

Interrupts are enabled by writing to the Set Interrupts Register (5W). Interrupts are disabled by writing to the Reset Interrupts Register (6W). Each bit set by the Set Interrupts Register (5W) will enable that level interrupt, and each bit set in the Reset Interrupts Register (6W) will disable that level interrupt. The user can determine which interrupts are enabled by reading the Interrupt Enable Register (5R).

Priority	Source
Highest L0	Timer 1
L1	Timer 2 or Port Interrupt
	External Interrupt (EXTINT)
ib ad Iliw L30	Timer 3 or Timers 3 & 5
L4	Receiver Interrupt
L5	Transmitter Interrupt
L6	Timer 4 or Timers 2 & 4
	Timer 5 or 2 and 3 d and 1 limer 5 or 2 limer 5 limer 5 or 2 limer 5 limer 5 limer 5 or 2 limer 5 limer

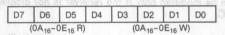
#### Port 259 1059 5059 5TO | ETO



Writing to Port 2 sets the data in the Port 2 output latch. Writing to an input pin does not affect the pin, but it does store the data in the latch. Reading Port 2 puts the input pins onto the bus or the contents of the output latch for output pins.

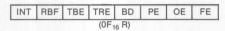


#### Timer 1-5



Reading Timer N puts the contents of the timer onto the data bus. If the counter changes while RD is low, the value on the data bus will not change. If two timers are cascaded, reading the high order byte will cause the low order byte to be latched. Reading the low order byte will unlatch them both. Writing to either timer or decascading them also clears the latch condition. Writing to a timer sets the starting value of that timer. If two timers are cascaded, writing to the high order byte presets the low order byte to all ones. Loading only the high order byte with a value of X leads to a count of X · 256 + 255. Timers count down continuously. If the interrupt is enabled, it occurs when the counter changes from 1 to 0. When the interrupt is set in the Interrupt Register, interrupts are disabled in the Interrupt Mask Register.

#### **Status Register**



#### FE — Framing Error, Transmission Mode

If transmission mode is disabled (in Modification Register), then FE indicates a framing error. A framing error is detected during the *first* stop bit. The error is reset by reading the Status Register or by a chip reset. A framing error does not inhibit the loading of the Receiver Buffer. If RXD remains low, the receiver will assemble the next character. The false stop bit is treated as the next start bit, and no high-to-low transition on RxD is required to synchronize the receiver.

If transmission mode is enabled, then this bit is used to suggest the transmitter was sending. FE will be high if the transmitter is active during the reception of the parity bit (or last data bit for no-parity). It is reset if the transmitter is not active or by a chip reset. The bit is intended to imply that the received character is from the transmitter in half-duplex systems.

#### OE - Overrun Error

If the user does not read the character in the Receiver Buffer before the next character is received and transferred to this register, then the OE bit is set. The OE flag is set during the reception of the first stop bit and is cleared when the Status Register is read or when a chip reset occurs.

#### PE — Parity Error

A parity error is set during the first stop bit and is reset by reading the Status Register or by a chip reset.

#### BD - Break Detect, Break-in Detect

If BRKI in Command Register 1 is set to enable break-in detect, then BD indicates a break-in condition. If Port 16 is low during the transmission of the last stop bit, then BD will be set near the end of the last stop bit. Break-in detect can only be detected if the internal baud rate generator is used. Break-in remains set until the Status Register is read or the chip is reset.

If BRKI is low, then BD indicates a break condition on the receiver. BD is set when the first stop bit of a break is sampled and will remain set until the Status Register is read or the chip is reset. The receiver will remain idle until the next high-to-low transition on RxD. A detected break inhibits the loading of the Receiver Buffer.

#### TRE — Transmitter Register Empty

This status bit indicates that the Transmitter Register is busy. It is set by a chip reset and when the last stop bit has left the transmitter. It is reset when a character is loaded into the Transmitter Register. If  $\overline{CTS}$  is low, the Transmitter Register will be loaded during the transmission of the start bit. If  $\overline{CTS}$  is high at the end of a character, TRE will remain high and no character will be loaded into the Transmitter Register until  $\overline{CTS}$  goes low. If the transmitter was inactive before a character is loaded into the Transmitter Buffer, the Transmitter Register will be empty temporarily while the buffer is full. However, the data in the buffer will be transferred to the transmitter register immediately and TRE will be cleared while TBE is set.

#### TBE — Transmitter Buffer Empty

TBE indicates the Transmitter Buffer is empty and is ready to accept a character. TBE is set by a chip reset or the transfer of data to the Transmitter Register and is cleared when a character is written to the transmitter buffer.

#### RBF — Receiver Buffer Full

RBF is set when the Receiver Buffer has been loaded with a new character during the sampling of the first stop bit. RBF is cleared by reading the receiver buffer or by a chip reset.

#### INT - Interrupt Pending

The INT bit reflects the state of the INT pin (pin 15) and indicates an interrupt is pending in the Interrupt Register. It is reset by INTA or by reading the Interrupt Address Register if only one interrupt is pending and by a chip reset.

FE, OE, PE, RBF, and break detect all generate a level 4 interrupt when the receiver samples the first stop bit. TRE, TBE, and break-in detect generate a level 5 interrupt. TRE generates an interrupt when TBE is set and the Transmitter Register finishes transmitting. The

break-in detect interrupt is issued at the same time as TBE or TRE.

#### **Modification Register**

0	RS4	RS3	RS2	RS1	RS0	TME	DS
---	-----	-----	-----	-----	-----	-----	----

#### DSC — Disable Start Bit Check

DSC disables the receiver's start bit check. In this state the receiver will not be reset if RxD is not low at the center of the start bit. This function is disabled by a chip reset. So A .0x8 no notification working it xxm and time.

#### TME — Transmission Mode Enable

TME enables transmission mode and disables framing error detection. A chip reset disables transmission mode and enables framing error detection.

#### RS0, RS1, RS2, RS3, RS4 - Receiver Sample Time

The number in RSn alters when the receiver samples RxD. A chip reset sets this value to 0 which is the center

loaded into the hansmitter Register until C1's goes low. If the transmitter was inactive before a character is loaded into the Transmitter Buffer, the Transmitter Register will be empty temporarily while the buffer is full. However, the data in the buffer will be transfered to the transmitter register immediately and TRE will be cleared while TBE is set.

#### 18E - Transmitter Suffer Emply

TRE indicates the Transmitter Buffer Is empty and is ready to accept a character. TBE is set by a chip reset or the transmitter Register and is the transmit when a character is written to the transmitter buffer.

#### REF - Receiver Buffer Full

RBF is set when the Receiver Buffer has been loaded with a new character during the sampling of the first stop bit. RBF is cleared by reading the receiver buffer or by a chip reset.

#### naihang inumatal .... 748

The INT bit reflects the state of the INT pin (pin 15) and indicates an interrupt is pending in the interrupt indicates. It is reset by INTA or by reading the interrupt Address Register if only one interrupt is pending and by a chirt reset.

FE, OE, PE, RBF, and break dated all generate a level 4 interrupt when the receiver samples the first stop bit. TRE, TBE, and break-in detect generate a level 5 interrupt. TRE generates an interrupt when TBE is set and the Transmitter Register (injahes transmitting. The

of the bit (sample time 字句: The receiver is not clocked by RxC.

	novit edt			Sample Time RS0 = 0 RS0 = 1			
RS4	RS3	RS2	RS1	RS0 = 0	RS0 = 1		
0	t owl the	posto to	o III an	d state and	no elvis		
0	suso <sup>1</sup> liw	styd 1ebro	0 0	tonib4er.	3		
				18 9 6 0 1 8			
				ted 8 en			
0	01110	the faton	guseto o	ala m10 li p	niba9a		
				128			
				0500140 6			
				oro v46 en			
iquos	ads to a	81 X 10 91	ulav a rij	18 18	D10170		
1	enoralitu	DO RYYGO	0	20	19		
1	1 1	0	near Trets	22 24	21		
1	matelt set	0	0	24	23		
1	0	1	1	26	25		
1	0	1	0	28	27		
1	0	0	1	30	29		
1	0	0	0	32	31		

#### FF -- Framing Error, Transmission Mode

If transmission mode is disabled (in Modification Register), then FE indicates a framing error. A framing error is detected during the II/st stop bit. The error is reset by reading the Status Register or by a chip reset. A framing error does not inhibit the loading of the Receiver Buffer. If RXD remains low, the receiver will assemble the next character. The false stop bit is treated as the next start bit, and no high-to-low transition on RXD is required to exceptionize the receiver.

If transmission mode is enabled, then this bit is used to suggest the transmitter was sending. PE will be high if the transmitter is active during the reception of the parity bit (or last data bit for no-parity). It is reset if the transmitter is not active or by a chip neset. The bit is intended to imply that the received character is from the transmitter is half-during systems.

#### No. - Overme Error

If the user does not read the character in the Receiver Buffer before the next character is received and transferred to this register, then the OE bit is sat. The OE flag is set during the reception of the first stop bit and is cleared when the Status Register is read or when a chiral set of the character.

#### PE -- Parity Error

A parity error is set during the first stop bit and is reset by reading the Status Register or by a chip reset.





# 8273, 8273-4, 8273-8 PROGRAMMABLE HDLC/SDLC PROTOCOL CONTROLLER

- **CCITT X.25 Compatible**
- **HDLC/SDLC Compatible**
- Full Duplex, Half Duplex, or Loop SDLC Operation
- Up to 64K Baud Synchronous Transfers
- Automatic FCS (CRC) Generation and Checking
- Up to 9.6K Baud with On-Board Phase Locked Loop

- Programmable NRZI Encode/Decode
- Two User Programmable Modem Control Ports
- Digital Phase Locked Loop Clock Recovery
- Minimum CPU Overhead
- Fully Compatible with 8048/8080/8085/ 8088/8086 CPUs
- Single +5V Supply

The Intel® 8273 Programmable HDLC/SDLC Protocol Controller is a dedicated device designed to support the ISO/CCITT's HDLC and IBM's SDLC communication line protocols. It is fully compatible with Intel's new high performance microcomputer systems such as the MCS-88/86<sup>TM</sup>. A frame level command set is achieved by a unique microprogrammed dual processor chip architecture. The processing capability supported by the 8273 relieves the system CPU of the low level real-time tasks normally associated with controllers.

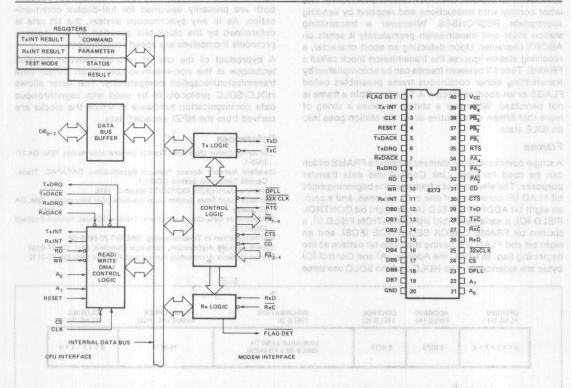


Figure 1. Block Diagram

Figure 2. Pin Configuration



#### A BRIEF DESCRIPTION OF HDLC/SDLC **PROTOCOLS**

#### General

The High Level Data Link Control (HDLC) is a standard communication link protocol established by International Standards Organization (ISO). HDLC is the discipline used to implement ISO X.25 packet switching systems.

The Synchronous Data Link Control (SDLC) is an IBM communication link protocol used to implement the System Network Architecture (SNA). Both the protocols are bit oriented, code independent, and ideal for full duplex communication. Some common applications include terminal to terminal, terminal to CPU, CPU to CPU, satellite communication, packet switching and other high speed data links. In systems which require expensive cabling and interconnect hardware, any of the two protocols could be used to simplify interfacing (by going serial), thereby reducing interconnect hardware costs. Since both the protocols are speed independent, reducing interconnect hardware could become an important application. troller is a dedicated device designed to suppor

#### Network

its it is fully compatible with intel's new high p In both the HDLC and SDLC line protocols, according to a pre-assigned hierarchy, a PRIMARY (Control) STATION controls the overall network (data link) and issues commands to the SECONDARY (Slave) STATIONS. The latter comply with instructions and respond by sending appropriate RESPONSES. Whenever a transmitting station must end transmission prematurely it sends an ABORT character. Upon detecting an abort character, a receiving station ignores the transmission block called a FRAME. Time fill between frames can be accomplished by transmitting either continuous frame preambles called FLAGS or an abort character. A time fill within a frame is not permitted. Whenever a station receives a string of more that fifteen consecutive ones, the station goes into an IDLE state.

A single communication element is called a FRAME which can be used for both Link Control and data transfer purposes. The elements of a frame are the beginning eight bit FLAG (F) consisting of one zero, six ones, and a zero, an eight bit ADDRESS FIELD (A), an eight bit CONTROL FIELD (C), a variable (N-bit) INFORMATION FIELD (I), a sixteen bit FRAME CHECK SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit pattern as the beginning flag. In HDLC the Address (A) and Control (C) bytes are extendable. The HDLC and the SDLC use three

types of frames; an Information Frame is used to transfer data, a Supervisory Frame is used for control purposes, and a Non-sequenced Frame is used for initialization and control of the secondary stations.

#### Frame Characteristics

An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adopt any format or code suitable for his system - it may even be a computer word length or a "memory dump". The frame is bit oriented that is, bits, not characters in each field, have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The Command and Response information frames contain sequence numbers in the control fields identifying the sent and received frames. The sequence numbers are used in Error Recovery Procedures (ERP) and as implicit acknowledgement of frame communication, enhancing the true fullduplex nature of the HDLC/SDLC protocols.

In contrast, BISYNC is basically half-duplex (two way alternate) because of necessity to transmit immediate acknowledgement frames. HDLC/SDLC therefore saves propagation delay times and have a potential of twice the throughput rate of BISYNC.

It is possible to use HDLC or SDLC over half duplex lines but there is a corresponding loss in throughput because both are primarily designed for full-duplex communication. As in any synchronous system, the bit rate is determined by the clock bits supplied by the modem, protocols themselves are speed independent.

A byproduct of the use of zero-bit insertion-deletion technique is the non-return-to-zero invert (NRZI) data transmission/reception compatibility. The latter allows HDLC/SDLC protocols to be used with asynchronous data communication hardware in which the clocks are derived from the NRZI encoded data.

#### References

IBM Synchronous Data Link Control General Information, IBM, GA27-3093-1.

Standard Network Access Protocol Specification, DATAPAC, Trans-Canada Telephone System CCG111

Recommendation X.25, ISO/CCITT March 2, 1976.

IBM 3650 Retail Store System Loop Interface OEM Information, IBM, GA 27-3098-0

Guidebook to Data Communications, Training Manual, Hewlett-Packard

IBM Introduction to Teleprocessing, IBM, GC 20-8095-02

System Network Architecture, Technical Overview, IBM, GA 27-3102 System Network Architecture Format and Protocol, IBM GA 27-3112

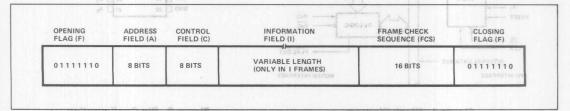


Figure 3. Frame Format



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The 2273 recognizes and can generate flags (Onicipella I., Pin Description) again statement and one extinguous E138 and

Symbol	Pin No.	Туре	Name and Function				
Vcc	40	t	Power Supply: +5V Supply.				
GND	20	7	Ground: Ground.				
RESET Huse ATM namit Date ceive Data	mT	0 1	Reset: A high signal on this pin w force the 8273 to an idle state. The 8273 will remain idle until a comman is issued by the CPU. The mode interface output signals are force high. Reset must be true for minimum of 10 TCY.				
CS and oraqu	24	ghit	Chip Select: The RD and WR inp are enabled by the chip select inp				
DB <sub>7</sub> -DB <sub>0</sub>	19- 12	1/0	Data Bus: The Data Bus lines are directional three-state lines which terface with the system Data Bus				
WR	10	l Legid	Write Input: The Write signal is used to control the transfer of either a command or data from CPU to the 8273.				
RD	9	ı	Read Input: The Read signal is used to control the transfer of either a data byte or a status word from the 8273 to the CPU.				
TxINT	2	0	<b>Transmitter Interrupt:</b> The Transmitter interrupt signal indicates that the transmitter logic requires service				
RxINT doog) not		O ovio	Receiver Interrupt: The Receiver interrupt signal indicates that the Receiver logic requires service.				
DRQXT	6	0	Transmitter Data Request: Requests a transfer of data between memory and the 8273 for a transmit operation.				
RxRDQ	8	0	Receiver DMA Request: Requests a transfer of data between the 8273 and memory for a receive operation.				
TxDACK tab triabno			Transmitter DMA Acknowledge The Transmitter DMA acknowledge signal notifies the 8273 that the TxDMA cycle has been granted				
RxDACK		toehib	Receiver DMA Acknowledge: The Receiver DMA acknowledge signal				
configure faces are:		AMO	notifies the 8273 that the RxDMA cycle has been granted.				
A <sub>1</sub> -A <sub>0</sub>	22- 21	1	Address: These two lines are CPU Interface Register Select lines.				
TxD	29	O	Transmitter Data: This line transmits the serial data to the communication channel.				
TxC	28	13 tha	Transmitter Clock: The transmitter clock is used to synchronize the				
RxD	26	etojii	transmit data.  Receiver Data: This line receives serial data from the communication channel.				
RxC nem bas 8	27	ert) rre	Receiver Clock: The Receiver Clock is used to synchronize the receive data.				

Symbol	Pin No.	Туре	Name and Function
32X CLK 1 and griding a nothing related st passing latig nothers good	ogra confl or da ne di	by pi sch a sed f ran t by	32X Clock: The 32X clock is used to provide clock recovery when an asynchronous modem is used. In loop configuration the loop station can run without an accurate 1X clock by using the 32X CLK in conjunction with the DPLL output. (This pin must be grounded when not used.)
nterface is OMA data It further	the l	ever	Digital Phase Locked Loop: Digital Phase Locked Loop output can be tied to RxC and/or TxC when 1X clock is not available. DPLL is used with 32X CLK.
FLAG DET	shii moc	2000	Flag Detect: Flag Detect signals that a flag (01111110) has been received by an active receiver.
RTS 8798	Section 1	O <sub>1</sub>	Request to Send: Request to Send signals that the 8273 is ready to transmit data.
eddreseed addreseed dependent	sters	ger n	Clear to Send: Clear to Send signals that the modem is ready to accept data from the 8273.
L A1, A1De he address D and WR I/OW. The	31	imans	Carrier Detect: Carrier Detect sig- nals that the line transmission has started and the 8273 may begin to sample data on RxD line.
PA <sub>2-4</sub>	32-	sebjic	General purpose input ports: The logic levels on these lines can be Read by the CPU through the Data Bus Buffer.
PB <sub>1-4</sub>	36- 39	0	General purpose output ports: The CPU can write these output lines through Data Bus Buffer.
CLK	3	1	Clock: A square wave TTL clock.

# FUNCTIONAL DESCRIPTION General

The Intel® 8273 HDLC/SDLC controller is a microcomputer peripheral device which supports the International Standards Organization (ISO) High Level Data Link Control (HDLC), and IBM Synchronous Data Link Control (SDLC) communications protocols. This controller minimizes CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. The 8273 can be used in either synchronous or asynchronous applications.

In asynchronous applications the data can be programmed to be encoded/decoded in NRZI code. The clock is derived from the NRZI data using a digital phase locked loop. The data transparency is achieved by using a zerobit insertion/deletion technique. The frames are automatically checked for errors during reception by verifying the Frame Check Sequence (FCS); the FCS is automatically generated and appended before the final flag in transmit.

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The 8273 recognizes and can generate flags (01111110); 4 Abort, Idle, and GA (EOP) characters.

The 8273 can assume either a primary (control) or a secondary (slave) role. It can therefore be readily implemented in an SDLC loop configuration as typified by the IBM 3650 Retail Store System by programming the 8273 into a one-bit delay mode. In such a configuration, a two wire pair can be effectively used for data transfer between controllers and loop stations. The digital phase locked loop output pin can be used by the loop station without the presence of an accurate Tx clock.

**CPU** Interface

The CPU interface is optimized for the MCS-80/85™ bus with an 8257 DMA controller. However, the interface is flexible, and allows either DMA or non-DMA data transfers, interrupt or non-interrupt driven. It further allows maximum line utilization by providing early interrupt mechanism for buffered (only the information field can be transferred to memory) Tx command overlapping. It also provides separate Rx and Tx interrupt output channels for efficient operation. The 8273 keeps the interrupt request active until all the associated interrupt results have been read.

The CPU utilizes the CPU interface to specify commands and transfer data. It consists of seven registers addressed via  $\overline{\text{CS}}$ ,  $A_1$ ,  $A_0$ ,  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  signals and two independent data registers for receive data and transmit data.  $A_1$ ,  $A_0$  are generally derived from two low order bits of the address bus. If an 8080 based CPU is utilized, the  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  signals may be driven by the 8228  $\overline{\text{I/OR}}$  and  $\overline{\text{I/OW}}$ . The table shows the seven register select decoding:

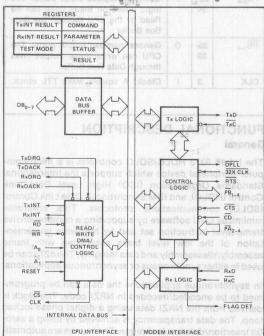


Figure 4. 8273 Block Diagram Showing CPU Interface Functions

A <sub>1</sub>	A <sub>0</sub>	TXDACK	RXDACK	CS	RD	WR	Register
0	0	1	1	0	1	0	Command
0	0	1	1	0	0	1	Status
0	1	official to	an ediela	0	1	0	Parameter
0	1	tooul va	- ruthout	0	0	1	Result
1	0	1	1	0	1	0	Reset
1	0	1	व्यवस्थित स	0	0	1	TxINT Result
11.1	1	er nd lone	a sala a	. 0	1	0	
1	1.	etbi m	. 1	0	0	1	RxINT Result
X	X	0	1	1	1	0	Transmit Data
X	X	a mgo ali	0	1	0	1	Receive Data

#### Register Description

#### Command

Operations are initiated by writing an appropriate command in the Command Register.

#### Parameter and state-search templacetts

Parameters of commands that require additional information are written to this register.

#### Result U90 most stab to brismmed

Contains an immediate result describing an outcome of an executed command.

#### Transmit Interrupt Result

Contains the outcome of 8273 transmit operation (good/bad completion).

#### Receive Interrupt Result

Contains the outcome of 8273 receive operation (good/bad completion), followed by additional results which detail the reason for interrupt.

# Status 101 EXCE of the gromen

The status register reflects the state of the 8273 CPU Interface.

#### **DMA Data Transfers**

The 8273 CPU interface supports two independent data interfaces: receive data and transmit data. At high data transmission speeds the data transfer rate of the 8273 is great enough to justify the use of direct memory access (DMA) for the data transfers. When the 8273 is configured in DMA mode, the elements of the DMA interfaces are:

#### TxDRQ: Transmit DMA Request

Requests a transfer of data between memory and the 8273 for a transmit operation.

#### TxDACK: Transmit DMA Acknowledge

The  $\overline{\text{Tx}}\text{DACK}$  signal notifies the 8273 that a transmit DMA cycle has been granted. It is also used with  $\overline{\text{WR}}$  to transfer data to the 8273 in non-DMA mode. Note:  $\overline{\text{RD}}$  must not be asserted while TxDACK is active.

#### **RxDRQ: Receive DMA Request**

Requests a transfer of data between the 8273 and memory for a receive operation.





#### RxDACK: Receive DMA Acknowledge

The RxDACK signal notifies the 8273 that a receive DMA cycle has been granted. It is also used with RD to read data from the 8273 in non-DMA mode. Note: WR must not be asserted while RxDACK is active.

# RD, WR: Read, Write nio fametxe ent vd gnimit elomas

The RD and WR signals are used to specify the direction of the data transfer.

DMA transfers require the use of a DMA controller such as the Intel 8257. The function of the DMA controller is to provide sequential addresses and timing for the transfer, at a starting address determined by the CPU. Counting of data block lengths is performed by the 8273.

To request a DMA transfer the 8273 raises the appropriate DMA REQUEST. DMA ACKNOWLEDGE and READ enables DMA data onto the bus (independently of CHIP SELECT). DMA ACKNOWLEDGE and WRITE transfers DMA data to the 8273 (independent of CHIP SELECT).

It is also possible to configure the 8273 in the non-DMA data transfer mode. In this mode the CPU module must pass data to the 8273 in response to non-DMA data requests indicated by the status word.

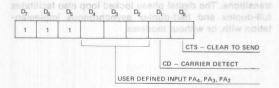
#### Modem Interface

The 8273 Modem interface provides both dedicated and user defined modem control functions. All the control signals are active low so that EIA RS-232C inverting drivers (MC 1488) and inverting receivers (MC 1489) may be used to interface to standard modems. For asynchronous operation, this interface supports programmable NRZI data encode/decode, a digital phase locked loop for efficient clock extraction from NRZI data, and modem control ports with automatic CTS, CD monitoring and RTS generation. This interface also allows the 8273 to operate in PRE-FRAME SYNC mode in which the 8273 prefixes 16 transitions to a frame to synchronize idle lines before transmission of the first flag.

It should be noted that all the 8273 port operations deal—with logical values, for instance, bit D0 of Port A will be a one when CTS (Pin 30) is a physical zero (logical one).

#### Port A - Input Port

During operation, the 8273 interrogates input pins  $\overline{\text{CTS}}$  (Clear to Send) and  $\overline{\text{CD}}$  (Carrier Detect).  $\overline{\text{CTS}}$  is used to condition the start of a transmission. If during transmission  $\overline{\text{CTS}}$  is lost the 8273 generates an interrupt. During reception, if  $\overline{\text{CD}}$  is lost, the 8273 generates an interrupt.



The user defined input bits correspond to the 8273  $PA_4$ ,  $PA_3$  and  $PA_2$  pins. The 8273 does not interrogate or manipulate these bits.

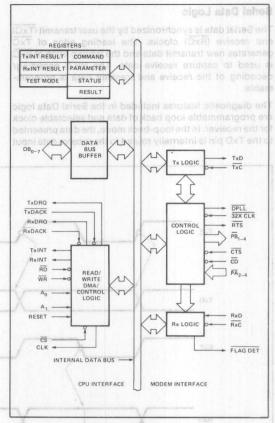
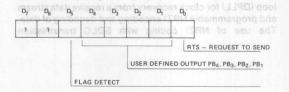


Figure 5. 8273 Block Diagram Showing Control Logic Functions

#### Port B - Output Port

During normal operation, if the CPU sets  $\overline{\text{RTS}}$  active, the 8273 will not change this pin; however, if the CPU sets  $\overline{\text{RTS}}$  inactive, the 8273 will activate it before each transmission and deactivate it one byte time after transmission. While the receiver is active the flag detect pin is pulsed each time a flag sequence is detected in the receive data stream. Following an 8273 reset, all pins of Port B are set to a high, inactive level.



The user defined output bits correspond to the state of PB<sub>4</sub>-PB<sub>1</sub> pins. The 8273 does not interrogate or manipulate these bits.





#### Serial Data Logic

The Serial data is synchronized by the user transmit  $(\overline{TxC})$  and receive  $(\overline{RxC})$  clocks. The leading edge of  $\overline{TxC}$  generates new transmit data and the trailing edge of  $\overline{RxC}$  is used to capture receive data. The NRZI encoding/decoding of the receive and transmit data is programmable.

The diagnostic features included in the Serial Data logic are programmable loop back of data and selectable clock for the receiver. In the loop-back mode, the data presented to the TxD pin is internally routed to the receive data input

circuitry in place of the RxD pin, thus allowing a CPU to send a message to itself to verify operation of the 8273.

In the selectable clock diagnostic feature, when the data is looped back, the receiver may be presented incorrect sample timing by the external circuitry. The user may select to substitute the TxC pin for the RxC input on-chip so that the clock used to generate the loop back data is used to sample it. Since TxD is generated off the leading edge of TxC and RxD is sampled on the trailing edge, the selected clock allows bit synchronism.

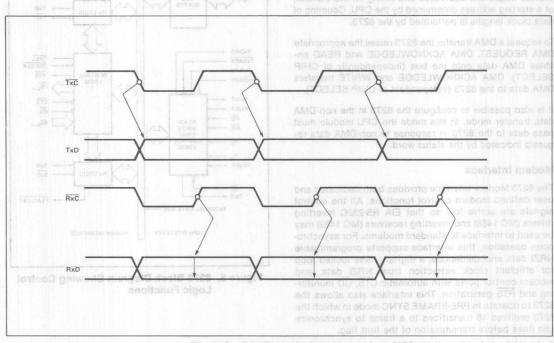


Figure 6. Transmit/Receive Timing on EXSS and its 1840 below ad bloods if

# Asynchronous Mode Interface

Although the 8273 is fully compatible with the HDLC/SDLC communication line protocols, which are primarily designed for synchronous communication, the 8273 can also be used in asynchronous applications by using this interface. The interface employs a digital phase locked loop (DPLL) for clock recovery from a receive data stream and programmable NRZI encoding and decoding of data. The use of NRZI coding with SDLC transmission

guarantees that within a frame, data transitions will occur at least every five bit times — the longest sequence of ones which may be transmitted without zero-bit insertion. The DPLL should be used only when NRZI coding is used since the NRZI coding will transmit zero sequence as line transitions. The digital phase locked loop also facilitates full-duplex and half-duplex asynchronous implementation with, or without modems.



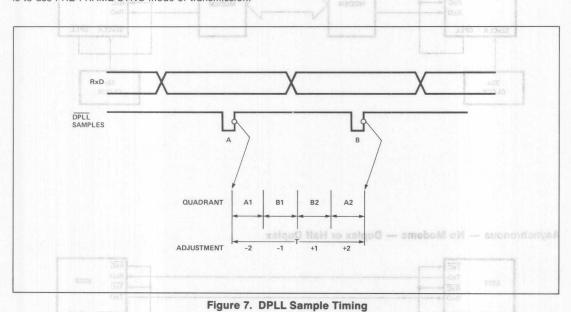


Asynchronous Modems - Duplex or Half Duplex O

#### **Digital Phase Locked Loop**

In asynchronous applications, the clock is derived from the receiver data stream by the use of the digital phase locked loop (DPLL). The DPLL requires a clock input at 32 times the required baud rate. The receive data (RxD) is sampled with this 32X CLK and the 8273 DPLL supplies a sample pulse nominally centered on the RxD bit cells. The DPLL has a built-in "stiffness" which reduces sensitivity to line noise and bit distortion. This is accomplished by making phase error adjustments in discrete increments. Since the nominal pulse is made to occur at 32 counts of the 32X CLK, these counts are subtracted or added to the nominal, depending upon which quadrant of the four error quadrants the data edge occurs in. For example if an RxD edge is detected in quadrant A1, it is apparent that the DPLL sample "A" was placed too close to the trailing edge of the data cell; sample "B" will then be placed at T = (Tnominal - 2 counts) = 30 counts of the 32X CLK to move the sample pulse "B" toward the nominal center of the next bit cell. A data edge occuring in quadrant B1 would cause a smaller adjustment of phase with T = 31 counts of the 32X CLK. Using this technique the DPLL pulse will converge to nominal bit center within 12 data bit times, worst case, with constant incoming RxD edges.

A method of attaining bit synchronism following a line idle is to use PRE-FRAME SYNC mode of transmission.



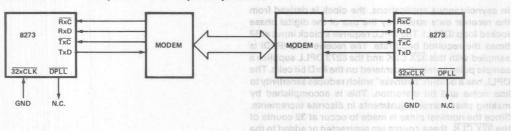




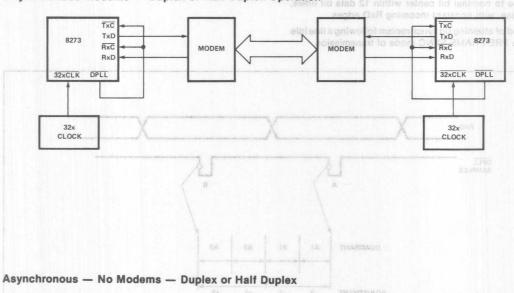
edge is detected in quadrant A1, it is apparent that the

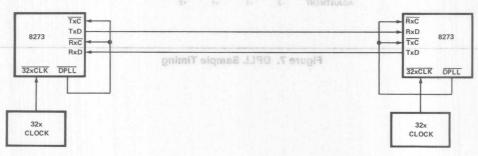
bit celt. A data edge occurring in quadrant B1 would cause

## Synchronous Modem — Duplex or Half Duplex Operation



# Asynchronous Modems — Duplex or Half Duplex Operation us 1190 ent supindosi sidt grisu XIO XSE









#### SDLC Loop

The DPLL simplifies the SDLC loop station implementation. In this application, each secondary station on a loop data link is a repeater set in one-bit delay mode. The signals sent out on the loop by the loop controller (primary station) are relayed from station to station then, back to the controller. Any secondary station finding its address in the A field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

Loop stations are required to derive bit timing from the incoming NRZI data stream. The DPLL generates sample Rx clock timing for reception and uses the same clock to implement Tx clock timing.

The 8273 is an intelligent peripheral controller which relieves the CPU of many of the role tasks associated with relieves the CPU of many of the role tasks associated with constructing and receiving frames. It is fully compatible at a cospts commands from a CPU, executes these commands and provides an interrupt and Result back to be CPU at the end of the execution. The communication with the CPU is done by activation of CS, RD, WR pins, while the An Ao select the appropriate registers on the thip as described in the Hardware Description Section.

The 8273 operation is composed of the following

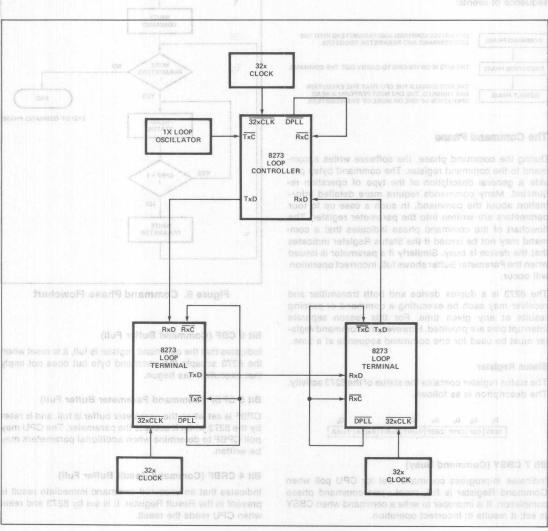


Figure 8. SDLC Loop Application

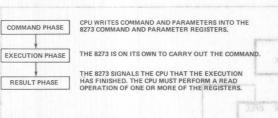




#### PRINCIPLES OF OPERATION

The 8273 is an intelligent peripheral controller which relieves the CPU of many of the rote tasks associated with constructing and receiving frames. It is fully compatible with the MCS-80/85™ system bus. As a peripheral device, it accepts commands from a CPU, executes these commands and provides an Interrupt and Result back to the CPU at the end of the execution. The communication with the CPU is done by activation of CS, RD, WR pins, while the A₁, A₀ select the appropriate registers on the chip as described in the Hardware Description Section.

The 8273 operation is composed of the following sequence of events:



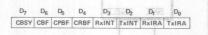
#### The Command Phase

During the command phase, the software writes a command to the command register. The command bytes provide a general description of the type of operation requested. Many commands require more detailed information about the command. In such a case up to four parameters are written into the parameter register. The flowchart of the command phase indicates that a command may not be issued if the Status Register indicates that the device is busy. Similarly if a parameter is issued when the Parameter Buffer shows full, incorrect operation will occur.

The 8273 is a duplex device and both transmitter and receiver may each be executing a command or passing results at any given time. For this reason separate interrupt pins are provided. However, the command register must be used for one command sequence at a time.

#### Status Register

The status register contains the status of the 8273 activity. The description is as follows.



#### Bit 7 CBSY (Command Busy)

Indicates in-progress command, set for CPU poll when Command Register is full, reset upon command phase completion. It is improper to write a command when CBSY is set; it results in incorrect operation.

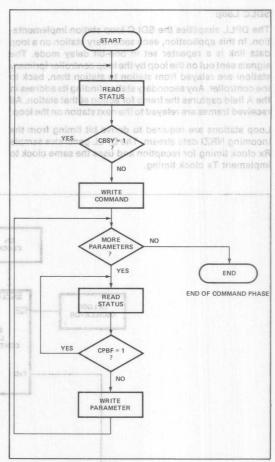


Figure 9. Command Phase Flowchart

#### Bit 6 CBF (Command Buffer Full)

Indicates that the command register is full, it is reset when the 8273 accepts the command byte but does not imply that execution has begun.

#### Bit 5 CPBF (Command Parameter Buffer Full)

CPBF is set when the parameter buffer is full, and is reset by the 8273 when it accepts the parameter. The CPU may poll CPBF to determine when additional parameters may be written.

#### Bit 4 CRBF (Command Result Buffer Full)

Indicates that an executed command immediate result is present in the Result Register. It is set by 8273 and reset when CPU reads the result.

Figure 8. SDLC Loop Application

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#### Bit 3 RxINT (Receiver Interrupt) and and not not hope of

RXINT indicates that the receiver requires CPU attention. It is identical to RXINT (pin 11) and is set by the 8273 either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has received a data byte from the 8273 in a Non-DMA data transfer.

#### Bit 2 TxINT (Transmitter Interrupt)

The TxINT indicates that the transmitter requires CPU attention. It is identical to TxINT (pin 2). It is set by 8273 either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has transferred transmit data byte to the 8273 in a Non-DMA transfer.

#### Bit 1 RxIRA (Receiver Interrupt Result Available)

The RxIRA is set by the 8273 when an interrupt result byte is placed in the RxINT register. It is reset after the CPU has read the RxINT register.

#### Bit 0 TxIRA (Transmitter Interrupt Result Available)

The TxIRA is set by the 8273 when an interrupt result byte is placed in the TxINT register. It is reset when the CPU has read the TxINT register.

# Immediate result is provided by seed Port B which have such as Read Port A and Read Port B which have

Upon accepting the last parameter, the 8273 enters into the Execution Phase. The execution phase may consist of a DMA or other activity, and may or may not require CPU intervention. The CPU intervention is eliminated in this phase if the system utilizes DMA for the data transfers, otherwise, for non-DMA data transfers, the CPU is interrupted by the 8273 via TxINT and RxINT pins, for each data byte request.

#### The Result Phase

During the result phase, the 8273 notifies the CPU of the execution outcome of a command. This phase is initiated by:

TxI/R or 8x Interrupt Result Register RxI/R. The result

- 1. The successful completion of an operation
- 2. An error detected during an operation.

To facilitate quick network software decisions, two types of execution results are provided:

- 1. An Immediate Result
- 2. A Non-Immediate Result

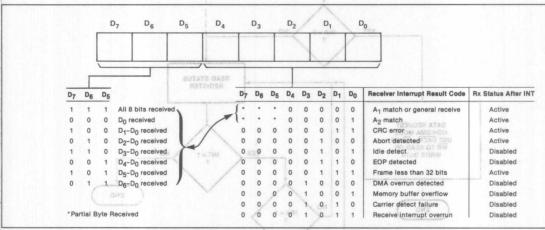


Figure 10. Rx Interrupt Result Byte Format

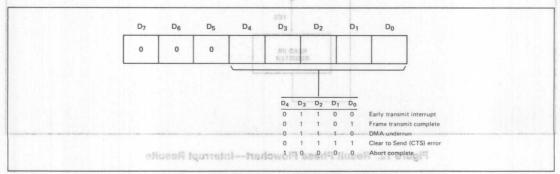


Figure 11. Tx Interrupt Result Byte Format



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Immediate result is provided by the 8273 for commands such as Read Port A and Read Port B which have information (CTS, CD, RTS, etc.) that the network software needs to make quick operational decisions.

A command which cannot provide an immediate result will generate an interrupt to signal the beginning of the Result phase. The immediate results are provided in the Result Register; all non-immediate results are available upon device interrupt, through Tx Interrupt Result Register TxI/R or Rx Interrupt Result Register RxI/R. The result may consist of a one-byte interrupt code indicating the

condition for the interrupt and, if required, one or more bytes which detail the condition.

#### Tx and Rx Interrupt Result Registers

The Result Registers have a result code, the three high order bits  $D_7 - D_5$  of which are set to zero for all but the receive command. This command result contains a count that indicates the number of bits received in the last byte. If a partial byte is received, the high order bits of the last data byte are indeterminate.

All results indicated in the command summary must be read during the result phase along about 40 control of the command summary must be

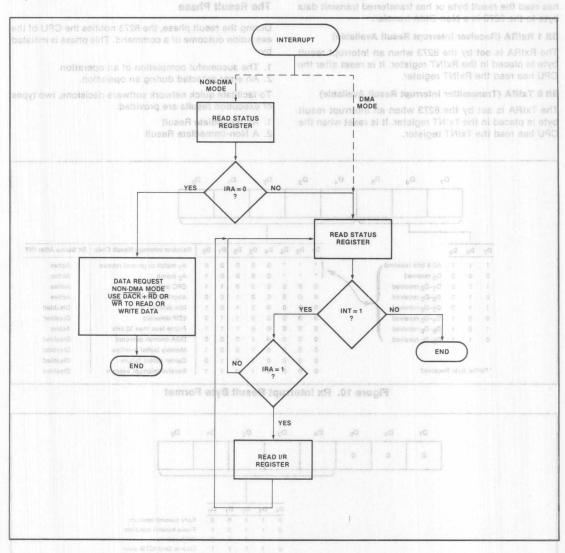
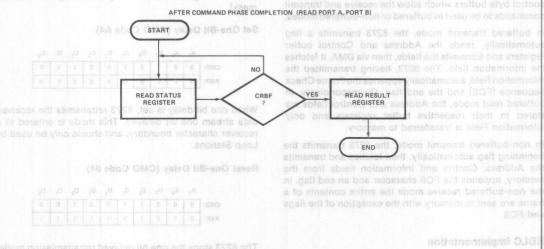


Figure 12. Result Phase Flowchart—Interrupt Results

These commands are used to manipulate data within t eter which is a mask that corresponds to the bits to be set. perform a logical-AND of the specified register with the

IMMEDIATE RESULTS



(Td ese CaMC) ebelle refigure 13. (Rx Interrupt Service) ni crex s, eno a of belief

transparently passed by the 8273 to user as either

characters unique to HOLC such as Abort, which is a

		$\mathfrak{D}_{\mathcal{S}}$	$\mathbf{D}_{\mathbf{g}}$	o.A.	, N	
						:OND
					0	

				0,4	





#### General

The 8273 HDLC/SDLC controller supports a comprehensive set of high level commands which allows the 8273 to be readily used in full-duplex, half-duplex, synchronous, asynchronous and SDLC loop configuration, with or without modems. These frame-level commands minimize CPU and software overhead. The 8273 has address and control byte buffers which allow the receive and transmit commands to be used in buffered or non-buffered modes.

In buffered transmit mode, the 8273 transmits a flag automatically, reads the Address and Control buffer registers and transmits the fields, then via DMA, it fetches the information field. The 8273, having transmitted the information field, automatically appends the Frame Check Sequence (FCS) and the end flag. Correspondingly, in buffered read mode, the Address and Control fields are stored in their respective buffer registers and only Information Field is transferred to memory.

In non-buffered transmit mode, the 8273 transmits the beginning flag automatically, then fetches and transmits the Address, Control and Information fields from the memory, appends the FCS character and an end flag. In the non-buffered receive mode the entire contents of a frame are sent to memory with the exception of the flags and FCS.

#### **HDLC** Implementation

HDLC Address and Control field are extendable. The extension is selected by setting the low order bit of the field to be extended to a one, a zero in the low order bit indicates the last byte of the respective field.

Since Address/Control field extension is normally done with software to maximize extension flexibility, the 8273 does not create or operate upon contents of the extended HDLC Address/Control fields. Extended fields are transparently passed by the 8273 to user as either interrupt results or data transfer requests. Software must assemble the fields for transmission and interrogate them upon reception.

However, the user can take advantage of the powerful 8273 commands to minimize CPU/Software overhead and simplify buffer management in handling extended fields. For instance buffered mode can be used to separate the first two bytes, then interrogate the others from buffer. Buffered mode is perfect for a two byte address field.

The 8273 when programmed, recognizes protocol characters unique to HDLC such as Abort, which is a string of seven or more ones (011111111). Since Abort character is the same as the GA (EOP) character used in SDLC Loop applications, Loop Transmit and Receive commands are not recommended to be used in HDLC. HDLC does not support Loop mode.

#### **Initialization Set/Reset Commands**

These commands are used to manipulate data within the 8273 registers. The Set commands have a single parameter which is a mask that corresponds to the bits to be set. (They perform a logical-OR of the specified register with the mask provided as a parameter). The Register commands have a single parameter which is a mask that has a zero in the bit positions that are to be reset. (They perform a logical-AND of the specified register with the mask).

#### Set One-Bit Delay (CMD Code A4)

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	$D_6$	D <sub>5</sub>	$D_4$	$D_3$	D <sub>2</sub>	D <sub>1</sub>	Do
CMD:										
PAR:	0	1	1	0	0	0	0	0	0	0

When one bit delay is set, 8273 retransmits the received data stream one bit delayed. This mode is entered at a receiver character boundary, and should only be used by Loop Stations.

#### Reset One-Bit Delay (CMD Code 64)

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	$D_6$	05	$D_4$	$D_3$	$D_2$	D	$D_0$
CMD:										
PAR:	0	1	0	1	1	1	1	1	1	1

The 8273 stops the one bit delayed retransmission mode.

#### Set Data Transfer Mode (CMD Code 97)

		Ao								
CMD:	0	0	1	0	0	1	0	1	1	1
PAR:	0	1	0	0	0	0	0	0	0	1

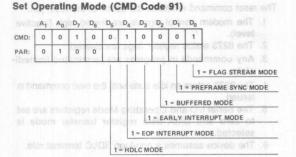
When the data transfer mode is set, the 8273 will interrupt when data bytes are required for transmission or are available from a receive. If a transmit interrupt occurs and the status indicates that there is no Transmit Result (TxIRA = 0), the interrupt is a transmit data request. If a receive interrupt occurs and the status indicates that there is no receive result (RxIRA = 0), the interrupt is a receive data request.

#### Reset Data Transfer Mode (CMD Code 57)

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	$D_5$	$D_4$	$D_3$	$D_2$	D <sub>1</sub>	Do
CMD:	0	0	0	1	0	1	0	1	1	1
PAR:	0	1	1	1	1	1	1	1	1	0

If the Data Transfer Mode is reset, the 8273 data transfers are performed through the DMA requests without interrupting the CPU.





#### Reset Operating Mode (CMD Code 51)

	A <sub>1</sub>	Ao	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D2	D <sub>1</sub>	Do
CMD:	0	0	0	1	0	1	0	0	0	61/1
PAR:	0	1	1	1		cincen.	UNIV.	-		

Any mode switches set in CMD code 91 can be reset using this command by placing zeros in the appropriate positions.

#### (D5) HDLC Mode

In HDLC mode, a bit sequence of seven ones (01111111) is interpreted as an abort character. Otherwise, eight ones (011111111) signal an abort.

#### (D4) EOP Interrupt Mode

In EOP interrupt mode, an interrupt is generated whenever an EOP character (01111111) is detected by an active receiver. This mode is useful for the implementation of an SDLC loop controller in detecting the end of a message stream after a loop poll.

#### (D3) Transmitter Early Interrupt Mode (Tx)

The early interrupt mode is specified to indicate when the 8273 should generate an end of frame interrupt. When set, an early interrupt is generated when the last data character has been passed to the 8273. If the user software responds with another transmit command before the final flag is sent, the final flag interrupt will not be generated and a new frame will immediately begin when the current frame is complete. This permits frames to be separated by a single flag. If no additional Tx commands are provided, a final interrupt will follow.

Note: In buffered mode, if a supervisory frame (no Information) Transmit command is sent in response to an early Transmit Interrupt, the 8273 will repeatedly transmit the same supervisory frame with one flag in between, until a non-supervisory transmit is issued.

Early transmitter interrupt can be used in buffered mode by waiting for a transmit complete interrupt instead of early Transmit Interrupt before issuing a transmit frame command for a supervisory frame. See Figure 14.

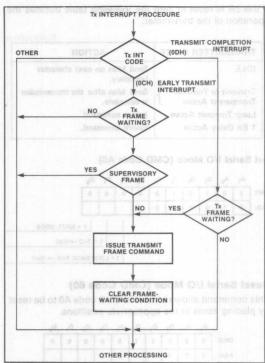


Figure 14.

If this bit is zero, the interrupt will be generated only after the final flag has been transmitted.

#### (D2) Buffered Mode

If the buffered mode bit is set to a one, the first two bytes (normally the address (A) and control (C) fields) of a frame are buffered by the 8273. If this bit is a zero the address and control fields are passed to and from memory.

#### (D1) Preframe Sync Mode

If this bit is set to a one the 8273 will transmit two characters before the first flag of a frame.

To guarantee sixteen line transitions, the 8273 sends two bytes of data  $(00)_{\rm H}$  if NRZI is set or data  $(55)_{\rm H}$  if NRZI is not set.

#### (D0) Flag Stream Mode 2-YSAD men book MSI of neteR

If this bit is set to a one, the following table outlines the operation of the transmitter.

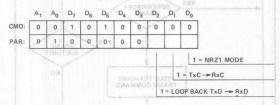
TRANSMITTER STATE	ACTION
Idle o o o o	Send Flags immediately.
Transmit or Transmit-	Send Flags after the
Transparent Active	transmission complete
Loop Transmit Active	Ignore command.
1 Bit Delay Active	Ignore command.



If this bit is reset to zero the following table outlines the operation of the transmitter.

TRANSMITTER STATE	THE ACTION HEHT
IDLE	Send Idles on next character boundary.
Transmit or Transmit-Transparent Active	Send Idles after the transmission is complete.
Loop Transmit Active	Ignore command.
1 Bit Delay Active	Ignore command.

#### Set Serial I/O Mode (CMD Code A0)



#### Reset Serial I/O Mode (CMD Code 60)

This command allows bits set in CMD code A0 to be reset by placing zeros in the appropriate positions.

	Α1	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
CMD:	0	0	0	1	1	0	0	0	0	0
PAR:	0	1	18	413	10108	9.18	110			

#### (D2) Loop Back

If this bit is set to a one, the transmit data is internally routed to the receive data circuitry.

(D2) Buffered Mode

Figure 14,

#### (D1) TxC → RxC

If this bit is set to a one, the transmit clock is internally routed to the receive clock circuitry. It is normally used with the loop back bit (D2). and bessed our abject fortings

#### (D0) NRZI Mode

If this bit is set to a one, NRZI encoding and decoding of transmit and receive data is provided. If this bit is a zero, the transmit and receive data is treated as a normal positive logic

NRZI encoding specifies that a zero causes a change in the polarity of the transmitted signal and a one causes no polarity change. NRZI is used in all asynchronous operations. Refer to IBM document GA27-3093 for details.

#### **Reset Device Command**

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
TMR:	1	0	0	0	0	0	0	0	0	121	A.F
TMR:	dig8	0	0	0	0	0	0	0	0	0	Si

An 8273 reset command is executed by outputing a (01)<sub>H</sub> followed by (00)<sub>H</sub> to the reset register (TMR). See 8273 AC timing characteristics for Reset pulse specifications.

The reset command emulates the action of the reset pin.

- 1. The modem control signals are forced high (inactive
- 2. The 8273 status register flags are cleared.
- 3. Any commands in progress are terminated immedi-
- 4. The 8273 enters an idle state until the next command is issued
- 5. The Serial I/O and Operating Mode registers are set to zero and DMA data register transfer mode is selected. agom тарияя атиг чо
- 6. The device assumes a non-loop SDLC terminal role.

#### Receive Commandshoo (IMO) show gallanego leasest

The 8273 supports three receive commands: General Receive, Selective Receive, and Selective Loop Receive.

#### General Receive (CMD Code C0)

General receive is a receive mode in which frames are received regardless of the contents of the address field.

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	$D_3$	$D_2$	D <sub>1</sub>	D <sub>0</sub>			
CMD:	0	0	1	1	0	0	0	0	0	0			
PAR:	0	1		LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)									
PAR:	0	111		OST SIGNIFICANT BYTE OF RECEIVE									

#### NOTES:

- 1. If buffered mode is specified, the R0, R1 receive frame length (result) is the number of data bytes received.
- 2. If non-buffered mode is specified, the R0, R1 receive frame length (result) is the number of data bytes received plus two (the count includes the address and control bytes).
- 3. The frame check sequence (FCS) is not transferred to memory.
- Frames with less than 32 bits between flags are ignored (no interrupt generated) if the buffered mode is specified.
- 5. In the non-buffered mode an interrupt is generated when a less than 32 bit frame is received, since data transfer requests have occurred.
- 6. The 8273 receiver is always disabled when an Idle is received after a valid frame. The CPU module must issue a receive command to re-enable the receiver.
- The intervening ABORT character between a final flag and an IDLE does not generate an interrupt.
- 8. If an ABORT Character is not preceded by a flag and is followed by an IDLE, an interrupt will be generated for the ABORT followed by an IDLE interrupt one character time later. The reception of an ABORT will disable the receiver.

#### Selective Receive (CMD Code C1) com benefited at selection

	A1.	Ao	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>				
CMD:	0	0	1	1.	0	0	0	0	0	1				
PAR:	0	1		LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)										
PAR:	0	1		MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)										
PAR:	0	o to			E FR	AME A1)	ADDI	RESS	MAT	СН				
PAR:	0	115	40.	RECEIVE FRAME ADDRESS MATCH										



Selective receive is a receive mode in which frames are ignored unless the address field matches any one of two address fields given to the 8273 as parameters.

When selective receive is used in HDLC the 8273 looks at the first character, if extended, software must then decide if the message is for this unit.

## Selective Loop Receive (CMD Code C2)

	A <sub>1</sub>	$A_0$	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	1091	
CMD:	0	0	1	1	0	0	0	0	1	0	]	
PAR:	0	0					NT B			HE	11100	
PAR:	0	1			GNIF			TE O	FRE	CEIVE	10	
PAR:	0	1			E FR		ADDI	RESS	MAT	СН	0	
PAR:	0	11			E FR		ADDI	RESS	MAT	СН		

Selective loop receive operates like selective receive except that the transmitter is placed in flag stream mode automatically after detecting an EOP (01111111) following a valid received frame. The one bit delay mode is also reset at the end of a selective loop receive.

#### Receive Disable (CMD Code C5)

Terminates an active receive command immediately.

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	$D_5$	D <sub>4</sub>	D <sub>3</sub>	$D_2$	D <sub>1</sub>	D <sub>0</sub>
CMD:	0.	0	1	1	0	0	0.	1	0	1

#### **Transmit Commands**

The 8273 supports three transmit commands: Transmit Frame, Loop Transmit, Transmit Transparent.

#### Transmit Frame (CMD Code C8)

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
CMD:	0	0	1	1	0	0	1	0	0	0	
PAR:	0	1			IGNI			YTE	OF	ALTR	on
PAR:	0	Y 1			GNIF			TE O	F <sub>(O,</sub>	A1,(A	0FI
PAR:	0	1	AD	DRES	S FIE	LD (	OF TE	RANS	MIT F	RAME	(A)
PAR:	0	1	COI	VTRO	L FI	ELD (	OF TE	RANS	MIT	FRAME	(C)

Transmits one frame including; initial flag, frame check sequence, and the final flag.

If the buffered mode is specified, the L0, L1, frame length provided as a parameter is the length of the information field and the address and control fields must be input.

In unbuffered mode the frame length provided must be the length of the information field plus two and the address and control fields must be the first two bytes of data. Thus only the frame length bytes are required as parameters.

#### Loop Transmit (CMD Code CA)

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	$D_3$	$D_2$	D <sub>1</sub>	D <sub>0</sub>			
CMD:	0	0	1	1	0	0	1	0	1	0			
PAR:	0	0.8				FICA TH (		YTE	OF	or und it Sat P			
PAR:	0	1		MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)									
PAR:	0	1	ADI	ORES	S FIE	LD O	FTR	ANS	/IT F	RAME (A)			
PAR:	0	1	CON	ITRO	L FIE	LDC	FTR	ANS	MITF	RAME (C)			

Transmits one frame in the same manner as the transmit frame command except:

- If the flag stream mode is not active transmission will begin after a received EOP has been converted to a flag.

  (SS abo C CMC) B not bear?
- If the flag stream mode is active transmission will begin at the next flag boundary for buffered mode or at the third flag boundary for non-buffered mode.
- At the end of a loop transmit the one-bit delay mode is entered and the flag stream mode is reset.

#### Transmit Transparent (CMD Coded C9)

	A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
CMD:	0	0	.1	1	0	0	1	0	0	1
PAR:	0	1		AST S				YTE (	OF	
PAR:	0 .	1		ST SI				TE O	F	

The 8273 will transmit a block of raw data without protocol, i.e., no zero bit insertion, flags, or frame check sequences.

SEPE Command Summers

#### **Abort Transmit Commands**

An abort command is supported for each type of transmit command. The abort commands are ignored if a transmit command is not in progress.

#### Abort Transmit Frame (CMD Code CC)

		A <sub>0</sub>								
CMD:	0	0	. 1	1	0	0	.1	1	0	0

After an abort character (eight contiguous ones) is transmitted, the transmitter reverts to sending flags or idles as a function of the flag stream mode specified.

#### Abort Loop Transmit (CMD Code CE)

		A <sub>1</sub>	A <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	$D_3$	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
L0,L1,(A,C)	CMD:	0	0	1	1	0	0	1	18	1	0	
LOLITIALCY	PAR:	NON	IE	1		7	15		tim	ans	TO	

After a flag is transmitted the transmitter reverts to one bit delay mode.

#### Abort Transmit Transparent (CMD Code CD)

						D <sub>4</sub>				
CMD:	0	0	. 1	1	0	. 0	1	1	0	1

The transmitter reverts to sending flags or idles as a function of the flag stream mode specified.



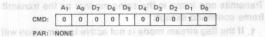


#### **Modem Control Commands**

The modem control commands are used to manipulate the modem control ports.

When read Port A or Port B commands are executed the result of the command is returned in the result register. The Bit Set Port B command requires a parameter that is a mask that corresponds to the bits to be set. The Bit Reset Port B command requires a mask that has a zero in the bit positions that are to be reset.

#### Read Port A (CMD Code 22)

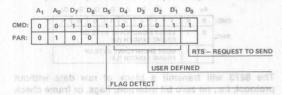


#### Read Port B (CMD Code 23)



#### Set Port B Bits (CMD Code A3)

This command allows user defined Port B pins to be set.



#### (D5) Flag Detect

This bit can be used to set the flag detect pin. However, it will be reset when the next flag is detected.

### (D4-D1) User Defined Outputs of risvip abidit assubbs

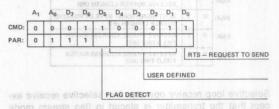
These bits correspond to the state of the PB<sub>4</sub>-PB<sub>1</sub> output pins.

#### (Do) Request to Send

This is a dedicated 8273 modem control signal, and reflects the same logical state of RTS pin.

#### Reset Port B Bits (CMD Code 63)

This command allows Port B user defined bits to be reset.



This command allows Port B (D<sub>4</sub>-D<sub>1</sub>) user defined bits to be reset. These bits correspond to Output Port pins (PB<sub>4</sub>-PB<sub>1</sub>).

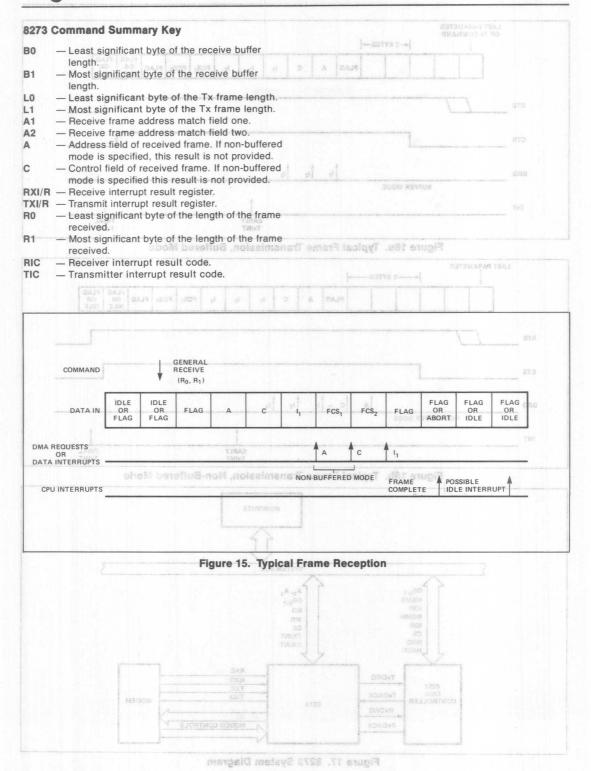
#### 8273 Command Summary

Command Description	Command (HEX)	Parameter	Results	Result Port	Completion Interrupt
Set One Bit Delay	nods A4 T b	Set Mask	None		No
Reset One Bit Delay	iq ni 64 ai bi	Reset Mask	None	_	No
Set Data Transfer Mode	97	Set Mask	None some	transmit :	273 solborts are
Reset Data Transfer Mode	57	Reset Mask	None January	snEmens	Loc of ansmit, Ti
Set Operating Mode	eA 91	Set Mask	None	_	No
Reset Operating Mode	51	Reset Mask	None	TBO ebo	O OMOL NO THE
Set Serial I/O Mode	A0	Set Mask	None	-	No
Reset Serial I/O Mode	60	Reset Mask	None	0 80 NO NO	No
General Receive	C0	B0,B1	RIC,R0,R1,(A,C)(2)	RXI/R	Yes
Selective Receive	C1	B0,B1,A1,A2	RIC,R0,R1,(A,C)(2)	RXI/R	Yes
Selective Loop Receive (IMD)	men C2 goo	B0,B1,A1,A2	RIC,R0,R1,(A,C)(2)	RXI/R	Yes PANEL
Receive Disable	A C5	None	None	WELD OF TRM	BEROGA NO BRAN
Transmit Frame	C8 :GM3	L0,L1,(A,C) <sup>(1)</sup>	TIC	TXI/R	Yes
Loop Transmit	CA	L0,L1,(A,C) <sup>(1)</sup>	TIC	TXI/R	Yes
Transmit Transparent and bell	imaniC9ai ge	L0,L1	lat tiag, framoithed	TXI/R	Yes Sin
Abort Transmit Frame	CC SOC	None	TIC	TXI/R	Yes
Abort Loop Transmit	CE	None	LO, L1, framolfing	TXI/R	a si econyes elluc
Abort Transmit Transparent	CD	None	Olamon and on	TXI/R	Telements Yes
Read Port A	22	None	Port Value	Result	No
Read Port B	23	None	Port Value	Result	uffereo/Node the fr
Set Port B Bit	A3	Set Mask	None	spid bleit	10178/TIDI No No 10
Reset Port B Bit	63	Reset Mask	None	HER SER FROM	No

#### NOTES:

- 1. Issued only when in buffered mode.
- 2. Read as results only in buffered mode.







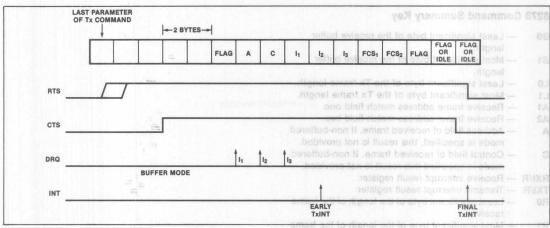


Figure 16a. Typical Frame Transmission, Buffered Mode

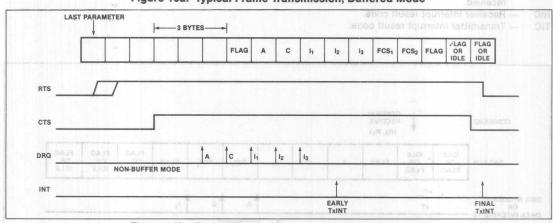


Figure 16b. Typical Frame Transmission, Non-Buffered Mode

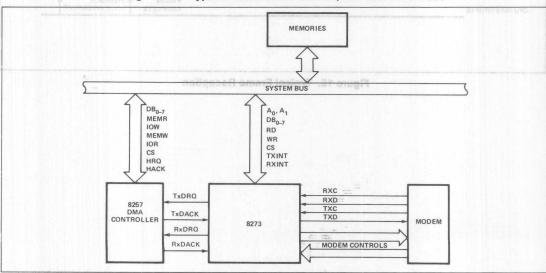


Figure 17. 8273 System Diagram





### ABSOLUTE MAXIMUM RATINGS\*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	65°C to +150°C
Voltage on Any Pin With	11.09
Respect to Ground	0.5V to +7V
Power Dissipation Selovi	1 Watt

"NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter

Input Signal Fall Time

### D.C. CHARACTERISTICS (8273, 8273-4, 8273-8) (TA = 0°C to 70°C, VCC = +5.0V ±5%)

Symbol	GM 101 To Parameter	Min.	Max.	Unit	Test Conditions
VIL	Input Low Voltage	-0.5	0.8	V	too BACK Setup to RD
VIH	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	top DACK Hold from RD
V <sub>OL</sub>	Output Low Voltage	006	0.45	V	I <sub>OL</sub> = 2.0 mA for Data Bus Pins I <sub>OL</sub> = 1.0 mA for Output Port Pins I <sub>OL</sub> = 1.6 mA for All Other Pins
V <sub>OH</sub>	Output High Voltage	2.4	0	V	$I_{OH} = -200 \mu\text{A}$ for Data Bus Pins $I_{OH} = -100 \mu\text{A}$ for All Other Pins
TIL	Input Load Current		±10	μΑ	V <sub>IN</sub> = V <sub>CC</sub> to 0V
loz	Off-State Output Current		±10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> to 0 V
Icc	CC V <sub>CC</sub> Supply Current		180	mA	two Data Hold from WR
		CALIFORNIA PROPERTY.	70 Ph	1	

#### CAPACITANCE (8273, 8273-4, 8273-8) (TA = 25°C, VCC = GND = 0V)

Symbol	Parameter Parameter	Min.	Тур.	Max.	Unit	Test Conditions
CIN	Input Capacitance	pao		10 to RI	V mpF blot	t <sub>c</sub> =1MHz
C <sub>I/O</sub>	I/O Capacitance			20	eboW 18mb	Unmeasured Pins Returned to GND

#### A.C. CHARACTERISTICS ( $T_A = 0$ °C to 70°C, $V_{CC} = +5.0V \pm 5\%$ )

#### **CLOCK TIMING (8273)**

Symbol	Parameter 1	Min.	Typ.	Max.	Unit	Test Conditions
tcy	Clock	250	Yof: 1.8	2000	ns	CY32 32X-Ctock
t <sub>CL</sub>	Clock Low	120	Y I CY		ns	64K Baud Max Operating Rate
t <sub>CH</sub>	Clock High	120	Y03 #	-	ns	MADOLU VELU III III III III III III III III III I

#### **CLOCK TIMING (8273-4)**

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
tcy	Clock	286	A01 - 0/20	2000	ns	1 timeses?
t <sub>CL</sub>	Clock Low	135	0.005		ns	56K Baud Max Operating Rate
t <sub>CH</sub>	Clock High	135	100		ns	bloH sis() us

#### CLOCK TIMING (8273-8)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
t <sub>CY</sub>	Clock	330	inu zagasio	2000	ns 8.0	Output "1" at 2 5 V. "0" at
t <sub>CL</sub>	Clock Low	150		ent specs.	ivorns ior	48K Baud Max Operating Rate
t <sub>CH</sub>	Clock High	150			ns	o p o raining raining



### A.C. CHARACTERISTICS (8273, 8273-4, 8273-8) (T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = +5.0V ±5%) Ambient Temperature Under Bras ...... 0° C to 70° C device. This is a stress rating only and fur BIDYS Ambient

Symbol	Parameter		Min.	Max.	Unit	Test Conditions
tAC	Select Setup to RD	ton	a nonsio	VEF of V3.0-	ns	Note 2
t <sub>CA</sub>	Select Hold from RD	DIMBI	0	HEW F	ns	Note 2
t <sub>RR</sub>	RD Pulse Width		250		ns	
t <sub>AD</sub>	Data Delay from Address	3		300	ns	Note 2
t <sub>RD</sub>	Data Delay from RD		or $O^*O = *T$	200	ns	C <sub>L</sub> = 150 pF, Note 2
t <sub>DF</sub>	Output Float Delay	IlnU	20	100	ns	C <sub>L</sub> = 20 pF for Minimum; 150 pF for Maximum
t <sub>DC</sub>	DACK Setup to RD	٧	25	8.0-	ns	V <sub>a</sub> I Input Low Vg
t <sub>CD</sub>	DACK Hold from RD	V	25	0.0	ns	V doill then! High Vo
t <sub>KD</sub>	Data Delay from DACK			300	ns	
RITE CYCL	EqhiO 101 Am 0.f = 101	V	0.45		egatlo'	Voi Output Low V

Symbol	Parameter	Min.	Max.	Unit	Test Cond	itions
t <sub>AC</sub>	Select Setup to WR	0	2.4	ens	( Output High )	но¥
t <sub>CA</sub>	Select Hold from WR	0		ns		
t <sub>WW</sub>	WR Pulse Width	250		ns	rer used regni	10
t <sub>DW</sub>	Data Setup to WR	150	1	ns	Jud etets-no.	20-
t <sub>WD</sub>	Data Hold from WR	0		ns	Voc Supply O	
t <sub>DC</sub>	DACK Setup to WR	25		ns		
t <sub>CD</sub>	DACK Hold from WR	25		ns		

#### DMA

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
too	Request Hold from WR or RD		200	Pacitanos	C <sub>IN</sub> input Ca
TCQ	(for Non-Burst Mode)		200	ns	

#### OTHER TIMING

Symbol	Parameter	Min.	Max.	Unit	Test (	Conditions
t <sub>RSTW</sub>	Reset Pulse Width	10		tcy		
t <sub>r</sub>	Input Signal Rise Time		20	ns	1540210	METATIO
tf	Input Signal Fall Time		20	ns	(6/28)	OFFICE ADDR
t <sub>RSTS</sub>	Reset to First IOWR	2 .cvT	,niM	t <sub>CY</sub>	ensis I	lodmy8
t <sub>CY32</sub>	32X Clock Cycle Time	9.7 · t <sub>CY</sub>	pas	ns	dent?	
t <sub>CL32</sub>	32X Clock Low Time	4 · tcy	OD F	ns	Laboration	
t <sub>CH32</sub>	32X Clock High Time	4 · t <sub>CY</sub>		ns		207
t <sub>DPLL</sub>	DPLL Output Low	1 · t <sub>CY</sub> - 50	UST	ns	T ADORO	H97
tDCL	Data Clock Low	1 · t <sub>CY</sub> - 50		ns	8273-4)	LOCK TIMING
tDCH	Data Clock High	2·t <sub>CY</sub>	ne\$100	ns	America D	Inches 9
tDCY	Data Clock	62.5 · t <sub>CY</sub>	500	ns		- Indiana
t <sub>TD</sub>	Transmit Data Delay		200	ns	AUTO	405
tos	Data Setup Time	200	GE1	ns	L NOOK I	19)
t <sub>DH</sub>	Data Hold Time	100	135	ns	Clock H	HO!
t <sub>FLD</sub>	FLAG DET Output Low	8 · t <sub>CY</sub> ± 50		ns	10.5000	DISTRICT NO. 1

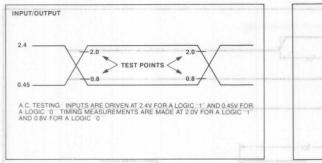
- 1. All timing measurements are made at the reference voltages unless otherwise specified: Input "1" at 2.0V, "0" at 0.8V; Output "1" at 2.0V, "0" at 0.8V.
- 2. tAD, tRD, tAC, and tCA are not concurrent specs.

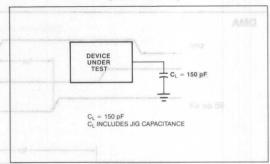




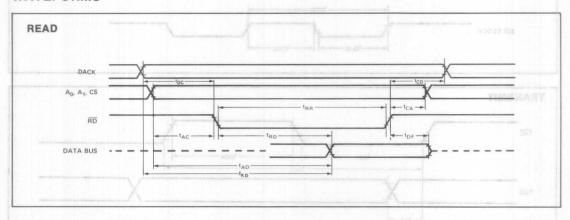
#### A.C. TESTING INPUT, OUTPUT WAVEFORM

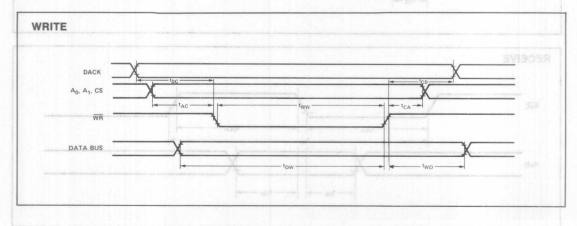
### A.C. TESTING LOAD CIRCUIT





#### **WAVEFORMS**



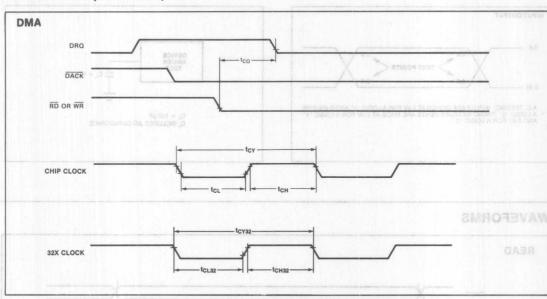


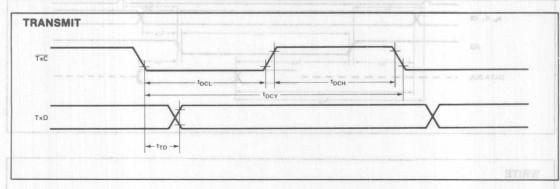


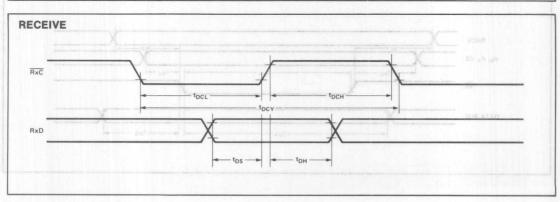


A.C. TESTING INPUT, OUTPUT WAVEFORM

## WAVEFORMS (Continued) AND DMITEST OF A



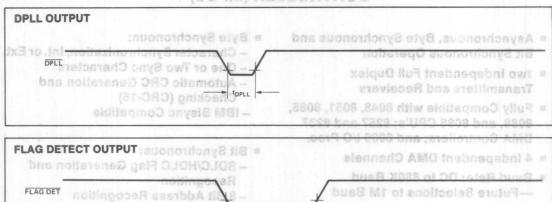




Automatic Zero Sit Insertion and

- Automatic CRC Generation and

- CCITT X.25 Compatible



The Intel® 8274 Muiti-Protocol Series Controller (MPSC) is designed to interface High Speed Communications Lines using Asynchronous, IBM Bisync, and SDLC/HDLC protocol to Intel microcomputer systems, it can be interfaced with Intel® MCS-48, -65, -51; IAPX-86, and -86 families, the 8237 DMA Controller, or the 8089 I/O Processor in polied, interrupt driven, or DMA driven modes of operation.

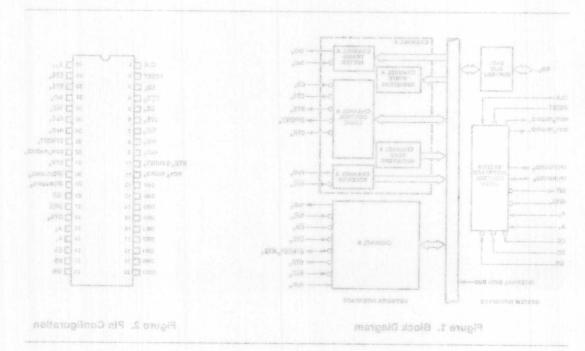
tFLD

The MPSC is a 40 pin device fabricated using Intel's High Performance HMOS Technology.

-5-8 Bit Character: Odd. Even. or No

Error Detection: Franting, Overnum,

Parity; 1, 1.5 or 2 Stop Bits



AFN-00743B

WAVEFORMS (Continued)



# 8274 MULTI-PROTOCOL SERIAL CONTROLLER (MPSC)

- Asynchronous, Byte Synchronous and Bit Synchronous Operation
- Two Independent Full Duplex Transmitters and Receivers
- Fully Compatible with 8048, 8051, 8085, 8088, and 8086 CPU's; 8257 and 8237
   DMA Controllers; and 8089 I/O Proc.
- 4 Independent DMA Channels
- Baud Rate: DC to 880K Baud
   —Future Selections to 1M Baud
- Asynchronous:
  - -5-8 Bit Character; Odd, Even, or No Parity; 1, 1.5 or 2 Stop Bits
  - —Error Detection: Framing, Overrun, and Parity

- Byte Synchronous:
  - Character Synchronization, Int. or Ext.
  - One or Two Sync Characters
  - Automatic CRC Generation and Checking (CRC-16)
  - IBM Bisync Compatible
- Bit Synchronous: TUSTUO TOETED DAJE
  - SDLC/HDLC Flag Generation and Recognition
  - 8 Bit Address Recognition
  - Automatic Zero Bit Insertion and Deletion
  - Automatic CRC Generation and Checking (CCITT-16)
  - CCITT X.25 Compatible

The Intel® 8274 Multi-Protocol Series Controller (MPSC) is designed to interface High Speed Communications Lines using Asynchronous, IBM Bisync, and SDLC/HDLC protocol to Intel microcomputer systems. It can be interfaced with Intel's MCS-48, -85, -51; iAPX-86, and -88 families, the 8237 DMA Controller, or the 8089 I/O Processor in polled, interrupt driven, or DMA driven modes of operation.

The MPSC is a 40 pin device fabricated using Intel's High Performance HMOS Technology.

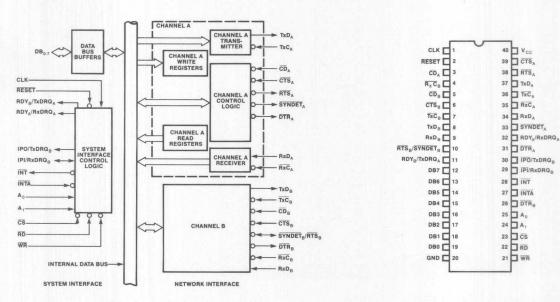


Figure 1. Block Diagram

Figure 2. Pin Configuration



#### Table 1. Pin Description

Symbol	Pin No.	Туре	Name and Function
CLK	1 gurnat	I still	Clock: System clock, TTL compatible.
RESET on be re- lerrupt con- scheme. e: This in- allows the	tgial uper thoirs ni tam niaria	tid ta. Euroeti eosor), eo exte gesey- a desey-	Reset: A low signal on this pin will force the MPSC to an idle state. TxD <sub>A</sub> and TxD <sub>B</sub> are forced high. The modem interface output signals are forced high. The MPSC will remain idle until the control registers are initialized. Reset must be true for one complete CLK cycle.
Channel B): se output. ects Chan-	ady (C purpo	ianii Ri eneral	Carrier Detect (Channel A): Carrier Detect (Channel A) signals that the line transmission has started. The MPSC will begin to sample data on the RxD <sub>A</sub> line if modern enables are selected.
RxC <sub>B</sub>	stoole	duping Arlow t	Receiver Clock: The Receiver Clock (Channel B) clocks in data on the RxD <sub>B</sub> pin.
CD <sub>B</sub> mod ets	enas	n woi :	Carrier Detect (Channel B): Carrier Detect (Channel B) signals that the line transmission has started. The MPSC will begin to sample data on the RxD <sub>B</sub> line if modem enables are selected.
CTS <sub>B</sub> em a	sionis	00 e8°	Clear To Send (Channel B): Clear To Send (Channel B) signals that the modem is ready to accept data from the MPSC. Clear To Send will enable Channel B transmitter if modem enables are selected, otherwise this pin may be used as a general purpose input.
TxC <sub>B</sub>			Transmit Clock (Channel B): Transmit Clock (Channel B) for TxD <sub>B</sub> pin.
TxD <sub>B</sub>	8	o o o o o o o o o o o o o o o o o o o	Transmit Data (Channel B): This line transmits the serial data to the communications channel (Channel B).
RxD <sub>B</sub>	9	I NTA	Receive Data (Channel B): This line receives serial data from the communications channel (Channel B).
the MPS of	ng in 1 WR stop 4; D1 er (N		Synchronous Detection (Channel B): This pin is used in byte synchronous mode as either an internal sync detect (output) or as a means to force external synchronization (input). In SDLC mode, this pin is an output indicating Flag detection. In asynchronous mode it is a general purpose input (Channel B). Request To Send (Channel B) is a general purpose output, generally used to signal that Channel B is ready to send data.

Symbol	Pin No.	Туре	Name and Function
RDY <sub>B</sub> / TxDRQ <sub>A</sub>	onillo on co xaRQ	e contr ne (op ind 2 B ifer of	Ready Transmit Data: In mode of this pin is used to synchronize data transfers for both Receive and Transmit of Channel B to the controlling processor's READY line (open collector). In modes 1 and 2 this pin requests a DMA transfer of data for a transmit operation (Channel A).
DB7 <sub>j eln</sub> T (A tennent) Oso output.	12	1/0	Data Bus: The Data Bus lines are bi-directional three state lines which interface with the system's Data Bus.
DB6	13	dingir	SQUARED SO O BRIGHT
DB5	14	ateo c	t besu ei .
DB4	15	vinonty	Iquiretni
DB3	16	HILLIAN	Ins well at
DB2	17	DESCRIPTION	Broding pi
DB1	18	PARRIE	,S. obom
DB0	19	of mini-	transferon .
GND	20	leanen	Ground. Ou es 199
The second second second	40	Misorial at	Talendaria Control Control
V <sub>cc</sub>	39	ei Jojy	Power: +5V Supply.  Clear To Send (Channel A): This
sor's inter- n mode 2, transfer of aration for	enit ine. tine. S DM s op	olling ce rou iqueste a recei	signals that the modem is ready to accept data from the MPSC. Clea To Send will enable Channel transmitter if modem enables are selected, otherwise this pin may bused as a general purpose input.
RTS	38	0	Request To Send (Channel A): Request To Send (Channel A) is a general purpose output generally used to signal that Channel A is ready to send data.
TxD <sub>A</sub>	37	0	Transmit Data (Channel A): Thi
n suppor ohronoi ohronoi	whiel Syn t Syn	evice Byte nd Bi	line transmits the serial data to the communications channel (Channel A).
TxC <sub>A</sub>	36	prpto llows hese	Transmitter Clock (Channel A) The transmitter clock (Channel A clocks out data on the TxD <sub>A</sub> pin.
RxC <sub>A</sub> .bs	35	art ov	Receiver Clock (Channel A): The receiver clock (Channel A) clocks in data on the RxD <sub>A</sub> pin.
RxD <sub>A</sub>			Receive Data (Channel A): This line receives serial data from the communications channel (Channel A).
SYNDET	33	1/0	Synchronous Detection (Channe
rt intel'r	equi airea	-	A): This pin is used in byte synchronous mode as either an interna sync detect (output) or as a means to force external synchronization (input). In SDLC mode, this pin is an
a defails	face.	r inter	output indicating flag detection. In asynchronous mode it is a genera
eral syste			

Symbol	Pin No.	Туре	Name and Function
RDY/ RxDRQ <sub>A</sub>	th Rainel B or's R th mor	tor to of Chan ocess (cotos), questa	Ready: In mode 0 this pin is used to synchronize data transfers for both receive and transmit of Channel A to the controlling processor? READY line (open collector). In modes 1 and 2 RXDRQ <sub>A</sub> requests a DMA transfer of data for a receive operation for Channel A.
DTR <sub>A</sub>	31	0	Data Terminal Ready: This pin is Data Terminal Ready (Channel A) which is a general purpose output.
IPO/ TxDRQ <sub>B</sub>	30 C		Interrupt Priority Out: In modes 0 and 1, IPO is Interrupt Priority Out. It is used to establish a hardware interrupt priority scheme with IPI, It is low only if IPI is low and the controlling processor is not servicing an interrupt from this MPSC. In mode 2, TxDRQ <sub>8</sub> requests a DMA transfer of data for a transmit operation for Channel B.
PI/ RXDRQ <sub>B</sub> at A). This is ready to perfect Clear Channel & chann	Chane noden the A lable dem dem	at the a more at the first	Interrupt Priority In: In modes 0 and 1, IPI is Interrupt Priority In. A low on IPI means that no higher priority device is being serviced by the controlling processor's interrupt service routine. In mode 2, RXDRQ <sub>8</sub> requests a DMA transfer of data for a receive operation for Channel B.

-	. A . A . SHIP		
GENI	FRAI	DESCR	IDTION

The Intel® 8274 Multi-Protocol Serial Controller is a microcomputer peripheral device which supports Asynchronous (Start/Stop), Byte Synchronous (Monosync, IBM Bisync), and Bit Synchronous (ISO's HDLC, IBM's SDLC) protocols. This controller's flexible architecture allows easy implementation of many variations of these three protocols with low software and hardware overhead.

The Multi-Protocol Serial Controller (MPSC) implements two independent serial receiver/transmitter channels.

The MPSC supports several microprocessor interface options; Polled, Wait, Interrupt driven and DMA driven. The MPSC is designed to support Intel's® MCS-85 and iAPX 86, 88 families.

This data sheet will describe the serial protocol functions, the microprocessor interface, a detailed register and command description, general system operations, specifications, and waveforms.

Symbol	Pin No.	Туре	Name and Function				
idle state d high. The	28 O		Interrupt: The interrupt signal in- dicates that the highest priority internal interrupt requires service (open collector). Priority can be re- solved via an external interrupt con- troller or a daisy-chain scheme.				
ÎNTA	27	tins con Reset dete C	Interrupt Acknowledge: This Interrupt Acknowledge allows the highest priority interrupting device to generate an interrupt vector.				
	26 O		Data Terminal Ready (Channel E This is a general purpose output				
A <sub>0</sub>			Address: This line selects Chan- nel A or B during data or command transfers. A low selects Channel A.				
A <sub>1</sub> el B): Car- signala that	(G len	(Chan	Address: This line selects between data or command information transfer. A low means data.				
CS elgmas	23	ed the	Chip Select: Chip Select enables RD or WR.				
RD al B): Clear algnals that	(S le	(Chann					
WR ness o	21	n is rek APSIO. C bannel	Write: Write controls transfer of data or commands to the MPSC.				

#### **FUNCTIONAL DESCRIPTION**

This section of the data sheet describes how the Asynchronous and Synchronous protocols are implemented in the MPSC. It describes general considerations, transmit operation, and receive operation for Asynchronous, Byte Synchronous, and Bit Synchronous protocols.

#### **ASYNCHRONOUS OPERATIONS**

Receive Data (Chounel B): This line

# General beau et riq ant ris

For operation in the asynchronous mode, the MPSC must be initialized with the following information: character length (WR3; D7, D6 and WR5; D6, D5), clock rate (WR4; D7, D6), number of stop bits (WR4; D3, D2), odd, even or no parity (WR4; D1, D0), interrupt mode (WR1, WR2), and receiver (WR3; D0) or transmitter (WR5; D3) enable. When loading these parameters into the MPSC, WR4 information must



be written before the WR1, WR3, WR5 parameters/ commands. (See Detailed Command Description Section).

For transmission via a modem or RS232C interface, the Request To Send (RTS) (WR5; D1) and Data Terminal Ready (DTR) (WR5; D7) bits must be set along with the Transmit Enable bit (WR5; D3). Setting the Auto Enables (WR3; D5) bit allows the programmer to send the first character of the message without waiting for a clear to send (CTS).

Both the Framing Error and Receive Overrun Error flags are latched and cause an interrupt, i.e., if status affects vector (WR1B; D2) is selected, the interrupt vector indicates a special Receive condition.

If the External/Status Interrupt bit (WR1; D0) is enabled, Break Detect (RR0; D7) and Carrier Detect (RR0; D3) will cause an interrupt. Reset External/Status Interrupts (WR0; D5, D4, D3) will clear Break Detect and Carrier Detect bits if they are set.

A status read after a data read will include error status for the next word in the buffer. If the Interrupt on First Character (WR1; D4, D3) is selected, then data and error status are held until an Error Reset command (WR0; D5, D4, D3) is given.

If the Interrupt on Every Character Mode bit (WR1; D4, D3) is selected, the interrupt vector is different if there is an error status in RR1. When the character is read, the error status bit is set and the Special Receive Condition vector is returned if Status Affects vector (WR1B; D2) is selected.

In a polled environment, the Receive Character Available bit (RR0; D0) must be monitored so that the CPU can determine when data is available. The bit is reset automatically when the data is read. If the X1 clock mode is selected, the bit synchronization must be accomplished externally.

#### **Transmit**

The transmit function begins when the Transmit Enable bit (WR5; D3) is set. The MPSC automatically adds the start bit, the programmed parity bit (odd, even or no parity) and the programmed number of stop bits (1, 1.5 or 2 bits) to the data character being transmitted.

The Serial data is shifted out from the Transmit Data (TxD) output on the falling edge of the Transmit Clock (TxC) input, at a rate programmable to 1, 1/16, 1/32nd, or 1/64th of the clock rate supplied to the TxC input.

The TxD output is held high when the transmitter has no data to send, unless, under program control, the Send Break (WR5; D4) command is issued to hold the TxD low.

If the External/STATUS Interrupt bit (WR1; D0) is set, the status of CD, CTS and SYNDET are monitored, and, if any changes occur for a period of time greater than the minimum specified pulse width, an interrupt is generated. CTS is usually monitored using this interrupt feature.

If the Auto Enables (WR; D5) option is selected the programmer need not wait for the CTS before sending the first character. The MPSC will automatically wait for the CTS pin to go active before the transmission begins.

The Transmit Buffer Empty bit (RR0; D2) is set by the MPSC when the data byte from the buffer is loaded in the transmit shift register. The data is written to the MPSC only when the Tx buffer becomes empty to prevent overwriting.

003	ra		Asynchron	nous Mode	Register Se	tup	07 08		
	D7 8	D6	D5	D4	D3	D2	rs D1d d	00 D0	
WR3	00 Rx 5 01 Rx 7 10 Rx 6	b/char b/char	AUTO ENABLES	BAMB 0	EGOM 0	ENABLES 0	6 b/char 6 b/char 6 b/char	Rx ENABLE	
PARITY	11 Rx 8		0	0	bit Sync	ar ro	0	0 <b>种利</b>	
ENVBRE	00 X1	Clock			MOE	LE SYNC DES	EVEN/		
WR4	01 X16 10 X32 11 X64	Clock	0 (SELEC	0	01 1 STC 10 1½ ST 11 2 STC	OP BITS	ODD	PARITY ENABLE	
ENABLE	110201	175	5 b/char	JBAMS	AASHB	6 b/char 8 b/char	XT O:		
WR5	DTR		7 b/char	SEND	Tx	0	RTS	0	
			6 b/char 8 b/char	BREAK	ENABLE				



#### Receive

The receive function begins when the Receive Enable (WR3; D0) bit is set. If the Auto Enables (WR3; D5) option is selected, then Carrier Detect (CD) must also be low. A valid start bit is detected if a low persists for at least 1/2 bit time on the Receive Data (RxD) input.

If the X1 clock mode is selected, the bit sy

tion must be accomplished externally

The data is sampled at mid-bit time, on the rising edge of RxC, until the entire character is assembled. The receiver inserts 1's when a character is less than 8 bits. If parity (WR4; D1, D0) is enabled and the character is less than 8 bits the parity bit is not stripped from the character.

The receiver also stores error status for each of the 3 data characters in the data buffer. When a parity error is detected, the parity error flag (RR1; D4) is set and remains set until it is reset by the Error Reset command (WR0; D5, D4, D3).

When a character is assembled without a stop bit being detected, the Framing Error bit (RR1; D6) is set. The detection of a Framing Error adds an additional 1/2 bit time to the character time so the Framing Error is not interpreted as a new start bit.

If the CPU fails to read a data character while more than three characters have been received, the Receive Overrun bit (RR1; D5) is set. Only the overwritten character is flagged with the Receive Overrun bit. When this occurs, the fourth character assembled replaces the third character in the receive buffers. The Receive Overrun bit (RR1; D5) is reset by the Error Reset command (WR0; D5, D4, D3).

# SYNCHRONOUS OPERATION— MONO SYNC, BI SYNC

#### General necession via a modern or Research For

The MPSC must be initialized with the following parameters: odd or even parity (WR4; D1,D0), X1 clock mode (WR4; D7, D6), 8- or 16-bit sync character (WR4; D5, D4), CRC polynomial (WR5; D2), Transmitter Enable (WR5; D3), interrupt modes (WR1, WR2), transmit character length (WR5; D6, D5) and receive character length (WR3; D7, D6). WR4 parameters must be written before WR1, WR3, WR5, WR6 and WR7.

The data is transmitted on the falling edge of the Transmit Clock, (TxC) and is received on the rising edge of Receive Clock (RxC). The X1 clock is used for both transmit and receive operations for all three sync modes: Mono, Bi and External.

#### Transmit Set-Up-Monosync, Bisync at A

Transmit data is held high after channel reset, or if the transmitter is not enabled. A break may be programmed to generate a spacing line that begins as soon as the Send Break (WR5; D4) bit is set. With the transmitter fully initialized and enabled, the default condition is continuous transmission of the 8- or 16-bit sync character.

Using interrupts for data transfer requires that the Transmit Interupt/DMA Enable bit (WR1; D1) be set. An interrupt is generated each time the transmit buffer becomes empty. The interrupt can be satisfied

#### Synchronous Mode Register Setup—Monosync, Bisync

	D7	D6	D5 piled	D4 9	D3 10111	nya D2	D1	D0
00	00 Rx 5	5 b/char	SG	ENTER	80	30	SYNC	
WR3	10 Rx 6	7 b/char 6 b/char 8 b/char	AUTO ENABLES	HUNT	Rx CRC ENABLE	O AUT	CHAR LOAD INHIBIT	Rx ENABLE
WR4	0	0	00 8 bit 01 16 bit 11 Ext Sy	Sync	0	0	EVEN/ ODD PARITY	PARITY ENABLE
WR5	A9 MB DTR	THE RESERVE AND ASSESSMENT OF THE PERSON NAMED IN	x 5 b/char x 7 b/char	SEND	0	1 (051.507	01 X16 Clock 10 X32 Clock	TH CDC
WHO	DIR	10 T	x 6 b/char x 8 b/char	BREAK	Tx ENABLE	(SELECT CRC-16		Tx CRC ENABLE



either by writing another character into the transmitter or by resetting the Transmitter Interrupt/DMA Pending latch with a Reset Transmitter Interrupt/DMA Pending Command (WR0; D5, D4, D3). If nothing more is written into the transmitter, there can be no further Transmit Buffer Empty interrupt, but this situation does cause a Transmit Underrun condition (RR0; D6).

Data Transfers using the RDY signal are for software controlled data transfers such as block moves. RDY tells the CPU that the MPSC is not ready to accept/provide data and that the CPU must extend the output/input cycle. DMA data transfers use the TxDRQ A/B signals which indicate that the transmit buffer is empty, and that the MPSC is ready to accept the next data character. If the data character is not loaded into the MPSC by the time the transmit shift register is empty, the MPSC enters the Transmit Underrun condition.

The MPSC has two programmable options for solving the transmit underrun condition: it can insert sync characters, or it can send the CRC characters generated so far, followed by sync characters. Following a chip or channel reset, the Transmit Underrun/EOM status bit (RR0; D6) is in a set condition allowing the insertion of sync characters when there is no data to send. The CRC is not calculated on these automatically inserted sync characters. When the CPU detects the end of message, a Reset Transmit Underrun/EOM command can be issued. This allows CRC to be sent when the transmitter has no data to send.

In the case of sync insertion, an interrupt is generated only after the first automatically inserted sync character has been loaded in Transmit Shift Register. The status indicates the Transmit Underrun/EOM bit and the Transmit Buffer Empty bit are set.

In the case of CRC insertion, the Transmit Underrun/EOM bit is set and the Transmit Buffer Empty bit is reset while CRC is being sent. When CRC has been completely sent, the Transmit Buffer Empty status bit is set and an interrupt is generated to indicate to the CPU that another message can begin (this interrupt occurs because CRC has been sent and sync has been loaded into the Tx Shift Register). If no more messages are to be sent, the program can terminate transmission by resetting RTS, and disabiling the transmitter (WR5; D3).

Bisync CRC Generation. Setting the Transmit CRC enable bit (WR5; D0) indicates CRC accumulation when the program sends the first data character to

the MPSC. Although the MPSC automatically transmits up to two sync characters (16 bit sync), it is wise to send a few more sync characters ahead of the message (before enabling Transmit CRC) to ensure synchronization at the receiving end.

The Transmit CRC Enable bit can be changed on the fly any time in the message to include or exclude a particular data character from CRC accumulation. The Transmit CRC Enable bit should be in the desired state when the data character is loaded from the transmit shift register. To ensure this bit in the proper state, the Transmit CRC Enable bit must be issued before sending the data character to the MPSC.

Transmit Transparent Mode. Transparent mode (Bisync protocol) operation is made possible by the ability to change Transmit CRC Enable on the fly and by the additional capability of inserting 16 bit sync characters. Exclusion of DLE characters from CRC calculation can be achieved by disabling CRC calculation immediately preceding the DLE character transfer to the MPSC.

reinitialized using the Enable Interrupt On Next Re-

In the transmit mode, the transmitter always sends the programmed number of sync bits (8 or 16) (WR4; D5, D4). When in the Monosync mode, the transmitter sends from WR6 and the receiver compares against WR7. One of two CRC polynomials, CRC 16 or SDLC, may be used with synchronous modes. In the transmit initialization process, the CRC generator is initialized by setting the Reset Transmit CRC Generator command (WR0; D7, D6).

The External/Status interrupt (WR1; D0) mode can be used to monitor the status of the CTS input as well as the Transmit Underrun/EOM latch. Optionally, the Auto Enable (WR3; D5) feature can be used to enable the transmitter when CTS is active. The first data transfer to the MPSC can begin when the External/Status interrupt occurs (CTS (RR0; D5) status bit set) following the Transmit Enable command (WR5; D3).

interrupt whenever a character enters the receive

### Receive

After a channel reset, the receiver is in the Hunt phase, during which the MPSC looks for character synchronization. The Hunt begins only when the receiver is enabled and data transfer begins only when character synchronization has been achieved. If character synchronization is lost, the hunt phase can be re-entered by writing the Enter Hunt Phase (WR3; D4) bit. The assembly of received data continues until the MPSC is reset or until the receiver is



disabled (by command or by  $\overline{\text{CD}}$  while in the Auto Enables mode) or until the CPU sets the Enter Hunt Phase bit. Under program control, all the leading sync characters of the message can be inhibited from loading the receive buffers by setting the Sync Character Load Inhibit (WR3; D1) bit. After character synchronization is achieved the assembled characters are transferred to the receive data FIFO.

Data may be transferred with or without interrupts. Transferring data without interrupts is used for a purely polled operation or for off-line conditions. There are three interrupt modes available for data transfer: Interrupt on First Character Only, Interrupt on Every Character, and Special Receive Conditions Interrupt.

Interrupt on First Character Only mode is normally used to start a polling loop, a block transfer sequence using RDY to synchronize the CPU to the incoming data rate or a DMA transfer using the RxDRQ signal. The MPSC interrupts on the first character and thereafter only interrupts after a Special Receive Condition is detected. This mode can be reinitialized using the Enable Interrupt On Next Receive Character (WR0; D5, D4, D3) command which allows the next character received to generate an interrupt. Parity Errors do not cause interrupts, but End of Frame (SDLC operation) and Receive Overrun do cause interrupts in this mode. If the external status interrupts (WR1; D0) are enabled an interrupt may be generated any time the CD changes state.

Interrupt On Every Character mode generates an interrupt whenever a character enters the receive buffer. Errors and Special Receive Conditions generate a special vector if the Status Affects Vector (WR1B; D2) is selected. Also the Parity Error may be

first data transfer to the MFSC can begin when the

programmed (WR1; D4, D3) not to generate the special vector while in the Interrupt On Every Character mode.

The Special Receive Condition interrupt can only occur while in the Receive Interrupt On First Character Only or the Interrupt On Every Receive Character modes. The Special Receive Condition interrupt is caused by the Receive Overrun (RR1; D5) error condition. The error status reflects an error in the current word in the receive buffer, in addition to any Parity or Overrun errors since the last Error Reset (WR0; D5, D4, D3). The Receive Overrun and Parity error status bits are latched and can only be reset by the Error Reset (WR0; D5, D4, D3) command.

#### SYNCHRONOUS OPERATION—SDLC

#### General

Like the other synchronous operations the SDLC mode must be initialized with the following parameters: SDLC mode (WR4; D5, D4), SDLC polynomial (WR5; D2), Request to Send, Data Terminal Ready, transmit character length (WR5; D6, D5), interrupt modes (WR1; WR2), Transmit Enable (WR5; D3), Receive Enable (WR3; D0), Auto Enable (WR3; D5) and External/Status Interrupt (WR1; D0).WR4 parameters must be written before WR1, WR3, WR5, WR6 and WR7.

The Interrupt modes for SDLC operation are similar to those discussed previously in the synchronous operations section.

### (ad :088) 2TO) supported Synchronous Mode Register Setup—SDLC/HDLC and ORO to see out of

	D7	D6	D5;anw	brieD4	D3	D2	D1	D0
WR3	01 Rx 10 Rx	5b/char 7b/char 6b/char 8b/char	AUTO ENABLES	ENTER HUNT MODE	Rx CRC ENABLE	ADDRESS SEARCH MODE	complete it is set a the CPU	Rx ENABLE
or <b>PRW</b> acte	C looks tins only	the MPS	1 (SELECTS HDLC M		Tx Sh <sup>0</sup> i Reg- sent, the pro-	oaded Onto the ges are to be	nas i <sup>0</sup> een ire messi	sent and sync ster). If no mo
ac <b>zaw</b> ed. a hunt phas r Hunt Phas ed data cor	ATOPI ATOPI Iost, the he Ente of receiv	01 Tx 10 Tx	≤5b/char ⟨7b/char ⟨6b/char ⟨8b/char	ohara chara can bi (WR3:	Tx ENABLE	0 (SELECTS SDLC/ HDLC CRC)	RTS	CRC



#### **Transmit**

After a channel reset, the MPSC begins sending SDLC flags.

Following the flags in an SDLC operation the 8-bit address field, control field and information field may be sent to the MPSC by the microprocessor. The MPSC transmits the Frame Check Sequence using the Transmit Underrun feature. The MPSC automatically inserts a zero after every sequence of 5 consecutive 1's except when transmitting Flags or Aborts.

SDLC—like protocols do not have provision for fill characters within a message. The MPSC therefore automatically terminates an SDLC frame when the transmit data buffer and output shift register have no more bits to send. It does this by sending the two bytes of CRC and then one or more flags. This allows very high-speed transmissions under DMA or CPU control without requiring the CPU to respond quickly to the end-of-message situation.

After a reset, the Transmit Underrun/EOM status bit is in the set state and prevents the insertion of CRC characters during the time there is no data to send. Flag characters are sent. The MPSC begins to send the frame when data is written into the transmit buffer. Between the time the first data byte is written, and the end of the message, the Reset Transmit Underrun/EOM (WR0; D5, D4, D1) command must be issued. The Transmit Underrun/EOM status bit (RR0; D6) is in the reset state at the end of the message which automatically sends the CRC characters.

The MPSC may be programmed to issue a send Abort command (WR0; D5, D4, D3). This command causes at least eight 1's but less than fourteen 1's to be sent before the line reverts to continuous flags.

#### Into the Command/Status Pointer. The reviews

After initialization, the MPSC enters the Hunt phase, and remains in the Hunt phase until the first Flag is received. The MPSC never again enters the Hunt phase unless the microprocessor writes the Enter Hunt command.

or write operation accesses the read or write re-

The MPSC can be programmed to receive all frames or it can be programmed to the Address Search Mode. In the Address Search Mode, only frames with addresses that match the value in WR6 or the global address (0FFH) are received by the MPSC. Extended address recognition must be done by the microprocessor software.

The control and information fields are received as data.

SDLC/HDLC CRC calculation does not have an 8-bit delay, since all characters are included in the calculation, unlike Byte Synchronous Protocols.

Reception of an abort sequence (7 or more 1's) will cause the Break/Abort bit (RR0; D7) to be set and will cause an External/Status interrupt, if enabled. After the Reset External/Status Interrupts Command has been issued, a second interrupt will occur at the end of the abort sequence.

#### **MPSC**

#### **Detailed Command Description**

#### **GENERAL**

The MPSC supports an extremely flexible set of serial and system interface modes.

The system interface to the CPU consists of 8 ports or buffers:

	CS A <sub>0</sub> A <sub>1</sub>		Α,	Read Operation	Write Operation	
	0	0	0.5	Ch. A Data Read	Ch. A Data Write	
	0	0	1	Ch. A Status Read	Ch. A Command/Parameter	
24	0	1	0	Ch. B Data Read	Ch. B Data Write	
-1	0	1	1	Ch. B Status Read	Ch. B Command/Parameter	
H	1	X	X	High Impedence	High Impedence	

Data buffers are addressed by  $A_1 = 0$ , and Command ports are addressed by  $A_1 = 1$ .

Command, parameter, and status information is held in 22 registers within the MPSC (8 write registers and 3 read registers for each channel). They are all accessed via the command ports.

An internal pointer register selects which of the command or status registers will be read or written during a command/status access of an MPSC channel.



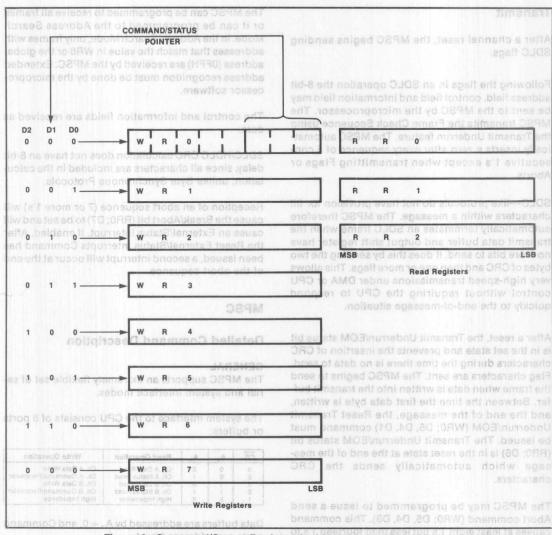


Figure 3. Command/Status Register Architecture (each serial channel)

After reset, the contents of the pointer register are zero. The first write to a command register causes the data to be loaded into Write Register 0 (WR0).

The three least significant bits of WR0 are loaded as the content of the c

Command, parameter, and status information is

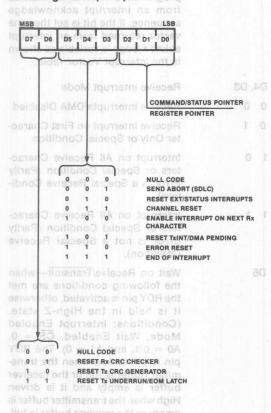
into the Command/Status Pointer. The next read or write operation accesses the read or write register selected by the pointer. The pointer is reset after the read or write operation is completed.



#### COMMAND/STATUS DESCRIPTION

The following command and status bytes are used during initialization and execution phases of operation. All Command/Status operations on the two channels are identical, and independent, except where noted.

#### Write Register 0 (WR0): mas poor



# Detailed Register Description

#### WRO

D2, D1, D0—Command/Status Register Pointer bits determine which write-register the next byte is to be written into, or which read-register the next byte is to be read from. After reset, the first byte written into either channel goes into WR0. Following a read or write to any register (except WR0) the pointer will point to WR0.

D5, D4, D3—Command bits determine which of the basic seven commands are to be performed.

Command 0 Null-has no effect.

Command 1 Send Abort—causes the generation of eight to thirteen 1's when in the SDLC mode.

Command 2 Reset External/Status Interrupts—
resets the latched status bits of
RR0 and re-enables them, allowing
interrupts to occur again.

Command 3

Channel Reset—resets the Latched Status bits of RR0, the interrupt prioritization logic and all control registers for the channel. Four extra system clock cycles should be allowed for MPSC reset time before any additional commands or controls are written into the channel.

Command 4 Enable Interrupt on Next Receive Character—if the Interrupt on First Receive Character mode is selected, this command reactivates that mode after each complete message is received to prepare the MPSC for the next message.

Command 5

Reset Transmitter Interrupt/DMA

Pending—if The Transmit
Interrupt/DMA Enable mode is
selected, the MPSC automatically
interrupts or requests DMA data
transfer when the transmit buffer
becomes empty. When there are no
more characters to be sent,
issuing this command prevents
further transmitter interrupts or
DMA requests until the next
character has been completely
sent.

Command 6 Fror Reset—error latches, Pari-UO and no and ty and Overrun errors in RR1 are

Command 7 End of Interrupt—resets the interrupt-in-service latch of the highest-priority internal device under service.

D7, D6 CRC Reset Code

Null—has no effect.

01 Reset Receive CRC Checker—
resets the CRC checker to 0's. If in
SDLC mode the CRC checker is
initialized to all 1's.

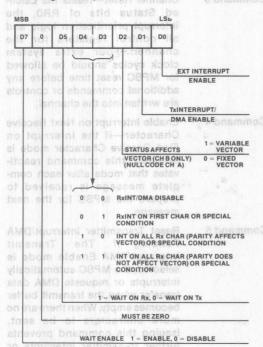
Deoxe , inebne



10 Reset Transmit CRC Generator
—resets the CRC generator to
0's. If in SDLC mode the CRC
generator's initialized to all 1's.

11 Reset Tx Underrun/End of Message Latch.

#### Write Register 1 (WR1):



D0 External/Status Interrupt Enable
—allows interrupt to occur as the
result of transitions on the CD,
CTS or SYNDET inputs. Also
allows interrupts as the result of a
Break/Abort detection and termination, or at the beginning of CRC,
or sync character transmission
when the Transmit Underrun/EOM
latch becomes set.

D1 Transmitter Interrupt/DMA Enable
beautiful and a service —allows the MPSC to interrupt or
request a DMA transfer when the
transmitter buffer becomes empty.

Status Affects vector—(WR1, D2 active in channel B only.) If this bit is not set, then the fixed vector, programmed in WR2, is returned from an interrupt acknowledge sequence. If the bit is set then the vector returned from an interrupt acknowledge is variable as shown in the Interrupt Vector Table.

D4, D3 Receive Interrupt Mode

0 0 Receive Interrupts/DMA Disabled

0 1 Receive Interrupt on First Character Only or Special Condition

1 0 Interrupt on All Receive Charac-

O Interrupt on All Receive Characters or Special Condition (Parity Error is a Special Receive Condition)

Interrupt on All Receive Characters or Special Condition (Parity Error is not a Special Receive Condition).

D5 Wait on Receive/Transmit-when the following conditions are met the RDY pin is activated, otherwise it is held in the High-Z state. (Conditions: Interrupt Enabled Mode, Wait Enabled,  $\overline{CS} = 0$ , A0 = 0/1, and A1 = 0). The RDY pin is pulled low when the transmitter buffer is full or the receiver buffer is empty and it is driven High when the transmitter buffer is empty or the receiver buffer is full. The RDYA and RDYB may be wired OR connected since only one signal is active at any one time while the other is in the High Z state.

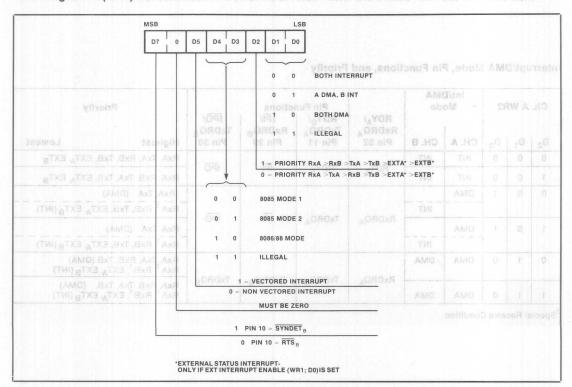
6 Must be Zero

D7: sixd xsn of Wait Enable—enables the wait one neith were function.



12	Channel A agbelwon/los fourneith	ns of sano D5, D4, D3	Interrupt Code—specifies the behavior of the MPSC when it re-
D1, D0	System Configuration—These specify the data transfer from	здом	ceives an interrupt acknowledge sequence from the CPU. (See Inter
	MPSC channels to the CPU, either		rupt Vector Mode Table).
	interrupt or DMA based.	X X Dectored X	Non-vectored interrupts-in
0 0 to	Channel A and Channel B both use interrupts		tended for use with external DMA CONTROLLER. The Data Bus re mains in a high impedence state
0 1 0	Channel A uses DMA, Channel B		during INTA sequences.
1 0	Channel A and Channel B both use DMA		8085 Vector Mode 1—intended fo use as the primary MPSC in a dais chained priority structure. (See System Interface section)
1 1 D2	Priority—this bit specifies the relative priorities of the internal MPSC interrupt/DMA sources.	1 0 1 85 Mode 2	8085 Vector Mode 2—intended for use as any secondary MPSC in daisy chained priority structure. (See System Interface section)
0	(Highest) RxA, TxA, RxB, TxB ExTA, ExTB (Lowest)	1 1 0 sboM 88	8086/88 Vector Mode—intender for use as either a primary of secondary in a daisy chainer
1	(Highest) RxA, RxB, TxA, TxB,		priority structure. (See Syster
	ExTA, ExTB (Lowest)		Interface section)
		D7, D6	Must be zero.

Write Register 2 (WR2): Channel A partnerpord meet and about "notices about a street and acent"





The following table describes the MPSC's response to an interrupt acknowledge sequence:

D5	D4	D3	IPI	MODE	INTA	Data Bus
eid). erru0 te-	aT abold	Vector I		Non-vectored	Any INTA	D7 D7 D0 D0 D0 High Impedance
Date Bu Pate Bu edence es.	ER. One	LLORT	10:0 niam	85 Mode 1	1st INTA 2nd INTA 3rd INTA	1 1 0 0 1 1 0 1 V7 V6 V5 V4* V3* V2* V1 V0 0 0 0 0 0 0 0 0 0
intende PSC In av Poture Non)	M O smi	is tife pr	lead erlo	85 Mode 1	1st INTA 2nd INTA 3rd INTA	1 1 0 0 1 1 0 1 High Impedance High Impedance
Intende ny MPSC ny structu se section	mong b	enisilo y	dais) (See	85 Mode 2	1st INTÁ 2nd INTA 3rd INTA	High Impedance High Impedance High Impedance
a prynai isy cha Sea Sv		acoesii andary	100 100R	86 Mode	1st INTA	High Impedance V7 V6 V5 V4 V3 V2* V1*V0*
1		13.0 Sec		86 Mode	1st INTA 2nd INTA	High Impedance

<sup>\*</sup>These bits are variable if the "status affects vector" mode has been programmed, (WR1B, p.2). (CRW) Chestage Residue

#### Interrupt/DMA Mode, Pin Functions, and Priority

Ch. A WR2 Int/DMA Mode			RDY <sub>A</sub> / RxDRQ <sub>A</sub>	Pin Fu RDY <sub>B</sub> / TxDRQ <sub>A</sub>	nctions IPI/ RxDRQ <sub>B</sub>	Priority																
$D_2$	D <sub>1</sub>	Do	CH. A	СН. В	Pin 32	Pin 11			Highest Lowe													
0	0	0	INT	INT	ATXEL BUT AND	E BYS - AVS YT	noint IPI		RxA, TxA, RxB, TxB, EXTA, EXTB													
1	0	0	INT	INT	RDYA	прів	потв	потв	nD1B	нотв	прів	прів	прів	прів	прів	ниув	HUYB	HUYB	RDYB	AGIAS - C	IPO	RxA, RxB, TxA, TxB, EXTA, EXTB
0	0	1	DMA				порм вког	0 0	RxA, TxA (DMA)													
				INT	D DD0	155			RxA 1, RxB, TxB, EXTA, EXTB (INT													
1	0	1	DMA		RxDRQA	TxDRQA	EGOM IPI	IPO	RxA, TxA (DMA)													
				INT		30	SUBSUPER MICH		RxA <sup>1</sup> , RxB, TxB, EXT <sub>A</sub> , EXT <sub>B</sub> (INT													
0	1	0	DMA	DMA			JADELII		RxA, TxA, RxB, TxB (DMA) RxA <sup>1</sup> , RxB <sup>1</sup> , EXT <sub>A</sub> , EXT <sub>B</sub> (INT)													
1	1	0	DMA	DMA	RxDRQA	TxDRQ	TxDRQ <sub>A</sub> RxDRQ <sub>B</sub>	TxDRQB	RxA, RxB, TxA, TxB, (DMA) RxA <sup>1</sup> , RxB <sup>1</sup> , EXT <sub>A</sub> , EXT <sub>B</sub> (INT)													

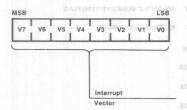
<sup>&</sup>lt;sup>1</sup>Special Receive Condition



#### (ARM) A seia Interrupt Vector Mode Table

8085 Modes 8086/88 Mode	V <sub>4</sub> V <sub>2</sub>	V <sub>3</sub>	<b>V</b> <sub>2</sub> <b>V</b> <sub>0</sub>	Channel	ona lid sidT iniged of re
Note 1: Special Receive Condition = Parity Error, RX Overrun Error, Framing Error, End of Frame (SDLC)	0 0 0 0	0 0 1 1	0 1 0 1	t—A offe pre- oading synd uffers.	Tx Buffer Empty Ext/Status Change Rx Char. Available Special Rx Condition (Note 1)
0 0 SHARLESYNESKO	1 1 1 1	0 0 1 1	0 1 0 1	PSC will re- it is a 1. If this e only frames on the global	Tx Buffer Empty Ext/Status Change Rx Char. Available Special Rx Condition (Note 1)

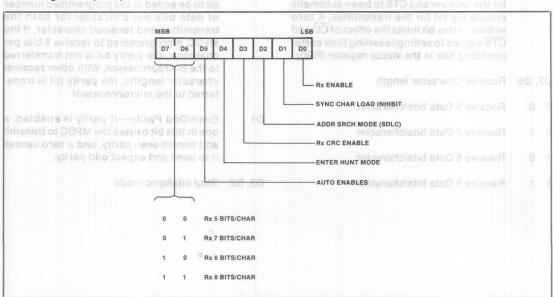
#### Write Register 2 (WR2): Channel B



### WR2 CHANNEL B (seldsne-et 10) seldsne

D7-D0 Interrupt vector—This register contains the value of the interrupt vector placed on the data bus during interrupt acknowledge sequences.

#### Write Register 3 (WR3): M and 8-VINS9

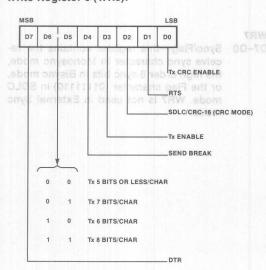




W	R3	or Mode Table	tos W	rite R	egi	ster	4 (	WR4	):		
D(	)	Receiver Enable—A one enables the re- ceiver to begin. This bit should be set only	Vg	MSB		- 3/			poi	intl Mari	LSB
		after the receiver has been initialized.	oV.	D7	D6	D5	D4	D3	D2	D1	DO
D.		Sync Character Load Inhibit—A one prevents the receiver from loading sync characters into the receive buffers.	0 1 0	0 0 1		0 0 0			le solti	O.	1 = ENABLE PARITY 0 = DISABLE PARITY
D2	2	Address Search Mode—If the SDLC mode has been selected, the MPSC will receive all frames unless this bit is a 1. If this bit is a 1, the MPSC will receive only frames with address bytes that match the global address (0FFH) or the value loaded into WR6. This bit must be zero in non-SDLC modes.	0 1 0 1	0 0 1			<b>Y</b>	0 0 1 1	0	1 STO	ODD PARITY
		to: placed in the flocontol in civi zero in			0	0 0 1 1	0	16 BIT		CHAR	te Register 2 (WF)
D4	1	Enter Hunt Phase—After initialization, the MPSC automatically enters the Hunt mode. If synchronization is lost, the Hunt phase can be re-entered by writing a one to this bit.		1	1 0 1	X16 C X32 C X64 C	LOCK				otisani Vacav
D	5	Auto Enables—A one written to this bit causes $\overline{CD}$ to be automatic enable signal for the receiver and $\overline{CTS}$ to be an automatic enable signal for the transmitter. A zero written to this bit limits the effect of $\overline{CD}$ and $\overline{CTS}$ signals to setting/resetting their corresponding bits in the status register (RR0).		WR4 D0 Parity—a one in this bit causes a bit to be added to the programmed n of data bits per character for bo transmitted and received character MPSC is programmed to receive 8 b character, the parity bit is not trans to the microprocessor. With other re-							programmed numb racter for both to ved character. If to to receive 8 bits posit is not transferr
Dī	7, D6	Receive Character length			ch	ara	cte	r len	gths	s, th	e parity bit is tran
0	0	Receive 5 Data bits/character	D.								parity is enabled
0	1	Receive 7 Data bits/character			or	ne in	this	s bit	caus	ses t	he MPSC to transr y, and a zero caus
1	0	Receive 6 Data bits/character			it	to s	end	and	exp	ect	odd parity.
1	1	Receive 8 Data bits/character	1	3, D2 наночет наночет наночет	(8 8 x)	8 8 8	0 1 0	0 0		de	

- 0 1 Async mode, 1 stop bit/character
- 1 0 Async mode, 1-1/2 stop bits/character
- 1 1 Async mode, 2 stop bits/character
- D5, D4 Sync mode select
- 0 0 8 bit sync character
- 0 1 16 bit sync character
- 1 0 SDLC mode (Flag sync)
- 1 1 External sync mode
- D7, D6 Clock mode—selects the clock/data rate of multiplier for both the receiver and the transmitter. 1x mode must be selected for synchronous modes. If the 1x mode is selected, bit synchronization must be done D3 externally.
- 0 0 Clock rate = Data rate x 1
- 0 1 Clock rate = Data rate x 16
- 1 0 Clock rate = Data rate x 32
- 1 1 Clock rate = Data rate x 64

#### Write Register 5 (WR5):



- I stop bit/character

  I-½ stop bits/character

  Stop bits/character
  - buffer into the shift register. A zero in this bit disables CRC calculations. If this bit is not set when a transmitter underrun occurs, the CRC will not be sent.
  - D1 Request to Send—a one in this bit forces the RTS pin active (low) and zero in this bit forces the RTS pin inactive (high).
  - D2 CRC Select—a one in this bit selects the CRC -16 polynomial ( $X^{16} + X^{15} + X^2 + 1$ ) and a zero in this bit selects the CCITT-CRC polynomial ( $X^{16} + X^{15} + X^5 + 1$ ).
  - D3 Transmitter Enable—a zero in this bit forces a marking state on the transmitter output. If this bit is set to zero during data or sync character transmission, the marking state is entered after the character has been sent. If this bit is set to zero during transmission of a CRC character, sync or flag bits are substituted for the remainder of the CRC bits.
  - D4 Send Break—a one in this bit forces the transmit data low. A one in this bit allows normal transmitter operation.
  - D6, D5 Transmit Character length
  - 0 0 Transmit 5 or less bits/character
  - 0 1 Transmit 7 bits/character
  - 1 0 Transmit 6 bits/character
  - 1 1 Transmit 8 bits/character

Bits to be sent must be right justified least significant bit first, eq:

D7 D6 D5 D4 D3 D2 D1 D0

0 0 B5 B4 B3 B2 B1 B0

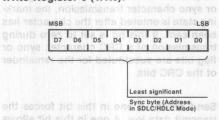


Five or less mode allows transmission of one to five bits per manys absided and aim and a —a character. The microprocessor must format the data in additional the following way:

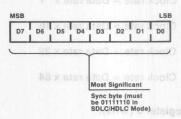
	D6				D2	D1	D0	ync mode.) 1-1/2 stop bits/character
	ne sh CRC				1	1	В0	Sends one data bit
	onen a				0	В1	В0	Sends two data bits
1	1 bns2	0	0	0	B2	B1	В0	Sends three data bits
q) s	0	0	0	В3				Sends four data bits
0	0	0	B4	ВЗ	B2	B1	В0	Sends five data bits

Data Terminal Ready—when set, this bit forces the DTR pin active (low). When reset, this bit forces the DTR pin inactive

Write Register 6 (WR6): 11d aid 11 Jugillo



#### Write Register 7 (WR7):



#### WR6

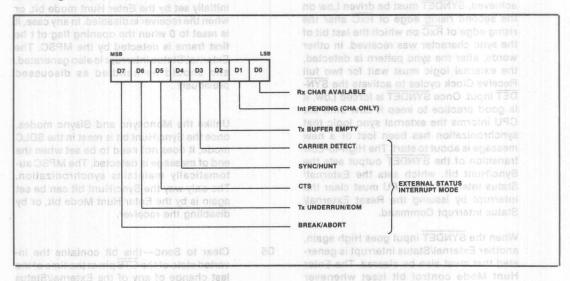
D7-D0 Sync/Address—this register contains the transmit sync character in Monosync mode, the low order 8 sync bits in Bisync mode, or the Address byte in SDLC mode.

WR7

D7-D0 Sync/Flag—this register contains the receive sync character in Monosync mode, the high order 8 sync bits in Bisync mode, or the Flag character (01111110) in SDLC mode. WR7 is not used in External Sync mode.



#### Read Register 0 (RR0): born 0.102 sdf al



#### bits (CD, CTS, Sync/Hunt, Break/Abortonn

- DO Receive Character Available—this bit is set when the receive FIFO contains data and is reset when the FIFO is empty.
- D1 Interrupt Pending\*—This Interrupt-Pending bit is reset when an EOI command is issued and there is no other interrupt request pending at that time.
- D2 Gas Transmit Buffer Empty—This bit is set whenever the transmit buffer is empty except when CRC characters are being sent in a synchronous mode. This bit is G.OFF reset when the transmit buffer is loaded. This bit is set after an MPSC reset.
- Carrier Detect—This bit contains the state of the CD pin at the time of the last change of any of the External/Status bits (CD, CTS, Sync/Hunt, Break/Abort, or Tx Underrun/EOM). Any change of state of the CD pin causes the CD bit to be latched and causes an External/Status interrupt. This bit indicates current state of the CD pin immediately following a Reset External/Status Interrupt command.

\*In vector mode this bit is set at the falling edge of the second INTA in an INTA cycle for an internal interrupt request. In non-vector mode, this bit is set at the falling edge of RD input after pointer 2 is specified. This bit is always zero in Channel B. D4 Sync/Hunt-In asynchronous modes, the operation of this bit is similar to the CD status bit, except that Sync/Hunt shows the state of the SYNDET input. Any High-to-Low transition on the SYNDET pin sets this bit, and causes an External/Status interrupt (if enabled). The Reset External/Status Interrupt command is issued to clear the interrupt. A Low-to-High transition clears this bit and sets the External/Status interrupt. When the External/Status interrupt is set by the change in state of any other input or condition, this bit shows the inverted state of the SYNDET pin at time of the change. This bit must be read immediately following a Reset External/Status Interrupt command to read the current state of the SYNDET input.

In the External Sync mode, the Sync/Hunt bit operates in a fashion similar to the Asynchronous mode, except the Enter Hunt Mode control bit enables the external sync detection logic. When the External Sync Mode and Enter Hunt Mode bits are set (for example, when the receiver is enabled following a reset), the SYNDET input must be held High by the external logic until external character synchronization is achieved. A High at the SYNDET input holds the Sync/Hunt status in the reset condition.



When external synchronization is achieved, SYNDET must be driven Low on the second rising edge of RxC after the rising edge of RxC on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the SYN-DET input. Once SYNDET is forced Low, it is good practice to keep it Low until the CPU informs the external sync logic that synchronization has been lost or a new message is about to start. The High-to-Low transition of the SYNDET output sets the Sync/Hunt bit, which sets the External/ Status interrupt. The CPU must clear the interrupt by issuing the Reset External/ Status Interrupt Command.

When the SYNDET input goes High again, another External/Status interrupt is generated that must also be cleared. The Enter Hunt Mode control bit isset whenever character synchronization is lost or the end of message is detected. In this case, the MPSC again looks for a High-to-Low transition on the SYNDET input and the operation repeats as explained previously. This implies the CPU should also inform the external logic that character synchronization has been lost and that the MPSC is waiting for SYNDET to become active.

In the Monosync and Bisync Receive modes, the Sync/Hunt status bit is initially set to 1 by the Enter Hunt Mode bit. The Sync/Hunt bit is reset when the MPSC establishes character synchronization. The High-to-Low transition of the Sync/Hunt bit causes an External/Status interrupt that must be cleared by the CPU issuing the Reset External/Status Interupt command. This enables the MPSC to detect the next transition of other External/Status bits.

When the CPU detects the end of message or that character synchronization is lost, it sets the Enter Hunt Mode control bit, which sets the Sync/Hunt bit to 1. The Low-to-High transition of the Sync/Hunt bit sets the External/Status Interrupt, which must also be cleared by the Reset External/Status Interrupt Command. Note that the SYNDET pin acts as an output in this mode, and goes low every time a sync pattern is detected in the data stream.

In the SDLC mode, the Sync/Hunt bit is initially set by the Enter Hunt mode bit, or when the receiver is disabled. In any case, it is reset to 0 when the opening flag of t he first frame is detected by the MPSC. The External/Status interrupt is also generated, and should be handled as discussed previously.

Unlike the Monosync and Bisync modes, once the Sync/Hunt bit is reset in the SDLC mode, it does not need to be set when the end of message is detected. The MPSC automatically maintains synchronization. The only way the Sync/Hunt bit can be set again is by the Enter Hunt Mode bit, or by disabling the receiver.

- Clear to Send—this bit contains the inverted state of the CTS pin at the time of the last change of any of the External/Status bits (CD, CTS, Sync/Hunt, Break/Abort, or Tx Underrun/EOM). Any change of state of the CTS pin causes the CTS bit to be latched and causes an External/Status interrupt. This bit indicates the inverse of the current state of the CTS pin immediately following a Reset External/Status Interrupt command.
- D6 Transmitter Underrun/End of Message—this bit is in a set condition following a reset (internal or external). The only command that can reset this bit is the Reset Transmit Underrun/EOM Latch command (WR0,  $D_6$  and  $D_7$ ). When the Transmit Underrun condition occurs, this bit is set, which causes the External/Status Interrupt which must be reset by issuing a Reset External/Status command (WR0; command 2).
- Break/Abort—in the Asynchronous Receive mode, this bit is set when a Break sequence (null character plus framing error) is detected in the data stream. The External/Status interrupt, if enabled, is set when break is detected. The interrupt service routine must issue the Reset External/Status Interrupt command (WRO, Command 2) to the break detection logic so the Break sequence termination can be recognized.



#### SDLC Residue Code Table (I Field Bits in 2 Previous Bytes) (1947) I relation been

			8 bit	s/char	7 bits	s/char	6 bits	s/char	5 bits/char	
RR1 D3, D2, D1			Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte
1	0	0	0	3		LACLISHET				
0	1	0	0	4			0	6		
1	1	0	0	5	I FIELD SITS	ETIG DIER				
0	0	1	0	6	2ND PREVIOUS B	STAR SOCIATION OF THE START OF	0.00		0	5
1	0	1	0	7						
0	1	1	0	8						
1	1	1	1	8			0.1.0			
0	0	0	2	ATAGSUGISSA	8 0	7	7 7 0			

The Break/Abort bit is reset when the termination of the Break sequence is detected in the incoming data stream. The termination of the Break sequence also causes the External/Status interrupt to be set. The Reset External/Status Interrupt command must be issued to enable the break detection logic to look for the next Break sequence. A single extraneous null character is present in the receiver after the termination of a break; it should be read and discarded.

In the SDLC Receive mode, this status bit is a vine set by the detection of an Abort sequence bileves is (seven or more 1's). The External/Status is identification interrupt is handled the same way as in the brisming case of a Break. The Break/Abort bit is not respective mode.

DO All sent—this bit is set when all characters have been sent, in asynchronous modes. It is reset when characters are in the transmitter, in asynchronous modes. In synchronous modes, this bit is always set.

D3, D2, D1 Residue Codes—bit synchronous protocols allow I-fields that are not an interior in deligral number of characters. Since transmed and offers from the MPSC to the CPU are characters oriented, the residue codes be negligible provide the capability of receiving revolute leftover bits. Residue bits are right justice to the last two data bytes received.

D4 m at 3 Parity Error—If parity is enabled, this bit number and is set for received characters whose parallibration ity does not match the programmed sense (Even/Odd). This bit is latched. Once an error occurs, it remains set until statement of the Error Reset command is written.



#### D7 D6 D5 D4 D3 D2 D1 DO Byte Byte L ALL SENT I FIELD BITS 2ND PREVIOUS BYTE I FIELD BITS PREVIOUS BYTE 2 8 0 0 0 0 0 1 0 1 1 8 RESIDUE DATA 8 BITS/CHAR, MODE 1 0 0 0 3 1 0 1 1 1 0 5 1 1 1 The Break/Abort bit is reset who some Yang ters have bee Rx OVERRUN ERROR MASS Stream RORRE IN INC. modes, it is re-CRC/FRAMING ERROR & SOME UDGS NEST S BITTED HOLD END OF FRAME (SDLC/HDLC MODE)

#### Read Register 1 (RR1): (Special Receive Condition Mode) de l'about subles R 0108

D5 Receive Overrun Error—this bit indi-

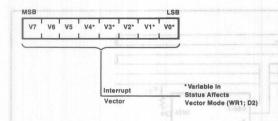
cates that the receive FIFO has been asboo all overloaded by the receiver. The last character in the FIFO is overwritten and flagged with this error. Once the overbevisces written character is read, this error condition is latched until reset by the Error Reset command. If the MPSC is in the status affects vector mode, the overrun bemman ocauses a special Receive Condition sense (Even/Odd). TrotoeV is latched.

D6 CRC/Framing Error—In async modes, a one in this bit indicates a receive fram-saimed oring error. In synchronous modes, a one in this bit indicates that the calculated CRC value does not match the last two bytes received. It can be reset by issuing an Error Reset command.

D7 End of Frame—this bit is valid only in SDLC mode. A one indicates that a valid ending flag has been received. This bit is ton all lid preset either by an Error Reset command or upon reception of the first character of the next frame.



#### Read Register 2 (RR2):



#### RR2 Channel B

D7-D0 Interrupt vector—contains the interrupt vector programmed into WR2. If the status affects vector mode is selected, it contains the modified vector. (See WR2) RR2 contains the modified vector for the highest priority interrupt pending. If no interrupts are pending, the variable bits in the vector are set to one.

#### SYSTEM INTERFACE

General near the conditions in each chan larene The MPSC to Microprocessor System interface can be configured in many flexible ways. The basic interface types are polled, wait, interrupt driven, or direct memory access driven. nerto dose not tesuper to in

Polled operation is accomplished by repetitively reading the status of the MPSC, and making decisions based on that status. The MPSC can be polled at any time, stanois event to vinoing ent. elampia

Wait operation allows slightly faster data throughput for the MPSC by manipulating the Ready input to the microprocessor. Block Read or Write Operations to the MPSC are started at will by the microprocessor and the MPSC deactivates its RDY signal if it is not yet ready to transmit the new byte, or if reception of new byte is not completed.

Interrupt driven operation is accomplished via an internal or external interrupt controller. When the MPSC requires service, it sends an interrupt request signal to the microprocessor, which responds with an interrupt acknowledge signal. When the internal or external interrupt controller receives the acknowledge, it vectors the microprocessor to a service routine, in which the transaction occurs. DMA operation is accomplished via an external DMA controller. When the MPSC needs a data transfer, it request a DMA cycle from the DMA controller. The DMA controller then takes control of the bus and simultaneously does a read from the MPSC and a write to memory or vice-versa.

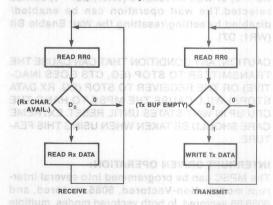
The following section describes the many configurations of these basic types of system interface techniques for both serial channels.

#### Polled Operation:

In the polled mode, the CPU must monitor the desired conditions within the MPSC by reading the appropriate bits in the read registers. All data available. status, and error conditions are represented by the appropriate bits in read registers 0 and 1 for channels A and B.

There are two ways in which the software task of monitoring the status of the MPSC has been reduced. One is the "ORing" of all conditions into the Interrupt Pending bit. (RR0; D1 channel A only). This bit is set when the MPSC requires service, allowing the CPU to monitor one bit instead of four status registers. The other is available when the "statusaffects-vector" mode is selected. By reading RR2 Channel B, the CPU can read a vector who's value will indicate that one or more of group of conditions has occurred, narrowing the field of possible conditions. See WR2 and RR2 in the Detailed Command Description section.

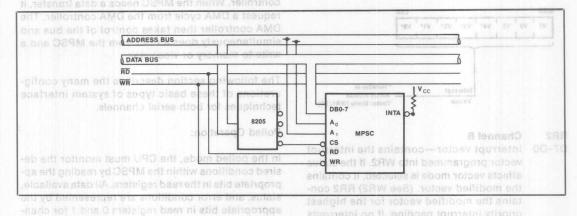
#### Software Flow, Polled Operation New 10 10 = 20



Interrupt acknowledge sequence by placing a call



#### Hardware Configuration, Polled Operation AMO



#### WAIT OPERATION:

Wait Operation is intended to facilitate data transmission or reception using block move operations. If a block of data is to be transmitted, for example, the CPU can execute a String I/O instruction to the MPSC. After writing the first byte, the CPU will attempt to write a second byte immediately as is the case of block move. The MPSC forces the RDY signal low which inserts wait states in the CPU's write cycle until the transmit buffer is ready to accept a new byte. At that time, the RDY signal is high allowing the CPU to finish the write cycle. The CPU then attempts the third write and the process is repeated.

Similar operation can be programmed for the receiver. During initialization, wait on transmit (WR2; D5 = 0) or wait on receive (WR1; D5 = 1) can be selected. The wait operation can be enabled/disabled by setting/resetting the Wait Enable Bit (WR1; D7).

CAUTION: ANY CONDITION THAT CAN CAUSE THE TRANSMITTER TO STOP (EG, CTS GOES INACTIVE) OR THE RECEIVER TO STOP (EG, RX DATA STOPS) WILL CAUSE THE MPSC TO HANG THE CPU UP IN WAIT STATES UNTIL RESET. EXTREME CARE SHOULD BE TAKEN WHEN USING THIS FEATURE.

#### INTERRUPT DRIVEN OPERATION:

The MPSC can be programmed into several interrupt modes: Non-Vectored, 8085 vectored, and 8088/86 vectored. In both vectored modes, multiple MPSC's can be daisy-chained.

In the vectored mode, the MPSC responds to an interrupt acknowledge sequence by placing a call instruction (8085 mode) and interrupt vector (8085

and 8088/86 mode) on the data bus. In the non-vectored mode, the MPSC does not respond to INTA sequences and must rely on an external interrupt controller such as the 8259A.

The MPSC can be programmed to cause an interrupt due to up to 14 conditions in each channel. The status of these interrupt conditions is contained in Read Registers 0 and 1. These 14 conditions are all directed to cause 3 different types of internal interrupt request for each channel: receive/interrupts, transmit interrupts and external/status interrupts (if enabled).

This results in up to 6 internal interrupt request signals. The priority of those signals can be programmed to one of two fixed modes:

of thighest Priority all Lowest Priority of the of another of the Orange of the Orange

RXA RXB TXA TXB EXTA EXTB

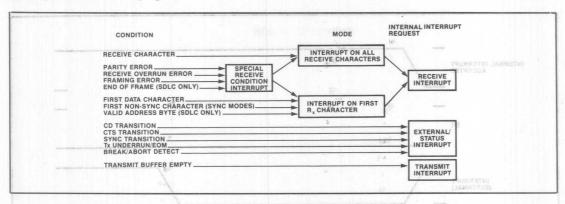
The interrupt priority resolution works differently for vectored and non-vectored modes.

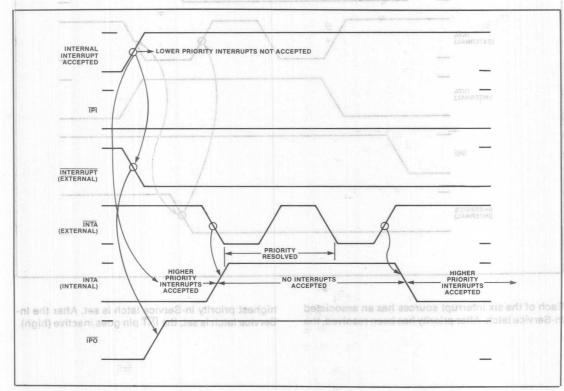
#### PRIORITY RESOLUTION: VECTORED MODE

Any interrupt condition can be accepted internally to the MPSC at any time, unless the MPSC's internal INTA signal is active, unless a higher priority interrupt is currently accepted, or if IPI is inactive (high). The MPSC's internal INTA is set on the leading (falling) edge of the first External INTA pulse and reset on the trailing (rising) edge of the second External INTA pulse. After an interrupt is accepted internally, an External INT request is generated and the IPO goes inactive. IPO and IPI are used for daisy-chaining MPSC's together.



#### **Interrupt Condition Grouping**





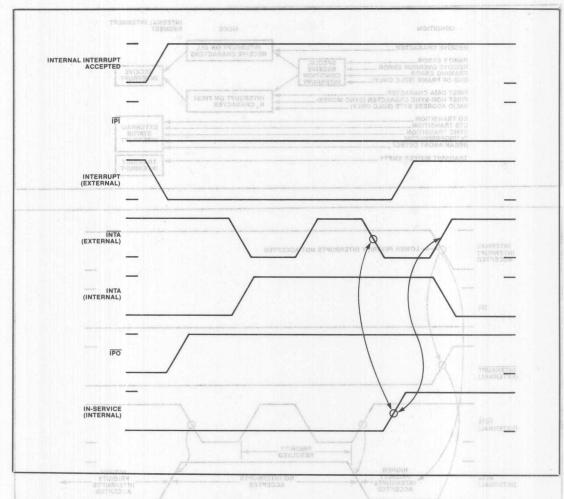
The MPSC's internal INTA is set on the leading (falling) edge of the first external INTA pulse, and reset on the trailing (rising) edge of the second external INTA pulse. After an interrupt is accepted internally,

an external  $\overline{\text{INT}}$  request is generated and  $\overline{\text{IPO}}$  goes inactive (high).  $\overline{\text{IPO}}$  and  $\overline{\text{IPI}}$  are used for daisy-chaining MPSC's together.



#### **In-Service Timing**



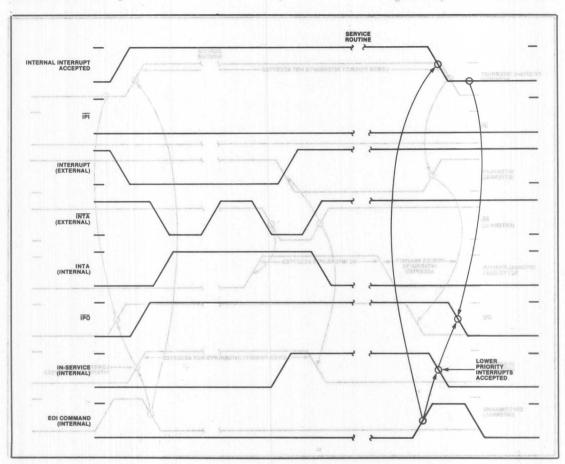


Each of the six interrupt sources has an associated In-Service latch. After priority has been resolved, the

highest priority In-Service latch is set. After the In-Service latch is set, the INT pin goes inactive (high).

an external INT request is generated and IPO goes inactive (high). IPO and IPi are used for darsychaining MPSC's together.

The MPSC's internal INTA is set on the leading (falling) edge of the first external INTA pulse, and reset on the trailing (rising) edge of the second external INTA pulse. After an interrupt is accepted internally.



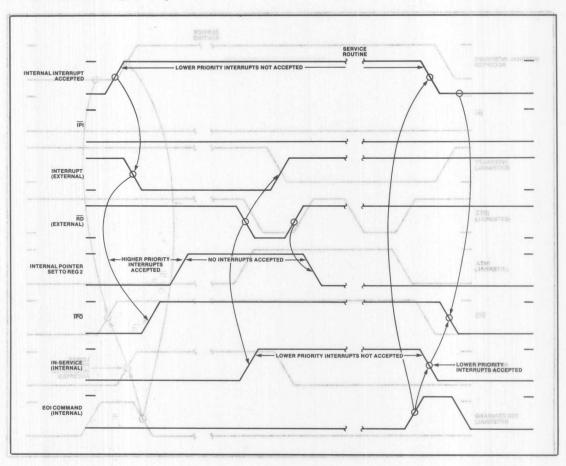
Lower priority interrupts are not accepted internally while the In-Service latch is set. However, higher priority interrupts are accepted internally and a new external INT request is generated. If the CPU responds with a new INTA sequence, the MPSC will respond as before, suspending the lower priority

ing edge of the read signal used by th.tqurretnic retrieve the modified vector. The leading edge of read sets the in-Service latch and forces the external INT output inactive (high). The internal pointer is reset to zero after the trailing edge of the read pulse.

After the interrupt is serviced, the End-of-Interrupt (EOI) command should be written to the MPSC. This command will cause an internal pulse that is used to reset the In-Service Latch which allows service for lower priority interrupts in the daisy-chain to resume, provided a new INTA sequence does not start for a higher priority interrupt (higher than the highest under service). If there is no interrupt pending internally, the IPO follows IPI.



#### **Non-Vectored Interrupt Timing**

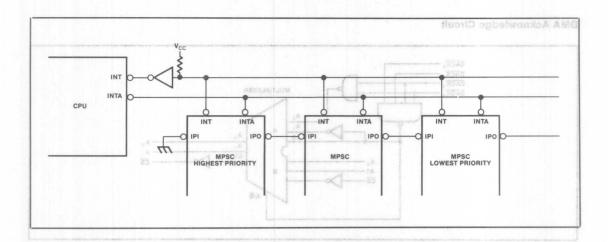


### PRIORITY RESOLUTION: is all further the first the street of the street o

In non-vectored mode, the MPSC does not respond to interrupt acknowledge sequences. The MPSC should be programmed to the Status-Affects-Vector mode, and the CPU should read RR2 (Ch. B) in its service routine to determine which interrupt requires service.

In this case, the internal pointer being set to RR2 provides the same function as the internal INTA signal in the vectored mode. It inhibits acceptance of any additional internal interrupts and its leading edge starts the interrupt priority resolution circuit. The interrupt priority resolution is ended by the leading edge of the read signal used by the CPU to retrieve the modified vector. The leading edge of read sets the In-Service latch and forces the external INT output inactive (high). The internal pointer is reset to zero after the trailing edge of the read pulse.





Note that if RR2 is specified but not read, no internal interrupts, regardless of priority, are accepted.

#### DAISY CHAINING MPSC:

In the vectored interrupt mode, multiple MPSC's can be daisy-chained on the same INT, INTA signals. These signals, in conjunction with the IPI and IPO allow a daisy-chain-like interrupt resolution scheme. This scheme can be configured for either 8085 or 8086/88 based system.

In either mode, the same hardware configuration is called for. The INT request lines are wire-OR'ed together at the input of a TTL inverter which drives the INT pin of the CPU. The INTA signal from the CPU drives all of the daisy-chained MPSC's.

The MPSC drives IPO (Interrupt Priority Output) inactive (high) if IPI (Interrupt Priority Input) is inactive (high), or if the MPSC has an interrupt pending.

The  $\overline{\text{IPO}}$  of the highest priority MPSC is connected to the  $\overline{\text{IPI}}$  of the next highest priority MPSC, and so on.

Wait Interrupt Polled	Walt Interrupt Polled	0.0	
	DMA Polled	1.0	
DMA Polled	DMA: Polled	1.0	

D1, D0 = 1, 1 is illegal.

If  $\overline{|P|}$  is active (low), the MPSC knows that all higher priority MPSC's have no interrupts pending. The  $\overline{|P|}$  pin of the highest priority MPSC is strapped active (low) to ensure that it always has priority over the rest.

MPSC's Daisy-chained on an 8088/86 CPU should be programmed to the 8088/86 Interrupt mode (WR2; D4, D3 (Ch. A). MPSC's Daisy-chained on an 8085 CPU should be programmed to 8085 interrupt mode 1 if it is the highest priority MPSC. In this mode, the highest priority MPSC issues the CALL instruction during the first INTA cycle, and the interrupting MPSC provides the interrupt vector during the following INTA cycles. Lower priority MPSC's should be programmed to 8085 interrupt mode 2.

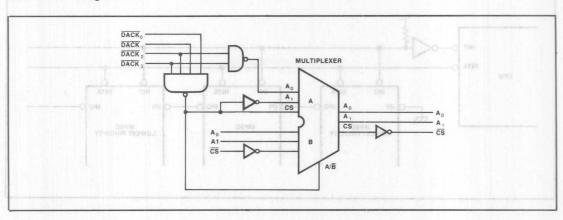
MPSC's used alone in 8085 systems should be programmed to 8085 mode 1 interrupt operation.

by encoding the  $\overline{\rm DACK}$  signals to generate  ${\rm A_0},{\rm A_1},$  and  $\overline{\rm CS}$  signals, and multiplexing them with the normal  ${\rm A_0},{\rm A_1}$  and  $\overline{\rm CS}$  signals.

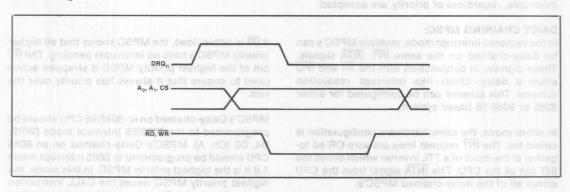
PERMUTATIONS

Channels A and B can be used with different system interface modes. In all cases it is impossible to poll the MPSC. The following table shows the possible.

# Jint Actiowieuge Circuit



#### **DMA Timing**



### MPSC provides the interrupt ve NOITRARAGO AMO

Each MPSC can be programmed to utilize up to four DMA channels: Transmit Channel A, Receive Channel A, Transmit Channel B, Receive Channel B. Each DMA Channel has an associated DMA Request line. Acknowledgement of a DMA cycle is done via normal data read or write cycles. This is accomplished by encoding the  $\overline{\rm DACK}$  signals to generate A<sub>0</sub>, A<sub>1</sub>, and  $\overline{\rm CS}$  signals, and multiplexing them with the normal A<sub>0</sub>, A<sub>1</sub>, and  $\overline{\rm CS}$  signals.

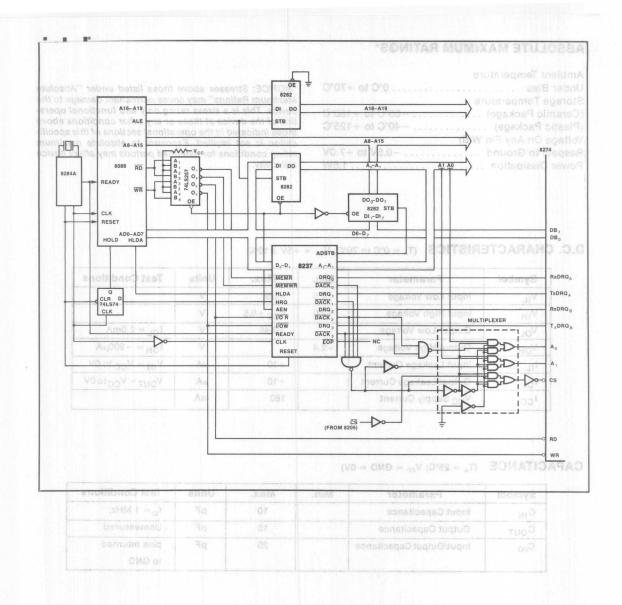
#### **PERMUTATIONS**

Channels A and B can be used with different system interface modes. In all cases it is impossible to poll the MPSC. The following table shows the possible

permutations of interupt, wait, and DAM modes for channels A and B. Bits  $D_1$ ,  $D_0$  of WR2 Ch. A determine these permutations.

Permutation WR2 Ch. A D <sub>1</sub> D <sub>0</sub>	Channel A	Channel B
0 0	Wait Interrupt Polled	Wait Interrupt Polled
0 1	DMA Polled	Interrupt Polled
1 0	DMA Polled	DMA Polled

D1, D0 = 1, 1 is illegal.



1-245

AFN-01701B



# **ABSOLUTE MAXIMUM RATINGS\***

**Ambient Temperature** Under Bias ......0°C to +70°C Storage Temperature

(Ceramic Package) .....-65°C to +150°C (Plastic Package) .....-40°C to +125°C

Voltage On Any Pin With

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (TA = 0°C to 70°C; Vcc = +5V ±10%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
VIL	Input Low Voltage	-0.5	+0.8	V	0 8.13
V <sub>IH</sub>	Input High Voltage	+2.0	V <sub>CC</sub> +0.5	V	<u> </u>
VOL	Output Low Voltage	ORG.	+0.45	V	I <sub>OL</sub> = 2.0mA
Voh	Output High Voltage	+2.4	733	V	$I_{OH} = -200\mu A$
10	Input Leakage Current	7	+10	μΑ	V <sub>IN</sub> = V <sub>CC</sub> to 0V
10L	Output Leakage Current		+10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> to 0V
Icc	V <sub>CC</sub> Supply Current		180	mA	

ES (6028 MORS)

# CAPACITANCE (T<sub>A</sub> = 25°C; V<sub>CC</sub> = GND = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
CIN	Input Capacitance		10	pF	f <sub>c</sub> = 1 MHz;
Cout	Output Capacitance		15	pF	Unmeasured
C <sub>I/O</sub>	Input/Output Capacitance		20	pF	pins returned to GND



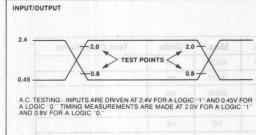
# A.C. CHARACTERISTICS (TA = 0°C to 70°C; Vcc = +5V ±10%) O TEVAN TUSTUO TUSTU DIATECT .O.A

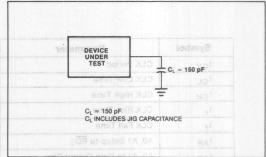
Symbol	Parameter	Min.	Max.	Units	Test Conditions
tcy	CLK Period	250	4000	ns eries	DE TEST PE
<sup>t</sup> CL	CLK Low Time	105	2000	ns	8.0-7
<sup>t</sup> CH	CLK High Time	105	2000	ns	LO M. UNANGO DIDA CV. (BOIL ADMINISTRA
t <sub>r</sub>	CLK Rise Time	0	30	ns	NO 10 TIMONG MEABUREMENTS AP DISVERSE A LOCKE OF
t <sub>f</sub>	CLK Fall Time	0	30	ns	
t <sub>AR</sub>	A0, A1 Setup to RD↓	0		ns	
t <sub>AD</sub>	A0, A1 to Data Output Dlay		200	ns	C <sub>L</sub> =150 pf
<sup>t</sup> RA	A0. A1 Hold After RD↑	0		ns	
<sup>t</sup> RD	RD↓ to Data Output Delay		200	ns	C <sub>L</sub> =150 pf
<sup>t</sup> RR	RD Pulse Width	250		ns	
t <sub>DF</sub>	Output Float Delay		120	ns	
t <sub>AW</sub>	CS, A0, A1 Setup to WR↓	0		ns	EFORKS
t <sub>WA</sub>	CS, A0, A1 Hold after WR↑	0		ns	
tww	WR Pulse Width	250		ns	DOK CYCLE
t <sub>DW</sub>	Data Setup to WR↑		150	ns	
<sup>t</sup> WD	Data Hold After WR↑	0		ns	
t <sub>Pl</sub>	IPI Setup to INTA↓	0	CHORD TELEVISION CO.	ns	
t <sub>IP</sub>	IPI Hold after INTA↑	0		ns	1(30)
t <sub>II</sub>	INTA Pulse Width	250		ns	
†IAPO	INTA↓ to IPO Delay		200	ns	
t <sub>PIPO</sub>	ĪPĪ↓ to ĪPŌ Delay		100	ns	
t <sub>ID</sub>	INTA↓ to Data Output Deay		200	ns	
<sup>t</sup> cq	RD or WR to DRQ↓		150	ns	M. Asserta Saya Saya Made Constitution of the
<sup>t</sup> RV	Recovery Time Between Controls	300		ns	0 cycle
tcw	CS, A0, A1 to RDYA or RDYB Delay		120	ns	
tDCY	Data Clock Cycle	400		ns	k /
t <sub>DCL</sub>	Data Clock Low Time	180		ns	FA,0A,23
<sup>t</sup> DCH	Data Clock High Time	180	***************************************	ns	F \
tтр	TxC to TxD Delay		300	ns	Control of the Strategy
t <sub>DS</sub>	RxD Setup to RxC↑	0	1/	ns	09
t <sub>DH</sub>	RxD Hold after RxC↑	140	and the	ns	
	TxC to INT Delay	4	6	tcy	
<sup>t</sup> ITD <sup>t</sup> IRD	RxC to INT Delay	7	10	tcy	22.00
	OTO OD OVIDET	LX.		I Extra la	. 60-, A0
t <sub>PL</sub>	CTS, CD, SYNDET Low Time	200		ns	-
<sup>t</sup> PH	CTS, CD, SYNDET High Time	200	-	ns	



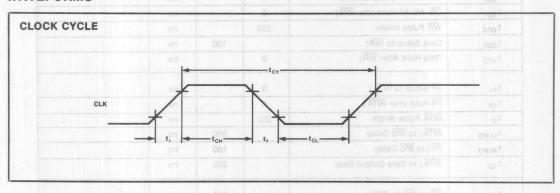
### A.C. TESTING INPUT, OUTPUT WAVEFORM

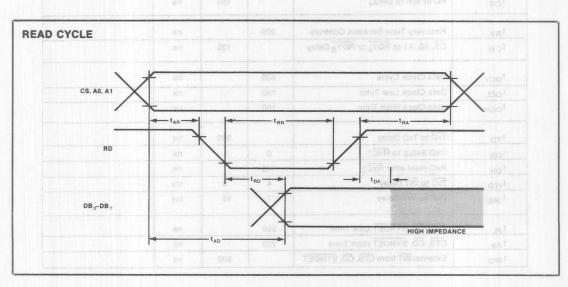
# A.C. TESTING LOAD CIRCUIT TO ARAMO O.A.





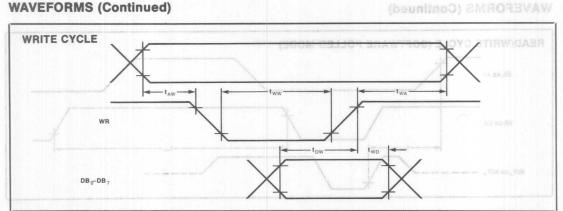
## **WAVEFORMS**

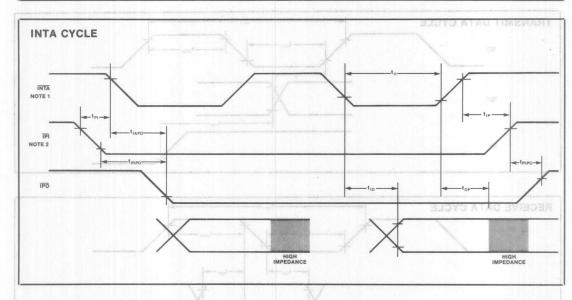


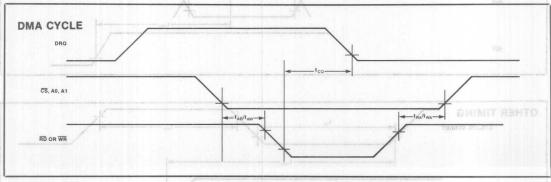




# **WAVEFORMS (Continued)**







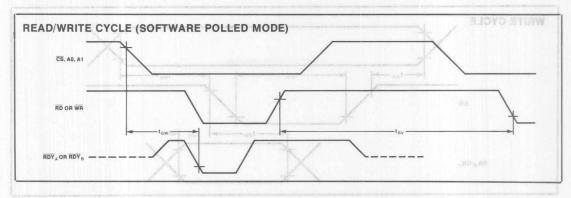
#### NOTES:

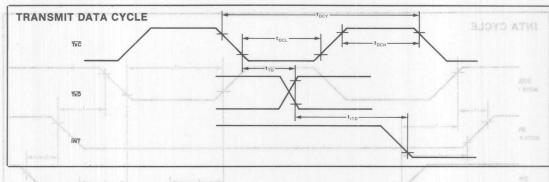
- 1. INTA signal acts as RD signal.
- 2. IPI signal acts as CS signal.

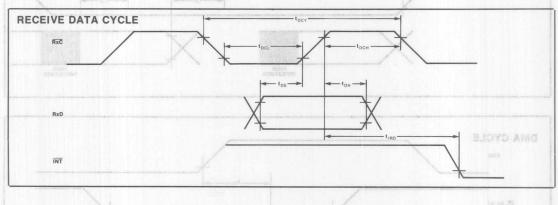
WAVEFORMS (Continued)

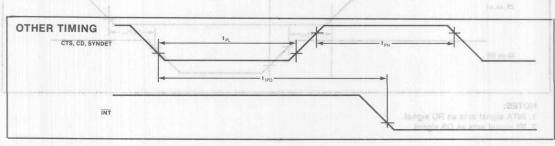


# **WAVEFORMS** (Continued)









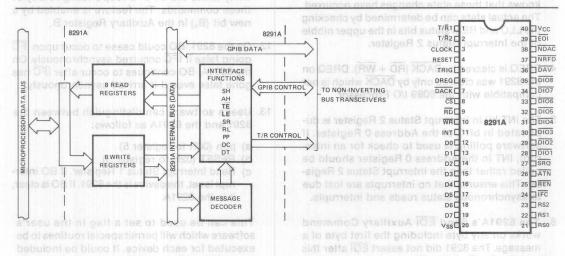


# 8291A FEATURES AND IMPROVEMENTATES. To avoid confusion between holdoff on DAV ver-

- Designed to Interface
  Microprocessors (e.g., 8048/49, 8051,
  8080/85, 8086/88) to an IEEE Standard
  488 Digital Interface Bus
- Programmable Data Transfer Rate
- Complete Source and Acceptor Handshake
- Complete Talker and Listener
   Functions with Extended Addressing
- Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local Functions
- Selectable Interrupts | bluos relications
- On-Chip Primary and Secondary Address Recognition
- Automatic Handling of Addressing and Handshake Protocol
- Provision for Software Implementation of Additional Features

- 1-8 MHz Clock Range and no at Aress and
- 16 Registers (8 Read, 8 Write), 2 for Data Transfer, the Rest for Interface Function Control, Status, etc.
- Non-Inverting Transceivers for Connection to the GPIB
- Provides Three Addressing Modes,
   Allowing the Chip to be Addressed
   Either as a Major or a Minor Talker/
   Listener with Primary or Secondary
   Addressing
- DMA Handshake Provision Allows for Bus Transfers without CPU
   Intervention
- Trigger Output Ping and of muter live
- On-Chip EOS (End of Sequence)
   Message Recognition Facilitates
   Handling of Multi-Byte Transfers

The 8291A is an enhanced version of the 8291 GPIB Talker/Listener designed to interface microprocessors to an IEEE Standard 488 Instrumentation Interface Bus. It implements all of the Standard's interface functions except for the controller. The controller function can be added with the 8292 GPIB Controller, and the 8293 GPIB Transceiver performs the electrical interface for Talker/Listener and Talker/Listener/Controller configurations.



as stubsoom noites! Figure 1. Block Diagram

owt no non agassam Figure 2. Pin Configuration



The 8291A is an improved design of the 8291 GPIB Talker/Listener. Most of the functions are identical to the 8291, and the pin configuration is unchanged.

The 8291A offers the following improvements to the

- 1. EOI is active with the data as a ninth data bit rather than as a control bit. This is to comply with some additions to the 1975 IEEE-488 Standard incorporated in the 1978 Standard.
- 2. The BO interrupt is not asserted until RFD is true. If the Controller asserts ATN synchronously, the data is guaranteed to be transmitted. If the Controller asserts ATN asynchronously, the SH (Source Handshake) will return to SIDS (Source Idle State), and the output data will be cleared. The, if ATN is released while the 8291A is addressed to talk, a new BO interrupt will be generated. This change fixes 8291 problems which caused data to be lost or repeated and a problem with the RQS bit (sometimes cannot be asserted while talking).
- 3. LLOC and REMC interrupts are setting flipflops rather than toggling flipflops in the interrupt backup register. This ensures that the CPU knows that these state changes have occurred. The actual state can be determined by checking the LLO and REM status bits in the upper nibble of the Interrupt Status 2 Register.
- 4. DREQ is cleared by DACK (RD + WR). DREQ on the 8291 was cleared only by DACK which is not compatible with the 8089 I/O Processor.
- 5. The INT bit in Interrupt Status 2 Register is duplicated in bit 7 of the Address 0 Register. If software polling is used to check for an interrupt, INT in the Address 0 Register should be polled rather than the Interrupt Status 2 Register. This ensures that no interrupts are lost due to asynchronous status reads and interrupts.
- 6. The 8291A's Send EOI Auxiliary Command works on any byte including the first byte of a message. The 8291 did not assert EOI after this command for a one byte message nor on two consecutive bytes.

- 8291A FEATURES AND IMPROVEMENTS 7. To avoid confusion between holdoff on DAV versus RFD if a device is readdressed from a talker to a listener role or vice-versa during a holdoff, the "Holdoff on Source Handshake" has been eliminated. Only "Holdoff on Acceptor Handshake" is available.
  - 8. The rsv local message is cleared automatically upon exit from SPAS if (APRS.STRS.SPAS) occurred. The automatic resetting of the bit after the serial poll is complete simplifies the service request software.
  - 9. The SPASC interrupt on the 8291 has been replaced by the SPC (Serial Poll Complete) interrupt on the 8291A. SPC interrupt is set on exit from SPAS if APRS.STRS.SPAS occurred, indicating that the controller has read the bus status byte after the 8291A requested service. The SPASC interrupt was ambiguous because a controller could enter SPAS and exit SPAS generating two SPASC interrupts without reading the serial poll status byte. The SPC interrupt also simplifies the CPU's software by eliminating the interrupt when the serial poll is half way done.
  - 10. The rtl Auxiliary Command in the 8291 has been replaced by Set and Clear rtl Commands in the 8291A. Using the new commands, the CPU has the flexibility to extend the length of local mode or leave it as a short pulse as in the 8291.
  - 11. A holdoff RFD on GET, SDC, and DCL feature has been added to prevent additional bus activity while the CPU is responding to any of these commands. The feature is enabled by a new bit (B4) in the Auxiliary Register B.
  - 12. On the 8291, BO could cease to occur upon IFC going false if IFC occurred asynchronously. On the 8291A, BO continues to occur after IFC has gone false even if it arrived asynchronously.
  - 13. User's software can distinguish between the 8291 and the 8291A as follows:
    - a) pon (00H to register 5)
    - b) RESET (02H to register 5)
    - c) Read Interrupt Status 1 Register. If BO interrupt is set, the device is the 8291. If BO is clear, it is the 8291A.

This can be used to set a flag in the user's software which will permit special routines to be executed for each device. It could be included as part of a normal initialization procedure as the first step after a chip reset.

Symbol	Pin No.	Туре	Name and Function
D <sub>0</sub> -D <sub>7</sub>	12–19	1/0	Data Bus Port: To be con- nected to microprocessor data bus.
RS <sub>0</sub> -RS <sub>2</sub>	21-23	the E0 poll. Postel (5V ± 1	Register Select: Inputs, to be connected to three non- multiplexed microproces- sor address bus lines. Select which of the 8 inter- nal read (write) registers will be read from (written into) with the execution of
CS langia 8t	of -0-6	Losos es poi dvits; U mort s should b	
RD	9	1	Read Strobe: When low with CS or DACK low, se- lected register contents are read.
WR	10	1	Write Strobe: When low with CS or DACK low, data is written into the selected register.
INT (INT)	11	0	Interrupt Request: To the microprocessor, set high for request and cleared when the appropriate register is accessed by the CPU. May be software configured to be active low.
DREQ	6	0	DMA Request: Normally low, set high to indicate byte output or byte input in DMA mode; reset by DACK.
DACK print reflori ortho0 a br	Standa		DMA Acknowledge: When low, resets DREQ and selects data in/data out register for DMA data transfer (actual transfer
	ed noit		Must be high if DMA is not used.
re GF GRAN handshak procedura request, an procedura	esing ervice	ata tra addre ering, s	pulse with 1 $\mu$ sec min.
CLOCK	3	no (fiui	External Clock: Input, used only for T, delay generator. May be any speed in 1-8 MHz range.

Symbol	Pin No.	Туре	Name and Function
RESET and control of the control of	t Line: on the on the on the on the		Reset Input: When high forces the device into an "idle" (initialization) mode The device will remain at "idle" until released by the microprocessor, with the "Immediate Execute pon" local message.
DIO <sub>1</sub> -DIO <sub>8</sub>	nd outpi		8-Bit GPIB Data Port: Used for bidirectional data byte transfer between 8291A and GPIB via non-inverting external line transceivers.
DAV	36	I/O	Data Valid: GPIB handshake control line. Indicates the availability and validity of information on the DIO <sub>1</sub> -DIO <sub>8</sub> and EOI lines.
NRFD	AMG REDURENTY LEAMONTS	I/O	Not Ready for Data: GPIB handshake control line. In- dicates the condition of readiness of device(s) con- nected to the bus to accept data.
NDAC	38	I/O	Not Data Accepted: GPIB handshake control line. In- dicates the condition of ac- ceptance of data by the device(s) connected to the bus.
ATN MARAMAD	26	1	Attention: GPIB command line. Specifies how data on DIO lines are to be interpreted.
IFC BOARA	24	3809	Interface Clear: GPIB command line. Places the interface functions in a known quiescent state.
	88-1978	dard 48 able 1 this st	Service Request: GPIB command line. Indicates the need for attention and requests an interruption of the current sequence of events on the GPIB.
REN Signaturi en Signaturi		s struct 3 refer the int te diag	Remote Enable: GPIB command line. Selects (in conjunction with other messages) remote or local control of the device.
EOI	39	000000	End or Identify: GPIB command line. Indicates the end of a multiple byte transfer sequence or, in conjunction with ATN, addresses the device during a polling sequence.

1-253 AFN-00229B



Table 1. Pin Description (Continued)

Symbol	Pin No.	Туре	Name and Function
When IRVI vice into an ation) mode. Ill remain at eased by the or, with the xecute pon"	the de initialization vice wantli rel rocess	forces "idle"   The de "idle"   microp	External Transceivers Control Line: Set high to indicate output data/ signals on the DIO, DIO, and DAV lines and input signals on the NRFD and NDAC lines (active source handshake). Set low to in-
ta Port: Used tal data byte veen 8291A con-inverting ransceivers.	rection er bett 18 via r	for bid transfe and GP	dicate input data/signals on the DIO <sub>1</sub> -DIO <sub>8</sub> and DAV lines and output signals on the NRFD and NDAC lines (active acceptor handshake).

Symbol	Pin No.	Туре	Name and Function
T/R2 <sub>ed of all toeseoongon</sub>	to mid		External Transceivers Control Line: Set to indicate output signals on the EOI line. Set low to indicate
pt: Inputs. to three nan- nicroproces-	nected n	be cont	expected input signal on the EOI line during parallel poll.
V <sub>cc 1</sub> 8 and 1			Positive Power Supply: (5V ±10%).
GND mo		P.S.	Circuit Ground Potential.

#### NOTE:

All signals on the 8291A pins are specified with positive logic. However, IEEE 488 specifies negative logic on its 16 signal lines. Thus, the data is inverted once from  $D_0-D_7$  to  $\overline{DIO}_0-\overline{DIO}_8$  and non-inverting bus transceivers should be used.

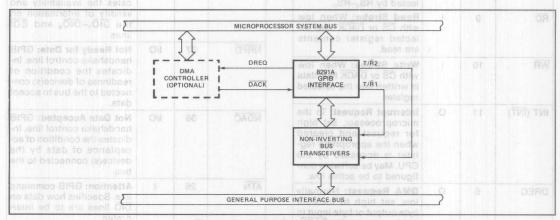


Figure 3. 8291A System Diagram

# THE GENERAL PURPOSE INTERFACE BUS (GPIB)

The General Purpose Interface Bus (GPIB) is defined in the IEEE Standard 488-1978 "Digital Interface for Programmable Instrumentation." Although a knowledge of this standard is assumed, Figure 4 provides the bus structure for quick reference. Also, Tables 2 and 3 reference the interface state mnemonics and the interface messages respectively. Modified state diagrams for the 8291A are presented in Appendix A.

#### **General Description**

The 8291A is a microprocessor-controlled device designed to interface microprocessors, e.g., 8048/49, 8051, 8080/85, 8086/88 to the GPIB. It implements all of the interface functions defined in the

IEEE-488 Standard except for the controller function. If an implementation of the Standard's Controller is desired, it can be connected with an Intel® 8292 to form a complete interface.

The 8291A handles communication between a microprocessor-controlled device and the GPIB. Its capabilities include data transfer, handshake protocol, talker/listener addressing procedures, device clearing and triggering, service request, and both serial and parallel polling. In most procedures, it does not disturb the microprocessor unless a byte has arrived (input buffer full) or has to be sent out (output buffer empty).

The 8291A architecture includes 16 registers. Eight of these registers may be written into by the microprocessor. The other eight registers may be read by the microprocessor. One each of these read and



write registers is for direct data transfers. The rest of the write registers control the various features of the chip, while the rest of the read registers provide the microprocessor with a monitor of GPIB states, various bus conditions, and device conditions.

# **GPIB Addressing**

Each device connected to the GPIB must have at least one address whereby the controller device in charge of the bus can configure it to talk, listen, or send status. An 8291A implementation of the GPIB offers the user three alternative addressing modes for which the device can be initialized for each application. The first of these modes allows for the device to have two separate primary addresses. The second mode allows the user to implement a single talker/listener with a two byte address (primary address + secondary address). The third mode again allows for two distinct addresses but in this instance, they can each have a ten-bit address (5 low-order bits of each of two bytes). However, this mode requires that the secondary addresses be passed to the microprocessor for verification. These three addressing schemes are described in more detail in the discussion of the Address Registers.

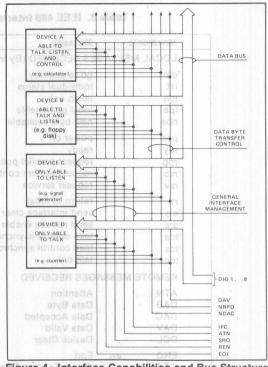


Figure 4. Interface Capabilities and Bus Structure

Table 2. IEEE 488 Interface State Mnemonics

Mnemonic	State Represented	Mnemonic	State Represented
ACDS ACRS AIDS ANRS APRS AWNS	Accept Data State Acceptor Ready State Acceptor Idle State Acceptor Not Ready State Affirmative Poll Response State Acceptor Wait for New Cycle State	PACS PPAS PPIS PPSS PUCS	Parallel Poll Addressed to Configure State Parallel Poll Active State Parallel Poll Idle State Parallel Poll Standby State Parallel Poll Unaddressed to Configure State
CACS	Controller Active State	REMS RWLS	Remote State Remote With Lockout State
CADS CAWS CIDS CPPS CPWS CSBS CSNS CSRS CSWS CTRS	Controller Addressed State Controller Active Wait State Controller Idle State Controller Parallel Poll State Controller Parallel Poll Wait State Controller Standby State Controller Service Not Requested State Controller Service Requested State Controller Synchronous Wait State Controller Transfer State	SACS SDYS SGNS SIAS	System Control Active State Source Delay State Source Generate State System Control Interface Clear Active State Source Idle State System Control Interface Clear Idle State System Control Interface Clear Not Active State Source Idle Wait State System Control Not Active State Serial Poll Active State
DCAS DCIS DTAS DTIS	Device Clear Active State Device Clear Idle State Device Trigger Active State Device Trigger Idle State	SPIS SPMS SRAS SRIS	Serial Poll Idle State Serial Poll Idle State Serial Poll Mode State System Control Remote Enable Active State System Control Remote Enable Idle State
LACS LADS LIDS LOCS LPAS	Listener Active State Listener Addressed State Listener Idle State Local State Listener Primary Addressed State	SRNS SRQS STRS SWNS	System Control Remote Enable Not Active State Service Request State Source Transfer State Source Wait for New Cycle State Talker Active State
LPIS LWLS NPRS	Listener Primary Idle State Local With Lockout State Negative Poll Response State	TADS TIDS TPIS	Talker Addressed State Talker Idle State Talker Primary Idle State

<sup>\*</sup>The Controller function is implemented on the Intel® 8292.



Table 3. IEEE 488 Interface Message Reference List Ioning a setziger with with

	Mnemonic	Message	-ingv an	Interface Function(s)	aproposate
AC J	LOCAL MESSA	GES RECEIVED (By Inter	face Fund	onditions, and device conditionit	as bus en
	¹ats			C	0000
	ist	go to standby individual status		DD	
	lon	listen only		L.LE gnisasib	BRIB AN
	Ipe	local poll enable		PP	
	nba	new byte available	have at		ach devi
TAG		Yeard beginning	ni eoive		
ART CON	pon	power on	sten, or	SH,AH,T,TE,L,LE,SR,RL,PP,C	harde of
	rdy	ready		s. An 8291A implementation on	utate has
	¹rpp	request parallel poll		user three alternative addressing	arit mait
	¹rsc	request system control		ne device can be initialized for age	
	rsv	request service			
BMRD RBTM	rtl	return to local	aniven:	first of these modes allows for A	en nous
DAMAN	¹sic	send interface clear		separate primary addresses. To	
	¹sre	send remote enable		ows the user to implementate	
1-01	¹tca .			ner with a two byte address (pon	
	¹tcs	take control synchronol	usly Da 9	condary address). The third, HAd	ress + se
	ton	talk only	stance,	wo distinct addresses but in TiçTin	Hows for t
	REMOTE MESS	SAGES RECEIVED	w-order	ach have a ten-bit address (5 lov	hey can b
**************************************			-er abo	h of two bytes). However, this m	its of eac
ad	ATN	Attention	esed to	SH,AH,T,TE,L,LE,PP,C	uires that
Ris	DAB	Data Byte		(Via L, LE)	
	DAC	Data Accepted		20	
TA -	DAV	Data Valid		sion of the Address Register Od	
1.5	DCL	Device Clear			dracin bil
38				DC	
03	END	End		(via L, LE)	
03	END GET::///dags0	End Group Execute Trigger		(via L, LE) DT	
03	END GET /// dags O GTL	End Group Execute Trigger Go to Local		(via L, LE) DT	
03	END GET HI dage O GTL IDY	End Group Execute Trigger Go to Local Identify	ini 884 3	(via L, LE) DT RL L,LE,PP	
euß ba	END GET HIGHOO GTL IDY IFC	End Group Execute Trigger Go to Local Identify Interface Clear	foi 884 S	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C	omomenM
03	END GET Hidsop GTL IDY IFC LLO **SENDEA**	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout	E 488 int	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C Defines a go A et al 2 RL  4582 2008 2009 A	Magnonic
e auß ba	END GET Hidage 3 GTL IDY IFC LLO MLA ENDA H MA	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address	Ini 884 3	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C Defines ange 9 state RL L,LE,RL,T,TE State Vision A supposed	Mnemonic ACDS ACRS
e auß ba	END GET HIGH SO OF THE PROPERTY OF THE PROPERT	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address	5 488 Int	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C  RL L,LE,RL,T,TE Example State L,LE,RL,T,TE TE,LE,RL TE	Magnonic
e auß ba	END GET	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address		(via L, LE) DT RL L,LE,PP 10.51 T,TE,L,LE,C befressige 4 stat2 RL L,LE,RL,T,TE 10.52 years are a company of the	Moentonic ACDS ACRS ALDS
es euS ba	END GET HIGHEST GTL IDY IFC LLO MLA MSA MSA MTA	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address		(via L, LE) DT RL L,LE,PP T,TE,L,LE,C  RL L,LE,RL,T,TE Example State L,LE,RL,T,TE TE,LE,RL TE	Mnemonic ACDS ACRS ALDS ANRS
es euS ba	END GET IDY IFC LLO MLA MSA MTA OSA	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addre		(via L, LE) DT RL L,LE,PP fine T T,TE,L,LE,C befressinged etsiz  RL L,LE,RL atsiz state appear Acceptor lots State at State and state at State and state at State at State and state at State and state at State a	Minemonic ACDS ACRS ALDS ANRS ANRS
es euS ba	END GET IDY IFC LLO MLA MSA MTA OSA	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addres Other Talk Address	ess *_	(via L, LE) DT RL L,LE,PP fine T T,TE,L,LE,C befressinged etsiz  RL L,LE,RL atsiz state appear Acceptor lots State at State and state at State and state at State at State and state at State and state at State a	Mnemonic ACDS ACRS AIDS ANRS APRS APRS AVNS
configure Standard	END GET GTL IDY IFC LLO MLA MSA MTA OSA OTA	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addre	ess *_	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C DefinesangeR etst2 RL L,LE,RL,T,TE etst2 year and etst2 TE,LE,RL etst2 year and etst2 TE,LE,RL etst2 year and etst2 TE,LE,RL etst2 year and etst2 T,TE,L,LE especial etst2 T, TE TE,LE,RL etst2 year and etst2 T, TE TE,LE,RL etst2 year and etst2 T, TE TE,LE,RL etst2 year and etst2 T, TE TE,LE,PP etst2 year and etst2 T	Mnemon of ACDS ACDS ALDS ANAS ANAS AWNS CADS CADS CADS
to Bus Standard Stand	END GET IDY IFC LLO MLA MSA MTA OSA OTA PCG	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addres Other Talk Address Primary Command Grou	ess *_	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C Define angle state Acceptor Ready State L,LE,RL,T,TE State State TE,LE,RL state State TE,LE,RL state State T,TE,L,LE seasonable T,TE,L,LE seasonable T,TE state State T,TE TE,LE,PP state State PP State S	Mnemonic ACDS ACRS AURS ANRS APRS AWNS CAOS CAOS CAOS
configure State  Configure State  Configure	END GET House of GTL IDY IFC LLO MLA MSA MTA OSA OTA PCG 2PPC	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addre Other Talk Address Primary Command Grouparallel Poll Configure	ess *_	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C Defines Size Accept Data Size L,LE,RL,T,TE L,LE,RL Size Acceptor Not Ready Size T,T,E,L,LE, Data Size T,T,E,L,LE, Data Size T,T,E,L,LE, Data Size T,TE Controller Active Size PP PP Reserved Wait Size PP PP Reserved Size PP PP Size Data Size PD Data Size	Mnemonic ACDS ACRS ANRS ANRS ANRS ANRS CACS CADS CADS CADS CADS CAPS
configure State  Configure  ar Active 6	END GET IDY IFC LLO MLA MSA MTA OSA OTA PCG 2PPC 2[PPD] 2[PPE]	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addres Primary Command Group Parallel Poll Configure Parallel Poll Disable Parallel Poll Enable	ess up	(via L, LE) DT RL L,LE,PP 1997 T,TE,L,LE,C befreeinge stat2 RL L,LE,RL,T,TE stat2 stat0 stat0 stat0 TE,LE,RL,T,TE stat2 stat0 stat0 stat0 stat0 TE,LE,RL stat0 stat0 stat0 stat0 stat0 T,TE,L,LE stat0 stat0 stat0 stat0 stat0 T, TE stat0	Mineration of ACDS ACRS ANDS ANAS ANAS AVENS AVENS CACS CACS CAPS COPPS COPPS
configure Strain Configure Configure Strain Active Strain Ide Sta	END GET IDY IFC LLO MLA MSA MTA OSA OTA PCG 2PPC 2(PPD) 2(PPE) 1PPR MEET GET GET GET GET GET GET GET GET GET	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addres Other Talk Address Primary Command Group Parallel Poll Configure Parallel Poll Disable Parallel Poll Enable Parallel Poll Response N	ess *	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C Defresange A stat2 RL Acceptor Basic State Acceptor Acceptor Basic State Acceptor TE,LE,RL,T,TE State Acceptor Basic State TE,LE,RL,E series State TE,LE,RL series State TT,T,L,LE series State TT,TE TE,L,LE series State TT, TE TE,LE,PP state State TT, TE TE,LE,PP state State TT, TE TE,LE,PP state T	Mnemon of ACDS ACDS ANDS ANDS AVUS AVUS CADS CADS COADS COAWS COADS COAWS COAWS COEPS ACDS ACDS ACDS ACDS ACDS ACDS ACDS ACD
nd Bue Standard Stand	END GET IDY IFC LLO MLA MSA MTA OSA OTA PCG 2PPC 2(PPD) 2(PPE) 1PPR 2PPU	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addre Other Talk Address Primary Command Group Parallel Poll Configure Parallel Poll Disable Parallel Poll Enable Parallel Poll Response N Parallel Poll Unconfigure	ess *	(via L, LE) DT RL L,LE,PP T,TE,L,LE,C Defines and expense and state L,LE,RL,T,TE L,LE,RL,T,TE TE,LE,RL,T,TE TE,LE,PI TE,TE TE,TE TE,TE TE,TE TE,TE TE,TE TE,TE TE T	Mineration of ACDS ACRS ANDS ANAS ANAS AVENS AVENS CACS CACS CAPS COPPS COPPS
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nd Rus Stanfigure Stan	END GET IDY IFC LLO MLA MSA MTA OSA OTA PCG 2PPC 2[PPD] 2[PPE] 1PPR 2PPU REN RFD RQS [SDC] SPD	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Address Primary Command Group Parallel Poll Configure Parallel Poll Disable Parallel Poll Response Narallel Poll Response Narallel Poll Unconfigure Remote Enable Ready for Data Request Service Select Device Clear Serial Poll Disable	ess *	(via L, LE) DT RL L,LE,PP 1997 T,TE,L,LE,C befreeinger stat2 RL L,LE,RL,T,TE stat2 deep Accorded TE,LE,RL,T,TE stat2 deep Accorded TE,LE,RL 1,T,TE stat2 deep Accorded T,TE,L,LE stat2 deep Accorded T,TE,L,LE stat2 deep Accorded T,TE deep Accorded Accorded T,TE deep Accorded Accorded T,TE deep Accorded Accorded Accorded T,TE deep Accorded Accord	Mnemon of ACDS ACDS ACDS ACDS ACDS ACDS CAOS CAOS CAOS COPES COPES COSTAS COSTA
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configure Standard St	END GET GTL IDY IFC LLO MLA MSA MTA OSA OTA PCG 2PPC 2[PPD] 2[PPE] 1PPR 2PPU REN RFD RFD RQS [SDC] SPD SPE 1SQR	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addres Other Talk Address Primary Command Group Parallel Poll Configure Parallel Poll Disable Parallel Poll Enable Parallel Poll Enable Parallel Poll Unconfigur Remote Enable Ready for Data Request Service Select Device Clear Serial Poll Enable Service Request	ess *	(via L, LE)  DT  RL  L,LE,PP  T,TE,L,LE,C  RL  L,LE,RL,T,TE  L,LE,RL,T,TE  Second Accept Acce	Mnemon of ACDS ACDS ACDS ACDS ACDS ACDS CAOS CAOS CAOS COPES COPES COSTAS COSTA
configure Standard St	END GET IDY IFC LLO MLA MSA OSA OTA PCG PPC PPPD PPRN PPPU REN REN RFD RQS [SDC] SPD SPE	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Address Primary Command Group Parallel Poll Configure Parallel Poll Disable Parallel Poll Enable Parallel Poll Unconfigur Remote Enable Ready for Data Request Service Select Device Clear Serial Poll Disable Serial Poll Enable	ess *	(via L, LE)  DT RL  L,LE,PP T,TE,L,LE,C  RL  Acceptor Rusely State  Acceptor Not Ready State  Acceptor Work State  Acceptor Work State  Acceptor Work State  Acceptor Work State  T,TE,L,RE asposed State  Acceptor Work State  Acceptor Work State  T, TE  TE,LE,PP State  Controller Active State  PP  Acceptor Work State  Controller Active State  Controller Translet State  Controller	Mnemonic ACDS ACDS ALDS ALDS ALDS ALDS ALDS ALDS ALDS AL
nd Rus Start Start Start Start I Active Start I Act	END GET GTL IDY IFC LLO MLA MSA MTA OSA OTA PCG 2PPC 2[PPD] 2[PPE] 1PPR 2PPU REN RFD RFD RQS [SDC] SPD SPE 1SQR	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Addres Other Talk Address Primary Command Group Parallel Poll Configure Parallel Poll Disable Parallel Poll Enable Parallel Poll Enable Parallel Poll Unconfigur Remote Enable Ready for Data Request Service Select Device Clear Serial Poll Enable Service Request	ess *	(via L, LE)  DT RL  L,LE,PP T,TE,L,LE,C  RL  Acceptor Ready State L,LE,RL,T,TE  Jest State L,LE,RL,LE  JEST STATE L,LE  JEST STATE L,LE  JEST STATE L,LE  JEST STATE L,LE  JEST STATE L	Mnemon of ACDS ACDS ACDS ACDS ACDS ACMS CADS CADS COPES COPE
nd Rus Start Start Start Start I Active Start I Act	END GET IDY IFC LLO MLA MSA OSA OTA PCG PPC (PPD) (PPR) PPR) PPU REN RFD RQS [SDC] SPD SPE SQR STB	End Group Execute Trigger Go to Local Identify Interface Clear Local Lockout My Listen Address My Secondary Address My Talk Address Other Secondary Address Primary Command Group Parallel Poll Configure Parallel Poll Disable Parallel Poll Enable Parallel Poll Unconfigur Remote Enable Ready for Data Request Service Select Device Clear Serial Poll Enable Service Request Status Byte	ess *	(via L, LE) DT RL L,LE,PP INST T,TE,L,LE,C befreesing 9 stat2  RL L,LE,RL,T,TE stat2 visual stat0 stat	Mnemonic ACRS ACRS AND

#### NOTE:

- 1. These messages are handled only by Intel's 8292.
- 2. Undefined commands which may be passed to the microprocessor.



register, The RFD (Ready for Data) message (Cont'd) . Self-upt Registers IEEE 488 Interface Message Reference List 1 bevomes allered and little salst

		Mnemonic	Message	fatically	Interface F	unction(	(8) 1 881	telam	
()	号t) f	REMOTE MESSA	AGES SENT	er A), the	iry Registi comman	silixuA e	es) eb	om ti	ebler
MC ADSC		DAB OPE MAR DAC DAV ATE THUR DCL	Attention Data Byte Data Accepted Data Valid Device Clear	this way, r an over	C (via T, TE AH SH (via C)	se the f			
8 08 (V	AR Wr) r	END DE THE STATE OF THE STATE O	End Group Execute Trigg Go to Local Identify Interface Clear	RB. After vritten to	(via T) (via C) (via C) C	data or ved and	raceiv		regis ntern
EMC ADS	IR O	LLO MLA or [MLA]	Local Lockout My Listen Address		(via C) (via C)	bem eld			trii O
(1	WS) S	MSA or [MSA] MTA or [MTA] OSA	My Secondary Address Other Secondary Address	A (wileoft	(via C)		this w		n AM
() ADS-0 AD		MTA or [MTA]	My Talk Address Other Secondary Add	dress Group	(via C) (via C) (via C) (via C) (via C) (via C) (via C) (via C)	ili happe ister do	this wi r Regi		MA n the D
DA 0-SCA	3-0 A	MTA or [MTA] OSA OTA A A A A A A A A A A A A A A A A A A	My Talk Address Other Secondary Address Primary Command G Parallel Poll Configu Parallel Poll Disable Parallel Poll Enable Parallel Poll Respons Parallel Poll Unconfigu Remote Enable	dress Group re	(via C) (via C) (via C) (via C) (via C) (via C) (via C) (via C)	ili happe ister do	this wi Regi Data (		MA n the D
DA 0-SCA	3-0 A	MTA or [MTA] OSA OTA ADA D-BOA PCG PPC [PPD] [PPE] PPRN PPU REN RFD	My Talk Address Other Secondary Address Primary Command G Parallel Poll Configu Parallel Poll Disable Parallel Poll Enable Parallel Poll Respons Parallel Poll Unconfigu Remote Enable Ready for Data	dress Group re	(via C) (via C) (via C) (via C) (via C) (via C) (via C) (via C) PP (via C) C AH T, TE (via C) (via C)	itt happe ister do Jut Reg	this wi Regi Data (		MA n the D
ADS-OLAD	STER	MTA or MTA OSA OTA ADA DADA PCG PPC [PPD] [PPE] PPRN PPU REN RED RQS [SDC] SPD	My Talk Address Other Secondary Address Other Talk Address Primary Command G Parallel Poll Configu Parallel Poll Disable Parallel Poll Enable Parallel Poll Respons Parallel Poll Unconfigu Remote Enable Ready for Data Request Service Selected Device Clea Serial Poll Disable	dress Group re	(via C) (via C) (via C) (via C) (via C) (via C) (via C) (via C) (via C) C AH T, TE (via C) (via C)	ili happe ster do Out Reg ilsters ora pr	this wi n Regi Data C		m AMin G ethe Hook in

3. All Controller messages must be sent via Intel's 8292.

# 8291A Registers

A bit-by-bit map of the 16 registers on the 8291A is presented in Figure 5. A more detailed explanation of each of these registers and their functions follows. The access of these registers by the microprocessor is accomplished by using the CS, RD, WR, and RSo-RS2 pins.

Register	CS	RD	WR	RS <sub>0</sub> -RS <sub>2</sub>	
All Read Registers	0	0	. 1	CCC	
All Write Registers	0	1	0	CCC	
High Impedance	1	d	d	ddd	

# Data Registers

DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0

DATA-IN REGISTER (OR)

DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0

DATA-OUT REGISTER (0W)

The Data-In Register is used to move data from the GPIB to the microprocessor or to memory when the 8291A is addressed to listen. Incoming information is separately latched by this register, and its contents are not destroyed by a write to the data-out



register. The RFD (Ready for Data) message is held false until the byte is removed from the data in register, either by the microprocessor or by DMA. The 8291A then completes the handshake automatically. In RFD holdoff mode (see Auxiliary Register A), the handshake is not finished until a command is sent telling the 8291A to release the holdoff. In this way, the same byte may be read seveal times, or an over anxious talker may be held off until all available data has been processed.

When the 8291A is addressed to talk, it uses the data-out register to move data onto the GPIB. After the BO interrupt is received and a byte is written to this register, the 8291A initiates and completes the handshake while sending the byte out over the bus. In the BO interrupt disable mode, the user should wait until BO is active before writing to the register. (In the DMA mode, this will happen automatically.) A read of the Data-In Register does not destroy the information in the Data-Out Register.

# Interrupt Registers

CPT APT GET END DEC ERR BO BI

INTERRUPT STATUS 1 (1R)

INT SPAS LLO REM SPC LLOC REMC ADSC

INTERRUPT STATUS 2 (2R)

CPT APT GET END DEC ERR BO BI

INTERRUPT ENABLE 1 (1W)

0 0 DMAO DMAI SPC LLOC REMC ADSC

INTERRUPT ENABLE 2 (2W)

INT DT0 DL0 AD5-0 AD4-0 AD3-0 AD2-0 AD1-0

ADDRESS 0 REGISTER

Figure 5. 8291A Registers

						-			_		455							
		RE	AD REG	GISTER	S	HA I, TE		REGIST				Pead		WRITE	REGIS	STERS		
								RS2		BS0					ISDC			
DI7	D16	DI5	DI4	DI3	DI2	DI1	DIO	0		sids0			D05	D04	D03	D02	D01	D00
			DA	ATA IN	(37	FR Via T.					ce Rei			DAT	га оит			
CPT	APT	GET	END	DEC	ERR	ВО	ВІ	0	0	10	CPT	APT	GET	END	DEC	ERR	во	ВІ
		IN	TERRU	PT STA	TUS 1	U siv					nex	Units	INT	ERRUP	TENA	BLE 1		
INT	SPAS	LLO	REM	SPC	LLOC	REMC	ADSC	0.5858	1	oini oiv	100 8 90	021	DMAC	DMAI	SPC	LLOC	REMC	ADS
1		IN-	TERRU	PT STA	TUS 2								INTE	RRUP	ΓENAE	BLE 2		
S8	SRQS	\$6	S5	S4	S3	S2	S1	0	1	1	S8	rsv	S6	S5	S4	S3	S2	S1
	na I k			OLL ST		n l ain	710				e 829	dt no		ERIAL			m tid-	vcl-1
ton	lon	EOI	LPAS	TPAS		TA	MJMN	1	0		то			100				201
		(80)	ADDRE	SS STA	TUS	TAG					etions			ADDR				
CPT7	CPT6	CPT5	CPT4	СРТ3	CPT2	CPT1	CPTO	1	0	18,	CNT2	CNT1	CNTO	COM4	сомз	COM2	COM1	COM
		COMN	/AND P	ASS TH	ROUG	HTAG								AUX	MODE	RSe-I	and,	HW
INT	DT0	DLO		AD4-0			AD1-0	1	1	0	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
											dm-08	191 2	480 (	ADDI	RESS 0	/1	103	E156
								BESTA	1	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	ECO
oo si	and i	ster.	ADD	DRESS 1	berk evenste			is sep			bhh		0 5	b	EOS	gister		



The 8291A can be configured to generate an interrupt to the microprocessor upon the occurrence of any of 12 conditions or events on the GPIB. Upon receipt of an interrupt, the microprocessor must read the Interrupt Status Registers to determine which event has occurred, and then execute the appropriate service routine (if necessary). Each of the 12 interrupt status bits has a matching enable bit in the interrupt enable registers. These enable bits are used to select the events that will cause the INT pin to be asserted. Writing a logic "1" into any of these bits enables the corresponding interrupt status bits to generate an interrupt. Bits in the Interrupt Status Registers are set regardless of the states of the enable bits. The Interrupt Status Registers are then cleared upon being read or when a local pon-(power-on) message is executed. If an event occurs while one of the Interrupt Status Registers is being read, the event is held until after its register is cleared and then placed in the register.

register reflects the logic levels present on the data

The mnemonics for each of the bits in these registers and a brief description of their respective functions appears in Table 4. This tables also indicates how each of the interrupt bits is set.

NOTE: The INT bit in the Address 0 Register is a duplicate of the INT bit in the Interrupt Status 2 Register. It is only a status bit. It does not generate interrupts and thus does not have a corresponding enable bit.

The BO and BI interrupts enable the user to perform data transfer cycles. BO indicates that a data byte should be written to the Data Out Register. It is set by TACS · (SWNS + SGNS) · RFD. It is reset when the data byte is written, ATN is asserted, or the 8291A exits TACS. Data should never be written to the Data Out Register before BO is set. Similarly, BI is set when an input byte is accepted into the 8291A and reset when the microprocessor reads the Data In Register. BO and BI are also reset by pon (power-on local message) and by a read of the Interrupt

the sandshake until hold off the handshake until

is registor is read.	(1)	he user must define a known state to which a
Indicates Undefined Commands	CPT	An undefined command has been received.
Set by (TPAS + LPAS) •SCG•ACDS•MODE 3	APT	A secondary address must be passed through to the microprocessor for recognition.
SATO yet by DTAS	GET	A group execute trigger has occurred.
ent yd beidene ti hetele Set by (EOS + EOI) LACS	END	An EOS or EOI message has been received.
quine mi na seuso lliw stid eldane Set by DCAS	DEC	Device Clear Active State has occurred.
Set by TACS•nba•DAC•RFD	ERR	Interface error has occurred; no listeners are active.
TACS•(SWNS+SGNS)	ВО	A byte should be output, am fid formetni QME en
SCOA+SOAL vet testing in LOS or TIDS or MUMN Bit 1 REMC change in LOCS or REMS	BI 0	a byte has been input. It am a fact the base A byte has been input. The bit will be set when the 8201A is a
Shows status of the INT pin	INT	otive listener (LACS) and either EOS (provided to an eos seceived feature is enabled in the Aux
The device has been enabled for a serial poll	SPAS	These are status only. They will <u>not</u> generate
state. It is a state of case of a first state of the stat	LLO	interrupts, nor do they have corresponding mask bits.
The device is in a remote state. The corresponding the corresponding (REMS+RWLS) as taken place the corresponding to the corresponding	REM	terrupt will be generated when a true input stepted on EOI.
atus bit (bits 3-5 may be read to determine what	të.	
SPAS → SPAS if APRS.STRS.SPAS was true	SPC	Serial Poll Complete interrupt.
OJJ ON OJJ be read. The SPC interrupt (bit 3 in	LLOC	Local lock out change interrupt. ATC 1801 196180
(Isoul stome 2) is set upon exit from SPAS if	REMC	Remote/Local change interrupt.
editisht satsoloni doldw Addressed Unaddressed	ADSC	Address status change interrupt.1
		us, the basic operation of device trioner may be critical microprocessors.
to a facility of the property of the facility of the property of the facility of the property of the facility		



Status 1 Register. However, if it is so desired, data transfer cycles may be performed without reading the Interrupt Status 1 Register if all interrupts except for BO or BI are disabled; BO and BI will automatically reset after each byte is transferred.

If the 8291A is used in the interrupt mode, the INT and DREQ pins can be dedicated to data input and output interrupts respectively by enabling BI and DMAO, provided that no other interrupts are enabled. This eliminates the need to read the interrupt status registers if a byte is received or transmitted.

The ERR bit is set to indicate the bus error condition when the 8291A is an active talker and tries to send a byte to the GPIB, but there are no active listeners (e.g., all devices on the GPIB are in AIDS). The logical equivalent of (nba  $\cdot$  TACS  $\cdot$  DAC  $\cdot$  RFD) will set this bit.

The DEC bit is set whenever DCAS has occurred. The user must define a known state to which all device functions will return in DCAS. Typically this state will be a power-on state. However, the state of the device functions at DCAS is at the designer's discretion. It should be noted that DCAS has no effect on the interface functions which are returned to a known state by the IFC (interface clear) message or the pon local message.

The END interrupt bit may be used by the microprocessor to detect that a multi-byte transfer has been completed. The bit will be set when the 8291A is an active listener (LACS) and either EOS (provided the End on EOS Received feature is enabled in the Auxiliary Register A) or EOI is received. EOS will generate an interrupt when the byte in the Data In Register matches the byte in the EOS register. Otherwise the interrupt will be generated when a true input is detected on EOI.

The GET interrupt bit is used by the microprocessor to detect that DTAS has occurred. It is set by the 8291A when the GET message is received while it is addressed to listen. The TRIG output pin of the 8291A fires when the GET message is received. Thus, the basic operation of device trigger may be started without microprocessor software intervention.

The APT interrupt bit indicates to the processor that a secondary address is available in the CPT register for validation. This interrupt will only occur if Mode 3 addressing is in effect. (Refer to the section on addressing.) In Mode 2, secondary addresses will be recognized automatically on the 8291A. They will be ignored in Mode 1.

The CPT interrupt bit flags the occurrence of an undefined command and of all secondary commands following an undefined command. The Command Pass Through feature is enabled by the B0 bit of Auxiliary Register B. Any message not decoded by the 8291A (not included in the state diagrams in Appendix B) becomes an undefined command. Note that any addressed command is automatically ignored when the 8291A is not addressed.

Undefined commands are read by the CPU from the Command Pass Through register of the 8291A. This register reflects the logic levels present on the data lines at the time it is read. If the CPT feature is enabled, the 8291A will hold off the handshake until this register is read.

An especially useful feature of the 8291A is its ability to generate interrupts from state transitions in the interface functions. In particular, the lower 3 bits of the Interrupt Status 2 Register, if enabled by the corresponding enable bits, will cause an interrupt upon changes in the following states as defined in the IEEE 488 Standard.

Bit 0 ADSC change in LIDS or TIDS or MJMN Bit 1 REMC change in LOCS or REMS Bit 2 LLOC change in LWLS or RWLS

The upper 4 bits of the Interrupt Status 2 Register are available to the processor as status bits. Thus, if one of the bits 0–2 generates an interrupt indicating a state change has taken place, the corresponding status bit (bits 3–5 may be read to determine what the new state is. To determine the nature of a change in addressed status (bit 0) the Address Status Register is available to be read. The SPC interrupt (bit 3 in Interrupt Status 2) is set upon exit from SPAS if APRS.STRS.SPAS occurred which indicates that the GPIB controller has read the bus serial poll status byte after the 8291A requested service (asserted SRQ). The SPC interrupt occurs once after the controller reads the status byte if service was requested.

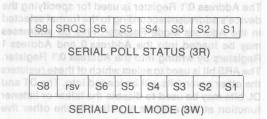


The controller may read the status byte later, and the byte will contain the last status the 8291A's CPU wrote to the Serial Poll Mode Register, but the SRQS bit will not be set and no interrupt will be generated. Finally, bit 7 monitors the state of the 8291A INT pin. Logically, it is an OR of all enabled interrupt status bits. One should note that bits 3–6 of the Interrupt Status 2 Register do not generate interrupts, but are available only to be read as status bits by the processor. Bit 7 in Interrupt Status 2 is duplicated in Address 0 Register, and the latter should be used when polling for interrupts to avoid losing one of the interrupts in Interrupt Status 2 Register.

Bits 4 and 5 (DMAI, DMAO) of the Interrupt Mask 2 Register are available to enable direct data transfers between memory and the GPIB; DMAI (DMA in) enables the DREQ (DMA request) pin of the 8291A to be asserted upon the occurrence of BI. Similarly, DMAO (DMA out) enables the DREQ pin to be asserted upon the occurrence of BO. One might note that the DREQ pin may be used as a second interrupt output pin, monitoring BI and/or BO and enabled by DMAI and DMAO. One should note that the DREQ pin is not affected by a read of the Interrupt Status 1 Register. It is reset whenever a byte is written to the Data Out Register or read from the Data In Register.

To ensure that an interrupt status bit will not be cleared without being read, and will not remain uncleared after being read, the 8291A implements a special interrupt handling procedure. When an enabled interrupt bit is set in either of the Interrupt Status Registers, the input of the registers are blocked until the set bit is read and reset by the microprocessor. Thus, potential problems arise when interrupt status changes while the register is being blocked. However, the 8291A stores all new interrupts in a temporary register and transfers them to the appropriate Interrupt Status Register after the interrupt has been reset. This transfer takes place only if the corresponding bits were read as zeroes.

### **Serial Poll Registers**



The Serial Poll Mode Register determines the status byte that the 8291A sends out on the GPIB data lines when it receives the SPE (Serial Poll Enable) message. Bit 6 of this register is reserved for the rsv (request service) local message. Setting this bit to 1 causes the 8291A to assert its SRQ line, indicating its need for attention from the controller-in-charge of the GPIB. The other bits of this register are available for sending status information over the GPIB. Sometime after the microprocessor initiates a request for service by setting bit 6, the controller of the GPIB sends the SPE message and then addresses the 8291A to talk. At this point, one byte of status is returned by the 8291A via the Serial Poll Mode Register. After the status byte is read by the controller, rsv is automatically cleared by the 8291A and an SPC interrupt is generated. The CPU may request service again by writing another byte to the Serial Poll Mode Register with the rsv bit set. If the controller performs a serial poll when the rsv bit is clear, the last status byte written will be read, but the SRQ line will not be driven by the 8291A and the SRQS bit will be clear in the status byte.

The Serial Poll Status Register is available for reading the status byte in the Serial Poll Mode Register. The processor may check the status of a request for service by polling bit 6 of this register, which corresponds to SRQS (Service Request State). When a Serial Poll is conducted and the controller-incharge reads the status byte, the SRQS bit is cleared. The  $\overline{\rm SRQ}$  line and the rsv bit are tied together.

by the microprocessor when Mode 3 is used. W

## Address Registers toba viabnoosa IIA leasabba

ton	lon	EOI	LPAS	TPAS	LA.	TA	MJMN
lisva Ilsva	erere te is	AD	DRESS	STAT	US (4F	io integ	
INT	DT0	DLO	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
o en bolv	rite o	w bas lixu#	ADDR	ESS 0	(6R)	iust rei swing	n soeer
Χ	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
see	nbbs	dary	ADDR	ESS 1	(7R) a	iliqmi I	10.071
ТО	LO	0	1.000	00.00	0 e	ADM1	ADM0
			DDRES	S MOD		,	
7	T		AD5			100000	the second



The Address Mode Register is used to select one of the five modes of addressing available on the 8291A. It determines the way in which the 8291A uses the information in the Address 0 and Address 1 Registers.

—In Mode 1, the contents of the Address 0 Register constitute the "Major" talker/listener address while the Address 1 Register represents the "Minor" talker/listener address. In applications where only one address is needed, the major talker/listener is used, and the minor talker/listener should be disabled. Loading an address via the Address 0/1 Register into Address Registers 0 and 1 enables the major and minor talker/listener functions respectively.

—In Mode 2 the 8291A recognizes two sequential address bytes: a primary followed by a secondary. Both address bytes must be received in order to enable the device to talk or listen. In this manner, Mode 2 addressing implements the extended talker and listener functions as defined in IEEE-488.

To use Mode 2 addressing the primary address must be loaded into the Address 0 Register, and the Secondary Address is placed in the Address 1 Register. With both primary and secondary addresses residing on chip, the 8291A can handle all addressing sequences without processor intervention.

—In Mode 3, the 8291A handles addressing just as it does in Mode 1, except that each Major or Minor primary address must be followed by a secondary address. All secondary addresses must be verified by the microprocessor when Mode 3 is used. When the 8291A is in TPAS or LPAS (talker/listener primary addressed state), and it does not recognize the byte on the DIO lines, an APT interrupt is generated (see section on Interrupt Registers) and the byte is available in the CPT (Command Pass-Through) Register. As part of its interrupt service routine, the microprocessor must read the CPT Register and write one of the following responses to the Auxiliary Mode Register:

- 1. 07H implies a non-valid secondary address
- 2. 0FH implies a valid secondary address

Setting the TO bit generates the local ton (talk-only) message and sets the 8291A to a talk-only mode. This mode allows the device to operate as a talker in an interface system without a controller.

Setting the LO bit generates the local lon (listenonly) message and sets the 8291A to a listen-only mode. This mode allows the device to operate as a listener in an interface system without a controller. The above bits may also be used by a controller-incharge to set itself up for remote command or data communication.

The mode of addressing implemented by the 8291A may be selected by writing one of the following bytes to the Address Mode Register.

#### Register Contents Mode

10000000	Enable talk only mode (ton)
01000000	Enable listen only mode (lon)
11000000	The 8291 may talk to itself
0000001	Mode 1, (Primary-Primary)
00000010	Mode 2 (Primary-Secondary)
00000011	Mode 3 (Primary/APT-Primary/APT)

The Address Status Register contains information used by the microprocessor to handle its own addressing. This information includes status bits that monitor the address state of each talker/ listener, "ton" and "lon" flags which indicate the talk and listen only states, and an EOI bit which, when set, signifies that the END message came with the last data byte. LPAS and TPAS indicate that the listener or talker primary address has been received. The microprocessor can use these bits when the secondary address is passed through to determine whether the 8291A is addressed to talk or listen. The LA (listener addressed) bit will be set when the 8291A is in LACS (Listener Active State) or in LADS (Listener Addressed State). Similarly, the TA (Talker Addressed bit) will be set to indicate TACS or TADS. but also to indicate SPAS (Serial Poll Active State). The MJMN bit is used to determine whether the information in the other bits applies to the Major or Minor talker/listener. It is set to "1" when the Minor talker/listener is addressed. It should be noted that only one talker/listener may be active at any one time. Thus, the MJMN bit will indicate which, if either, of the talker/listeners is addressed or active.

The Address 0/1 Register is used for specifying the device's addresses according to the format selected in the Address Mode Register. Five bit addresses may be loaded into the Address 0 and Address 1 Registers by writing into the Address 0/1 Register. The ARS bit is used to select which of these registers the other seven bits will be loaded into. The DT and DL bits may be used to disable the talker or listener function at the address signified by the other five



bits. When Mode 1 addressing is used and only one primary address is desired, *both* the talker and the listener should be disabled at the Minor address.

As an example of how the Address 0/1 Register might be used, consider an example where two primary addresses are needed in the device. The Major primary address will be selectable only as a talker and the Minor primary address will be selectable only as a listener. This configuration of the 8291A is formed by the following sequence of writes by the microprocessor.

Operation	CS	RD	WR	Data	RS2-RS0
1. Select addressing Mode 1	0	1	0	00000001	100
<ol><li>Load major address into Address 0 Register with listener function disabled.</li></ol>	0	1 <sub>e</sub>	0	001AAAAA	110
<ol> <li>Load minor address into Address 1 Register with talker function disabled.</li> </ol>	0	id di disi	-600	110BBBBB	ian <sup>110</sup> a

At this point, the addresses AAAAA and BBBBB are stored in the Address 0 and Address 1 Registers respectively, and are available to be read by the microprocessor. Thus, it is not necessary to store any address information elsewhere. Also, with the information stored in the Address 0 and Address 1 Registers, processor intervention is not required to recognize addressing by the controller. Only in Mode 3, where secondary addresses are passed through, must the processor intervene in the addressing sequence.

The Address 0 Register contains a copy of bit 7 of the Interrupt Status 2 Register (INT). This is to be used when polling for interrupts. Software should poll register 6 checking for INT (bit 7) to be set. When INT is set, the Interrupt Status Register should be read to determine which interrupt was received.

# **Command Pass Through Register**

CPT7	СРТ6	CPT5	CPT4	CPT3	CPT2	CPT1	CPTO
Fors	leesa.	0, 10	0	01 10	01 12		01 10

This command sets (1001) or clears (0001) the pural-

COMMAND PASS THROUGH (5R)

The Command Pass Through Register is used to transfer undefined 8-bit remote message codes from the GPIB to the microprocessor. When the CPT feature is enabled (bit B0 in Auxiliary Register B), any message not decoded by the 8291A becomes an undefined command. When Mode 3 addressing is used secondary addresses are also passed through

the CPT Register. In either case, the 8291A will holdoff the handshake until the microprocessor reads this register and issues the VSCMD auxiliary command.

The CPT and APT interrupts flag the availability of undefined commands and secondary addresses in the CPT Register. The details of these interrupts are explained in the section on Interrupt Registers.

An added feature of the 8291A is its ability to handle undefined secondary commands following undefined primaries. Thus, the number of available commands for future IEEE-488 definition is increased; one undefined primary command followed by a sequence of as many as 32 secondary commands can be processed. The IEEE-488 Standard does not permit users to define their own commands, but upgrades of the standard are thus provided for.

The recommended use of the 8291A's undefined command capabilities is for a controller-configured Parallel Poll. The PPC message is an undefined primary command typically followed by PPE, an undefined secondary command. For details on this procedure, refer to the section on Parallel Poll Protocol.

# **Auxiliary Mode Register**

CNT2 CNT1 CNT0 COM4 COM3 COM2 COM1 COM0
---

AUX MODE (5W)

CNT0-2:CONTROL BITS
COM0-4:COMMAND BITS

The Auxiliary Mode Register contains a three-bit control field and a five-bit command field. It is used for several purposes on the 8291A:

- 1. To load "hidden" auxiliary registers on the 8291A
- To issue commands from the microprocessor to the 8291A.
- To preset an internal counter used to generate T1, delay in the Source Handshake function, as defined in IEEE-488.

Table 5 summarizes how these tasks are performed with the Auxiliary Mode Register. Note that the three control bits determine how the five command bits are interpreted.



the CPT Register, in eith celds the 8291A will hold-

CO	DE	no renictor and increase				
CONTROL	COMMAND BITS	COMMAND				
000 to viilidali	0CCCC	Execute auxiliary command				
errupts are	ecddddo ac of these intended ntendot Re	Preset internal counter to match external clock frequency of DDDD MHz (DDDD binary representation of 1 to 8 MHz)				
elb100 of	DDDDD A	Write DDDDD into auxiliary register A				
ald101 vs	DDDDD	Write DDDDD into auxiliary register B				
d foil10 ed dary com- Standard own com-	USP <sub>3</sub> P <sub>2</sub> P <sub>1</sub>	Enable/disable parallel poll either in response to remote messages (PPC followed by PPE or PPD) or as a local lpe message. (Enable if U = 0, disable if U = 1.)				

# AUXILIARY COMMANDS VIISOIGY BRAMMOO VISM

Auxiliary commands are executed by the 8291A whenever 0000CCCC is written into the Auxiliary Mode Register, where CCCC is the 4-bit command code.

0000—Immediate Execute pon: This command resets the 8291A to a power up state (local pon message as defined in IEEE-488).

The following conditions constitute the power up state:

- 1. All talkers and listeners are disabled.
- 2. No interrupt status bits are set.

The 8291A is designed to power up in certain states as specified in the IEEE-488 state diagrams. Thus, the following states are in effect in the power up state: SIDS, AIDS, TIDS, LIDS, NPRS, LOCS, and PPIS.

The "0000" pon is an immediate execute command (a pon pulse). It is also used to release the "initialize" state generated by either an external reset pulse or the "0010" Chip Reset command.

**0010**—Chip Reset (Initialize): This command has the same effect as a pulse applied to the Reset pin. (Refer to the section on Reset Procedure.)

0011 — Finish Handshake: This command finishes a handshake that was stopped because of a holdoff on RFD. (Refer to Auxiliary Register A.)

0100—Trigger: A "Group Execute Trigger" is forced by this command. It has the same effect as a GET command issued by the controller-in-charge of the GPIB, but does not cause a GET interrupt.

0101, 1101—Clear/Set rtl: These commands correspond to the local rtl message as defined by the IEEE-488. The 8291A will go into local mode when a Set rtl Auxiliary Command is received if local lockout is not in effect. The 8291A will exit local mode after receiving a Clear rtl Auxiliary Command if the 8291A is addressed to listen.

0110—Send EOI: The EOI line of the 8291A may be asserted with this command. The command causes EOI to go true with the next byte transmitted. The EOI line is then cleared upon completion of the handshake for that byte.

0111, 1111—Non Valid/Valid Secondary Address or Command (VSCMD): This command informs the 8291A that the secondary address received by the microprocessor was valid or invalid (0111 = invalid, 1111 = valid). If Mode 3 addressing is used, the processor must field each extended address and respond to it, or the GPIB will hang up. Note that the COM3 bit is the invalid/valid flag.

The valid (1111) command is also used to tell the 8291A to continue from the command-pass-through-state, or from RFD holdoff on GET, SDC or DCL.

1000—pon: This command puts the 8291A into the pon (power on) state and holds it there. It is similar to a Chip Reset except none of the Auxiliary Mode Registers are cleared. In this state, the 8291A does not participate in any bus activity. An Immediate Execute pon releases the 8291A from the pon state and permits the device to participate in the bus activity again.

0001, 1001—Parallel Poll Flag (local "ist" message): This command sets (1001) or clears (0001) the parallel poll flag. A "1" is sent over the assigned data line (PRR = Parallel Poll Response true) only if the parallel poll flag matches the sense bit from the Ipe local message (or indirectly from the PPE message). For a more complete description of the Parallel Poll features and procedures refer to the section on Parallel Poll Protocol.

## INTERNAL COUNTER

The internal counter determines the delay time allowed for the setting of data on the DIO lines. This delay time is defined as T<sub>1</sub> in IEEE-488 and appears in the Source Handshake state diagram between the



SDYS and STRS. As such, DAV is asserted  $T_1$  after the DIO lines are driven. Consequently,  $T_1$  is a major factor in determining the data transfer rate of the 8291A over the GPIB ( $T_1 = TWRDV2-TWRD15$ ).

When open-collector transceivers are used for connection to the GPIB,  $T_1$  is defined by IEEE-488 to be  $2\mu$ sec. By writing 0010DDDD into the Auxiliary Mode Register, the counter is preset to match a  $f_C$  MHz clock input, where DDDD is the binary representation of  $N_F$  [1 $\leq$ N<sub>F</sub> $\leq$ 8,  $N_F$ =(DDDD)<sub>2</sub>]. When  $N_F$  =  $f_C$ , a  $2\mu$ sec  $T_1$  delay will be generated before each DAV asserted.

$$T_{1(\mu sec)} = \frac{2N_F}{f_C} + t_{SYNC} , 1 \le N_F \le 8$$

 $t_{\scriptsize \text{SYNC}}$  is a synchronization error, greater than zero and smaller than the larger of T clock high and T clock low. (For a 50% duty cycle clock,  $t_{\scriptsize \text{SYNC}}$  is less than half the clock cycle).

If it is necessary that  $T_1$  be different from  $2\mu sec$ ,  $N_F$  may be set to a value other than  $f_C$ . In this manner, data transfer rates may be programmed for a given system. In small systems, for example, where transfer rates exceeding GPIB specifications are required, one may set  $N_F < f_C$  and decrease  $T_1$ .

When tri-state transceivers are used, IEEE-488 allows a higher transfer rate (lower  $T_1$ ). Use of the 8291A with such transceivers is enabled by setting  $B_2$  in Auxiliary Register B. In this case, setting  $N_F = f_C$  causes a  $T_1$  delay of  $2\mu$ sec to be generated for the first byte transmitted — all subsequent bytes will have a delay of 500 nsec.

$$T_1$$
(High Speed)  $\mu$ sec =  $\frac{N_F}{2f_C} + t_{SYNC}$ 

Thus, the shortest T<sub>1</sub> is achieved by setting  $N_F = 1$  using an 8 MHz clock with a 50% duty cycle clock ( $t_{SYNC} < 63$  nsec):

$$T_{1(HS)} = \frac{1}{2x8} + 0.063 = 125 \text{ nsec max.}$$

#### AUXILIARY REGISTER A set calls at opassem aid T

Auxiliary Register A is a "hidden" 5-bit register which is used to enable some of the 8291A features. Whenever a 100 A<sub>4</sub>A<sub>3</sub>A<sub>2</sub>A<sub>1</sub>A<sub>0</sub> byte is written into the

Auxiliary Register, it is loaded with the data  $A_4A_3A_2A_1A_0$ . Setting the respective bits to "1" enables the following features.

A<sub>0</sub>— RFD Holdoff on all Data: If the 8291A is listening, RFD will not be sent true until the "finish handshake" auxiliary command is issued by the microprocessor. The holdoff will be in effect for each data byte.

B .- Enable Undefined Command Pass Through:

A,—RFD Holdoff on End: This feature enables the holdoff on EOI or EOS (if enabled). However, no holdoff will be in effect on any other data bytes.

A<sub>2</sub>—End on EOS Received: Whenever the byte in the Data In Register matches the byte in the EOS Register, the END interrupt bit will be set in the Interrupt Status 1 Register.

A<sub>3</sub>—Output EOI on EOS Sent: Any occurrence of data in the Data Out Register matching the EOS Register causes the EOI line to be sent true along with the data.

A<sub>4</sub>—EOS Binary Compare: Setting this bit causes the EOS Register to function as a full 8-bit word. When it is not set, the EOS Register is a 7-bit word (for ASCII characters).

If A<sub>0</sub>=A<sub>1</sub>=1, a special "continuous Acceptor Handshake cycling" mode is enabled. This mode should be used only in a controller system configuration, where both the 8291A and the 8292 are used. It provides a continuous cycling through the Acceptor Handshake state diagram, requiring no local messages from the microprocessor; the rdy local message is automatically generated when in ANRS. As such, the 8291A Acceptor Handshake serves as the controller Acceptor Handshake. Thus, the controller cycles through the Acceptor Handshake without delaying the data transfer in progress. When the tcs local message is executed, the 8291A should be taken out of the "continuous AH cycling" mode, the GPIB will hang up in ANRS, and a BI interrupt will be generated to indicate that control may be taken. A simpler procedure may be used when a "tcs on end of block" is executed; the 8291A may stay in "continuous AH cycling". Upon the end of a block (EOI or EOS received), a holdoff is generated, the GPIB hangs up in ANRS, and control may be taken.



# AUXILIARY REGISTER B. H. Hereige A. YashixuA

Auxiliary Register B is a "hidden" 4-bit register which is used to enable some of the features of the 8291A. Whenever a 101 B<sub>4</sub>B<sub>3</sub>B<sub>2</sub>B<sub>1</sub>B<sub>0</sub> is written into the Auxiliary Mode Register, it is loaded with the data B<sub>4</sub>B<sub>3</sub>B<sub>2</sub>B<sub>1</sub>B<sub>0</sub>. Setting the respective bits to "1" enables the following features:

A.A.A.A.A. Setting the respective bits to "1"

B<sub>o</sub>—Enable Undefined Command Pass Through: This feature allows any commands not recognized by the 8291A to be handled in software. If enabled, this feature will cause the 8291A to holdoff the handshake when an undefined command is received. The microprocessor must then read the command from the Command Pass Through Register and send the VSCMD auxiliary command. Until the VSCMD command is sent, the handshake holdoff will be in effect.

B<sub>1</sub>—Send EOI in SPAS: This bit enables EOI to be sent with the status byte; EOI is sent true in Serial Poll Active State. Otherwise, EOI is sent false in SPAS.

 $B_2$ —Enable High Speed Data Transfer: This feature may be enabled when tri-state external transceivers are used. The data transfer rate is limited by  $T_1$  delay time generated in the Source Handshake function, which is defined according to the type of transceivers used. When the "High Speed" feature is enabled,  $T_1=2$  microseconds is generated for the first byte transmitted after each true to false transition of ATN. For all subsequent bytes,  $T_1=500$  nanoseconds. Refer to the Internal Counter section for an explanation of  $T_1$  duration as a function of  $B_2$  and of clock frequency.

**B**<sub>3</sub>—Enable Active Low Interrupt: Setting this bit causes the polarity of the INT pin to be reversed, providing an output signal compatible with Intel's MCS-48® Family. Interrupt registers are not affected by this bit.

Handshake state diagram, requiring no local mes-

B<sub>4</sub>—Enable RFD Holdoff on GET or DEC; Setting this bit causes RFD to be held false until the "VSCMD" auxiliary command is written after GET, SDC, and DCL commands. This allows the device to hold off the bus until it has completed a clear or trigger similar to an unrecognized command.

# PARALLEL POLL PROTOCOL SA SRTS bas SYOS

Writing a 011USP $_3$ P $_2$ P $_1$  into the Auxiliary Mode Register will enable (U=0) or disable (U=1) the 8291A for a parallel poll. When U=0, this command is the "lpe" (local poll enable) local message as defined in IEEE-488. The "S" bit is the sense in which the 8291A is enabled; only if the Parallel Poll Flag ("ist" local message) matches this bit will the Parallel Poll Response, PPR $_N$ , be sent true (Response= S + ist). The bits P $_3$ P $_2$ P $_1$  specify which of the eight data lines PPR $_N$  will be sent over. Thus, once the 8291A has been configured for Parallel Poll, whenever it senses both EOI and ATN true, it will automatically compare its PP flag with the sense bit and send PPR $_N$  true or false according to the comparison.

the DiO lines are driven. Consequently, T, is a major

If a PP2\* implementation is desired, the "Ipe" and "ist" local messages are all that are needed. Typically, the user will configure the 8291A for Parallel Poll immediately after initialization. During normal operation the microprocessor will set or clear the Parallel Poll Flag (ist) according to the device's need for service. Consequently the 8291A will be set up to give the proper response to IDY (EOI • ATN) without directly involving the microprocessor.

If a PP1\* implementation is desired, the undefined command features of the 8291A must be used. In PP1, the 8291A is indirectly configured for Parallel Poll by the active controller on the GPIB. The sequence at the 8291A being enabled or disabled remotely is as follows:

- The PPC message is received and is loaded into the Command Pass Through Register as an undefined command. A CPT Interrupt is sent to the microprocessor; the handshake is automatically held off.
- The microprocessor reads the CPT Register and sends VSCMD to the 8291A, releasing the handshake.

Tries = 4 0.063 = 125 nsec max.

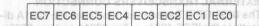
3. Having received an undefined primary command, the 8291A is set up to receive an undefined secondary command (the PPE or PPD message). This message is also received into the CPT Register, the handshake is held off, and the CPT interrupt is generated.

NOTE: \*As defined in IEEE Standard 488. 001 a nevener W



4. The microprocessor reads the PPE or PPD message and writes the command into the Auxiliary Mode Register (bit 7 should be cleared first). Finally, the microprocessor sends VSCMD and the ed handshake is released. A) beau ensight asemble

# **End of Sequence (EOS) Register**



dan be configure REGISTER soughno ed nab

The EOS Register and its features offer an alternative to the "Send EOI" auxiliary command. A seven or eight bit byte (ASCII or binary) may be placed in the register to flag the end of a block or read. The type of EOS byte to be used is selected in Auxiliary Register bit A4.

If the 8291A is a listener, and the "End on EOS Received" is enabled with bit A2, then an END interrupt is generated in the Interrupt Status 1 Register whenever the byte in the Data-In Register matches the byte in the EOS Register.

If the 8291A is a talker, and the "Output EOI on EOS Sent" is enabled with bit A3, then the EOI line is sent true with the next byte whenever the contents of the Data Out Register match the EOS register.

#### Reset Procedure

The 8291A is reset to an initialization state either by a pulse applied to its Reset pin, or by a reset auxiliary command (02H written into the Auxiliary Command Register). The following conditions are caused by a reset pulse (or local reset command):

- 1. A "pon" local message as defined by IEEE-488 is held true until the initialization state is released.
- 2. The Interrupt Status Registers are cleared (not Interrupt Enable Registers).
- 3. Auxiliary Registers A and B are cleared.
- 4. The Serial Poll Mode Register is cleared.
- 5. The Parallel Poll Flag is cleared.
- 6. The EOI bit in the Address Status Register is
- 7. N<sub>F</sub> in the Internal Counter is set to 8 MHz. This setting causes the longest possible T1 delay to be generated in the Source Handshake (16 µsec for 1 MHz clock).

The initialization state is released by an "immediate execute pon" command (00H written into the Auxiliary Command Register). both detailed 3. The 8291A sends DAV true on the GPIB and pro-

The suggested initialization sequence is:

- 1. Apply a reset pulse or send the reset auxiliary Status Register should be read and the bnammon
- 2. Set the desired intial conditions by writing into the Interrupt Enable, Serial Poll Mode, Address Mode, Address 0/1, and EOS Registers. Auxiliary Registers A and B, and the internal counter should also be initialized.
- 3. Send the "immediate execute pon" auxiliary command to release the initialization state.
- 4. If a PP2 Parallel Poll implementation is to be used 8 the "lpe" local message may be sent, enabling the 8291A for a Parallel Poll Response on an assigned line. (Refer to the section on Parallel Poll Protocol.)

# Using DMA

The 8291A may be connected to the Intel® 8237 or 8257 DMA Controllers or the 8089 I/O Processor for DMA operation. The 8237 will be used to refer to any DMA controller. The DREQ pin of the 8291A requests a DMA byte transfer from the 8237. It is set by BO or BI flip flops, enabled by the DMAO and DMAI bits in the Interrupt Enable 2 Register. (After reading, the INT1 register BO and BI interrupts will be cleared but not BO and BI in DREQ equation.)

The DACK pin is driven by the 8237 in response to the DMA request. When DACK is true (active low) it sets CS = RS0 = RS1 = RS2 = 0 such that the RD and WR signals sent by the 8237 refer to the Data In and Data Out Registers. Also, the DMA request line is reset by DACK (RD + WR).

### DMA input sequence:

- 1. A data byte is accepted from the GPIB by the 8291A.
- 2. A BI interrupt is generated and DREQ is set.
- 3. DACK and RD are driven by the 8237, the contents of the Data In Register are transferred to the system bus, and DREQ is reset.
- 4. The 8291A sends RFD true on the GPIB and proceeds with the Acceptor Handshake protocol.

#### DMA output sequence:

1. A BO interrupt is generated (indicating that a byte 8. The rdy local message is sent. The rdy local message is sent. The rdy local message is sent.



- DACK and WR are driven by the 8237, a byte is transferred from the MCS bus into the Data Out Register, and DREQ is reset.
- 3. The 8291A sends DAV true on the GPIB and proceeds with the Source Handshake protocol.

It should be noted that each time the device is addressed (MTA + MLA + ton + Ion), the Address Status Register should be read, and the 8237 should be initialized accordingly. (Refer to the 8237 or 8257 Data Sheets.)

#### APPLICATION BRIEF

# System Configuration sibemail edit bae?

#### MICROPROCESSOR BUS CONNECTION

The 8291A is 8048/49, 8051, 8080/85, and 8086/88

compatible. The three address pins  $(RS_0, RS_1, RS_2)$  should be connected to the non-multiplexed address bus (for example:  $A_8$ ,  $A_9$ ,  $A_{10}$ ). In case of 8080, any address lines may be used. If the three lowest address bits are used  $(A_0, A_1, A_2)$ , then they must be demultiplexed first.

# **EXTERNAL TRANSCEIVERS CONNECTION**

The 8293 GPIB Transceiver interfaces the 8291A directly to the IEEE-488 bus. The 8291A and two 8293's can be configured as a talker/listener (see Figure 6) or with the 8292 as a talker/listener/controller (see Figure 7). Absolutely no active or passive external components are required to comply with the complete IEEE-488 electrical specification.

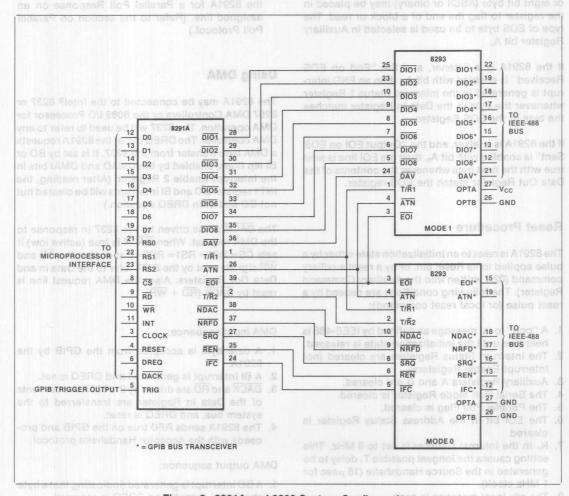
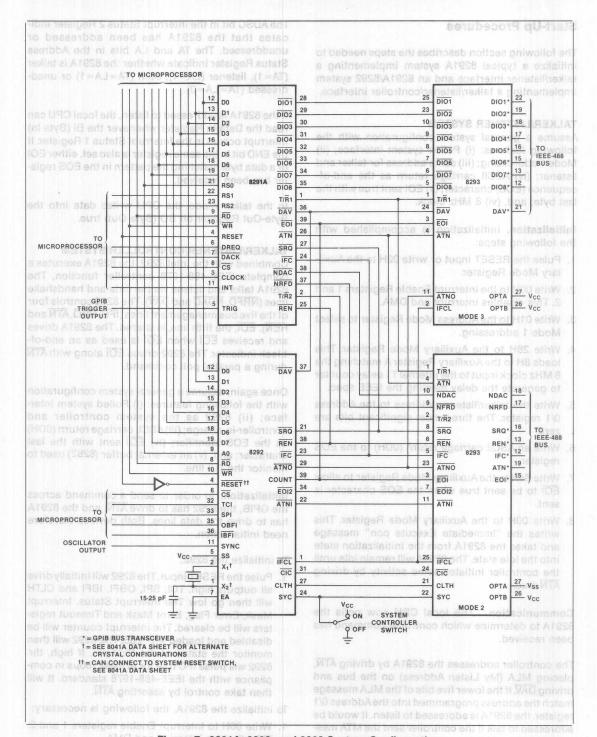


Figure 6. 8291A and 8293 System Configuration of 908 2207 (800) ybs and 8



AMC Prigure 7. 8291A, 8292, and 8293 System Configuration

1-269



# **Start-Up Procedures**

The following section describes the steps needed to initialize a typical 8291A system implementing a talker/listener interface and an 8291A/8292 system implementing a talker/listener/controller interface.

#### TALKER/LISTENER SYSTEM

Assume a general system configuration with the following features: (i) Polled system interface; (ii) Mode 1 addressing; (iii) same address for talker and listener; (iv) ASCII carriage return as the end-of-sequence (EOS) character; (v) EOI sent true with the last byte; and, (vi) 8 MHz clock.

**Initialization.** Initialization is accomplished with the following steps:

- Pulse the RESET input or write 02H to the Auxiliary Mode Register.
- Write 00H to the Interrupt Enable Registers 1 and 2. This disables interrupt and DMA.
- Write 01H to the Address Mode Register to select Mode 1 addressing.
- 4. Write 28H to the Auxiliary Mode Register. This loads 8H to the Auxiliary Register A matching the 8 MHz clock input to the internal T1 delay counter to generate the delay meeting the IEEE spec.
- Write the talker/listener address to the Address 0/1 register. The three most significant bits are zero.
- Write an ASCII carriage return (0DH) to the EOS register.
- 7. Write 84H to the Auxiliary Mode Register to allow EOI to be sent true when the EOS character is sent.
- 8. Write 00H to the Auxiliary Mode Register. This writes the "Immediate Execute pon" message and takes the 8291A from the initialization state into the idle state. The 8291A will remain idle until the controller initiates some activity by driving ATN true.

**Communication.** The local CPU now polls the 8291A to determine which controller command has been received.

The controller addresses the 8291A by driving ATN, placing MLA (My Listen Address) on the bus and driving DAV. If the lower five bits of the MLA message match the address programmed into the Address 0/1 register, the 8291A is addressed to listen. It would be addressed to talk if the controller sent the MTA message instead of MLA.

The ADSC bit in the Interrupt Status 2 Register indicates that the 8291A has been addressed or unaddressed. The TA and LA bits in the Address Status Register indicate whether the 8291A is talker (TA=1), listener (LA=1), both (TA=LA=1) or unaddressed (TA=LA=0).

If the 8291A is addressed to listen, the local CPU can read the Data-In Register whenever the BI (Byte In) interrupt occurs in the Interrupt Status 1 Register. If the END bit in the same register is also set, either EOI or a data byte matching the pattern in the EOS register has been received.

In the talker mode, the CPU writes data into the Byte-Out Register on BO (Byte Out) true.

#### TALKER/LISTENER/CONTROLLER SYSTEM

Combined with the Intel 8292, the 8291A executes a complete IEEE-488-1978 controller function, The 8291A talks and listens via the data and handshake lines (NRFD, NDAC and DAV). The 8292 controls four of the five bus management lines (IFC, SRQ, ATN and REN). EOI, the fifth line, is shared. The 8291A drives and receives EOI when EOI is used as an end-of-block indicator. The 8292 drives EOI along with ATN during a parallel poll command.

Once again, assume a general system configuration with the following features: (i) Polled system interface; (ii) 8292 as the system controller and controller-in-charge; (iii) ASCII carriage return (0DH) as the EOS identifier; (iv) EOI sent with the last character; and, (v) an external buffer (8282) used to monitor the TCI line.

Initialization. In order to send a command across the GPIB, the 8292 has to drive ATN, and the 8291A has to drive the data lines. Both devices therefore need initialization.

#### To initialize the 8292:

1. Pulse the RESET input. The 8292 will initially drive all outputs high. TCI, SPI, OBFI, IBFI and CLTH will then go low. The Interrupt Status, Interrupt Mask, Error Flag, Error Mask and Timeout registers will be cleared. The interrupt counter will be disabled and loaded with 255. The 8292 will then monitor the status of the SYC pin. If high, the 8292 will pulse IFC true for at least 100μs in compliance with the IEEE-488-1978 standard. It will then take control by asserting ATN.

To initialize the 8291A, the following is necessary:

ntroller sent the MTA mes
1. Write 00H to Interrupt Enable registers 1 and 2.

nothing find metay 2 8828 bns. This disables interrupt and DMA.



- With the 8292 as the controller-in-charge, it is impossible to address the 8292 via the GPIB. Therefore, the ton or lon modes of the 8291A must be used. To send comands, set the 8291A in the ton mode by writing 80H to the Address Mode Register.
- 3. Write 26H to the Auxiliary Mode Register to match the T1 data settling time to the 6 MHz clock input.
- Write an ASCII carriage return (0DH) to the EOS Register.
- 5. Write 84H to the Auxiliary Mode Register in order to enable "Output EOI on EOS sent" and thus send EOI with the last character.
- Write 00H—Immediate Execute pon—to the Auxiliary Mode Register to put the 8291A in the idle state.

   Aman Aman Aman and a state.

Communication. Since the 8291A is in the ton mode, a BO interrupt is generated as soon as the immediate Execute pon command is written. The CPU writes the command into the Data Out Register, and repeats it on BO becoming true for as many commands as necessary. ATN remains continuously

true unless the GTSB (Go To Standby) command is sent to the 8292.

ATN has to be false in order to send data rather than commands from the controller. To do this, the following steps are needed:

- 1. Enable the TCI interrupt if not already enabled.
- Wait for IBF (Input Buffer Full) in the 8292 Interrupt Status Register to be reset.
- Write the GTSB (F6H) command to the 8292 Command Field Register.
- 4. Read the 8282 and wait for TCl to be true.
- Write the ton (80H) and pon (00H) command to the 8291A Address Mode Register and Auxiliary Mode Registers respectively.
- 6. Wait for the BO interrupt to be set in the 8291A.
- 7. Write the data to the 8291A Data-Out Register.

Identically, the user could command the controller to listen rather than talk. To do that, write Ion (40H) instead of ton into the Address Mode Register. Then wait for BI rather than BO to go true. Read the data Register.

Test Conditions		.xxXX	.oiM	Payameter	
	nsec	250		Address Stable to Data Valid	gaf
	nsec			READ to Data Valid	
				Data Float After READ	
				Address Stable Before WRITE	
				Address Hold After WRITE	
				WRITE Width	
				Data Set Up Time to the Trailing Edge of WRITE	
				Data Hold Time After WRITE	
DACK! to RDJ 0 ≤t ≤50nsec	388C			RDJ to Valid Data (D <sub>0</sub> -D <sub>1</sub> )	



# ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	
With Respect to Ground	0.5V to +7V
Power Dissipation	0.65 Watts

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4. Write an ASCII carriage return (0DH) to the EOS

# D.C. CHARACTERISTICS [V<sub>cc</sub> = 5V ±10%, T<sub>A</sub> = 0°C to 70°C (Commercial)] both visilixuA ent of HAB ethal.

Symbol	(HOO) nod Parameter not entile	Min.	Max.	Unit	Test Conditions
nalVicuA bn	Input Low Voltage	-0.5	-x0.8	of You	Write 00H - Immediate Execute
VIH	Input High Voltage	oM 2	Vcc+0.5	ii AlVisa	litary Mode Register to put the
Vol on	Output Low Voltage	6. Wal	0.45	V	IOL=2mA (4mA for TR1 pin)
ТОТОН В	Output High Voltage stab ent e	W/2.4	400 000	V	$I_{OH} = -400\mu A (-150\mu A \text{ for SRQ pin})$
VOH-INT	Interrupt Output High Voltage	2.4	ent as n	oce Vs b	I <sub>OH</sub> =-400μA
ite Ion (40H	n rather than talk. To do that, we	3.5	enT .nei	inw Vai b	IOH=-50µA
gister <sub>ul</sub> her	Input Leakage A 911 office 101	insteal	neto gen	tu CuA'sC	VIN=0V to Vcc mos and satisfy US
ILOL	Output Leakage Current	Wait 10	-10	μΑ	Vout=0.45V
Ісон	Output Leakage Current	neigon	10	μΑ	Vout=Vcc
lcc	Vcc Supply Current		120	mA	T <sub>A</sub> =0°C

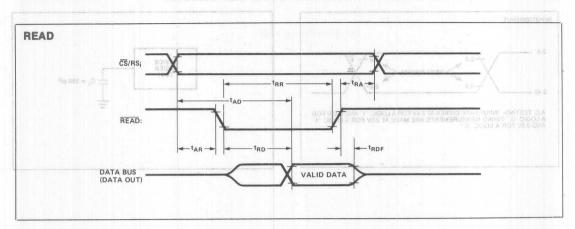
# A.C. CHARACTERISTICS [ $V_{cc} = 5V \pm 10\%$ , $T_A = 0^{\circ}C$ to $70^{\circ}C$ (Commercial)]

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
tar	Address Stable Before READ	0	ú	nsec	
tra	Address Hold After READ	0	2 -	nsec	
tRR	READ width	140		nsec	
tad	Address Stable to Data Valid		250	nsec	
t <sub>RD</sub>	READ to Data Valid		100	nsec	
trdf	Data Float After READ	0	60	nsec	
taw	Address Stable Before WRITE	0		nsec	
twa	Address Hold After WRITE	0			
tww	WRITE Width	170		nsec	
tow	Data Set Up Time to the Trailing Edge of WRITE	130		nsec	
two	Data Hold Time After WRITE	0		nsec	
t <sub>DKDR4</sub>	RD↓ or WR↓ to DREQ↓		130	nsec	
tDKDA6	RD↓ to Valid Data (D₀-D₁)		200	nsec	DACK↓ to RD↓ 0 ≤t ≤50nsec

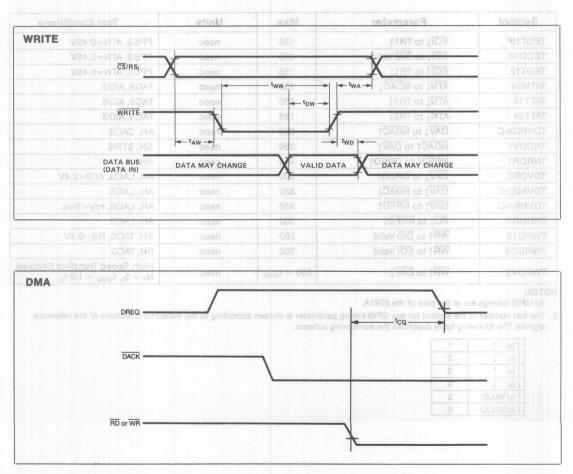


#### **WAVEFORMS**

# A.C. TIMING MEASUREMENT POINTS AND LOAD CONDITIONS

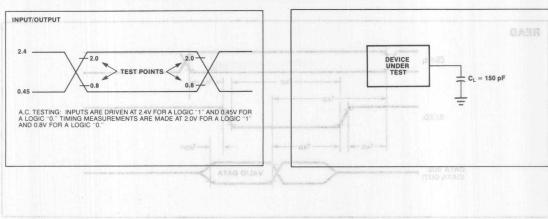


#### GPIB TIMINGS!





# A.C. TIMING MEASUREMENT POINTS AND LOAD CONDITIONS



# **GPIB TIMINGS**<sup>1</sup>

Symbol	Parameter	Max.	Units	Test Conditions	
TEOT13 <sup>2</sup>	EOI↓ to TR1↑	135	nsec	PPSS, ATN=0.45V	
TEOD16	EOI↓ to DIO Valid	155	nsec	PPSS, ATN=0.45V	
TEOT12	EOI↑ to TR1↓	155	nsec	PPSS, ATN=0.45V	
TATND4	ATN↓ to NDAC↓	155	nsec	TACS, AIDS	
TATT14	ĀTN↓ to TR1↓	155	nsec	TACS, AIDS	
TATT24	ATN↓ to TR2↓	155	nsec	TACS, AIDS	
TDVND3-C	DAV↓ to NDAC↑	650	nsec	AH, CACS	
TNDDV1	NDAC↑ to DAV↑	350	nsec	SH, STRS	
TNRDR1	NRFD↑ to DREQ↑	400	nsec	SHaua Atao	
TDVDR3	DAV↓ to DREQ↑	600	nsec	AH, LACS, ATN=2.4V	
TDVND2-C	DAV↑ to NDAC↓	350	nsec	AH, LACS	
TDVNR1-C	DAV↑ to NRFD↑	350	nsec	AH, LACS, rdy=True	
TRDNR3	RD↓ to NRFD↑	500	nsec	AH, LACS	
TWRD15	WR↑ to DIO Valid	280	nsec	SH, TACS, RS=0.4V	
TWREO5	WR↑ to EOI Valid	350	nsec	SH, TACS	
TWRDV2	WR↑ to DAV↓	830 + t <sub>SYNC</sub>	nsec	nsec High Speed Transfers Enable $N_F = f_C$ , $t_{SYNC} = 1/2 \cdot f_C$	

#### NOTES:

- 1. All GPIB timings are at the pins of the 8291A.
- 2. The last number in the symbol for any GPIB timing parameter is chosen according to the transition directions of the reference signals. The following table describes the numbering scheme.

↑to ↑	1
↑to ↓	2
↓to ↑	3
↓to ↓	4
↑ to VALID	5
↓ to VALID	6



# **APPENDIX A**

## MODIFIED STATE DIAGRAMS

Figure A-1 presents the interface function state diagrams. It is derived from IEEE Std. state diagrams, with the following changes:

A. The 8291A supports the complete set of IEEE-488 interface functions except for the controller. These include: SH1, AH1, T5, TE5, L3, LE3, SR1, RL1, PP1, DC1, DT1, and C0.

B. Addressing modes included in T,L state diagrams.

Note that in Mode 3, MSA, OSA are generated only after secondary address validity check by the microprocessor (APT interrupt).

C. In these modified state diagrams, the IEEE-488-1978 convention of negative (low true) logic is followed. This should not be confused with the Intel pin- and signal-naming convention based on positive logic. Thus, while the state diagrams below carry low true logic, the signals described elsewhere in this data sheet are consistent with Intel notation and are based on positive logic.

-		Convention		
Level	Logic	IEEE-488	Intel	
0 (25)	METTER T	DAV	DAV	
1	F	DAV	DAV	
0	T	NDAC	NDAC	
1	F	NDAC	NDAC	
O VAO	T	NRFD	NRFD	
1	F	NRFD	NRFD	

Consider the condition when the Not-Ready-For-Data signal (pin 37) is active. Intel indicates this active low signal with the symbol  $\overline{\text{NRFD}}$  ( $V_{\text{OuT}} \leq V_{\text{OL}}$  for AH;  $V_{\text{IN}} \leq V_{\text{IL}}$  for SH). The IEEE-488-1978 Standard, in its state diagrams, indicates the active state of this signal (True condition) with NRFD.

D. All remote multiline messages decoded are conditioned by ACDS. The multiplication by ACDS is not drawn to simplify the diagrams.

E. The symbol



indicates:

- When event X occurs, the function returns to state S.
- 2. X overrides any other transition condition in the function.

Statement 2 simplifies the diagram, avoiding the explicit use of X to condition all transitions from S to other states.

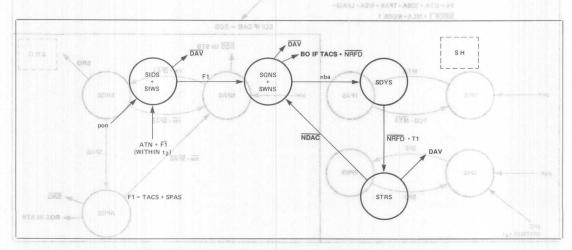


Figure A-1. 8291A State Diagrams (Continued next page)



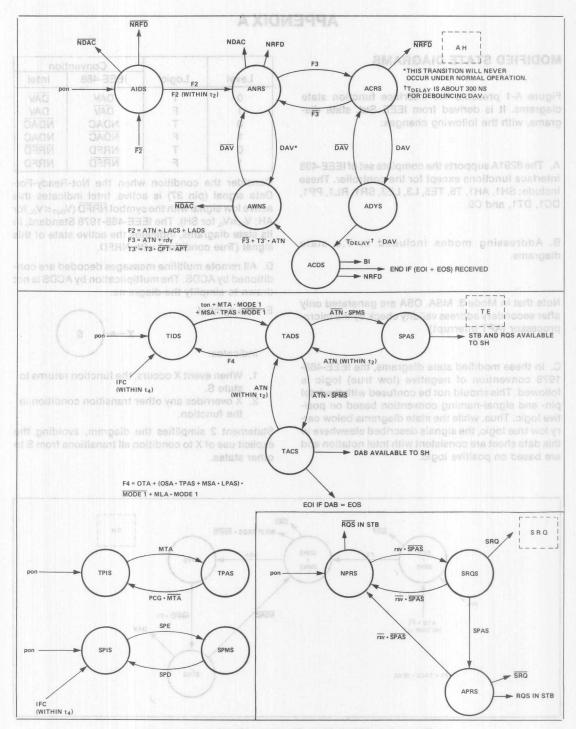


Figure A-1. 8291A State Diagrams (Continued next page)



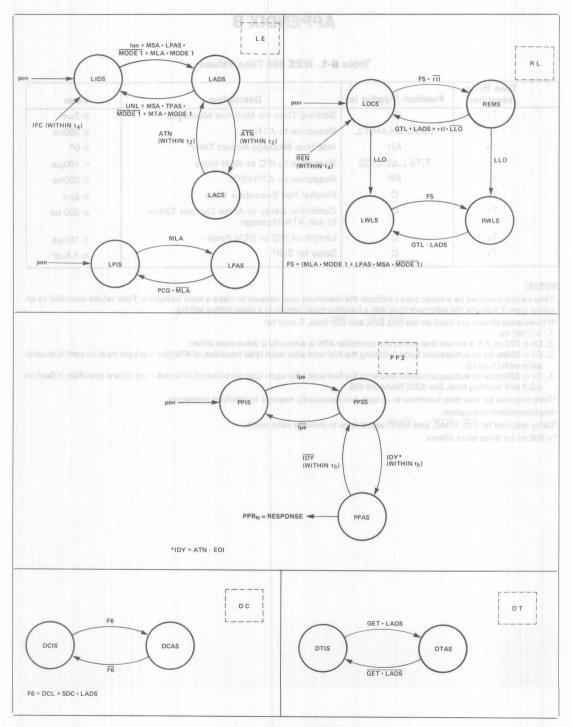


Figure A-1. 8291A State Diagrams

# APPENDIX B

Table B-1. IEEE 488 Time Values

Time Value	Function (Applies to)	Description Description	Value
T1 /	SH	Settling Time for Multiline Messages	$\geq 2\mu s^2$
t <sub>2</sub>	LC,IC,SH,AH,T,L	Response to ATN	≤ 200ns
T <sub>3</sub>	AH	Interface Message Accept Time <sup>3</sup>	> 04
t4	T,TE,L,LE,C,CE	Response to IFC or REN False	< 100µs
t <sub>5</sub>	PP	Response to ATN+EOI	≤ 200ns
Т6	a C	Parallel Poll Execution Time	≥ 2 <i>µ</i> s
T <sub>7</sub>	( sawa )	Controller Delay to Allow Current Talker to see ATN Message	≥ 500 ns
T8	EGAL HD	Length of IFC or REN False	> 100µs
T <sub>9</sub>	C	Delay for EOI <sup>5</sup>	$\geq 1.5\mu s^6$

#### NOTES:

<sup>1</sup>Time values specified by a lower case t indicate the maximum time allowed to make a state transition. Time values specified by an upper case T indicate the minimum time that a function must remain in a state before exiting.

<sup>2</sup>If three-state drivers are used on the DIO, DAV, and EOI lines, T<sub>1</sub> may be:

- 1. ≥ 1100 ns
- 2. Or  $\geq$  700 ns if it is known that within the controller ATN is driven by a three-state driver.
- 3. Or ≥ 500ns for all subsequent bytes following the first sent after each false transition of ATN (the first byte must be sent in accordance with (1) or (2).
- Or ≥ 350ns for all subsequent bytes following the first sent after each false transition of ATN under conditions specified in Section 5.2.3 and warning note. See IEEE Standard 488.

<sup>3</sup>Time required for interface functions to accept, not necessarily respond to interface messages.

<sup>4</sup>Implementation dependent.

<sup>5</sup>Delay required for EOI, NDAC, and NRFD signal lines to indicate valid states.

6≥ 600 ns for three-state drivers.

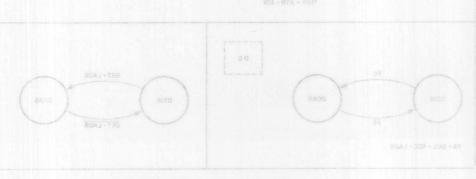
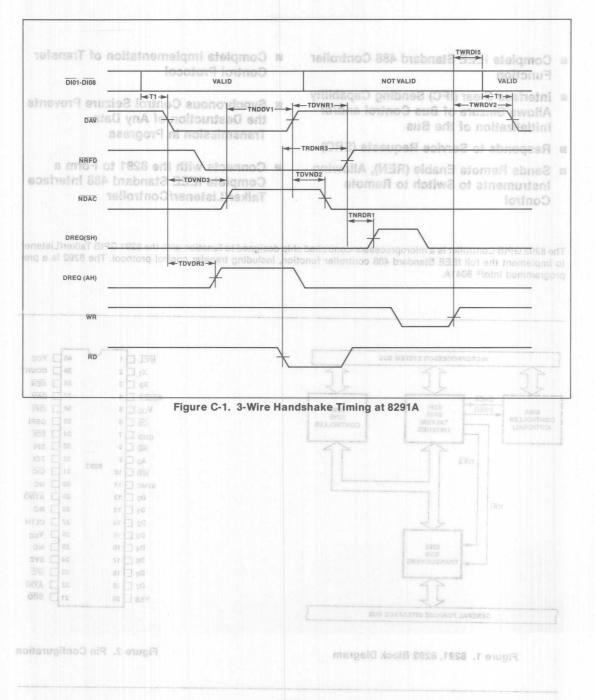


Figure A-1. 8291A State Diagrams

# APPENDIX C THE THREE-WIRE HANDSHAKE





#### 8292 GPIB CONTROLLER

- Complete IEEE Standard 488 Controller Function
- Interface Clear (IFC) Sending Capability Allows Seizure of Bus Control and/or Initialization of the Bus
- Responds to Service Requests (SRQ)
- Sends Remote Enable (REN), Allowing Instruments to Switch to Remote Control
- Complete Implementation of Transfer Control Protocol
- Synchronous Control Seizure Prevents the Destruction of Any Data Transmission in Progress
- Connects with the 8291 to Form a Complete IEEE Standard 488 Interface Talker/Listener/Controller

The 8292 GPIB Controller is a microprocessor-controlled chip designed to function with the 8291 GPIB Talker/Listener to implement the full IEEE Standard 488 controller function, including transfer control protocol. The 8292 is a preprogrammed Intel® 8041A.

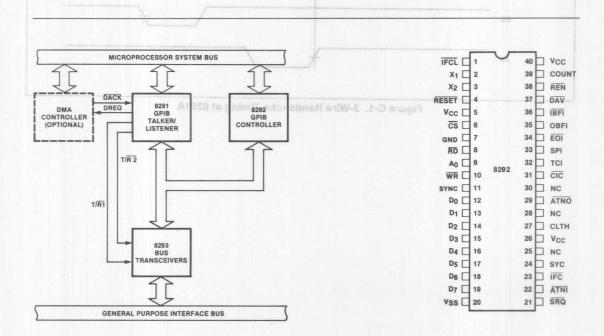


Figure 1. 8291, 8292 Block Diagram

Figure 2. Pin Configuration



0232

Symbol	Name and Function	Туре	Pin No.	Symbol
V <sub>CC</sub> COUNT	IFC Received (Latched): The 8292 monitors the IFC Line (when not system controller) through this pin.	ni pru ns. Ug must	n e <b>di</b> to ion rece been	IFCL 1011 of to 1016 the 828
Sess entrained	Crystal Inputs: Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.	eterm the ap rupt splion	2, 3 Isingono aulsta 180 lo	X <sub>1</sub> , X <sub>2</sub>
	Reset: Used to initialize the chip to a known state during power on.	ve tire	4	RESET
8190	Chip Select Input: Used to select the 8292 from other devices on the common data bus.	is wai		CS d baen ed d) nadw
REN	Read Enable: Allows the master CPU to read from the 8292.	repa.	8 iousiy	RD d netthw
	Address Line: Used to select be- tween the data bus and the status	t neitif		A <sub>0</sub>
DAV	register during read operations and to distinguish between data and commands written into the 8292 during write operations.	orec datab dT .b		
İBFI	Write Enable: Allows the master CPU to write to the 8292.		ei ai br	WR edi
	Sync: 8041A instruction cycle synchronization signal; it is an output clock with a frequency of XTAL ÷ 15.	0	squ <b>tt</b> ste n transf	SYNC b
OBFI	Data: 8 bidirectional lines used for communication between the central processor and the 8292's data bus buffers and status register.	g I/O ad esr basad	Section of the section of	D <sub>0</sub> -D <sub>7</sub> s
figuration	Ground: Circuit ground potential.	P.S.	7, 20	V <sub>SS</sub>
EO12 seed to bessesses	Service Request: One of the IEEE control lines. Sampled by the 8292 when it is controller in charge. If true, SPI interrupt to the master will be generated.	n Cha	Ad <b>12</b> od nge. No system	SRQ medical strains on trails
SPI Seldar	Attention In: Used by the 8292 to monitor the GPIB ATN control line. It is used during the transfer control procedure.	.bn.am	22	ATNI
TCI	Interface Clear: One of the GPIB management lines, as defined by IEEE Std. 488-1978, places all de-	1/0	23	IFC oA
1 750	vices in a known quiescent state.	1981	0	Q DRI
00	System Conroller: Monitors the system controller switch.	1	24	SYC
CIC	Clear Latch: Used to clear the IFCR latch after being recognized by the 8292. Usually low (except after hardware Reset), it will be pulsed high when IFCR is recognized by the 8292.	0	27	CLTH
sno   one	Attention Out: Controls the ATN control line of the bus through external logic for tcs and tca proce-	0	29	ATNO
9 0	dures. (ATN is a GPIB control line, as defined by IEEE Std. 488-1978.)	0	0	10 0

Symbol	Pin No.	Туре	Name and Function
Vcc	5, 26, 40	P.S.	Voltage: +5V supply input ±10%.
COUNT	18 39 81 1 Vd 81	is do	Event Count: When enabled by the proper command the internal counter will count external events
sino	au soal		through this pin. High to low transition will increment the internal counter by one. The pin is sampled once per three internal instruction cycles (7.5µsec sample period when using 5 MHz XTAL). It can be used for byte counting when connected to NDAC, or for block counting when connected to the EOI.
REN	00	0	E programme,
REN	- M.	O N	Remote Enable: The Remote Enable bus signal selects remote or local control of the device on the bus. A GPIB bus management line as defined by IEEE Std. 488-1978.
DAV	37	I/O	Data Valid: Used during paralle poll to force the 8291 to accept the parallel poll status bits. It is also used during the tcs procedure.
IBFI /	36	O O	Input Buffer Not Full: Used to interrupt the central processo while the input buffer of the 8292 is empty. This feature is enabled and disabled by the interrupt mask register.
OBFI	35 1000 to	O	Output Buffer Full: Used as an interrupt to the central processor while the output buffer of the 8292 is full. The feature can be enabled and disabled by the interrupt mask register.
	usa <b>46</b> es 2. Most 3) can be de 2 ide	100	End Or Identify: One of the GPIE management lines, as defined by IEEE Std. 488-1978. Used with ATN as Identify Message during paralle poll.
SPI S olds?	33	0	Special Interrupt: Used as an interrupt on events not initiated by the central processor.
TCI	32	O	Task Complete Interrupt: Interrup
980 00	300 8	DAI	dicate that the task requested was completed by the 8292 and the in- formation requested is ready in the
CIC	31	0	data bus buffer.
DHE		BUTATE	Controller in Charge: Controls the S/R input of the SRQ bus transceiver. It can also be used to indicate that the 8292 is in charge of the GPIB bus.
one	THA 3	a I	REN DAV EGI X SYC
	pe	TATE R	EVENT COUNT
	9	0	0 0 0 0 0
	-1		

FUNCTIONAL DESCRIPTION



#### **FUNCTIONAL DESCRIPTION**

The 8292 is an Intel 8041A which has been programmed as a GPIB Controller interface element. It is used with the 8291 GPIB Talker/Listener and two 8293 GPIB Transceivers to form a complete IEEE-488 Bus Interface for a microprocessor. The electrical interface is performed by the transceivers, data transfer is done by the talker/listener, and control of the bus is done by the 8292. Figure 3 is a typical controller interface using Intel's GPIB peripherals.

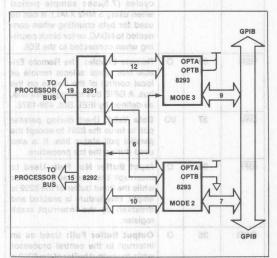


Figure 3. Talker/Listener/Controller Configuration

The internal RAM in the 8041A is used as a special purpose register bank for the 8292. Most of these registers (except for the interrupt flag) can be accessed through commands to the 8292. Table 2 identifies the registers used by the 8292 and how they are accessed.

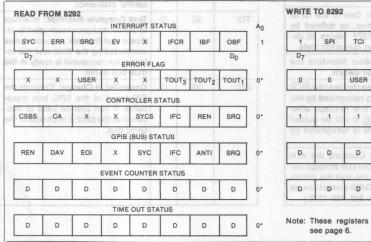
#### Interrupt Status Register

SYC	ERR	SRQ	EV	X	IFCR	IBF	OBF
-----	-----	-----	----	---	------	-----	-----

The 8292 can be configured to interrupt the microprocessor on one of several conditions. Upon receipt of the interrupt the microprocessor must read the 8292 interrupt status register to determine which event caused the interrupt, and then the appropriate subroutine can be performed. The interrupt status register is read with  $A_0$  high. With the exception of OBF and IBF, these interrupts are enabled or disabled by the SPI interrupt mask, OBF and IBF have their own bits in the interrupt mask (OBFI and  $\overline{\rm IBFI}$ ).

- OBF Output Buffer Full. A byte is waiting to be read by the microprocessor. This flag is cleared when the output data bus buffer is read.
- IBF Input Buffer Full. The byte previously written by the microprocessor has not been read yet by the 8292. If another byte is written to the 8292 before this flag clears, data will be lost. IBF is cleared when the 8292 reads the data byte.
- IFCR Interface Clear Received. The GPIB system controller has set IFC. The 8292 has become idle and is no longer in charge of the bus. The flag is cleared when the IACK command is issued.
- EV Event Counter Interrupt. The requested number of blocks or data bytes has been transferred. The EV interrupt flag is cleared by the IACK command.
- SRQ Service Request. Notifies the 8292 that a service request (SRQ) message has been received. It is cleared by the IACK command.
- ERR Error occurred. The type of error can be determined by reading the error status register. This interrupt flag is cleared by the IACK command.
- SYC System Controller Switch Change. Notifies the processor that the state of the system controller switch has changed. The actual state is contained in the GPIB Status Register. This flag is cleared by the IACK command.

#### Table 2. 8292 Registers



yd by	eniteb :	inos, as	INTE	RRUPT M	IASK			A
1	SPI	TCI	SYC	OBFI	IBFI	0	SRQ	
D <sub>7</sub>	notino	M nelio	YOU ER	ROR MA	sk	24	D <sub>0</sub>	SYC
0	0	USER	0	0	тоит3	TOUT <sub>2</sub>	TOUT <sub>1</sub>	7.10
ent y	d besin	20361 DI	COM	IMAND FI	ELD			
pst lu	q ed II	v 11 (is	OP	С	С	С	С	
ya bi	cogniza	91 E! HR	EVE	NT COUN	TER			
D	ti Pilo	D	D	D	D	D	D	0
-2-2-01	guorini a ant b	eus en/ os est :	nt pin	IME OUT				
D	D	DO	D	D	D	D	D	0

Note: These registers are accessed by a special utility command, see page 6.

1 | SPI | TCI | SYC | OBFI | IBFI | 0 | SRQ

The Interrupt Mask Register is used to enable features and to mask the SPI and TCI interrupts. The flags in the Interrupt Status Register will be active even when masked out. The Interrupt Mask Register is written when  $A_0$  is low and reset by the RINM command. When the register is read,  $D_1$  and  $D_7$  are undefined. An intertupt is enabled by setting the corresponding register bit.

SRQ Enable interrupts on SRQ received to anabecome

IBFI Enable interrupts on input buffer empty.

OBFI Enable interrupts on output buffer full.

SYC Enable interrupts on a change in the system controller switch.

TCI Enable interrupts on the task completed.

SPI Enable interrupts on special events.

NOTE: The event counter is enabled by the GSEC command, the error interrupt is enabled by the error mask register, and IFC cannot be masked (it will always cause an interrupt).

#### Controller Status Register

CSBS	CAT	25 <b>(x</b> co u	(TX/8	SYCS	egFCd	REN	SRQ
D <sub>7</sub>	10.0 Ehr	by state	ssiand	All Bills	to tellor	moo en	D <sub>0</sub>

The Controller Status Register is used to determine the status of the controller function. This register is accessed by the RCST command.

SRQ Service Request line active (CSRS).

REN Sending Remote Enable.

IFC Sending or receiving interface clear.

SYCS System Controller Switch Status (SACS).

CA Controller Active (CACS + CAWS + CSWS).

CSBS Controller Stand-by State (CSBS, CA) = (0,0) — Controller Idle

#### will be generated by the 8292. The 8292 will respond to GPIB Bus Status Register: The Bus Status Register

REN	DAV	EOI	X	SYC	IFC	ATNI	SRQ
				time of	OF -		

This register contains GPIB bus status information. It can be used by the microprocessor to monitor and manage the bus. The GPIB Bus Register can be read using the RBST command.

Each of these status bits reflect the current status of the corresponding pin on the 8292.

SRQ Service Request 3 1980 and tellettage materia

ATNI Attention In

IFC Interface Clear of easternine - MBR2 - ST

SYC System Controller Switch was been poor sid!

EOI End or Identify and the Line is relievance metale

DAV Data Valid

**REN** Remote Enable

D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub> D<sub>3</sub> D<sub>2</sub> D<sub>1</sub> D<sub>0</sub>

The Event Counter Register contains the initial value for the event counter. The counter can count pulses on pin 39 of the 8292 (COUNT). It can be connected to EOI or NDAC to count blocks or bytes respectively during standby state. A count of zero equals 256. This register cannot be read, and is written using the WEVC command.

#### Event Counter Status Register bellioses bolled

20201 10	COURS DAY 1	A SEEKES	10/1 2/03	CHILIT	2013 111	White A	-
07	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D3	2280	D <sub>1</sub>	D0

This register contains the current value in the event counter. The event counter counts back from the initial value stored in the Event Counter Register to zero and then generates an Event Counter Interrupt. This register cannot be written and can be read using a REVC command.

#### **Time Out Register**

					north charles	SEL MEN	THE PARTY LAND
D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>

The Time Out Register is used to store the time used for the time out error function. See the individual timeouts (TOUT1, 2, 3) to determine the units of this counter. This Time Out Register cannot be read, and it is written with the WTOUT command.

#### Time Out Status Register 201 814T .1618190FL/88M 10113

		March Co.	1.1111111111111111111111111111111111111	2221125	THUS WITH	I THE PARTY OF	The second
D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>

This register contains the current value in the time out counter. The time out counter decrements from the original value stored in the Time Out Register. When zero is reached, the appropriate error interrupt is generated. If the register is read while none of the time out functions are active, the register will contain the last value reached the last time a function was active. The Time Out Status Register cannot be written, and it is read with the RTOUT command.

#### Error Flag Register, villity and al viccesso bridges and

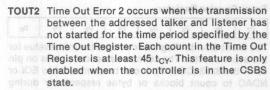
X	×	USER	X	×	TOUT <sub>3</sub>	TOUT <sub>2</sub>	TOUT
---	---	------	---	---	-------------------	-------------------	------

Four errors are flagged by the 8292 with a bit in the Error Flag Register. Each of these errors can be masked by the Error Mask Register. The Error Flag Register cannot be written, and it is read by the IACK command when the error flag in the Interrupt Status Register is set.

TOUT1 Time Out Error 1 occurs when the current controller has not stopped sending ATN after receiving the TCT message for the time period specified by the Time Out Register. Each count in the Time Out Register is at least 1800 toy.

After flagging the error, the 8292 will remain in a loop trying to take control until the current controller stops sending ATN or a new command is written by the microprocessor. If a new command is written, the 8292 will return to the loop after executing it.





# TOUT3 Time Out Error 3 occurs when the handshake signals are stuck and the 8292 is not succeeding in taking control synchronously for the time period specified by the Time Out Register. Each count in the Time Out Register is at least 1800 t<sub>CY</sub>. The 8292 will continue checking ATNI until it becomes true or a new command is received. After performing the new command, the 8292 will return to the ATNI checking loop.

USER User error occurs when request to assert IFC or REN was received and the 8292 was not the system controller.

#### **Error Mask Register**

0	0	USER	0	0	TOUT <sub>3</sub>	TOUT <sub>2</sub>	TOUT-

The Error Mask Register is used to mask the interrupt from a particular type of error. Each type of error interrupt is enabled by setting the corresponding bit in the Error Mask Register. This register can be read with the RERM command and written with  $A_0$  low.

#### **Command Register**

	1	1	1	OP	C	С	C	C
--	---	---	---	----	---	---	---	---

Commands are performed by the 8292 whenever a byte is written with  $A_0$  high. There are two categories of commands distinguished by the OP bit (bit 4). The first category is the operation command (OP=1). These commands initiate some action on the interface bus. The second category is the utility commands (OP=0). These commands are used to aid the communication between the processor and the 8292.

#### OPERATION COMMANDS

Operation commands initiate some action on the GPIB interface bus. It is using these commands that the control functions such as polling, taking and passing control, and system controller functions are performed. A TCI interrupt is generated upon successful completion of each of these functions.

#### F0 — SPCNI — Stop Counter Interrupts

This command disables the internal counter interrupt so that the 8292 will stop interrupting the master on event counter underflows. However, the counter will continue counting and its contents can still be used.

#### F1 - GIDL - Go To Idle

This command is used during the transfer of control procedure while transferring control to another controller. The 8292 will respond to this command only if it is in the active state. ATNO will go high, and CIC will be high so that this 8292 will no longer be driving the ATN line on the GPIB interface bus.

#### F2 - RST - Reset 9 entry disease but woll at A nadw

This command has the same effect as asserting the external reset on the 8292. For details, refer to the reset procedure described later.

#### F3 - RSTI - Reset Interrupts

This command resets any pending interrupts and clears the error flags. The 8292 will not return to any loop it was in (such as from the time out interrupts).

#### F4 - GSEC - Go To Standby, Enable Counting

The function causes ATNO to go high and the counter will be enabled. If the 8292 was not the active controller, this command will exit immediately. If the 8292 is the active controller, the counter will be loaded with the value stored in the Event Counter Register, and the internal interrupt will be enabled so that when the counter reaches zero, the SPI interrupt will be generated. SPI will be generated every 256 counts thereafter until the controller exits the standby state or the SPCNI command is written. An initial count of 256 (zero in the Event Counter Register) will be used if the WEVC command is not executed. If the data transmission does not start, a TOUT2 error will be generated.

#### F5 - EXPP - Execute Parallel Poll

This command initiates a parallel poll by asserting ATN and EOI (IDY message) true. The 8291 should be previously configured as a listener. Upon detection of DAV true, the 8291 enters ACDS and latches the parallel poll response (PPR) byte into its data in register. The master will be interrupted by the 8291 Bl interrupt when the PPR byte is available. No interrupts except the IBFI will be generated by the 8292. The 8292 will respond to this command only when it is the active controller.

#### F6 — GTSB — Go To Standby

If the 8292 is the active controller,  $\overline{\text{ATNO}}$  will go high then TCI will be generated. If the data transmission does not start, a TOUT2 error will be generated.

#### F7 — SLOC — Set Local Mode minos Tedal ent phiate

If the 8292 is the system controller, then REN will be asserted false for at least 100  $\mu sec.$  If it is not the system controller, the User Error bit will be set in the Error Flag Register.

#### F8 - SREM - Set Interface To Remote Control

This command will set REN true if this 8292 is the system controller. If not, the User Error bit will be set in the Error Flag Register.





This command will cause IFC to be asserted true for at least 100  $\mu$ sec if this 8292 is the system controller. If it is in CIDS, it will take control over the bus (see the TCNTR command).

#### FA - TCNTR - Take Control has used bluods 192 en

The transfer of control procedure is coordinated by the master with the 8291 and 8292. When the master receives a TCT message from the 8291, it should issue the TCNTR command to the 8292. The following events occur to take control:

- 1. The 8292 checks to see if it is in CIDS, and if not, it exits.
- Then ATNI is checked until it becomes high. If the current controller does not release ATN for the time specified by the Time Out Register, then a TOUT1 error is generated. The 8292 will return to this loop after an error or any command except the RST and RSTI commands.
- 3. After the current controller releases ATN, the 8292 will assert ATNO and CIC low.
- Finally, the TCI interrupt is generated to inform the master that it is in control of the bus.

#### FC — TCASY — Take Control Asynchronously

TCAS transfers the 8292 from CSBS to CACS independent of the handshake lines. If a bus hangup is detected (by an error flag), this command will force the 8292 to take control (asserting ATN) even if the AH function is not in ANRS (Acceptor Not Ready State). This command should be used very carefully since it may cause the loss of a data byte. Normally, control should be taken synchronously. After checking the controller function for being in the CSBS (else it will exit immediately), ATNO will go low, and a TCI interrupt will be generated.

#### FD — TCSY — Take Control Synchronously

There are two different procedures used to transfer the 8292 from CSBS to CACS depending on the state of the 8291 in the system. If the 8291 is in "continuous AH cycling" mode (Aux. Reg. A0 = A1 = 1), then the following procedure should be followed:

- The master microprocessor stops the continuous AH cycling mode in the 8291;
- 2. The master reads the 8291 Interrupt Status 1 Register:
- If the END bit is set, the master sends the TCSY command to the 8292;
- 4. If the END bit was not set, the master reads the 8291 Data In Register and then waits for another BI interrupt from the 8291. When it occurs, the master sends the 8292 the TCSY command.

If the 8291 is not in AH cycling mode, then the master just waits for a BI interrupt and then sends the TCSY command. After the TCSY command has been issued, the 8292 checks for CSBS. If CSBS, then it exits the routine. Otherwise, it then checks the DAV bit in the GPIB status. When DAV becomes false, the 8292 will

wait for at least 1.5  $\mu$ sec. (T10) and then  $\overline{\text{ATNO}}$  will go low. If DAV does not go low, a TOUT3 error will be generated.

#### FE — STCNI — Start Counter Interrupts

This command enables the internal counter interrupt. The counter is enabled by the GSEC command.

## UTILITY COMMANDS The between at 1900 and

All these commands are either Read or Write to registers in the 8292. Upon completion of Read commands, the TCI (Task Completed Interrupt) will be generated. Note that writing to the Error Mask Register and the Interrupt Mask Register are done directly.

#### E1 — WTOUT — Write To Time Out Register

The byte written to the data bus buffer (with  $A_0\!=\!0$ ) following this command will determine the time used for the time out function. Since this function is implemented in software, this will not be an accurate time measurement. This feature is enable or disable by the Error Mask Register. No interrupts except for the  $\overline{\text{IBFI}}$  will be generated upon completion.

#### E2 — WEVC — Write To Event Counter

The byte written to the data bus buffer (with  $A_0\!=\!0$ ) following this command will be loaded into the Event Counter Register and the Event Counter Status for byte counting or EOI counting. Only  $\overline{\text{IBFI}}$  will indicate completion of this command.

#### E3 - REVC - Read Event Counter Status

This command transfers the contents of the Event Counter into the data bus buffer. A TCI is generated when the data is available in the data bus buffer.

#### E4 — RERF — Read Error Flag Register

This command transfers the contents of the Error Flag Register into the data bus buffer. A TCI is generated when the data is available.

#### E5 - RINM - Read Interrupt Mask Register

This command transfers the contents of the Interrupt Mask Register into the data bus buffer. This register is available to the processor so that it does not need to store this information elsewhere. A TCI is generated when the data is available in the data bus buffer.

#### E6 — RCST — Read Controller Status Register

This command transfers the contents of the Controller Status Register into the data bus buffer and a TCI interrupt is generated.

#### E7 — RBST — Read GPIB Bus Status Register

This command transfers the contents of the GPIB Bus Status Register into the data bus buffer, and a TCI interrupt is generated when the data is available.

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#### E9 — RTOUT — Read Time Out Status Register

This command transfers the contents of the Time Out Status Register into the data bus buffer, and a TCI interrupt is generated when the data is available.

#### EA — RERM — Read Error Mask Register

This command transfers the contents of the Error Mask Register to the data bus buffer so that the processor does not need to store this information elsewhere. A TCI interrupt is generated when the data is available.

#### Interrupt Acknowledge antia era abnammoo easiti IA

SYC	ERR	SRQ	EV	bete	IFCR	es 7)	1
D <sub>7</sub>	tereig	971, 718s	vi 1011	1 8/11	of Built	w tad	Do

Each named bit in an Interrupt Acknowledge (IACK) corresponds to a flag in the Interrupt Status Register. When the 8292 receives this command, it will clear the SPI and the corresponding bits in the Interrupt Status Register. If not all the bits were cleared, then the SPI will be set true again. If the error flag is not acknowledged by the IACK command, then the Error Flag Register will be transferred to the data bus buffer, and a TCI will be generated.

NOTE: XXXX1X11 is an undefined operation or utility command, so no conflict exists between the IACK operation and utility commands.

## SYSTEM OPERATION 103 TO DIVINUO

#### 8292 To Master Processor Interface

Communication between the 8292 and the Master Processor can be either interrupt based communication or based upon polling the interrupt status register in predetermined intervals.

#### Interrupt Based Communication | 1998 - 1998 - 1998

Four different interrupts are available from the 8292:

OBFI Output Buffer Full Interrupt

IBFI Input Buffer Not Full Interrupt

TCI Task Completed Interrupt | bask - MAIR - 88

SPI at Special Interrupt and analyment basemon aidT

Each of the interrupts is enabled or disabled by a bit in the interrupt mask register. Since OBFI and IBFI are directly connected to the OBF and IBF flags, the master can write a new command to the input data bus buffer as soon as the previous command has been read.

The TCI interrupt is useful when the master is sending commands to the 8292. The pending TCI will be cleared with each new command written to the 8292. Commands sent to the 8292 can be divided into two major groups:

- Commands that require response back from the 8292 to the master, e.g., reading register.
- Commands that initiate some action or enable features but do not require response back from the 8292, e.g., enable data bus buffer interrupts.

With the first group, the TCI interrupt will be used to indicate that the required response is ready in the data bus buffer and the master may continue and read it. With the second group, the interrupt will be used to indicate completion of the required task, so that the master may send new commands.

The SPI should be used when immediate information or special events is required (see the Interrupt Status Register).

#### "Polling Status" Based Communication of RTAGT ent

When interrupt based communication is not desired, all interrupts can be masked by the interrupt mask register. The communication with the 8292 is based upon sequential poll of the interrupt status register. By testing the OBF and IBF flags, the data bus buffer status is determined while special events are determined by testing the other bits.

#### Receiving IFC

The IFC pulse defined by the IEEE-488 standard is at least 100  $\mu sec.$  In this time, all operation on the bus should be aborted. Most important, the current controller (the one that is in charge at that time) should stop sending ATN or EOI. Thus, IFC must externally gate  $\overline{\text{CIC}}$  (controller in charge) and  $\overline{\text{ATNO}}$  to ensure that this occurs.

## Reset and Power Up Procedure

After the 8292 has been reset either by the external reset pin, the device being powered on, or a RST command, the following sequential events will take place:

- All outputs to the GPIB interface will go high (SRQ, ATNI, IFC, SYC, CLTH, ATNO, CIC, TCI, SPI, EOI, OBFI, IBFI, DAV, REV).
- The four interrupt outputs (TCI, SPI, OBFI, IBFI) and CLTH output will go low.
- 3. The following registers will be cleared:

Interrupt Status as upsoon a hareful own are ered T

8292 from CSBS to CACS depending skak trunners.

8291 in the system; if the 8291 is in 1939 grant of the g

Time Out

Event Counter (= 256), Counter is disabled.

- 4. If the 8292 is the system controller, an ABORT command will be executed, the 8292 will become the controller in charge, and it will enter the CACS state.
- If it is not the system controller, it will remain in

#### System Configuration next both netalger of stack

The 8291 and 8292 must be interfaced to an IEEE-488 bus meeting a variety of specifications including drive capability and loading characteristics. To interface the 8291 and the 8292 without the 8293's, several external gates are required, using a configuration similar to that used in Figure 5.

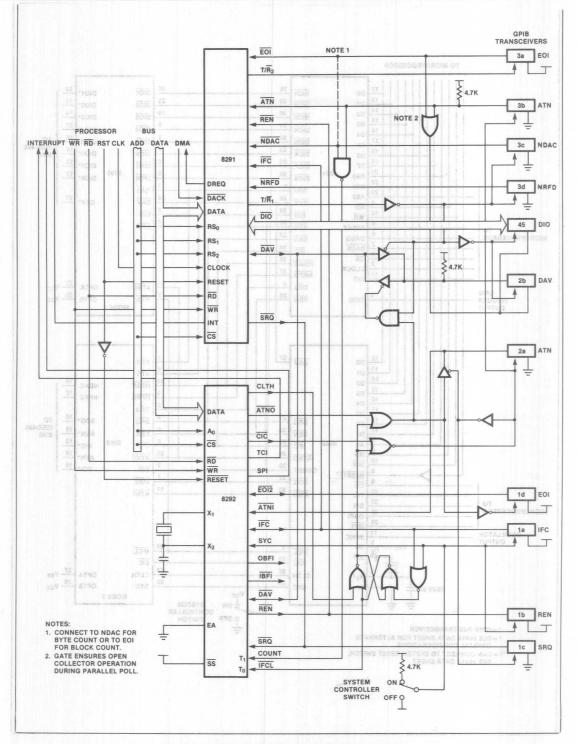


Figure 4. 8291 and 8292 System Configuration

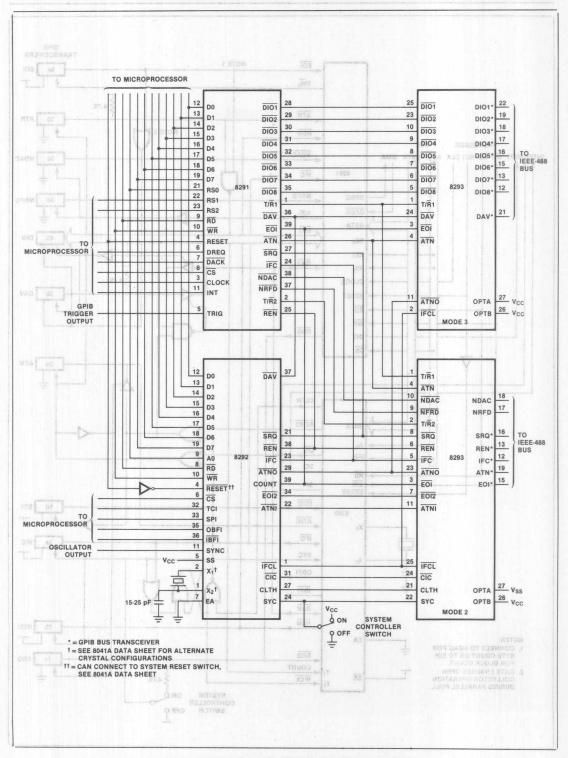


Figure 5. 8291, 8292, and 8293 System Configuration



#### **ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	
Voltage on Any Pin With Respect	
to Ground	0.5V to +7V

Power Dissipation......1.5 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### D.C. CHARACTERISTICS $(T_A = 0^{\circ}\text{C to }70^{\circ}\text{C}, V_{SS} = 0\text{V}: 8292, V_{CC} = \pm5\text{V} \pm 10\%)$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
Villa A. egg	Input Low Voltage (All Except X <sub>1</sub> , X <sub>2</sub> , RESET)	-0.5	0.8	V 8	FO L BROWL S
V <sub>IL2</sub> of m	Input Low Voltage (X <sub>1</sub> , X <sub>2</sub> , RESET)	-0.5	0.6	V M	PR PBY
V <sub>IH1</sub>	Input High Voltage (All Except X <sub>1</sub> , X <sub>2</sub> , RESET)	2.2	Vcc	V	188 54
V <sub>IH2</sub>	Input High Voltage (X <sub>1</sub> , X <sub>2</sub> , RESET)	3.8	V <sub>CC</sub>	V as	P4 GSEC
V <sub>OL1</sub>	Output Low Voltage (D <sub>0</sub> -D <sub>7</sub> )		0.45	V 8	I <sub>OL</sub> = 2.0 mA
V <sub>OL2</sub>	Output Low Voltage (All Other Outputs)	. 00:	0.45	V 81	I <sub>OL</sub> = 1.6 mA
V <sub>OH1</sub>	Output High Voltage (D <sub>0</sub> -D <sub>7</sub> )	2.4	1 26	V	$I_{OH} = -400 \mu\text{A}$
V <sub>OH2</sub>	Output High Voltage (All Other Outputs)	2.4 88	1 48	V	$I_{OH} = -50 \mu\text{A}$
I <sub>IL</sub>	Input Leakage Current (COUNT, IFCL, RD, WR, CS, A	0)	±10	μΑ	V <sub>SS</sub> V <sub>IN</sub> V <sub>CC</sub>
loz	Output Leakage Current (D <sub>0</sub> -D <sub>7</sub> , High Z State)	i ii	±10	μΑ	V <sub>SS</sub> + 0.45 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
Ithreita icu	Low Input Load Current (Pins 21-24, 27-38)		0.5	mA	V <sub>IL</sub> = 0.8V
I <sub>LI2</sub>	Low Input Load Current (RESET)	812	0.2	mA	V <sub>IL</sub> = 0.8V
Icc ibns 4 1	Total Supply Current	alt	125	mA	Typical = 65 mA
Iн	Input High Leakage Current (Pins 21-24, 27-38)	nimetei bosone	100	μΑ	V <sub>IN</sub> = V <sub>CC</sub>
CIN	Input Capacitance	dale made also	10	on pF	L. TOI cloats siter 7 to on all
C <sub>I/O</sub>	I/O Capacitance		20	pF	

#### A.C. CHARACTERISTICS ( $T_A = 0^{\circ}C$ to $70^{\circ}C$ , $V_{SS} = 0V$ : 8292, $V_{CC} = +5V \pm 10\%$ )

#### DBB READ

Symbol	Parameter	Min.		Max.	Unit	Test Conditions
t <sub>AR</sub>	CS, A <sub>0</sub> Setup to RD↓		0		ns	704700/104
t <sub>RA</sub>	CS, A <sub>0</sub> Hold After RDt		0		ns	
t <sub>RR</sub>	RD Pulse Width		250		ns	OS A PARIS NO
t <sub>AD</sub>	CS, A <sub>0</sub> to Data Out Delay		X	225	ns	C <sub>L</sub> = 150 pF
t <sub>RD</sub>	RD↓ to Data Out Delay			225	ns	C <sub>L</sub> = 150 pF
t <sub>DF</sub>	RDt to Data Float Delay			100	ns	
tcy	Cycle Time	i i i i i i	2.5	15	μS	A LOCAC 101 TIMING MEASURES

#### **DBB WRITE**

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t <sub>AW</sub>	CS, A₀ Setup to WR↓	0		ns	
twa	CS, A <sub>0</sub> Hold After WR†	0		ns	
tww	WR Pulse Width	250		ns	
tow	Data Setup to WRf	150		ns	
t <sub>WD</sub>	Data Hold After WR↓	0		ns	

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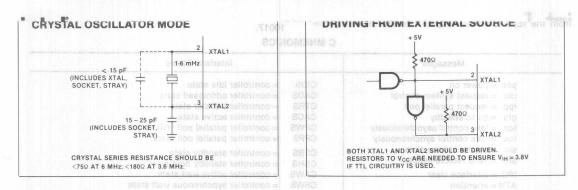


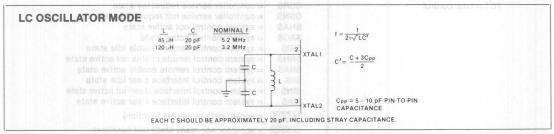
COMMAND TIMINGS[1,3]

Code	Name	Execution	IBFII	TCI <sup>[2]</sup>	SPI	ATNO	CIC	IFC	REN	EOI	DAV	Comm	T trieldmi
E1 001	WTOUT	63	24	device s	ed) to	nott	0 001	4. 40. 1	April 111 y	4 2 7 7 7 7	7777	CONTROL CONTROL	or a solely
E2	WEVC	63	24 91	atec in i	allomi e	enti	s ne	100.0		Chamilio	SEL CLEAN	LAny Pin V	
E3	REVC	71	QX 24 09	51	d at m	itiro .	A A A D	1 1 0.0		T got to 1	1.76 X 4 P. P.		
E4 0	RERF	67	24	847	g con	N/18Y	DIRAA C					nonsqu	
E5	RINM	69	24	49	billigs	relie							
E6	RCST	97	24	77	le ul famili	L ROFT							
E7	RBST	92	24	72						1			
E8			1901 ± Vi	2 2	1292, 1	:V0 = 2	0°C, 10	( a) 0°	(TA = 1	C. C.	I CHI	ARACTE	
E9	RTOUT	69	24	49	-								
EA	RERM	69	24	49				32	PERSON				
F0	SPCNI	53	24	1 20		- 4	178316	N N	nany2	IAVene	Almie we	Count Stop	s After 39
F1	GIOL	88	24	70		161	161	and the same	The second	12 d AS			1.41
F2	RST	94	24	0.5	↓52			SED	SH 6X	(X) 60s	DOA M	Not System	n Controller
F2	RST	214	24	192	↓52	↓179	↓174	↓101	L Eycar	A) and	liny do	System Co	ntroller
F3	RSTI	61	24	1				24					
F4	GSEC	125	2400	107		198		(138)	M.SA.	(M) alle	HOA U.B	H Jugal	
F5	EXPP	10 75 V	24						↓53 †59	↓55 ↑57	01/-W0_	Output	
F6	GTSB	118 V	24	100		191	(87)	gfuO 1	WITO III	Rage (	ay wo.	fuqiu0	
F7	SLOC	73	24	55				†46	Corrects	anuth	W doils	tuetuo	
F8	SREM	91	24	73	-			<b>↓64</b>	0		- 2		
F9	ABORT	155	24	133		↓120	↓115	142	HIJU HA	I effetti	th udit		
FA	TCNTR	108	24	86	1.1.	↓71	<b>↓68</b>	DOT T	411000	manu.	Danasia		
FC	TCAS	92	24	67	X	↓55							
FD	TCSY	115	24	91		180	819.7 U	Star ide	-0m) 1u	STUD S	PQIEMS13.	Output	20,
FE	STCNI	59	24				27-38	21-24	eni® to	Curre	onoj lu	Starts Cou	nt After 43
PIN	RESET	29	-	<b>↓</b> 7	<b>↓</b> 7 ····			199				Not System	Controller
X	IACK	116	- 201		↓73 †98			110	03/1/10	SHOW	2007.3 113	of the town	Danding
A A	m 28 = 185	may liver		1	190					frierit	W Y OQ	If Interrupt	renaing

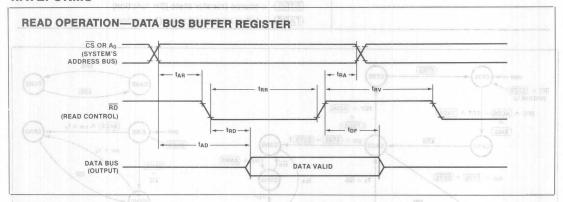
- All times are multiples of t<sub>CY</sub> from the 8041A command interrupt.
   TCI clears after 7 t<sub>CY</sub> on all commands.
   † indicates a level transition from low to high, ‡ indicates a high to low transition.

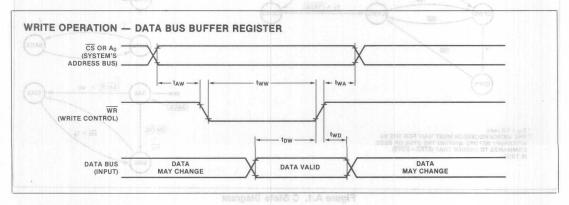
A.C. TESTING INPUT, OUTPUT WAVEFORM A.C. TESTING LOAD CIRCUIT INPUT/OUTPUT DEVICE UNDER TEST TEST POINTS CL teData Float Delay A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC -1" AND 0.45V FOR A LOGIC 0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC -1" AND 0.8V FOR A LOGIC 0." CL INCLUDES JIG CAPACITANCE





#### **WAVEFORMS**





#### **C MNEMONICS**

Messages		Interface States
pon = power on	CIDS	= controller idle state
rsc = request system control	CADS	= controller addressed state
rpp = request parallel poll	CTRS	= controller transfer state
gts = go to standby	CACS	= controller active state
tca = take control asynchronously	CPWS	= controller parallel poll wait state
tcs = take control synchronously	CPPS	= controller parallel poll state
sic = send interface clear	CSBS	= controller standby state
sre = send remote enable	CSHS	= controller standby hold state
IFC = interface clear	CAWS	= controller standby hold state
ATN = attention	CSWS	= controller synchronous wait state
TCT = take control	CSRS	= controller synchronous wart state = controller service requested state
TOT = take control	CSNS	= controller service net requested state
	SNAS	= system control not active state
103 Ves 21	SACS	= system control not active state
	SRIS	= system control remote enable idle state
4.00 +0	SRNS	= system control remote enable not active state
3 79	SRAS	= system control remote enable active state
	SIIS	= system control interface clear idle state
	SINS	= system control interface clear not active state
Cod ≥ 5 - 10 oF PIN TO PIN	SIAS	= system control interface clear active state
CAPACITANCE  STRAY CAPACITANCE	(ACDS)	
S SMALLSHAW, S YARLE AN	SHOULD BE OF EACH	= acceptor not ready state (AH function)
	(SDVS)	= source delay state (SH function)
		SWITHINAN
	(STRS)	= source transfer state (SH function)
	(TADS)	= talker addressed state (T function)

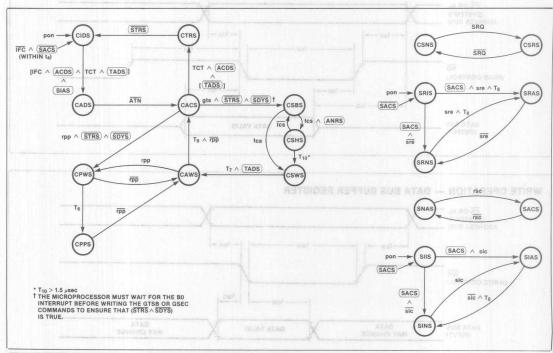


Figure A.1. C State Diagram



#### REMOTE MESSAGE CODING

						A								d Co					
			T	C	D							D		NN	ine	qs ma	88	- 1:	
Mnemonic	Message Name		PE	ASS	0	La la	6	5	4	3		0	D A V	FA	ATN		SRO	F	REN
ACG	Addressed Command Group	e paparatary	M	AC	Y	2116	10	2/2	00	100	X	2100	<del>) 0  </del>	XX	100	99	94		
ATN	Attention		U	UC	X							X		XX	1	X			X
DAB	Data Byte	(Notes 1, 9)	2000	DD	D			D	- 10-			Ď		XX		X			
DAB	Data Byte	(140165 1, 9)	IVI	טט	8			5				1	^	^ ^	U	^	^	^	^
DAC	Data Accepted	poll is execu	U	HS			X					100000	X	X O	X	X	X	X	X
DAV	Data Valid		U	HS	X						X			XX		X		X	
DCL	Device Clear		M	UC	Y		0	1	0	1	0	0		XX		X			
END	End		U	ST	X	100					X			XX	0	1			X
EOS	End of String	(Notes 2, 9)	М	DD	E 8	E		E 5	E	E	E	E		XX		X			
GET	Group Execute Trigger		M	AC	Y		0				0		X	XX	1	X	X	X	X
GTL	Go to Local		M	AC	Y		0	0		0		1		XX		X			
	Identify moder at it solved on			UC	X		X							XX		1			X
IFC	Interface Clear		U	UC			X							XX		X			
LAG	Listen Address Group			AD		0								XX					
LLO	Local Lock Out		M	UC							0								
MLA	My Listen Address	(Note 3)	M	AD	Y		1							XX					
WILA			IVI	AD		U	1,1	5	4	3	2	1	^.	^ ^	sate	^	^	^	^
MTA	My Talk Address	(Note 4)	М	AD	Y	1	0	T 5	T 4	T 3	T 2	T	X	XX	1	X	X	X	Х
MSA	My Secondary Address	(Note 5)	М	SE	8 Y	1	1		-		S	S	X	XX	1	X	X	X	X
NUL	Null Byte		M	DD	0	0	0						X	XX	Х	X	X	X	X
OSA	Other Secondary Address		M	SE				-						MS	_		,		,
OTA	Other Talk Address		M	AD										MTA					
PCG	Primary Command Group		M	_			(P	CG						LA	,	ТΔ	G		
PPC	Parallel Poll Configure		M	AC	Υ	0			0			1		XX	1		X	X	X
PPE	Parallel Poll Enable	(Note 6)	M	SE	Y		1		S	P	P	P		XX	1		X		
PPD	Parallel Poll Disable	(Note 7)	М	SE	Υ	1	1	1	D 4	3 D 3	2 D 2	1 D 1	X	ΧX	1	X	Х	X	Χ
PPR1	Parallel Poll Response 1		U	ST	X	×	X	Y	200			100	Y.	ΧX	1	1	Y	X	Y
PPR2	Parallel Poll Response 2		U	ST		X			X					XΧ	1	1	X		X
PPR3	Parallel Poll Response 3		Ü	ST			X							X	1	1		X	-
PPR4	Parallel Poll Response 4		U	ST			X							(X	1	1	X	X	
PPR5	Parallel Poll Response 5	(Note 10)	U	ST							X			(X	1	1		X	
PPR6	Parallel Poll Response 6		U	ST	X		1				X			(X	1				
PPR7	Parallel Poll Response 7		U	ST	X	-					X			(X		1	X	X	
PPR8	Parallel Poll Response 8		U	ST	1		X							(X	1	1		X	
PPU	Parallel Poll Unconfigure		М	UC	Y			1		1				( X	1	1		X	
REN	Remote Enable		U		-	-			0		1	1			1		X		
RFD	Ready for Data		-	UC			X							(X				X	
RQS		(Note O)	U	HS	X		X				-			X		X			
SCG	Request Service	(Note 9)	U	ST	X						X			X					
SDC	Secondary Command Group		M	SE	Y	1	1		-	-	X			(X	1		X		
	Selected Device Clear		M	AC			0							(X					
SPD	Serial Poll Disable		М	UC					1				XX			X			
SPE	Serial Poll Enable		M	UC			0						X)			X			
SRQ	Service Request	(NI=+== 0, 0)	U	ST	X	X	X	X	X	X	X	X	XX			X			
STB	Status Byte	(Notes 8, 9)	М	ST	8	X	S 6	5	4	3	2	1	X	X	0	X	X	X	X
TCT	Take Control		M	AC	Y	0	0	0	1	0	0	1	XX	X		X			
TAG	Talk Address Group		M	AD	Y	1	0	X	X	X	X	X	XX	X	1	X	X	X	X
UCG	Universal Command Group		M	UC	Y				X		X		XX		1		X		
UNL	Unlisten		M	AD	Y		1						XX	X		X	X	X	X
UNT	Untalk	(Note 11)	M	AD	Y	1	0	1	1	1	1	1	XX	(X				X	

The 1/0 coding on ATN when sent concurrent with multiline messages has been added to this revision for interpretive convenience.

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#### REMOTE MESSAGE CODING

#### NOTES:

- 1. D1-D8 specify the device dependent data bits.
- 2. E1-E8 specify the device dependent code used to indicate the EOS message.
- 3. L1-L5 specify the device dependent bits of the device's listen address.
- 4. T1-T5 specify the device dependent bits of the device's talk address.
- 5. S1-S5 specify the device dependent bits of the device's secondary address. 6. S specifies the sense of the PPR. XXX DU U Response = S⊕ist agg agg agg ag M (9.1 asioH)
- P1\_P3 specify the PPR message to be sent when a parallel poll is executed

	VAA	PPR Message		294.3		el poll is executed.	Data Accepted Data Valid	DAG
X 0 X 0	XO.X	0 PPR1 1 0						
XXX T.O	XXX	XXXXXX						
X X X X 0	XXX	E E E E E E E E E E E E E E E E E E E		QQ		(Notes 2, 9)		
XXXXI	XXX	PPR8	0		N/I		Group Execute Trigger	

- GTL Go to Local M AC Y 0 0 0 0 0 1 XX 1 X X 7. D1-D4 specify don't-care bits that shall not be decoded by the receiving device. It is recommended that all zeroes be sent, x xxx x x x x x x x x x ou
- 8. XS1-S6, S8 specify the device dependent status. (DIO7 is used for the RQS message.)
- 9. The source of the message on the ATN line is always the C function, whereas the messages on the DIO and EOI lines are enabled by the T function.
- 10. The source of the messages on the ATN and EOI lines is always the C function, whereas the source of the messages on the DIO lines is always the PP function.
- 11. This code is provided for system use, see 6.3. 8 M (2 stot) assembly yiethoos 8 VM ARM

11.	4	ins	5 00	ue	is bic	VIU	eu		Sys			126	, 5	ee c	0.0.		(C 010(1)	My Secondary Address	
													0	0				Null Byte	
						AE												Other Secondary Address	A20
									TO									Other Talk Address	ATO
											00							Primary Command Group	
			X															Parallel Poll Configure	
- 3	X		X				· q							Y		M	(Note 6)	Parailet Poli Enable	
					X	XX							1		38			Perallel Poll Disable	
										20								Washington and the contract	
			X								X							Parallel Poli Response 1	
						XX			X						TE			Parellel Poll Response 2	
						XX								X	TR			Parallel Poll Response 3	
																U	(Of etoks)	Parallel Poll Response 4	
		X							×			X						Parallet Poll Response 5	
						XX			X					X	TB	U		Parallel Poli Response 6	
						XX			X		X	X	1					Parallel Poll Response 7	
	×.				X			X					X	1	Ta			Parallel Poli Response 8	
							1	0	1			0		Y	OU			Parailei Poil Unconfigure	
		X	X				X	X		X	X			X	OU	U		Remote Enable	
												X	X		SH	U		Ready for Data	
		X	X							X	X		1	X			(Note 9)	Request Service	RQS
						XX	X	X	X	X			1					Secondary Command Group	SCG
	X								1		0	0				M		Selected Davice Clear	
	X											0		Y		14		Serial Poll Disable	
						XX				- 1	1		0						
			1						X	X		X	X	X		U		Service Request	
												8	X		18	(4)	(Notes 6, 9)	Status Byte	
														8					
					r X								0		OA.			Take Control	
												0	P	Y		W			
					1 X		X				1			Y				Universal Command Group	
							1	r		1	-	-				M			UNU
		X			E X								2						

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#### 8293 GPIB TRANSCEIVER

- Nine Open-collector or Three-state
   Line Drivers
- 48 mA Sink Current Capability on Each Line Driver
- Nine Schmitt-type Line Receivers
- High Capacitance Load Drive Capability
- Single 5V Power Supply
- 28-Pin Package
- Low Power HMOS Design On-Chip IEEE-

- On-chip Decoder for Mode
   Configuration
- Power Up/Power Down Protection to Prevent Disrupting the IEEE Bus
- Connects with the 8291A and 8292 to Form an IEEE Standard 488 Interface Talker/Listener/Controller with no Additional Components
- Only Two 8293's Required per GPIB Interface
- On-Chip IEEE-488 Bus Terminations

The Intel® 8293 GPIB Transceiver is a high-current, non-inverting buffer chip designed to interface the 8291A GPIB Talker/Listener, or the 8291A/8292 GPIB Talker/Listener/Controller combination, to the IEEE Standard 488-1978 Instrumentation Interface Bus. Each GPIB interface would contain two 8293 Bus Transceivers. In addition, the 8293 can also be used as a general-purpose bus driver.

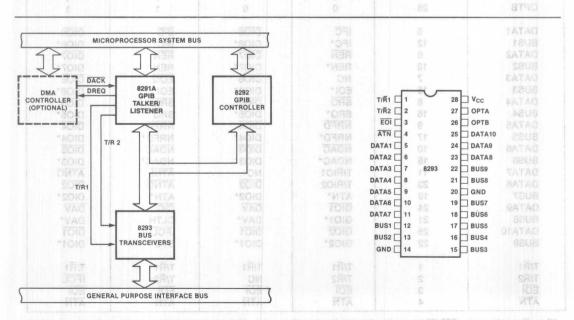


Figure 1. 8291A, 8292, 8293 Block Diagram

Figure 2. Pin Configuration

a 28-Pin Package



Table 1. Pin Description

Symbol	Pin No.	Туре	Name and Function
BUS1- BUS9	12, 13, 15–19, 21, 22	1/0	GPIB Lines, GPIB Side: These are the IEEE-488 bus interface driver/receivers, or TTL-compatible inputs on the 8291A/8292 side depending on the mode used. Their use is programmed by the two mode select pins, OPTA and OPTB.
DATA1- DATA10	5–11, 23–25		GPIB Lines, 8291A/92 Side: These are the pins to be connected to the 8291A and 8292 to interface with the GPIB. Their use is programmed by the two mode select pins, OPTA and OPTB. All these pins are TTL compatible.
	eså bi Linter Althor	384 [	Transmit Receive 1: This pin controls the direction for NDAC, NRFD, DAV, and DIO1-DIO8. Input is TTL compatible.
T/R2	2	1 ;	Transmit Receive 2: This pin controls the direction for EOI. Input is TTL compatible.

■ On-Chip IEEE-488 Bus Terminations

Symbol	Pin No.	Туре	Name and Function					
ĒΟΙ	3	1/0	End Or Identify: This pin indicates the end of a multiple byte transfer or in conjunction with ATN, addresses the device during a polling se quence. It connects to the 8291A and is switched between transmit and receive by T/R2. This pin is TTL compatible.					
ATN S	10 Y311	O	Attention: This pin is used by the 8291A to monitor the GPIB ATN control line. It specifies how data on the DIO lines is to be interpreted. This output is TTL compatible.					
OPTA OPTB	27 26	Rec	Mode Select: These two pins are to control the function of the 8293. A truth table of how they program the various modes is in Table 2.					
V <sub>CC</sub>	28	P.S.	Voltage: Positive power supply (5V ± 10%).					
GND	14, 20	P.S.	Ground: Circuit ground.					

a Low Power HMOS Design Table 2. 8293 Mode Selection Pin Mapping

interface

tice the 8291A GI 488-1978 instrum	designed to interf	verting buffer chip	IEEE Impleme	ntation Name	
Din Mana	Bent Pin No. ni are	Mode 0	owt n Mode 1 luow s	oate Mode 2 nosil	Mode 3
ОРТА	27	0	1	0 aud 6	general-purpos
ОРТВ	26	0	0	1	1
DATA1	5	ĪFC	DIO8	ĪFC	DIO8
BUS1	12	IFC*	DIO8*	IFC*	DI08*
DATA2	6	REN	DIO7	REN	DIO7
BUS2	13	REN*	DIO7*	REN*	DI07*
DATA3	7	NC	DI06	EOI2	DI06
BUS3	15	EOI*	DIO6*	EOI*	DI06*
DATA4	285 8 1 PMT	SRQ	DIO5	SRQ	DIO5
BUS4	16 S S SHIT	SRQ*	DIO5*	SRQ*	DIO5*
DATA5	9 0 108	NRFD	DIO4	NRFD	DIO4
BUS5 CTATAC	17 N NTA	NRFD*	DIO4*	NRFD*	DIO4*
DATA6	TATA 10 STATA	NDAC	DIO3	NDAC	DIO3
BUS6	Tes 18 SATA	NDAC*	DIO3*	NDAC*	DIO3*
DATA7	SE CHES T TECH	T/RIO1	NC	ATNI	ATNO
DATA8	23 S NATA	1/8102	DIO2	ATNO	DIO2
BUS7	19 19 BATA	ATN*	DIO2*	ATN*	DI02*
DATA9	24 OF 30TA	GIO1	DAV	CIC	DAV
BUS8	21	GIO1*	DAV*	CLTH	DAV*
DATA10	25	GIO2	DIO1	IFCL	DIO1
BUS9	22 ar 3800	GIO2*	DIO1*	SYCTHORNART	DIO1*
T/R1	1	T/R1	T/R1	T/R1	T/R1
T/R2	2	T/R2	NC	T/R2	IFCL
EOI	3	EOI	FOI	FOI	EOI
ATN	4	ATN	ATN	ATN	ATN

<sup>\*</sup>Note: These pins are the IEEE-488 bus non-inverting driver/receivers. They include all the bus terminations required by the Standard and may be connected directly to the GPIB bus connector.



#### GENERAL DESCRIPTION (beauthred) notice of

The 8293 is a bidirectional transceiver. It was designed to interface the Intel 8291A GPIB Talker/Listener and the Intel® 8292 GPIB Controller to the IEEE Standard 488-1978 Instrumentation Bus (also referred to as the GPIB). The Intel GPIB Transceiver meets or exceeds all of the electrical specifications defined in the IEEE Standard 488-1978, Section 3.3-3.5, including the bus termination specifications.

The 8293 can be hardware programmed to one of four modes of operation. These modes allow the 8293 to be configured to support both a Talker/Listener/Controller environment and a Talker/Listener environment. In addition, the 8293 can be used as a general-purpose, three-state (push-pull) or open-collector bus transceiver with nine receiver/drivers. Two modes each are used to support a Talker/Listener (see Figure 3) and a Talker/Listener/Controller environment (see Figure 4). Mode 1 is used in general-purpose environments.

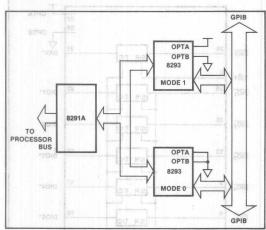


Figure 3. Talker/Listener Configuration

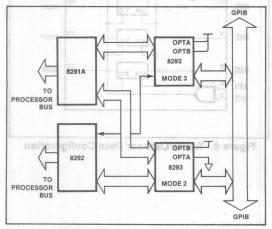


Figure 4. Talker/Listener/Controller Configuration

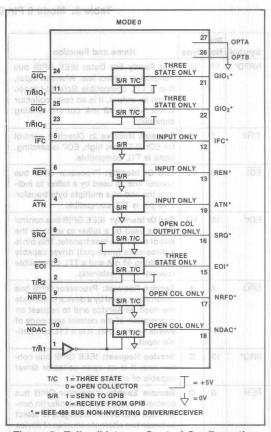


Figure 5. Talker/Listener Control Configuration

Table 3. Mode 0 Pin Description

Symbol	Pin No.	Туре	Name and Function			
T/R1	tnoo	TTI s	Transmit Receive 1 Direction control for NDAC and NRFD. If T/R1 is high, ther NDAC* and NRFD* are receiving. Input is TTL compatible.			
NDAC aud 919 of relic	10	I/O 88900 8 40	Not Data Accepted: Processor GPIE bus handshake control line; used to indicate the condition of acceptance of data by device(s). It is TTL compatible.			
NDAC*	18	18 I/O Not Data Accepted: IEEE GPIE handshake control line. When an it is a TTL compatible Schmitt-it When an output, it is an open-coll driver with 48 mA sinking capabili				
NRFD	9	I/O	Not Ready For Data: Processor GPIE handshake control line; used to indicate the condition of readiness of device(s to accept data. This pin is TTL compatible.			



Symbol	Pin No.	Туре	Name and Function				
NRFD* 17 1/O		1/0	Not Ready For Data: IEEE GPIB bus handshake control line. When an input, it is a TTL compatible Schmitt-trigger. When an output, it is an open-collector driver with a 48 mA current sinking capability.				
T/R2	2	Y <b>1</b> 380	<b>Transmit Receive 2:</b> Direction contro for EOI. If T/R2 is high, EOI* is sending Input is TTL compatible.				
EOI	3	1/0	End Or Identify: Processor GPIB to control line; is used by a talker to in cate the end of a multiple byte transf This pin is TTL compatible.				
EOI*	15	1/0	End Or Identify: IEEE GPIB bus contro line; is used by a talker to indicate the end of a multiple byte transfer. This pin is a three-state (push-pull) driver capable of sinking 48 mA and a TTL compatible receiver with hysteresis.				
SRQ	8	Y.180	Service Request: Processor GPIB bus control line; used by a device to indicate the need for service and to request an interruption of the current sequence of events on the GPIB. It is a TTL compatible input.				
SRQ*	16	0					
REN	6	esvisi noo l	Remote Enable: Processor GPIB bus control line; used by a controller (in con- junction with other messages) to select between two alternate sources of device programming data (remote or local con- trol). This output is TTL compatible.				
REN*	13	I Igno	Remote Enable: IEEE GPIB bus controlline. This input is a TTL compatible Schmitt-trigger.				
ATN  //  //  //  //  //  //  //  //  //	4 not	0	Attention: Processor GPIB bus control line; used by the 8291 to determine how data on the DIO signal lines are to be interpreted. This is a TTL compatible output.				
ATN*	19	904 s 619 si	Attention: IEEE GPIB bus control line this input is a TTL compatible Schmittrigger.				
IFC OF DE BONS AND ADDRESS AND		0	Interface Clear: Processor GPIB bus control line; used by a controller to place the interface system into a known quiescent state. It is a TTL compatible output.				

Symbol	Pin No.	Туре	allst 8190 Aresa letel ent cosh				
IFC* (BIS	12	b Ls s abe	Interface Clear: IEEE GPIB bus controlline. This input is a TTL compatible Schmitt-trigger.				
T/RIO1 T/RIO2	11 23	eud s	Transmit Receive General IO: Direction control for the two spare transceivers. These pins are TTL compatible				
GIO1 GIO2	24 25	I/O I/O	General IO: This is the TTL side of the two spare transceivers. These pins are TTL compatible.				
GIO1* GIO2*	21 22	1/0	General IO: These are spare three state (push-pull) drivers/Schmitt-trigge receivers. The drivers can sink 48 mA				

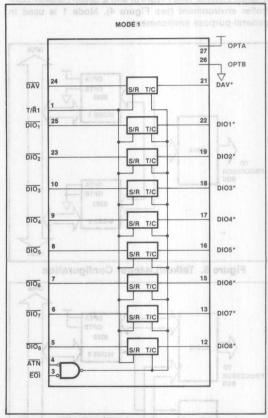


Figure 6. Talker/Listener Data Configuration

Table 4. Mode 1 Pin Description

Symbol	Pin No.	Туре	Name and Function		
T/R1 <sub>1s</sub> is digit be entited by the entitle by the		thw fi n ai be	Transmit Receive 1: Controls the direction for DAV and the DIO lines. It T/R1 is high, then all these lines are sending information to the IEEE GPIE lines. This input is TTL compatible.		
stroller stroller in is TTL us con-	4aiq ii) rosse s rol bee live col tre sequent ii) sequent iii) iii)	n Unis : Proc sthe ne ne ac curre iB bus	End Of Sequence And Attention Processor GPIB control lines. These two control signals are ANDed to gether to determine whether all the transceivers in the 8293 are three state (push-pull) or open-collector When both signals are low (true) then the controller is performing a parallel poll and the transceivers are all open-collector. These inputs are TTL compatible.		
		handshake control line; used cate the condition (availabili validity) of information on the			
DAV*		21 I/O Data Valid: IEEE GPIB bus shake control line. When an i is a TTL compatible Schmitt- When DAV* is an output, it can mA.			
DIO1- DIO8	25, 23, 10, 9, 8, 7, 6, 5	10, 9, bus data lines; used to carry and data bytes in a bit-para serial form controlled by thandshake signals. These			
	22, 19, 18, 17, 16, 15, 13, 12	1/0° 01 SES 177 2	Data Input/Output: IEEE GPIB bus data lines. They are TTL compatible Schmitt-triggers when used for input and can sink 48 mA when used for output. See ATN and EOI description for output mode.		

MODE 2 OPTA 26 T OPTR 18 NDAC NDAC\* 17 NRED NRFD\* T/R1 12 IEC\* IFC SYC 13 REN REN\* SRQ\* SRQ 11 ATNI ATN\* A | ATN EOI\* EOI2 ATNO FOI T/R2 IFCL CLTH CIC NOTE: FUNCTION OF ATN TRANSCEIVER S/R = LOW S/R - HIGH ATNI = ATN\* ATN = ATN\* ATNI = ATNO ATN = HIGH ATN = INPUT
ATNO = INPUT ATN\* = ATNO ATNO = INPUT

Figure 7. Talker/Listener/Controller Control

Translat Configuration W.sail lible Schmitt-trigger. When an



Table 5. Mode 2 Pin Description

Symbol	Pin No.	Туре	Name and Function				
T/R1	1 L	1 25 20	Transmit Receive 1: Direction contro for NDAC and NRFD. If T/R1 is high, ther NDAC and NRFD are receiving. Input is TTL compatible.				
NDAC	10	I/O	Not Data Accepted: Processor GPIE bus handshake control line; used to in dicate the condition of acceptance o data by device(s). This pin is TTL compatible.				
NDAC*	18	I/O	Not Data Accepted: IEEE GPIB but handshake control line. It is a TTL compatible Schmitt-trigger when used fo input and an open-collector driver with a 48 mA current sink capability when used for output.				
NRFD	9	I/O	Not Ready For Data: Processor GPIE bus handshake control line; used to in dicate the condition of readiness of de vice(s) to accept data. This pin is TTI compatible.				
NRFD*	17	I/O	Not Ready For Data: IEEE GPIB but handshake control line. It is a TTL compatible Schmitt-trigger when used fo input and an open-collector driver with a 48 mA current sink capability when used for output.				
syc <sup>1</sup>	22	1	System Controller: Used to monitor the system controller switch and control the direction for IFC and REN. This pin is a TTL compatible input.				
REN	tro (in to s of		Remote Enable: Processor GPIB con trol line; used by the active controlle (in conjunction with other messages to select between two alternate sources of device programming data (remote o local control). This pin is TTL compatible.				
REN*	13	I/O	Remote Enable: IEEE GPIB bus controlline. When used as an input, this is a TTL compatible Schmitt-trigger. When aroutput, it is a three-state driver with a 48 mA current sinking capability.				
ĪFC	5	I/O	Interface Clear: Processor GPIB bus control line; used by the active con- troller to place the interface system into a known quiescent state. This pin is TTL compatible.				
IFC*	12	I/O	Interface Clear: IEEE GPIB cont line. This is a TTL compatible Schm trigger when used for input and a thre state driver capable of sinking 48 r current when used for output.				
CIC	24	I	Controller In Charge: Used to control the direction of the SRQ and to indicate that the 8292 is in charge of the bus. CIC is a TTL compatible input.				

Symbol	Pin No.	Туре	Name and Function				
CLTH <sup>1</sup> -(b) orit e 11 . senit ens seni	DIO ese	Clear Latch: Used to clear the ceived latch after it has been rec by the 8292. Normally low (excep hardware reset). It will be puls when IFC Received is recognize 8292. This input is TTL compati					
ĪFCL	25	0	IFC Received Latch: The 8292 monitors the IFC line when it is not the active controller through this pin.				
SRQ notocke (sunt) a galant	en-na e lov	or or als at	Service Request: Processor GPIB control line; indicates the need for attention and requests the active controller to interrupt the current sequence of events on the GPIB bus. This pin is TTL compatible.				
sRQ*//u	io n	nsesor soli lice	Service Request: IEEE GPIB bus control line. When used as an input, this pin is a TTL compatible Schmitt-trigger. When used as an output, it is an opencollector driver with a 48 mA current sinking capability.				
T/R2	-	ide <b>t</b> ine ine ani	rection for EOI. This input is TTL conpatible.				
ATNO SALANIE I	iso fi aasoi i yrts	surpus at: Per	Attention Out: Processor GPIB bus control line; used by the 8292 for ATN control of the IEEE bus during "take control synchronously" operations. A low on this input causes ATN to be asserted if CIC indicates that this 8292 is in charge. ATNO is a TTL compatible input.				
ATNI	110	0	Attention In: Processor GPIB bus control line; used by the 8292 to monitor the ATN line. This output is TTL compatible.				
ATN age	o 4 J	TOns	Attention: Processor GPIB bus control line; used by the 8292 to monitor the ATN line. This output is TTL compatible.				
ATN*	19	I/O	Attention: IEEE GPIB bus control line; used by a controller to specify how data on the DIO signal lines are to be interpreted and which devices must respond to data. When used as an output, this pin is a three-state driver capable of sinking 48 mA current. As an input, it is a TTL compatible Schmitt-trigger.				
EOI2	7	I/O	End Or Identify 2: Processor GPIB bus control line; used in conjunction with ATN by the active controller (the 8292) to execute a polling sequence. This pin is TTL compatible.				
EOI	3	1/0	End Or Identify: Processor GPIB bus control line; used by a talker to indicate the end of a multiple byte transfer sequence. This pin is TTL compatible.				

#### NOTES:

V<sub>IL3</sub> is guaranteed at 1.1V on these inputs to accommodate the high current-sourcing capability of these pins during a low input in Mode 2.



Table 5. Mode 2 Pin Description (Continued)

Symbol	Pin No.	Туре	Name and Function
EOI*	15	1/0	End Or Identify: IEEE GPIB bus control line; used by a talker to indicate the end of a multiple byte transfer sequence or, by a controller in conjunction with ATN, to execute a polling sequence. When an output, this pin can sink 48 mA current. When an input, it is a TTL compatible Schmitt-trigger.

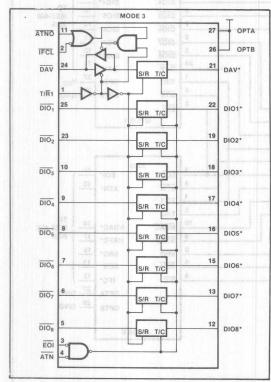


Figure 8. Talker/Listener/Controller Data Configuration

Table 6. Mode 3 Pin Description

Symbol	Pin No.	Туре	Name and Function					
T/R1	1		Transmit Receive 1: Controls the direction for DAV and the DIO lines. I T/R1 is high, then all these lines are sending information to the IEEE GPIB lines. This input is TTL compatible.					
EOI ATN	3 4	APS	End Of Sequence and Attention Processor GPIB control lines. Thes two control lines are ANDed togethe to determine whether all the transceivers in the 8293 are push-pull of open-collector. When both signal are low (true), then the controller in performing a parallel poll and the transceivers are all open-collector. These inputs are TTL compatible.					
ATNO	trol line; used by the 8292 c "take control synchronously" c tions. This pin is TTL compatil							
IFCL	2	1	Interface Clear Latched: Used to make DAV received after the system controller asserts IFC. This input in TTL compatible.					
DAV* 21 I/O			Data Valid: Processor GPIB hand shake control line; used to indicate the condition (availability and validity) of information on the DIC signals. This pin is TTL compatible.					
			Data Valid: IEEE GPIB handshake control line. When an input, this pin is a TTL compatible Schmitt-trigger When DAV* is an output, it can sink 46 mA.					
DIO1- DIO8	25, 23, 10, 9, 8, 7, 6, 5	I/O	Data Input/Output: Processor GPIE bus data lines; used to carry message and data bytes in a bit-parallel byte serial from controlled by the three handshake signals. These lines are TTL compatible.					
DIO1* DIO8*	22, 19, 18, 17, 16, 15, 13, 12	I/O	Data Input/Output: IEEE GPIB bus data lines. They are TTL compatible Schmitt-triggers when used for inpu and can sink 48 mA when used for output.					

Figure 9. 8291A and 8293 System Configuration

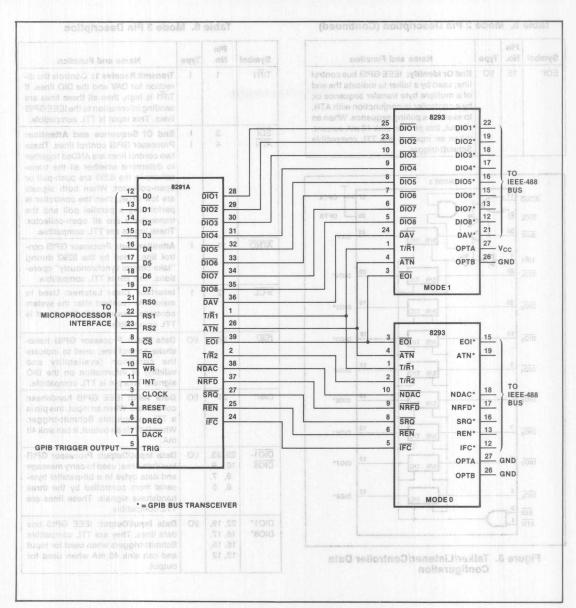


Figure 9. 8291A and 8293 System Configuration

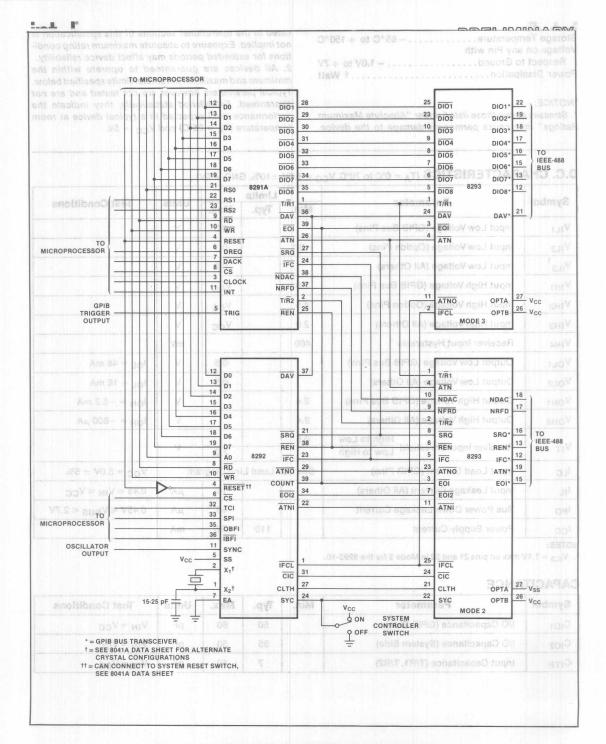


Figure 10. 8291A, 8292, and 8293 System Configuration



#### **ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias . . . . . . . . 0°C to 70°C Storage Temperature..... - 65°C to + 150°C Voltage on any Pin with Respect to Ground..... - 1.0V to +7V Power Dissipation.....1 Watt

#### \*NOTICE:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. 2. All devices are guaranteed to operate within the minimum and maximum parameter limits specified below. Typical parameters however are not tested and are not guaranteed. Established statistically, they indicate the performance level expected in a typical device at room temperature ( $T_A = 25^{\circ}$ C) and  $V_{CC} = 5V$ .

#### D.C. CHARACTERISTICS ( $T_A = 0^{\circ}C$ to $70^{\circ}C$ , $V_{CC} = 5.0V \pm 10^{\circ}$ , GND = 0V)

0	sold sold s	1 80K	Limits	22 83		To at Oan distance
Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
V <sub>IL1</sub>	Input Low Voltage (GPIB Bus Pins)	EOI 103		0.8	V	
V <sub>IL2</sub>	Input Low Voltage (Option Pins)	-0.1		0.1	V	TO T
V <sub>IL3</sub> <sup>1</sup>	Input Low Voltage (All Others)	1FC 24		0.8	V	
V <sub>IH1</sub>	Input High Voltage (GPIB Bus Pins)	2.0	8	Vcc	V	
V <sub>IH2</sub>	Input High Voltage (Option Pins)	4.5		Vcc	V	8190
V <sub>IH3</sub>	Input High voltage (All Others)	2.0		Vcc	V	тичтио
V <sub>IH4</sub>	Receiver Input Hysteresis	400			mV	
V <sub>OL1</sub>	Output Low Voltage (GPIB Bus Pins)	70		0.5	V	I <sub>OL</sub> = 48 mA
V <sub>OL2</sub>	Output Low Voltage (All Others)	Vac		0.5	V	I <sub>OL</sub> = 16 mA
V <sub>OH1</sub>	Output High Voltage (GPIB Bus Pins)	2.4		so at	V	I <sub>OH</sub> = -5.2 mA
V <sub>OH2</sub>	Output High Voltage (All Others)	2.4		17 00	V	$I_{OH} = -800  \mu A$
VIT SUB	High to Low	0.8		ag   87,	V	
VIT and	Receiver Input Threshold Low to High	05 700	5228	2.0	V	
ILC	Input Load Current (GPIB Pins)	See Bu	s Load L	ine Diagr	am	$V_{CC} = 5.0V \pm 5\%$
I <sub>IL</sub>	Input Leakage Current (All Others)	78 210	11 CD	10	μΑ	0.45 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
IPD	Bus Power Down Leakage Current	7N1		40	μΑ	0.45V ≤ V <sub>BUS</sub> ≤ 2.7V
lcc	Power Supply Current		110	175	mA	CROPROCESSOR

#### CAPACITANCE

Symbol	Parameter ppv	Min.	Тур.	Max.	Units	Test Conditions
C <sub>IO1</sub>	I/O Capacitance (GPIB Side)		50	80	pF	VIN = VCC
C <sub>102</sub>	I/O Capacitance (System Side)		35	50	pF	VIN = VCC
CITR	Input Capacitance (T/R1, T/R2)		7	,но10 а т	pF	VIN = VCC

<sup>1.</sup>  $V_{IL3} = 1.1V$  max on pins 21 and 22 in Mode 2 for the 8293-10.



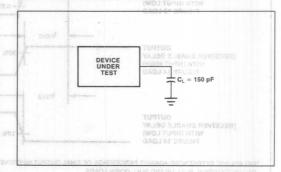
#### A.C. CHARACTERISTICS (T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5.0V ±10%, GND = 0V)

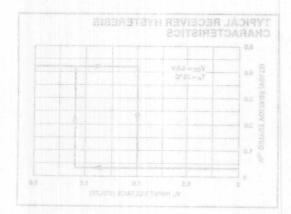
Symbol	Parameter	Max.	Units
t <sub>P1</sub>	Transmitter Propagation Delay (All Lines)	30	ns
t <sub>P2</sub>	Receiver Propagation Delay (EOI, ATN and Handshake Lines)	50	ns
t <sub>P3</sub>	Receiver Propagation Delay (All Other Lines)	60	ns
t <sub>PHZ1</sub>	Transmitter Disable Delay (High to 3-State)	40	ns
<sup>t</sup> PZH1	Transmitter Enable Delay (3-state to High)	40	ns
t <sub>PLZ1</sub>	Transmitter Disable Delay (Low to 3-State)	40	ns
tPZL1	Transmitter Enable Delay (3-State to Low)	40	ns
tPHZ2	Receiver Disable Delay (High to 3-State)	40	ns
tPZH2	Receiver Enable Delay (3-State to High)	40	ns
t <sub>PLZ2</sub>	Receiver Disable Delay (Low to 3-State)	40	ns
tPZL2	Receiver Enable Delay (3-State to Low)	40	ns
tMS	Mode Switch Delay	10	μs

#### A.C. TESTING INPUT, OUTPUT WAVEFORM

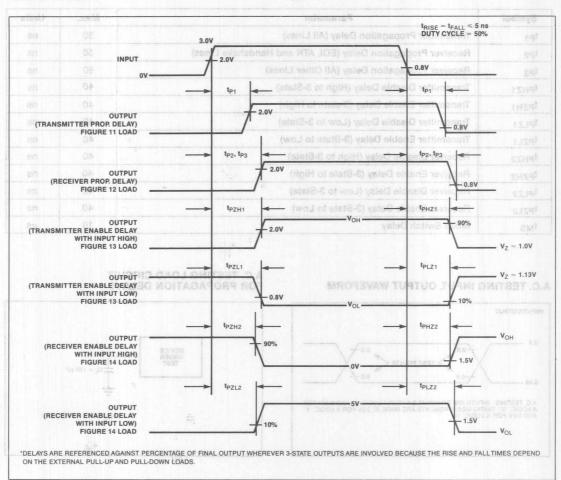
# 2.4 2.0 TEST POINTS 0.45 A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

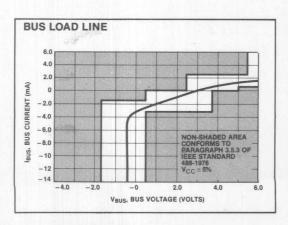
#### A.C. TESTING LOAD CIRCUIT FOR PROPAGATION DELAYS

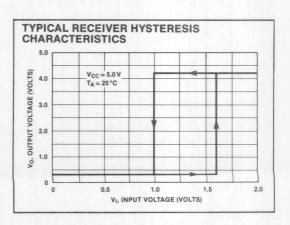












#### PROGRAMMABLE INTERVAL TIMER

m MCS-85™ Compatible 8253-5

# 3 Independent 16-Bit Counters

1 ...

e Single + 5Y Supply

a Count Binary or BCD

MERC OF DELLA

#### a Programmable Counter Modes

m 24-Pin Dual In-Line Package

The Intel® 8253 is a programmable counterfilmer chip designed for use as an Intel microcomputer peripheral. It uses a microcomputer single +5V supply and is packaged in a 24-pln plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MMz. All modes of operation are softwere programmable.

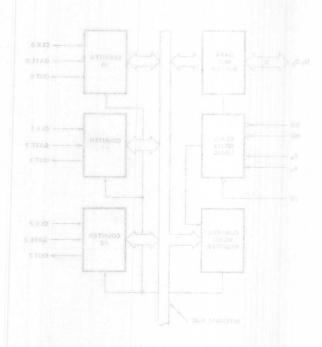


Figure 1. Block Diagram



Figure 2. Pin Configuration



# 8253/8253-5 PROGRAMMABLE INTERVAL TIMER

- MCS-85<sup>TM</sup> Compatible 8253-5
- **Count Binary or BCD**
- 3 Independent 16-Bit Counters
- Single + 5V Supply

- DC to 2 MHz
- Programmable Counter Modes
- 24-Pin Dual In-Line Package

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

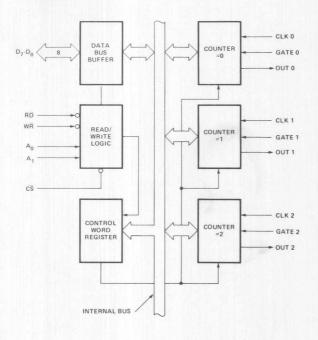




Figure 1. Block Diagram

Figure 2. Pin Configuration



#### **FUNCTIONAL DESCRIPTION**

#### General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- . Binary Rate Multiplier
- · Real Time Clock
- · Digital One-Shot
- Complex Motor Controller

#### **Data Bus Buffer**

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

- 1. Programming the MODES of the 8253.
- 2. Loading the count registers.
- 3. Reading the count values.

#### Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

#### RD (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

#### WR (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading

#### A0. A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection. CS (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The CS input has no effect upon the actual operation of the

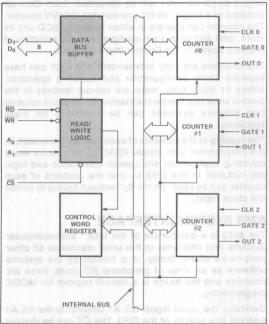


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

CS	RD	WR	A <sub>1</sub>	A <sub>0</sub>	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State



#### **Control Word Register**

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

#### Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

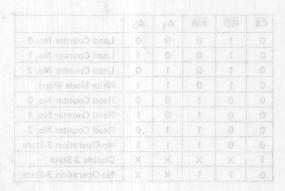
The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

#### 8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral №O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The  $\overline{CS}$  can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.



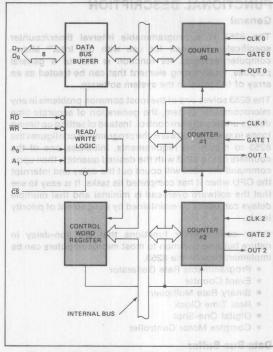


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

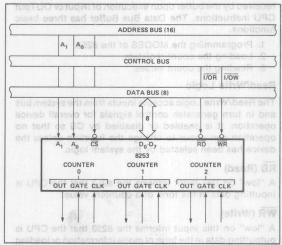


Figure 5. 8253 System Interface

#### OPERATIONAL DESCRIPTION

#### General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words <u>must</u> be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

#### **Programming the 8253**

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

#### **Control Word Format**

į								D <sub>0</sub>	
The second	SC1	SC0	RL1	RL0	M2	M1	MO	BCD	

#### **Definition of Control**

#### SC - Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

#### RL - Read/Load:

#### RL1 RL0

0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M2	M1	MO
_		

0	0	0	Mode 0
0	0	1,0	Mode 1
X	10130	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

#### BCD

0	Binary Counter 16-bits
danoi I one	Binary Coded Decimal (BCD) Counter (4 Decades)

#### Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

#### **MODE Definition**

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

- (1) Write 1st byte stops the current counting.
- (2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

MODE 1: Programmable One-Shot. The outs

The output will go high on the terminal count. It a new count value is loaded while the output is low if will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the

white innibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

Signal Status Modes	Low Or Going Low	nat the back tonitoring and us evenishor t	
0	Disables counting	stenimile need e	Enables counting
rammed by the s.	nunter are prog	Initiates     counting     Resets output     after next clock	H of the M
.nate <sup>2</sup> gan bro	Disables     counting     Sets output     immediately     high	1) Reloads counter 2) Initiates counting	Enables counting
D3 FG	Disables     counting     Sets output     immediately     high	Initiates 3	Enables
4	Disables counting	toTmo0 to	Enables counting
5		Initiates counting	0 - 5918

Figure 6. Gate Pin Operations Summary

	RLO	1.11
Counter Latching operation (see READ/WRITE Procedure Section)	0	
Read Load most significant byte only		
Read/Load least significant byte only.		
Read/Load least significant byte first, then exect significant byte.		





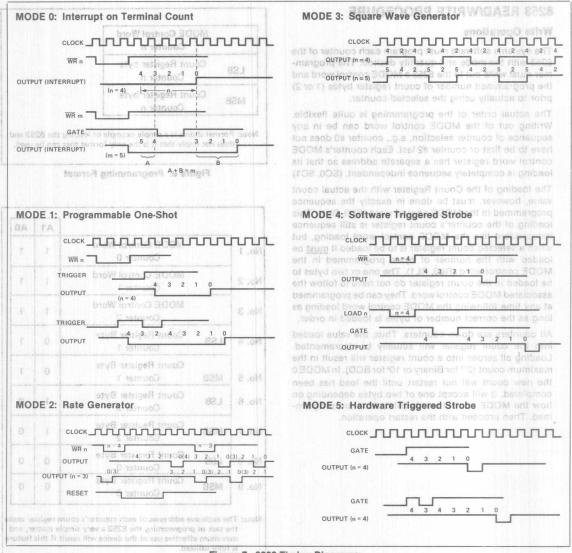


Figure 7. 8253 Timing Diagrams



#### 8253 READ/WRITE PROCEDURE

#### **Write Operations**

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it <u>must</u> be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (216 for Binary or 104 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RLO, RL1) are programmed. Then proceed with the restart operation.

uu	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 8. Programming Format

			A1	AO
No. 1	חחח	MODE Control Word Counter 0	1	1
No. 2	0 1	MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	3130	0
No. 7	MSB	Count Register Byte Counter 2	0 1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 9. Alternate Programming Formats

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0. A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB). second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Test Conditions	Unit	
fc = 1 MHz		
Unmeasured pins returned to		

A1	A0	RD	
0	0	0,	Read Counter No. 0
10-050	o°aa1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
I Mai	1	0	Illegal inscission rework

#### **Reading While Counting**

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

#### **MODE Register for Latching Count**

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	DO
SC1	SC0	0	0	X	Х	X	X

SC1,SC0 — specify counter to be latched.

D5,D4 — 00 designates counter latching operation.

- don't care. some hosped rugal

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.

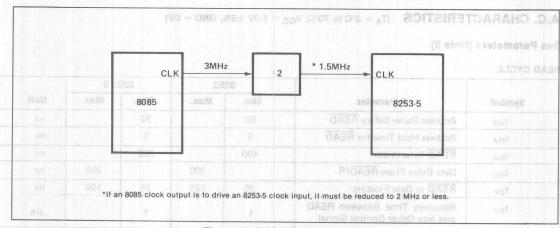


Figure 10. MCS-85™ Clock Interface\*

# **ABSOLUTE MAXIMUM RATINGS**

Ambient Temperature Under Bias	. 0°C to 70°C
	65° C to +150° C
Voltage On Any Pin With Respect to Ground	-0.5 V to +7 V
Power Dissipation	1 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# D.C. CHARACTERISTICS (TA = 0°C to 70°C, V<sub>CC</sub> = 5V ±10%)

Symbol	pharmino Parameter a prizu bezas	as Min.	Max.	Unit	Test Conditions
VIL	Input Low Voltage	-0.5	8.0	em avu al	1-11). The only requirement w
aVinus launiVs	w Input High Voltage w 1972 per ECC	2.2	V <sub>CC</sub> +.5V	V	der to assure a stable countre.
VoL	Output Low Voltage	as as	0.45	sellVneix	ontrolling the Gate I stoN by
Voн	Output High Voltage	2.4	r selected w	ine Vunie	Note 2
steined regipte	Input Load Current	98	±10	μА	V <sub>IN</sub> = V <sub>CC</sub> to 0V
I <sub>OFL</sub>	Output Float Leakage	el	±10	μΑ	Vout = Vcc to 0V
Icc	V <sub>CC</sub> Supply Current	084	140	mA	ASB).

# CAPACITANCE (TA = 25°C, VCC = GND = 0V)

05 D4 D3 D2 D1 D6

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
CIN	Input Capacitance	b	X	10	pF	fc = 1 MHz
C <sub>1/O</sub>	I/O Capacitance	imil ems	edT	20	pF	Unmeasured pins returned to V <sub>SS</sub>

# A.C. CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5.0V ±5%, GND = 0V)

**Bus Parameters** (Note 3)

#### READ CYCLE

		8:	253	82	53-5	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t <sub>AR</sub>	Address Stable Before READ	50		30		ns
t <sub>RA</sub>	Address Hold Time for READ	5	1	5		ns
t <sub>RR</sub>	READ Pulse Width	400	- Box	300		ns
t <sub>RD</sub>	Data Delay From READ [4]		300		200	ns
t <sub>DF</sub>	READ to Data Floating	25	125	25	100	ns
t <sub>RV</sub>	Recovery Time Between READ and Any Other Control Signal	1		1		μs





# A.C. CHARACTERISTICS (Continued)

#### WRITE CYCLE

	OKIMIT GABR	83	253	825	53-5	STIRW
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t <sub>AW</sub>	Address Stable Before WRITE	50		30		ns
t <sub>WA</sub>	Address Hold Time for WRITE	30	Ty-	30	V	ns
tww	WRITE Pulse Width	400		300		ns
t <sub>DW</sub>	Data Set Up Time for WRITE	300		250		ns
t <sub>WD</sub>	Data Hold Time for WRITE	40		30		ns
t <sub>RV</sub>	Recovery Time Between WRITE and Any Other Control Signal	1	- N	11		μs

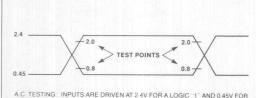
#### **CLOCK AND GATE TIMING**

		82	53	82	253-5	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tCLK	Clock Period	380	dc	380	dc	ns
tpWH	High Pulse Width	230		230		ns
tpWL	Low Pulse Width	150		150		ns
tgw	Gate Width High	150		150		ns
tGL	Gate Width Low	100		100		ns
t <sub>GS</sub>	Gate Set Up Time to CLK↑	100/	X =	100	CER /	ns
t <sub>GH</sub>	Gate Hold Time After CLK↑	50		50		ns
top	Output Delay From CLK↓[4]	7	400		400	ns
todg	Output Delay From Gate↓[4]	in the same of the	300	Military of the Control	300	ns

#### NOTES:

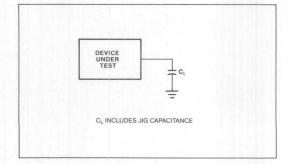
- 1.  $I_{OL} = 2.2$  mA. 2.  $I_{OH} = -400 \, \mu A$ . 3. AC timings measured at  $V_{OH}$  2.2,  $V_{OL} = 0.8$ . 4.  $C_L = 150 pF$ .

# A.C. TESTING INPUT, OUTPUT WAVEFORM



A C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

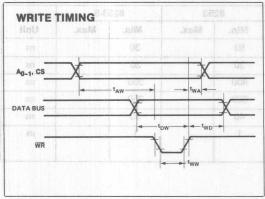
# A.C. TESTING LOAD CIRCUIT



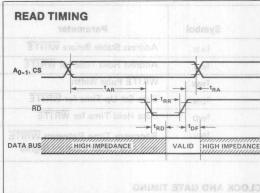


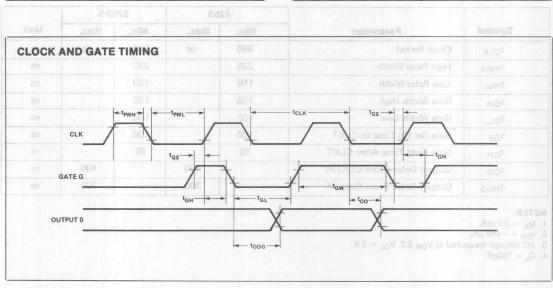


### **WAVEFORMS**

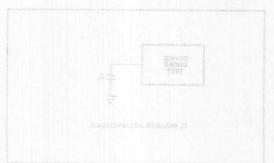








LC. TESTING LOAD CIRCUIT



A.C. TESTING INPUT, OUTPUT WAVEFORM





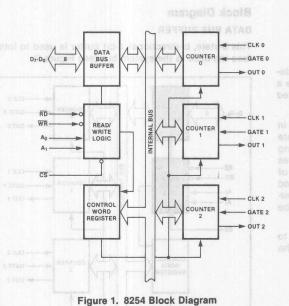
# 8254 Programmable Interval Timer

- Compatible with Most Microprocessors Including 8080A, 8085A, iAPX 88 and iAPX 86
- Handles Inputs from DC to 5 MHz(10 MHz for 8254-2)
- Six Programmable Counter Modes
- Status Read-Back Command

- Three Independent 16-bit Counters
- **■** Binary or BCD Counting
- Single +5V Supply
- Uses HMOS Technology

The Intel® 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable.

The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.



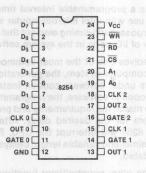


Figure 2. Pin Configuration



Table	15	Pin	Descrip	otion
-------	----	-----	---------	-------

	Туре	Name and Function
1-8	1/0	Data: Bi-directional three state data bus lines, connected to system data bus.
9	1	Clock 0: Clock input of Counter 0.
10	0	Output 0: Output of Counter 0.
11	1	Gate 0: Gate input of Counter 0.
12	0	Ground: Power supply connection.
		e Single +5V Supply
	V	u Uses HMOS Technolo
		he common timing control proble each capable of handling clock in
		atic or CERDIP package.
	9 10 0 11 12	9   1   10   0   0   1   1   1   1   1

Symbol	Pin No.	Туре	- C3	Nam	e and Function
V <sub>CC</sub>	24	100	Power: -	-5V pov	wer supply connection.
WR	23	1	Write Co		his input is low during CPU s.
RD	22	main nan	Read Co		nis input is low during CPU
CS	21	1	8254 to 1	respond	to RD and WR signals. RD pred otherwise.
A <sub>1</sub> , A <sub>0</sub>	20-19	O RO	Counters read or	s or the	to select one of the three Control Word Register for operations. Normally con- stem address bus.
2.0	boli	nein	A A	A <sub>0</sub>	Selects Selects
			0	0	Counter 0
	12	18111	0	Hat o	Counter 1
	viseh s	nhyah-	1	1	Control Word Register
CLK 2		-	Clock 2:	Clock i	nput of Counter 2.
OUT 2	17	0.8	Out 2: 0	utput of	Counter 2.9 9 8 8 8 9 9 9 9 9
GATE 2	16	n Hos	Gate 2: 0	Gate inp	out of Counter 2.
CLK 1	15	1	Clock 1:	Clock i	nput of Counter 1.
	14	1	Gate 1: 0	Gate inc	out of Counter 1.
GATE 1	1.4				

#### **FUNCTIONAL DESCRIPTION**

#### General

The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are:

- · Real time clock
- Event counter
- · Digital one-shot
- · Programmable rate generator
- · Square wave generator
- · Binary rate multiplier
- · Complex waveform generator
- · Complex motor controller

# **Block Diagram**

# DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 8254 to the system bus (see Figure 3).

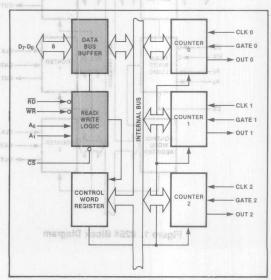


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions



#### READ/WRITE LOGICOTT 180230 JAMOS ARBOO

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 8254. A<sub>1</sub> and A<sub>0</sub> select one of the three counters or the Control Word Register to be read from/written into, A "low" on the  $\overline{\text{RD}}$  input tells the 8254 that the CPU is reading one of the counters. A "low" on the  $\overline{\text{WR}}$  input tells the 8254 that the CPU is writing either a Control Word or an initial count. Both  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  are ignored unless the 8254 has been selected by holding  $\overline{\text{CS}}$  low.

#### CONTROL WORD REGISTER

The Control Word Register (see Figure 4) is selected by the Read/Write Logic when  $A_1, A_0 = 11$ . If the CPU then does a write operation to the 8254, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

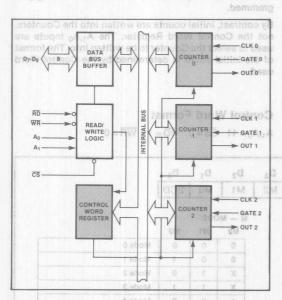


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

#### **COUNTER 0, COUNTER 1, COUNTER 2**

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 5.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

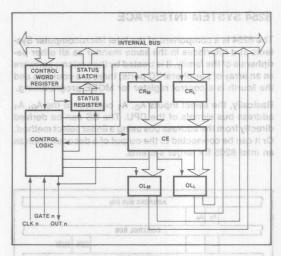


Figure 5. Internal Block Diagram of a Counter-

The status register, shown in the Figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presettable synchronous down counter.

 ${\sf OL_M}$  and  ${\sf OL_L}$  are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 8254, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called  $CR_M$  and  $CR_L$  (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously.  $CR_M$  and  $CR_L$  are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

e figure; it is

The Control Logic is also shown in the diagram. CLK n, ts determine

GATE n, and OUT n are all connected to the outside world through the Control Logic.



#### 8254 SYSTEM INTERFACE

The 8254 is a component of the Intel Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs  $A_0$ ,  $A_1$  connect to the  $A_0$ ,  $A_1$  address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.

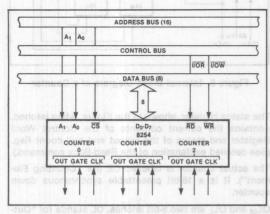


Figure 6. 8254 System Interface

#### OPERATIONAL DESCRIPTION

# General o theies AA bas AA A828 ent to shoold landit

After power-up, the state of the 8254 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

## Programming the 8254 north placed with Whose R and

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when  $A_1,A_0=11$ . The Control Word itself specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The  $A_1,A_0$  inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

#### **Control Word Format**

 $A_1,A_0=11$   $\overline{CS}=0$   $\overline{RD}=1$   $\overline{WR}=0$ 

			D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	Do	
		e thuco mea	SC1	SC0	RW1	RW0	M2	M1	MO	BCD	
c – s	elect	Counter:					3.1	M — N	IODE:	MO	
(	)	0	Select C	ounter 0	Ands.			0	0	0	Mode 0
(	)	1						0	0	1	Mode 1
an I	1	0	Select Counter 2					X	1	0	Mode 2
neter	yitaa	Seth ark norm	Read-Back Command (See Read Operations)					X	1	1	Mode 3
el anti-	CO W	en acherry 25	od just c					1	0	0	Mode 4
W — F	Read/V	viile.	the CE.					1	0	Soft Cold	Mode 5
0	0	Counter Late Operations)	h Commai	nd (see F	Read			BCD:		NTER:	ER 6, COUNTER 1, COU
0	1	Read/Write le	ast signifi	cant byt	e only.			0	n isat	Binary C	ounter 16-bits
lidple	0	Read/Write m	ost signifi	cant byt	e only.			1	T down	Binary Co	oded Decimal (BCD) Counter
st to	9/13	Read/Write le			e first,				1 AMO	(4 Decade	es) 00 signic a 10 margai
	W BC	then most sig	gnificant b	yte.	0183					dent. E.	negebni vilut ans diesna

Figure 7. Control Word Format



# Write Operations and at Naca ent to enumed rentionA

The programming procedure for the 8254 is very flexible. Only two conventions need to be remembered:

- For each Counter, the Control Word must be written before the initial count is written.
- 2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A<sub>1</sub>,A<sub>0</sub> inputs), and each Control Word specifies the Counter it applies to (SC0,SC1 bits), no special instruction sequence is re-

quired. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Control Word — Counter 2 1 1 Control Word — Counter 1 1 1 Control Word — Counter 0 1 1
Control Word - Counter 0 1 1
Control Word — Counter o
LSB of count — Counter 2 1 0
MSB of count — Counter 2 1 0
LSB of count — Counter 1 0 1
MSB of count — Counter 1 0 1
LSB of count — Counter 0 0 0 0
MSB of count — Counter 0 0 0
DON'T DARE SITS ON SHOULD BE DITO INCURE COMPATIBILITY WITH PUTURE INTEL PRODUCTS.
A <sub>1</sub> A <sub>0</sub>
Control Word — Counter 1 1 1
Control Word — Counter 0 1 1
LSB of count — Counter 1 0 1
Control Word — Counter 2 1 1
LSB of count — Counter 0 0 0
MSB of count — Counter 1 0 0 1 1
LSB of count — Counter 2
MSB of count — Counter 0 0 0
MSB of count — Counter 2 1 0
is to "following" the counting element (CE). This is reading the contents of the Counters "on the fly".
TE TWO-BYTE COUNTS. good at gallinuoo galloetis du

ent 10) been at it time blee at 1 Figure 8. A Few Possible Programming Sequences to abow permanagor and toellas vilicottempors at termino program at the programming Sequences to a possible programming Sequences to a

#### **Read Operations**

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 8254.

There are three possible methods for reading the Counters. The first is through the Read-Back command,

which is explained later. The second is a simple read operation of the Counter, which is selected with the A<sub>1</sub>,A<sub>0</sub> inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

# int a lanca access

The other method involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when  $A_1, A_0 = 11$ . Also like a Control Word, the SC0,SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

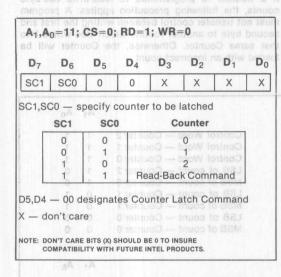


Figure 9. Counter Latching Command Format

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 8254 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

- 1. Read least significant byte.
- 2. Write new least significant byte.
- 3. Read most significant byte.
  - 4. Write new most significant byte.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

#### **READ-BACK COMMAND**

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 10. The command applies to the counters selected by setting their corresponding bits D3,D2,D1=1.

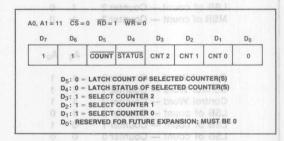


Figure 10. Read-Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the  $\overline{\text{COUNT}}$  bit D5=0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.



The counter status format is shown in Figure 11. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

							D <sub>0</sub>
DUTPUT	COUNT	RW1	RW0	M2 0	M1	MO	BCD
	COUNT						A
	D <sub>7</sub> 1 = 0	UT PIN	IS 1				
-	De 1 = N	ULL CO					

Figure 11. Status Byte

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 12.

	THIS ACTION:	CAUSES:
A.	WRITE TO THE CONTROL WORD REGISTER:[1]	NULL COUNT=1
B.	WRITE TO THE COUNT REGISTER (CR);[2]	NULL COUNT=1
C.	NEW COUNT IS LOADED INTO CE (CR→CE);	NULL COUNT=0
[1]	ONLY THE COUNTER SPECIFIED BY THE CONTRITS NULL COUNT SET TO 1. NULL COUNT BITS CARE UNAFFECTED.	OL WORD WILL HADE OTHER COUNTE
[2]	IF THE COUNTER IS PROGRAMMED FOR TWO-E SIGNIFICANT BYTE THEN MOST SIGNIFICANT GOES TO 1 WHEN THE SECOND BYTE IS WRITT	BYTE) NULL COU

Figure 12. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5,D4=0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 13.

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	_	mano D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Description at ages palls	Result
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	<b>[1</b> ]	0	15	17	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter

Figure 13. Read-Back Command Example and Island bras broty to ting our settle



If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

CS	RD	WR	A <sub>1</sub>	A <sub>0</sub>	(S) IF THE COUNTER IS PROBRA
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	( <b>1</b> )	0 1	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	d 111 ,a	0.8	ed1 g	Read from Counter 1
0	0	s reput	d div	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	Х	X	X	X	No-Operation (3-State)
0	m <b>1</b> 3)1	cornin	X	Xau	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

#### **Mode Definitions**

The following are defined for use in describing the operation of the 8254.

CLK pulse: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

trigger: a rising edge of a Counter's GATE input.

Counter loading: the transfer of a count from the CR to the CE (refer to the "Functional Description")

#### MODE 0: INTERRUPT ON TERMINAL COUNT

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

- Writing the first byte disables counting. OUT is set low immediately (no clock pulse required)
- 2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

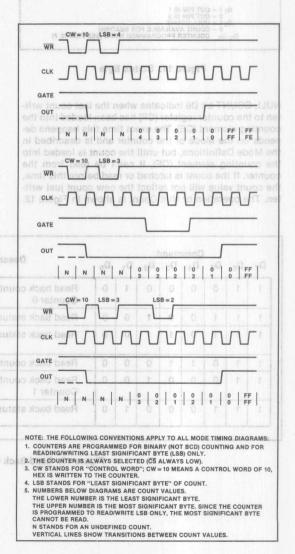


Figure 15. Mode 0



#### MODE 1: HARDWARE RETRIGGERABLE ONE-SHOT

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a oneshot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

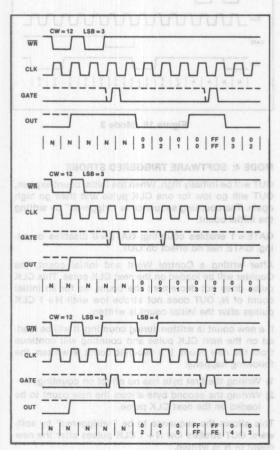


Figure 16. Mode 1

# MODE 2: RATE GENERATOR

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

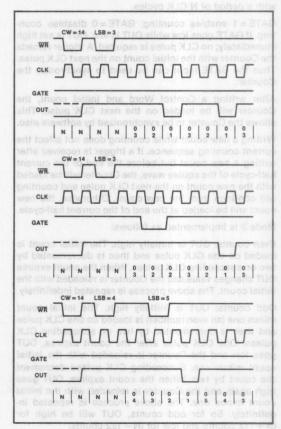


Figure 17. Mode 2

writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.

the same sequence is repeated indefinitely. For an Initial count of N, the sequence repeats every N CLK

GATE = 1 enables counting; GATE = 0 disables counting, if GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N OLK pulses after the trigger. Thus the GATE input can

#### MODE 3: SQUARE WAVE MODE

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N+1)/2 counts and low for (N-1)/2 counts.

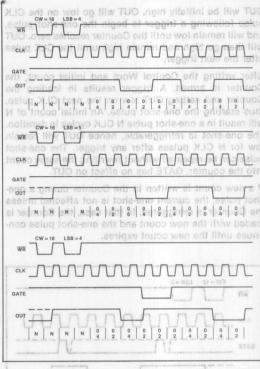


Figure 18. Mode 3

#### **MODE 4: SOFTWARE TRIGGERED STROBE**

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

- 1) Writing the first byte has no effect on counting.
- 2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

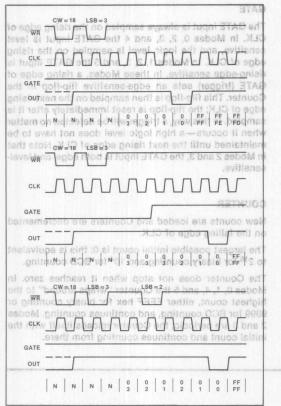


Figure 19. Mode 4

# MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N+1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the curent counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

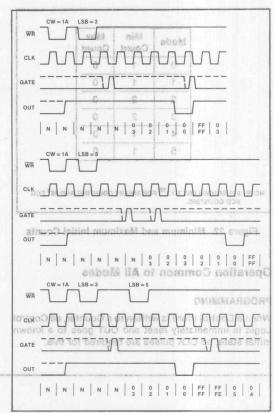


Figure 20. Mode 5

Signal Status Modes	Low Or Going Low	Rising	High	
0	Disables counting	-	Enables counting	
1		Initiates     counting     Resets output     after next clock		
2	Disables     counting     Sets output     immediately     high	Initiates counting	Enables counting Enables counting	
3	Disables     counting     Sets output     immediately     high	Initiates counting		
4	Disables counting		Enables counting	
5		Initiates		

Figure 21. Gate Pin Operations Summary



Mode	Min Count	Max Count
0	4-1-1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 IS EQUIVALENT TO 2<sup>16</sup> FOR BINARY COUNTING AND 10<sup>4</sup> FOR BCD COUNTING.

Figure 22. Minimum and Maximum Initial Counts

# **Operation Common to All Modes**

#### **PROGRAMMING**

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

#### GATE

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs—a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive.

#### COUNTER

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2<sup>16</sup> for binary counting and 10<sup>4</sup> for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

Enables counting				
	t) Initiates counting 2) Resets output after paut officit.			
	infilates counting	Disables counting Sets output Immediately high		
		Disubles counting Sate output immediately bigb		
Enables				
	initiates counting			

(RETRIGGERABLE)

OUT will initially be high. Counting is triggered by a rieng edge of GATE. When the initial count has expired,

OUT will go low for one CLK pulse and then go high

sgain.

Viter writing the Control Word and initial count, the

counter will not be loaded until the CLK pulse after a

rigger. This CLK pulse does not decrement the count,

so for an initial count of N, OUT does not strobe low un
is N + 1 CLK pulses after a trigger.

Figure 19. Meda 4

It is new count is written during counting, the curent counting sequence will not be affected. It a trigger occurs after the new count is written but before the curent count expires, the Counter will be loaded with the lew count on the next CUK pulse and counting will con-

## **ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under	Bias	0°C to 70°C
Storage Temperature	6	5°C to + 150°C
Voltage on Any Pin with Respect to Ground	Min.	
Power Dissipation		1 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

# D.C. CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V <sub>IL</sub> sn	Input Low Voltage	-0.5	0.8 em/	nd ReWovery	ay Comma
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 0.5V	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 2.0 mA
V <sub>OH</sub>	Output High Voltage	(2.4= OND	$V_{GO} = 5V \pm 10\%$	0°07 V 0°0	$I_{OH} = -400 \mu A$
IIL	Input Load Current	8256	±10	μА	V <sub>IN</sub> = V <sub>CC</sub> to 0V
I <sub>OFL</sub>	Output Float Leakage	ws Ail	±10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> to 0V
Icc	V <sub>CC</sub> Supply Current	oa	140	mA	Clock F

# CAPACITANCE (TA=25°C, VCC=GND=0V)

Symbol	con Parameter	oo Min.	Max.	Units	Test Conditions
CIN	Input Capacitance		08 10	pF dgill i	Mf <sub>c</sub> =1 MHz
CI/O	I/O Capacitance		08 20 08	pF WoJ I	Unmeasured pins returned to V <sub>SS</sub>

# **A.C. CHARACTERISTICS** ( $T_A = 0$ °C to 70°C, $V_{CC} = 5V \pm 10$ %, GND = 0V) **Bus Parameters** (Note 1)

#### READ CYCLE

		82	254	8254	1-2		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	
t <sub>AR</sub>	Address Stable Before RD↓	30		25		ns	
t <sub>SR</sub>	CS Stable Before RD↓	0		0		ns	
t <sub>RA</sub>	Address Hold Time After RD↑	0	- A	0	0.5-\-	ns	
t <sub>RR</sub>	RD Pulse Width	150	X	95	ar <	ns	
t <sub>RD</sub>	Data Delay from RD↓[2]		120	.0	70	ns	
t <sub>DF</sub>	RDt to Data Floating	5	90	5	65	ns	
t <sub>RV</sub>	Command Recovery Time	200	F JOOJ A ROSEV	95	AG MEASUREMEN	ns	

Note 1: AC timings measured at V<sub>OH</sub> = 2.0V, V<sub>OL</sub> = 0.8V.

Note 2: Test Conditions: CL = 150 pF.



# A.C. CHARACTERISTICS (Continued)

# WRITE CYCLE bineremed asses yem "agnitud" muxeM

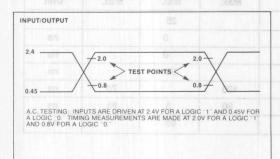
	of the device at these or any other col	825	5411 + of O*81	8254-	rage Tempe	
Symbol	Parameter	Min.	Max.	Min.	Max.	d.Unit egati
t <sub>AW</sub>	Address Stable Before WR↓	0	* CI VC.0	0	biiuaii	ns
tsw	CS Stable Before WR↓	0	Winner	0	vivivi ADII	ns
t <sub>WA</sub>	Address Hold Time WR↑	0		0		ns
tww	WR Pulse Width	150	AF DEDE DE	95	TRIGETS.	ns
t <sub>DW</sub>	Data Setup Time Before WR↑	100		95		ns
t <sub>WD</sub>	Data Hold Time After WR↑	0	lii,	O referred	9	ns
t <sub>RV</sub>	Command Recovery Time 8.0	200	-	95 alloV wo	Lingal -	ns

# CLOCK AND GATE ( $T_A = 0$ °C to 70°C, $V_{CC} = 5V \pm 10$ %, GND = 0V)

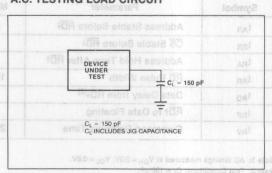
V0 of 00	(	8254		82		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tCLK	Clock Period	200	DC	100	DC	ns oo
t <sub>PWH</sub> <sup>1</sup>	High Pulse Width	60		30		ns
tPWL	Low Pulse Width	60		40		ns
t <sub>R</sub>	Clock Rise Time		100	N Voc=GND=	100	ns
t <sub>F</sub> anollions	Clock Fall Time	xsM	100	remeter	100	ns
tgw	Gate Width High	Ot 50		80 50 as as a	1nput C	ns
t <sub>GL</sub> eniq benut	Gate Width Low	50		50	e-0-00	ns
t <sub>GS</sub> <sup>1</sup>	Gate Setup Time to CLK↑	50		40		ns
t <sub>GH</sub>	Gate Hold Time After CLK↑	50		50		ns
top	Output Delay from CLK↓		150		100	ns
topg	Output Delay from Gate	5V ± 10%, G	120	at 0.0 = 7.0 s	90	ns

#### NOTES:

# A.C. TESTING INPUT, OUTPUT WAVEFORM



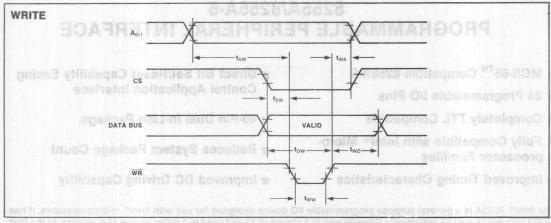
# A.C. TESTING LOAD CIRCUIT

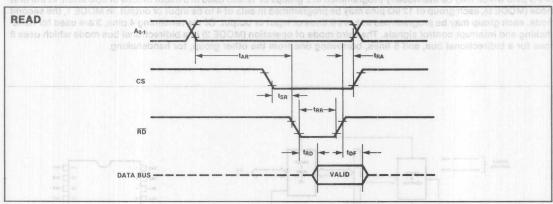


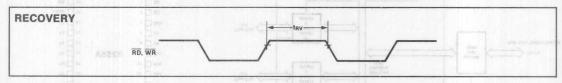
<sup>1.</sup> If the gate input is used asynchronously  $t_{PWH} = 50$  ns,  $t_{GS} = 50$  ns for 8254-2.

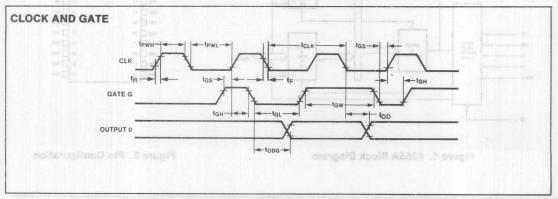


# **WAVEFORMS**











Latri

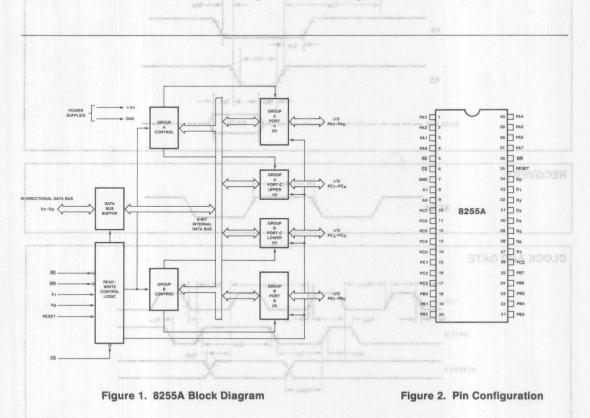
WAVEFORMS

# 8255A/8255A-5 PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85<sup>TM</sup> Compatible 8255A-5
- 24 Programmable I/O Pins
- **Completely TTL Compatible**
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics

- Direct Bit Set/Reset Capability Easing
   Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.



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#### General na . E . A) anog fid-8 parti anistrop A2658 and

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

#### **Data Bus Buffer**

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

# Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

# (CS)

Chip Select. A "low" on this input pin enables the communiction between the 8255A and the CPU.

send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

# (WR)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

# (Ao and A1) upitros tenditorut ent socilatiful ferit cote

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A<sub>0</sub> and A<sub>1</sub>).

## 8255A BASIC OPERATION

A <sub>1</sub>	A <sub>0</sub>	RD	WR	CS	INPUT OPERATION (READ
0	0	0		0	PORT A ⇒ DATA BUS
0	1	0	1	0	PORT B ⇒ DATA BUS
1	0	0	1	0	PORT C ⇒ DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS ⇒ PORT A
0	1	1	0	0	DATA BUS ⇒ PORT B
1	0	1	0	0	DATA BUS ⇒ PORT C
1	1	1	0	0	DATA BUS ⇒ CONTROL
-19					DISABLE FUNCTION
X	X	X	X	1	DATA BUS ⇒ 3-STATE
1	1	0	1 -	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS ⇒ 3-STATE

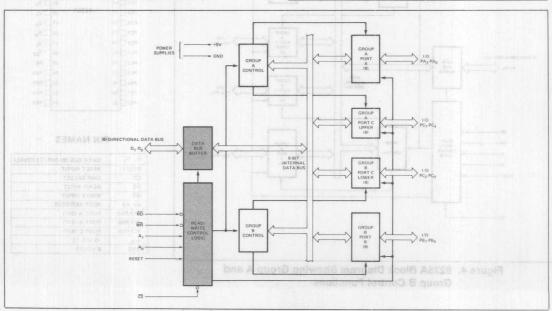


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions



#### (RESET)

Reset. A "high on this input clears the control register and all ports (A, C, C) are set to the input mode.

#### Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A — Port A and Port C upper (C7-C4) Control Group B — Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

# Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch. An ai olgo issue ixe on vilsimon ferit oa

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

#### SUFER TO TOTAL DATA STATE PIN CONFIGURATION OF THE

Read/Write and Control Logic

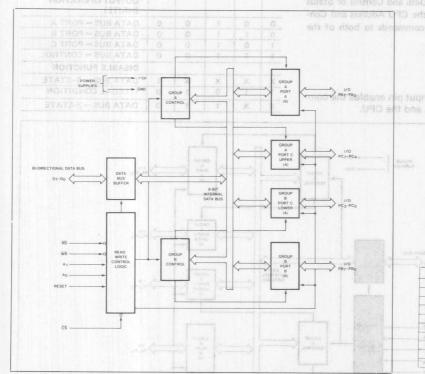


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions



#### PIN NAMES

D, D0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7 PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
Vcc	+5 VOLTS
GND	ØVOLTS

Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Minte Control Logic Functions





#### **Mode Selection**

There are three basic modes of operation that can be selected by the system software:

When Port C Is being used as status/control for Port A or B.

- Mode 0 - Basic Input/Output Jugni (seuper Journal)

Mode 1 - Strobed Input/Output stereo alsopia leaup

Mode 2 - Bi-Directional Bus and patter ve belowie

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

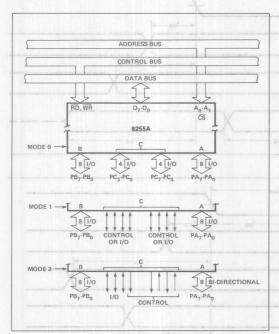


Figure 5. Basic Mode Definitions and Bus Interface

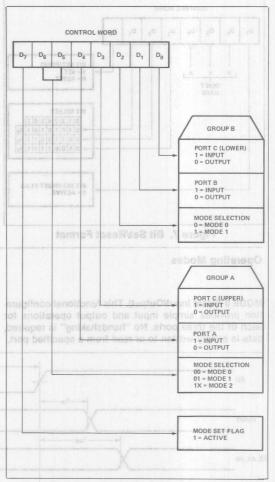


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

#### Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

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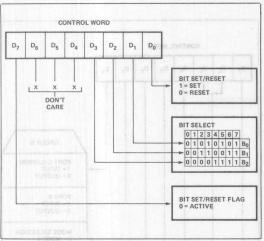


Figure 7. Bit Set/Reset Format

# **Operating Modes**

MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

# Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flipflop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

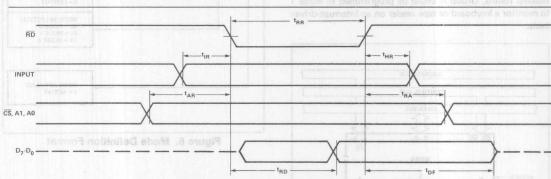
INTE flip-flop definition: Clubexe sat pahud berlupen

(BIT-SET) - INTE is SET - Interrupt enable (BIT-RESET) - INTE is RESET - Interrupt disable

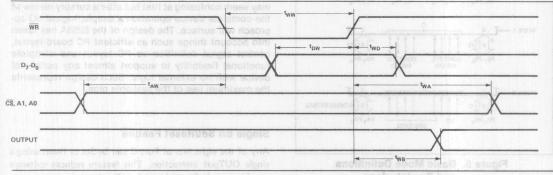
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



#### MODE 0 (Basic Input)



MODE 0 (Basic Output)



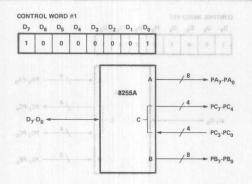


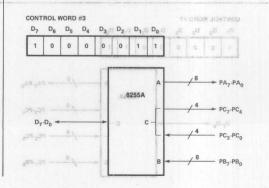
# MODE 0 Port Definition

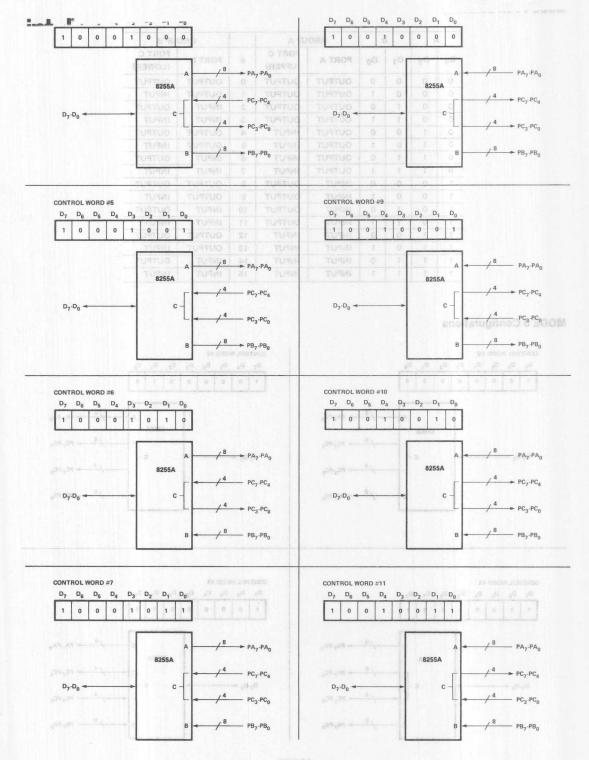
	0 0	UP B	GRO		UP A	GRO	3	0 E	4	1
		PORT C (LOWER)	PORT B	#	PORT C (UPPER)	PORT A	D <sub>0</sub>	D <sub>1</sub>	D <sub>3</sub>	D <sub>4</sub>
		OUTPUT	OUTPUT	0	OUTPUT	OUTPUT	0	0	0	0
		INPUT	OUTPUT	1	OUTPUT	OUTPUT	1	0	0	0
		OUTPUT	INPUT	2	OUTPUT	OUTPUT	0	1	0	0
		INPUT	INPUT	3	OUTPUT	OUTPUT	1	1	0	0
		OUTPUT	OUTPUT	4	INPUT	OUTPUT	0	0	1	0
		INPUT	OUTPUT	5	INPUT	OUTPUT	1	0	1	0
		OUTPUT	INPUT	6	INPUT	OUTPUT	0	1	1	0
		INPUT	INPUT	7	INPUT	OUTPUT	1	1	1	0
		OUTPUT	OUTPUT	8	OUTPUT	INPUT	0	0	0	1
	200.000	INPUT	OUTPUT	9	OUTPUT	INPUT	1	0	0	1
90	at at	OUTPUT	INPUT a	10	OUTPUT	INPUT	0	1	0	1
	-	INPUT	INPUT	11	OUTPUT	INPUT	1	1	0	1
9	0 0	OUTPUT	OUTPUT	12	INPUT	INPUT	0	0	1	1
		INPUT	OUTPUT	13	INPUT	INPUT	1	0	1	1
		OUTPUT	SINPUT	14	INPUT	INPUT	0	1	1	1
		INPUT	INPUT	15	INPUT	INPUT	1	1	1	1

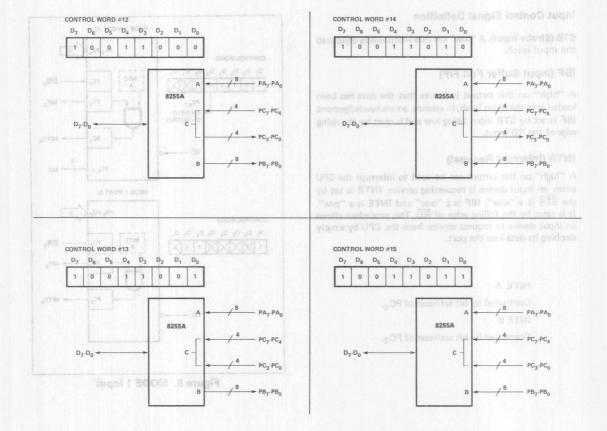
## **MODE 0 Configurations**

CONTROL WORD #0 CONTROL WORD #2 D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub>  $D_3$   $D_2$ D7 D6 D5 D4 D<sub>3</sub> 0 0 0 0 0 0 0 0 0 0 1 0 8255A 8255A D<sub>7</sub>-D<sub>0</sub> D7-D0 -C. PB<sub>7</sub>-PB<sub>0</sub> PB<sub>7</sub>-PB<sub>0</sub> 18 PB PB









## **Operating Modes**

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

#### Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output.
   Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Figure 9, MODE 1 (Strobed Input)





# **Input Control Signal Definition**

STB (Strobe Input). A "low" on this input loads data into the input latch.

# IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement IBF is set by STB input being low and is reset by the rising edge of the RD input.

# **INTR** (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the  $\overline{STB}$  is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of  $\overline{RD}$ . This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

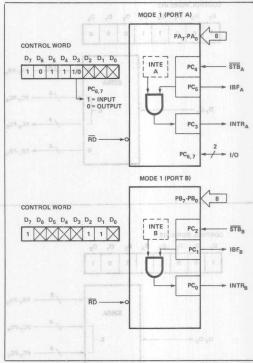


Figure 8. MODE 1 Input

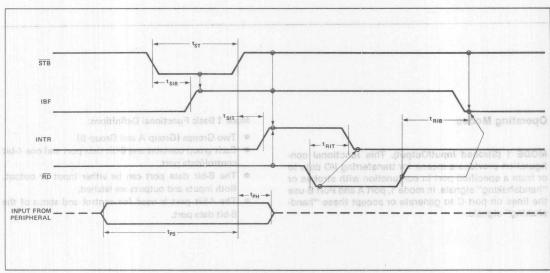


Figure 9. MODE 1 (Strobed Input)





## **Output Control Signal Definition**

OBF (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK Input being low.

ACK (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTEA

Controlled by bit set/reset of PC6.

INTE B

Controlled by bit set/reset of PC2.

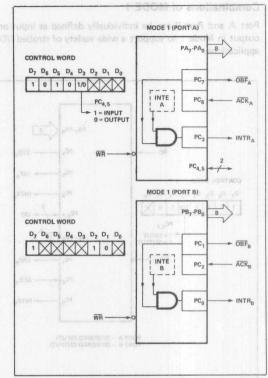


Figure 10. MODE 1 Output

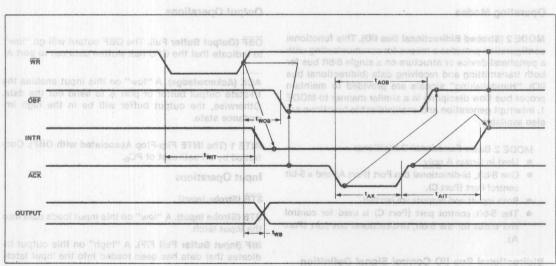


Figure 11. Mode 1 (Strobed Output)



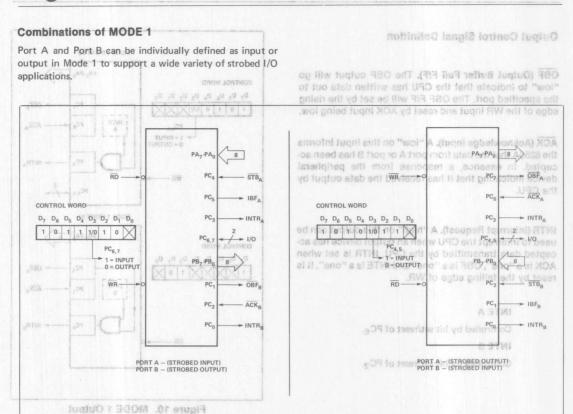


Figure 12. Combinations of MODE 1

#### **Operating Modes**

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

#### MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

# Bidirectional Bus I/O Control Signal Definition

**INTR (Interrupt Request).** A high on this output can be used to interrupt the CPU for both input or output operations.

#### **Output Operations**

OBF (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

ACK (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC<sub>6</sub>.

#### **Input Operations**

#### STB (Strobe Input)

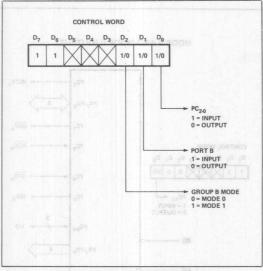
STB (Strobe Input). A "low" on this input loads data into the input latch.

**IBF (Input Buffer Full F/F).** A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of  $PC_4$ .







PA<sub>7</sub>-PA<sub>0</sub>

PC<sub>7</sub>

INTE | PC<sub>6</sub>

RD

PC<sub>8</sub>

INTE | PC<sub>6</sub>

RD

PC<sub>8</sub>

INTE | PC<sub>6</sub>

IN

Figure 13. MODE Control Word

Figure 14. MODE 2

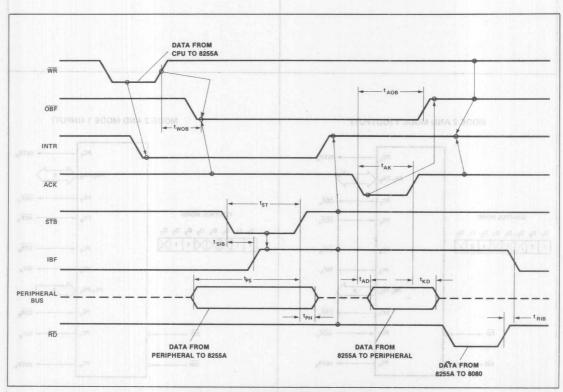


Figure 15. MODE 2 (Bidirectional)

NOTE: Any sequence where  $\overline{WR}$  occurs before  $\overline{ACK}$  and  $\overline{STB}$  occurs before  $\overline{RD}$  is permissible. (INTR = IBF •  $\overline{MASK}$  •  $\overline{STB}$  •  $\overline{RD}$  +  $\overline{OBF}$  •  $\overline{MASK}$  •  $\overline{ACK}$  •  $\overline{WR}$ )





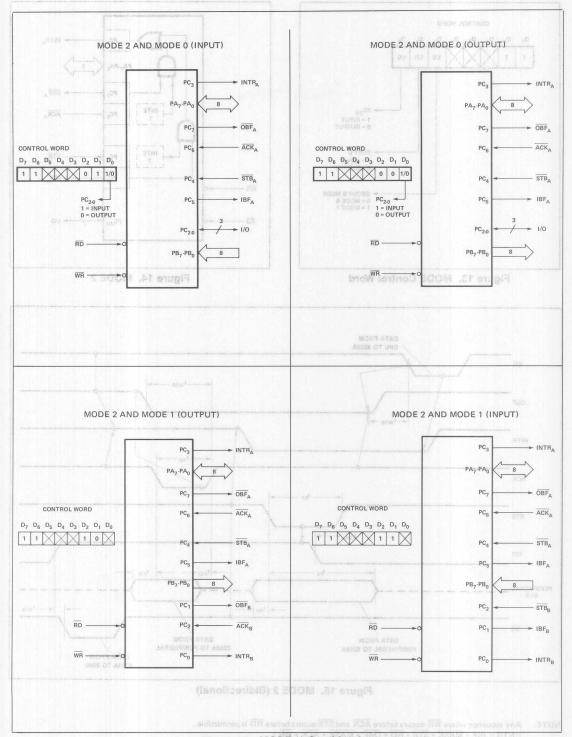


Figure 16. MODE 1/4 Combinations





	MC	DE 0		MO	DE 1	MODE 2
	IN	OUT	48850	IN	OUT	GROUP A ONLY of themquipe laterighe
YJJU PAO	IN	OUT		IN	OUT	egregents the optimum use of a situate pins and is
GRADEVPA1	IN	OUT		IN	OUT	ble enough to interface almost any ve device with
PA <sub>2</sub>	IN	OUT		IN	OUT	he need for additional external <del><agic.< del="">►</agic.<></del>
PA <sub>3</sub>	IN	OUT	MODE	IN	OUT	Each peripheral device in a microcomputer syst
PA <sub>4</sub>	IN	OUT	(trains)	IN	OUT	usually has a "service routine" associated with it.
PA <sub>5</sub>	IN	OUT		IN	OUT	outine manages the sortware Interface between
PA <sub>6</sub>	IN	OUT		IN	OUT	device and the CPU. The functional calinition of
PA <sub>7</sub>	IN	OUT		IN	OUT	3255A is programmed by the <del>≪ su≻</del> ce routine
PBO	IN	OUT		IN	OUT	secomes an extension of the system software. By
PB <sub>1</sub>	IN	OUT		IN	OUT	amining the I/O devices interface characteristics
PB <sub>2</sub>	IN	OUT		IN	OUT	och data transfer and timing, and matching this if nation to the examples and tables in the detailed on
PB <sub>3</sub>	IN	OUT		IN	OUT	ional descrio adoma control word can easily be d
PB4	IN	OUT		IN	OUT	oped to ItadoM No - 25th to exactly "fit" the app
PB <sub>5</sub>	IN	OUT		IN		ion. Figures 'YJNO ough 25 present a few example
PB <sub>6</sub>	IN	OUT	TOOM	IN	OUT	ypical applications of the 8255A.
PB <sub>7</sub>	IN	OUT	(OUTPU	IN	OUT	
PC <sub>0</sub>	IN	OUT		INTRB	INTRB	1/0
PC1	IN	OUT		IBFB	OBFB	1/0
PC <sub>2</sub>	IN .	OUT		STBB	ACKB	1/0
PC <sub>3</sub>	IN	OUT	4	INTRA	INTRA	INTRA
PC <sub>4</sub>	IN	OUT		STBA	1/0	STB <sub>A</sub>
PC <sub>5</sub>	IN	OUT	P	IBFA	1/0	IBFA
PC <sub>6</sub>	IN	OUT		1/0	ACKA	ACKA
PC7	IN .	OUT	00 -	1/0	OBFA	OBFA ANDRESS

#### **Special Mode Combination Considerations**

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs -

All input lines can be accessed during a normal Port C read.

If Programmed as Outputs -

Bits in C upper (PC<sub>7</sub>-PC<sub>4</sub>) must be individually accessed using the bit set/reset function.

Bits in C lower (PC<sub>3</sub>-PC<sub>0</sub>) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

## Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

#### Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C

allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

APPLICATIONS OF THE 8255A

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

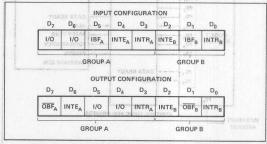


Figure 17. MODE 1 Status Word Format

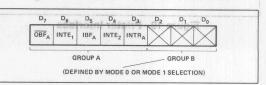


Figure 18. MODE 2 Status Word Format

#### **APPLICATIONS OF THE 8255A**

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 present a few examples of typical applications of the 8255A.

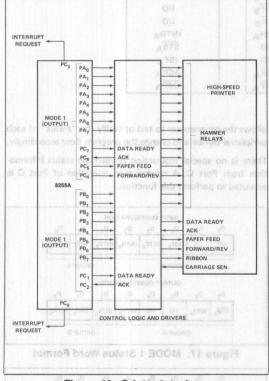


Figure 19. Printer Interface

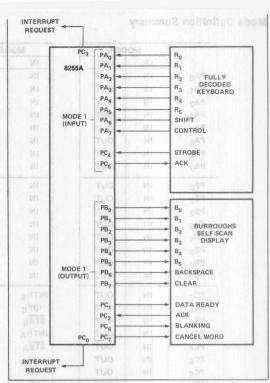


Figure 20. Keyboard and Display Interface

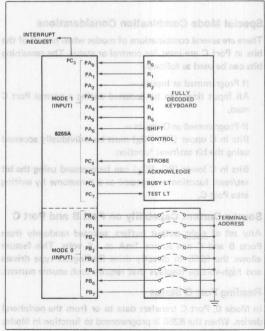
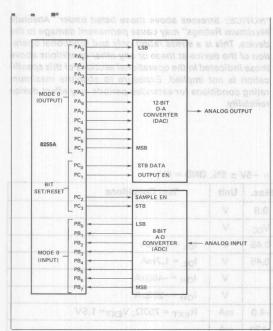


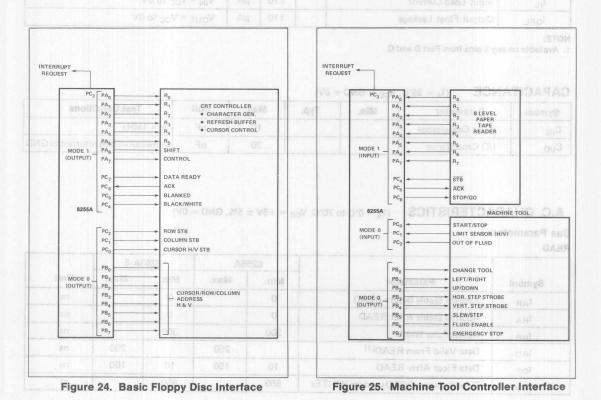
Figure 21. Keyboard and Terminal Address Interface



INTERRUPT REQUEST PA: D<sub>2</sub> FLOPPY DISK CONTROLLER AND DRIVE PA: PA D<sub>4</sub> PA<sub>5</sub> D<sub>5</sub> MODE 2 PA D<sub>6</sub> Dy PA: DATA STR PC ACK (IN) PC, PC, DATA READY PC ACK (OUT) 8255A TRACK "0" SENSOR PC2 SYNC READY PC. PC. INDEX PBn ENGAGE HEAD PB<sub>1</sub> FORWARD/REV READ ENABLE PB<sub>3</sub> WRITE ENABLE MODE 0 DISC SELECT PB4 (OUTPUT) PB<sub>5</sub> ENABLE CRC TEST PB PB<sub>7</sub> BUSY LT

Figure 22. Digital to Analog, Analog to Digital

Figure 23. Basic CRT Controller Interface



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# **ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	65°C to +150°C
Voltage on Any Pin	
With Respect to Ground	0.5V to +7V
Power Dissipation	1 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS  $(T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}, V_{CC} = +5\text{V} \pm 5\%, \text{GND} = 0\text{V})$ 

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
VIL	Input Low Voltage	-0.5	0.8	V	PC STB
VIH	Input High Voltage	2.0	V <sub>CC</sub>	V	718 92.1
VOL (DB)	Output Low Voltage (Data Bus)		0.45	V	I <sub>OL</sub> = 2.5mA
VOL (PER)	Output Low Voltage (Peripheral Port)		0.45	V	I <sub>OL</sub> = 1.7mA
V <sub>OH</sub> (DB)	Output High Voltage (Data Bus)	2.4		V	Ι <sub>ΟΗ</sub> = -400μΑ
VOH (PER)	Output High Voltage (Peripheral Port)	2.4		V	I <sub>OH</sub> = -200μA
I <sub>DAR</sub> [1]	Darlington Drive Current	-1.0	-4.0	mA	$R_{EXT} = 750\Omega; V_{EXT} = 1.5V$
1cc	Power Supply Current		120	mA	
կլ	Input Load Current		±10	μΑ	V <sub>IN</sub> = V <sub>CC</sub> to 0V
lofL	Output Float Leakage		±10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> to 0V

1. Available on any 8 pins from Port B and C.

# CAPACITANCE

 $(T_A = 25^{\circ}C, V_{CC} = GND = 0V)$ 

Symbol .	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
CIN	Input Capacitance	1,19		10	pF	fc = 1MHz
C <sub>I/O</sub>	I/O Capacitance	19 1-300U		20	pF	Unmeasured pins returned to GND

# A.C. CHARACTERISTICS

 $(T_A = 0^{\circ}C \text{ to } 70^{\circ}C, V_{CC} = +5V \pm 5\%, GND = 0V)$ 

# **Bus Parameters**

READ

	роог зрими зиримпязи — Parameter	825	55A	8255A-5		
Symbol		Min.	Max.	Min.	Max.	Unit
t <sub>AR</sub>	Address Stable Before READ	0	BARDWICOLUMN 285	0 0		ns
t <sub>RA</sub>	Address Stable After READ	0		0		ns
t <sub>RR</sub>	READ Pulse Width	300		300	H3.	ns
t <sub>RD</sub>	Data Valid From READ <sup>[1]</sup>		250		200	ns
t <sub>DF</sub>	Data Float After READ	10	150	10	100	ns
tRV	Time Between READs and/or WRITEs	850	Sector and	850	See Class	ns





# A.C. CHARACTERISTICS (Continued)

WRITE

Symbol	Parameter	82	55A	8255A-5		LES O MITCH
		Min.	Max.	Min.	Max.	Unit
t <sub>AW</sub>	Address Stable Before WRITE	0		0		ns
t <sub>WA</sub>	Address Stable After WRITE	20	1	20		ns
tww	WRITE Pulse Width	400		300		ns
t <sub>DW</sub>	Data Valid to WRITE (T.E.)	100		100		ns
t <sub>WD</sub>	Data Valid After WRITE	30	1 X	30		ns

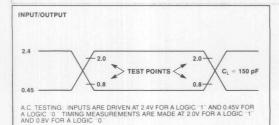
#### OTHER TIMINGS

		825	5A	8255A-5		0A,1A,2
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
twB	WR = 1 to Output <sup>[1]</sup>	) ·	350		350	ns
t <sub>IR</sub>	Peripheral Data Before RD	s <sup>1</sup> 0		0		ns
t <sub>HR</sub>	Peripheral Data After RD	0		0		ns
t <sub>AK</sub>	ACK Pulse Width	300		300		ns
t <sub>ST</sub>	STB Pulse Width	500	Control of the Control of the	500		ns
tps	Per. Data Before T.E. of STB	0		0		ns
t <sub>PH</sub>	Per. Data After T.E. of STB	180		180		ns
tAD	ACK = 0 to Output <sup>[1]</sup>		300	my	300	e) ons
t <sub>KD</sub>	ACK = 1 to Output Float	20	250	20	250	ns
t <sub>WOB</sub>	WR = 1 to OBF = 0[1]		650		650	ns
t <sub>AOB</sub>	ACK = 0 to OBF = 1[1]		350		350	ns
t <sub>SIB</sub>	STB = 0 to IBF = 1 <sup>[1]</sup>		300		300	ns
t <sub>RIB</sub>	$RD = 1 \text{ to } IBF = 0^{[1]}$	presidential	300		300	ns
t <sub>RIT</sub>	RD = 0 to INTR = 0 <sup>[1]</sup>		400		400	ns
t <sub>SIT</sub>	STB = 1 to INTR = 1 <sup>[1]</sup>		300	WA <sup>3</sup>	300	ns
tAIT	ACK = 1 to INTR = 1 <sup>[1]</sup>		350		350	ns
twiT	WR = 0 to INTR = $0^{[1,3]}$		450		450	ns

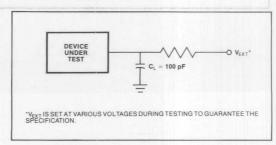
#### NOTES

- 1. Test Conditions: 8255A: C<sub>L</sub> = 100pF; 8255A-5: C<sub>L</sub> = 150pF.
- 2. Period of Reset pulse must be at least 50 µs during or after power on. Subsequent Reset pulse can be 500 ns min.
- 3. INTR↑ may occur as early as WR↓.

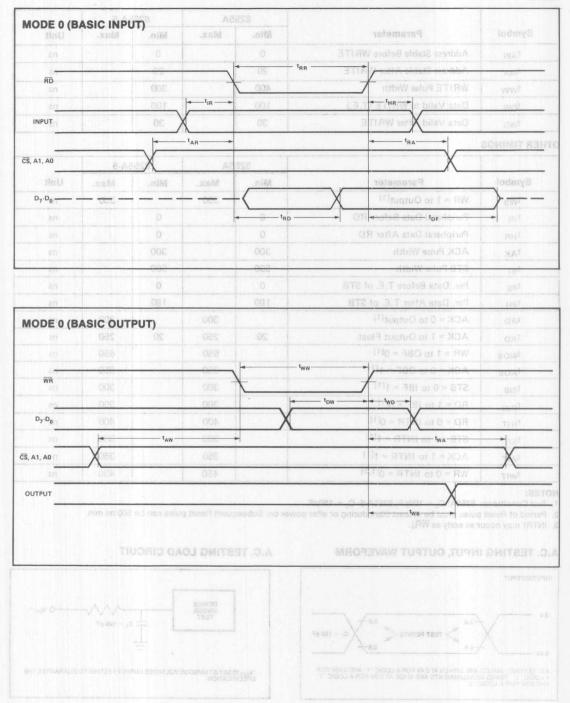
# A.C. TESTING INPUT, OUTPUT WAVEFORM



## A.C. TESTING LOAD CIRCUIT



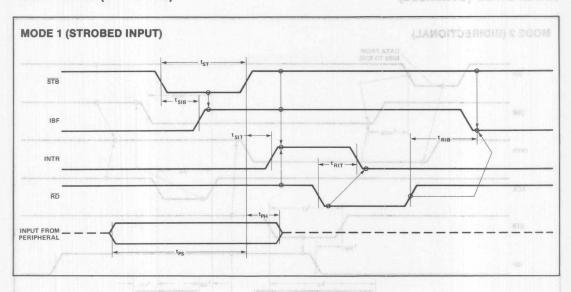
WRITE

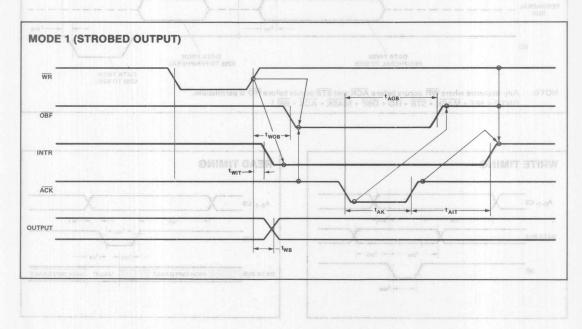






## **WAVEFORMS** (Continued)

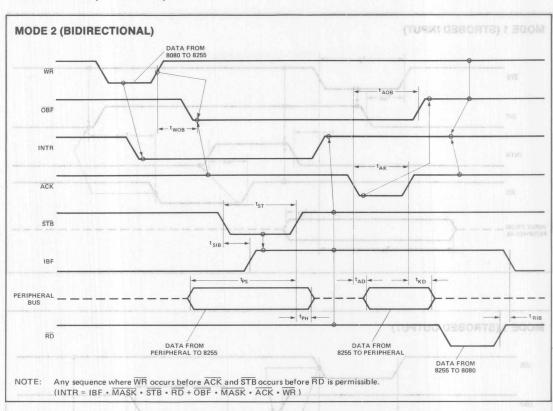


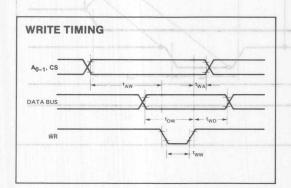


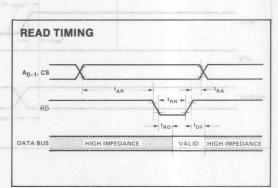




## **WAVEFORMS** (Continued)









## 8275

## PROGRAMMABLE CRT CONTROLLER

- Programmable Screen and Character
  Format
- 6 Independent Visual Field Attributes
- 11 Visual Character Attributes (Graphic Capability)
- **Cursor Control (4 Types)**
- Light Pen Detection and Registers

- Fully MCS-80<sup>TM</sup> and MCS-85<sup>TM</sup> Compatible
- m Dual Row Buffers
- Programmable DMA Burst Mode
- Single +5V Supply
- 40-Pin Package

The Intel® 8275 Programmable CRT Controller is a single chip device to interface CRT raster scan displays with Intel® microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

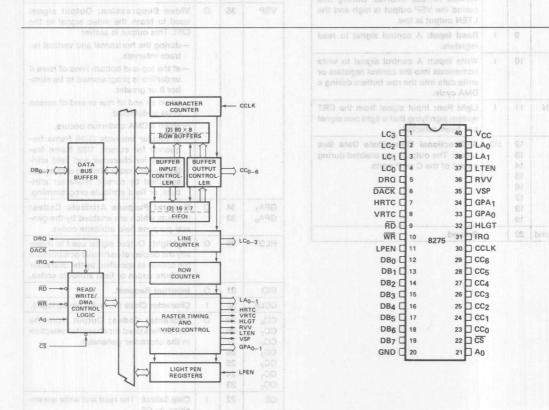


Figure 1. Block Diagram

Figure 2. Pin Configuration

Symbol	Pin No.	Туре	Name and Function						
LC <sub>3</sub> LC <sub>2</sub> LC <sub>1</sub> LC <sub>0</sub>	1 2 3 4	0	Line Count: Output from the line count- er which is used to address the charac- ter generator for the line positions on the screen.						
DRQ	5	0	<b>DMA Request:</b> Output signal to the 8257 DMA controller requesting a DMA cycle.						
DACK	6	oM i	DMA Acknowledge: Input signal from the 8257 DMA controller acknowledging that the requested DMA cycle has been granted.						
HRTC	7 sigai	O mad	Horizontal Retrace: Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.						
VRTC	e en principal	10 8 10 8	Vertical Retrace: Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.						
RD	9	1	Read Input: A control signal to read registers.						
WR	10	1	Write Input: A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.						
LPEN	11	1	Light Pen: Input signal from the CRT system signifying that a light pen signal has been detected.						
DB <sub>0</sub> DB <sub>1</sub> DB <sub>2</sub> DB <sub>3</sub> DB <sub>4</sub> DB <sub>5</sub> DB <sub>6</sub> DB <sub>7</sub>	12 13 14 15 16 17 18 19	74 979 97 97 98	a read of the C or P ports.						
Ground	20		Ground.						

923 G 82

Figure 2. Pin Configuration

Symbol	Pin No.	Туре	Name and Function
V <sub>CC</sub>	40		+5V Power Supply.
LA <sub>0</sub> LA <sub>1</sub>	39 38	0	Line Attribute Codes: These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified.
LTEN	37	0	by the character attribute codes.  Light Enable: Output signal used to enable the video signal to the CRT. Thi output is active at the programme underline cursor position, and at positions specified by attribute codes.
RVV  is a si si noif: arit to no si ritiw v	inut oitis		Reverse Video: Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
VSP	35	0	Video Suppression: Output signal used to blank the video signal to the CRT. This output is active:  —during the horizontal and vertical retrace intervals.  —at the top and bottom lines of rows underline is programmed to be number 8 or greater.  —when an end of row or end of screen code is detected.
s-0 <sup>5</sup>	• ==	789 100 TUPPU 100 TUPPU 10	—when a DMA underrun occurs.  —at regular intervals (1/16 frame fre quency for cursor, 1/32 frame fre quency for character and field attributes)—to create blinking displays a specified by cursor, character attribute, or field attribute programming
GPA <sub>1</sub> GPA <sub>0</sub>	34 33	0	General Purpose Attribute Codes Outputs which are enabled by the general purpose field attribute codes.
HLGT	32	0	Highlight: Output signal used to intensify the display at particular positions of the screen as specified by the characte attribute codes or field attribute codes
IRQ	31	0	Interrupt Request.
CCLK	30	1	Character Clock (from dot/timing logic)
CC <sub>6</sub> CC <sub>5</sub> CC <sub>4</sub> CC <sub>3</sub> CC <sub>2</sub> CC <sub>1</sub> CC <sub>0</sub>	29 28 27 26 25 24 23	0	Character Codes: Output from the row buffers used for character selection in the character generator.
CS	22	1	Chip Select: The read and write are en abled by CS.
A <sub>0</sub>	21	I <sub>ma</sub>	Port Address: A high input on A selects the "C" port or command registers and a low input selects the "P" port or parameter registers.





#### **Data Bus Buffer**

This 3-state, bidirectional, 8-bit buffer is used to interface the 8275 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

A <sub>0</sub>	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1 00	Write	CREG

#### RD (Read)

A "low" on this input informs the 8275 that the CPU is reading data or status information from the 8275.

## WR (Write)

A "low" on this input informs the 8275 that the CPU is writing data or control words to the 8275.

## CS (Chip Select)

A "low" on this input selects the 8275. No reading or writing will occur unless the device is selected. When  $\overline{CS}$  is high, the Data Bus in the float state and  $\overline{RD}$  and  $\overline{WR}$  will have no effect on the chip.

## DRQ (DMA Request) house of tugue of the land and

A "high" on this output informs the DMA Controller that the 8275 desires a DMA transfer.

## DACK (DMA Acknowledge) 12 got2-next2 to bn3"

A "low" on this input informs the 8275 that a DMA cycle is in progress.

## **IRQ** (Interrupt Request)

A "high" on this output informs the CPU that the 8275 desires interrupt service.

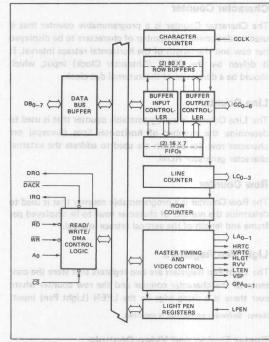


Figure 3. 8275 Block Diagram Showing Data Bus Buffer and Read/Write Functions

Ao	RD	WR	CS	tion of LA <sub>Q-1</sub> (Line Attribute), (Second Victor), 1 TEN (Links Ex
0	0	di 1nA	0	Write 8275 Parameter
0	1	0	0	Read 8275 Parameter
1	0	1	0	Write 8275 Command
1	_1	0	0	Read 8275 Status
X	1	1	0	Three-State
X	X	X	1	Three-state



#### **Character Counter**

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be a derivative of the external dot clock.

#### **Line Counter**

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Sweeps) per character row. Its outputs are used to address the external character generator ROM.

#### **Row Counter**

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

## Light Pen Registers

The Light Pen Registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

Note: Software correction is required.

## **Raster Timing and Video Controls**

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of  $LA_{0-1}$  (Line Attribute), HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and  $GPA_{0-1}$  (General Purpose Attribute) outputs.

## Row Buffers and all series

The Row Buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

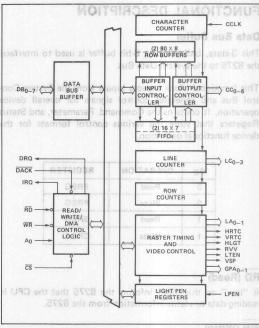


Figure 4. 8275 Block Diagram Showing Counter and Register Functions

#### **FIFOs**

There are two 16 character FIFOs in the 8275. They are used to provide extra row buffer length in the Transparent Attribute Mode (see Detailed Operation section).

## **Buffer Input/Output Controllers**

The Buffer Input/Output Controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action. (Examples: An "End of Screen—Stop DMA" special code will cause the Buffer Input Controller to stop further DMA requests. A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

A "high" on this output informs the CPU that the 8275





## SYSTEM OPERATION and tog somil to redmun and

The 8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

tion, and blanking of top a

It is designed to interface with the 8257 DMA Controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

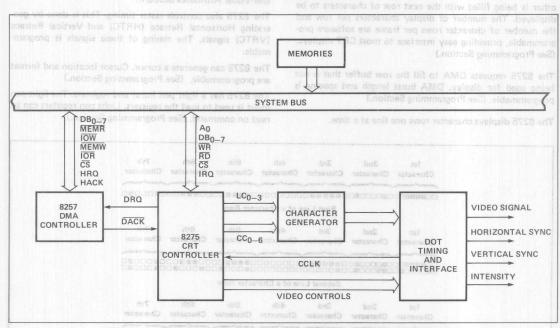


Figure 5. 8275 Systems Block Diagram Showing Systems Operation



Figure 6. Display of a Character Row

mable. (See Programming Section.)

Display characters are retrieved from memory and displayed on a row by row basis. The 8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The 8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See Programming Section.)

The 8275 displays character rows one line at a time.

The 8275 provides special Control Codes which can be used to minimize DMA or software overhead. It also provides Visual Attribute Codes to cause special action or symbols on the screen without the use of the character generator (see Visual Attributes Section).

The 8275 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is programmable.

The 8275 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

The 8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See Programming Section.)

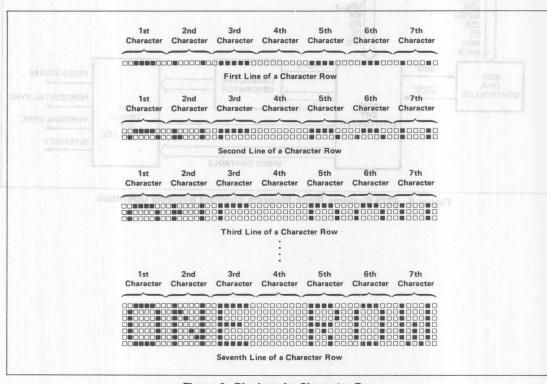


Figure 6. Display of a Character Row

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1<sub>9</sub>mi

## **Display Row Buffering**

Before the start of a frame, the 8275 requests DMA and one row buffer is filled with characters.

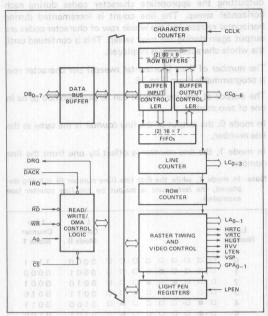


Figure 7. First Row Buffer Filled

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

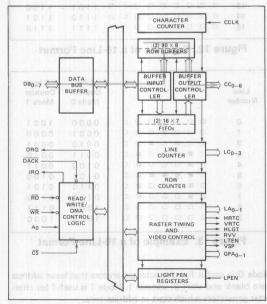


Figure 8. Second Buffer Filled, First Row Displayed

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

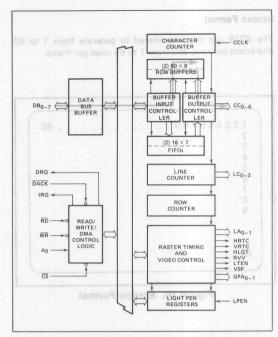
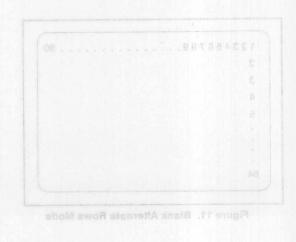


Figure 9. First Buffer Filled with Third Row,
Second Row Displayed

This is repeated until all of the character rows are displayed.



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Display Format syon are staffed won owe arts to salor

#### **Screen Format**

The 8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

After all the lines of the character roy

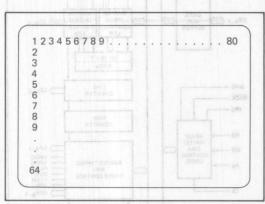


Figure 10. Screen Format

The 8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

Figure 9. First Buffer Fided with Third Row,

123456789	)	 	8
2			
3			
4			
5			
. 4.2.5			
•			
•			
64			

Figure 11. Blank Alternate Rows Mode

#### **Row Format**

The 8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

**Note:** In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number			psim					X	100	Line Counter Mode 0	Line Counter Mode 1
0							0	0		0000	1111
1		0				0				0001	0000
2		. []								0010	0001
3					0				0	0011	0010
4		-								0100	0011
5										0101	0100
6						-			0	0110	0101
7								-		0111	0110
eboo 8	0			0					0	1000	0.1.1.1
9										61001	1000
10						-				1010	
11										1011	1010
12										1100	1011
13							0		0	1101	1100
14										1110	1101
15								0	0	1111	1110

Figure 12. Example of a 16-Line Format

Line Number						Counter Mode 0	Counter Mode 1
0	0	0	0		0	0000	1001
1	0	0		0		0001	0000
2						0010	0001
3						0011	0010
4						0100	0011
5	W					0101	0100
6	11		0			0110	0101
7	Ш				-	0 1 1 1	0110
8						1000	0111
9						1001	1000

Figure 13. Example of a 10-Line Format

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

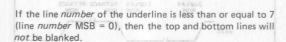


Underline placement is also programmable (from line number 0 to 15). This is independent of the line counter mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number										Line Counter Mode 0	Line Counter Mode 1
			1	2	d Jac	1			A	5.0	
0										0000	1011
1					=					0001	0000
2					0					0010	0001
3	0		jń,	0					0	0011	0010
4		-	0				0		0	0100	0011
5				0	-0	0	0	-01-		0101	0100
6						10		W		0110	0101
. 7										0111	0110
8		B.,	0	Q		0	90			1000	0111
9							0	-		1001	1000
10	-		=			10		80		1010	1001
ment 11 mi				0	0	0	0	.0	0	1011	1010
ng out the											mogramma errical retr

Figure 14. Underline in Line Number 10



Line Number	8							Line Counter Mode 0	Line Counter Mode 1
TENEDAL I	-								
these output				-				0000	0111
and de ocour	0	0	-					0001	0000
2		-	0			-		0010	0001
3		10						0011	0010
4				-		-		0100	0011
5								0101	0100
6								0110	0101
7			88	-		-	=	0111	0110
					Bott		nked		

Figure 15. Underline in Line Number 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

#### **Dot Format**

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

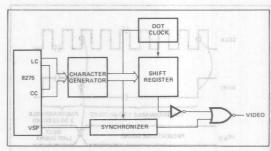


Figure 16. Typical Dot Level Block Diagram

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

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## **Raster Timing**

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This is constantly repeated.

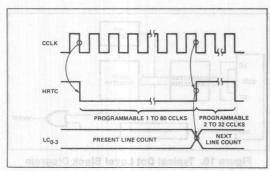


Figure 17. Line Timing

The line counter is driven by the character counter. It is used to generate the line address outputs  $(LC_{0-3})$  for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

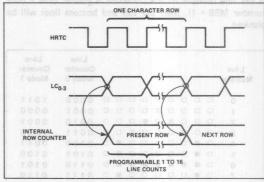


Figure 18. Row Timing

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

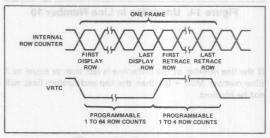


Figure 19. Frame Timing

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

. . . . . . . .

. . . . . . . .

The 8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods  $\pm$ 1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the 8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

The first DMA request for a row will start at the first character clock of the preceding row. If the burst mode is used, the first DMA request may occur a number of character clocks later. This number is equal to the programmed burst space.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

The 8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the 8275 interrupt enable flag is set, an interrupt request will occur at the beginning of the last display row.

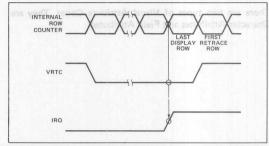


Figure 21. Beginning of Interrupt Request

IRQ will go inactive after the status register is read.

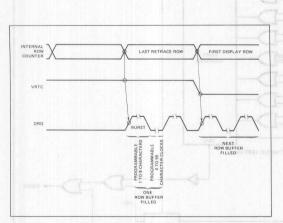


Figure 20. DMA Timing

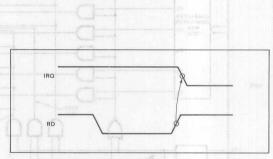


Figure 22. End of Interrupt Request

A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the 8275 interrupt enable flag should not be set.

The DMA controller is typically initialized for the next frame at the end of the current frame.

Note: Upon power-up, the 8275 Interrupt Enable Flag may be set.

As a result, the user's cold start routine should write a reset command to the 8275 before system interrupts are enabled.



# VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the 8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

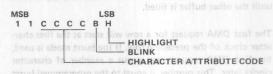
There are two types of Visual Attribute Codes. They are Character Attributes and Field Attributes.

#### **Character Attribute Codes**

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the Line Attribute outputs  $(LA_{0-1})$ , the Video Suppression output (VSP), and the Light Enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the Video Suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the Highlight output (HGLT).

## Character Attributes to a stranger AMO , smit tent tA



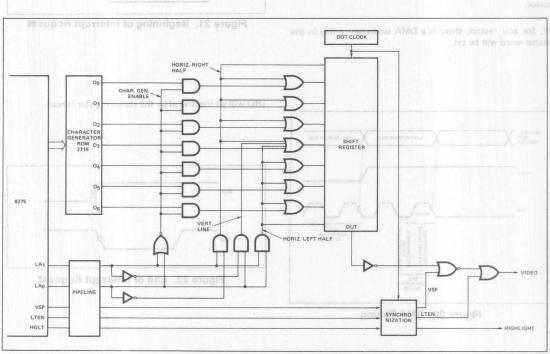


Figure 23. Typical Character Attribute Logic

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**Table 2. Character Attributes** 

Character attributes were designed to produce the following graphics:

CHARA	ACTER ATTRIBUTE	recenter.	OUT	PUTS		OVAADOL	tware, or DMA overhead	
(	CODE "CCCC"	LA <sub>1</sub>	LA <sub>0</sub>	VSP	LTEN	SYMBOL	DESCRIPTION  Velocities 10 to the 0 leice	
	Above Underline	0	0	ens alient	0			
0000	Underline	etoded3	0	0	0		Top Left Corner	
ue neix		0	simild of	0	0			
to or is		0	2V0 100	1	0	SOO JOHTY	SPECIAL CO	
0001	Underline	Deni piaer	en nation	0	0		Top Right Corner	
s sino	Below Underline	0	rdmillions	0	0		S S PUNCTION	
the His	Above Underline	0	r b1zus	0	0		0 0 End of Row	
0010	Underline	J011 1	0	0	0		Bottom Left Corner	
s show	Below Underline	0	0	1	0	N. C. T. A.	Total End of Screen	
	THE DESIGNATION OF STREET	0	1 12.55	0	0		HAND gare-needs to bid	
0011	Underline	peb 1/ 92	the Level	0	0		Bottom Right Corner	
0011	Below Underline	0	0	1	0	THE STATE OF THE S		
code a	DET BRITISHES DESTROY	0	0	1	0	THOR DOL	s End of Row Code (00) activates VSP	
0100	Underline Underline	0	0	0	1 00		end of the line.	
		0	1 1	0	0		Top Intersect To	
708 lene	Below Underline	0	100000	0	0	ne row white	tile ten ent not AMO note or pland leste	
0101	Above Underline	1	na Idina	0	0		witten Into the Row Buffer, It affects th	
0101	Underline	0	na Vitns	0	0		Right Intersect of to bod add as your so	
	Below Underline	0	1	0	0	ti abišili bris	End of Sursen Code (10) software VSP	
0110	Above Underline Underline	1	0	0	0		end of the frame.	
0110		0	1	0	0	6 (B. 197) E. G. 1971	Left Intersect	
	Below Underline		-		2100	the france with	the two edit set AMO gets on signal fests	
0111	Above Underline	0	1	0	0	1 636 1556	s written into the Row Buffer. It affect	
0111	Underline		0		-		Bottom Intersect Ball and as your amount	
	Below Underline	0	0	1	0	north trainer	ne Stop DNAA (corum is not used, all obs	
1000	Above Underline	0	0	1	0		d of Row character are ignored, except	
1000	Underline	0	0	0	1		Horizontal Line	
	Below Underline	0	0	1	0	tamemerous constitution.	er an End of Screen diseaster are ignored	
4004	Above Underline	1 0	101 <b>1</b> FIGH	0	0			
1001	Underline	0	1 10	0	0	2 1 2 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2	Vertical Line	
	Below Underline	0	GIAL RO-	0	0 0	77097890 TX96	tow, DMA is not stopped until effet the	
	Above Underline	0	gA91 APA	0	0		Crossed Lines	
1010	Underline	0	0	0	1		Crossed Lines	
AND IN COLUMN	Below Underline	0	1.	0	0	TOWNSHIP AND THE OWNER.	The second secon	
ing tim	Above Underline	0	0	0	0	1002 State		
1011	Underline	0	0	0	0	14	Not Recommended *	
.Artito	Below Underline	0 /10	0	0	0		ual charecteristics for a field of character	
	Above Underline	0	0	1	0			
1100	Underline	0	0	1	0		Special Codes	
	Below Underline	0	0	1	0			
	Above Underline							
1101	Underline		Unde	fined _			Illegal	
	Below Underline		119					
	Above Underline			70				
1110	Underline		Unde	fined			Illegal	
	Below Underline						在大学 计一个 医心管测量性 化	
	Above Underline	48/11/5						
1111	Underline		Unde	fined	Contract of		Illegal	
	Below Underline				13.11			

<sup>\*</sup>Character Attribute Code 1011 is not recommended for normal operation. Since none of the attribute outputs are active, the character Generator will not be disabled, and an indeterminate character will be generated.

Character Attribute Codes 1101, 1110, and 1111 are illegal. Blinking is active when B=1. Highlight is active when H=1.



## **Special Codes**

Four special codes are available to help reduce memory, software, or DMA overhead.

## Special Control Character

S	S	FUNCTION
0	0	End of Row
0	1	End of Row-Stop DMA
1	0	End of Screen
1	1	End of Screen-Stop DMA

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop DMA Code (01) causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame

The End of Screen-Stop DMA Code (11) causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the Row Buffer. It affects the display in the same way as the End of Screen Code (10).

If the Stop DMA feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

Note: If a Stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop DMA character.

#### **Field Attributes**

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the

character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

## There are six field attributes:

- Blink Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
- 2. Highlight Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
- 3. Reverse Video Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
- Underline Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).
- 5,6. General Purpose There are two additional 8275 outputs which act as general purpose, independently programmable field attributes. GPA<sub>0-1</sub> are active high outputs.

#### **Field Attribute Code**

MSB
1 0 U R G G B H HIGHLIGHT
BLINK
GENERAL PURPOSE
REVERSE VIDEO
UNDERLINE

H = 1 FOR HIGHLIGHTING B = 1 FOR BLINKING R = 1 FOR REVERSE VIDEO U = 1 FOR UNDERLINE GG = GPA<sub>1</sub>, GPA<sub>0</sub>

\*More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

Character Attribute Codes 1101, 1110, and 1111 are flegal.

normal operation. Since none of the attribute outputs en active, the character Generator will not be disabled, and an indeterminate character will be generated.



l<sub>o</sub>lni

The 8275 can be programmed to provide visible or invisible field attribute characters.

If the 8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.



Figure 24. Example of the Visible Field Attribute
Mode (Underline Attribute)

If the 8275 is programmed in the invisible field attribute mode, the 8275 FIFO is activated.

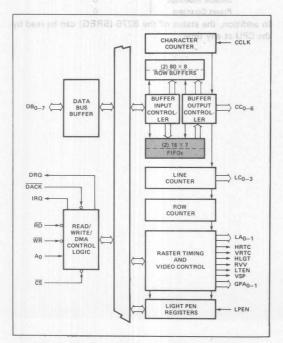


Figure 25. Block Diagram Showing FIFO Activation

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the *next* character in the proper FIFO.

When a field attribute is placed in the Buffer Output Controller during display, it causes the controller to immediately put a character from the FIFO on the Character Code outputs ( $CC_{0-6}$ ). The chosen Visual Attributes are also activated.

Since the FIFO is 16 characters long, no more than 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

Note: Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a Visual Attribute or Special Code must *not* immediately follow a field attribute code. If this situation does occur, the Visual Attribute or Special Code will be treated as a normal display character.

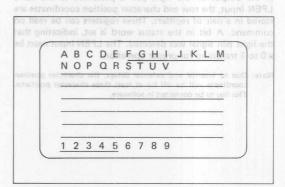


Figure 26. Example of the Invisible Field Attribute Mode (Underline Attribute)

## Field and Character Attribute Interaction

Character Attribute Symbols are affected by the Reverse Video (RVV) and General Purpose ( $\mathsf{GPA}_{0-1}$ ) field attributes. They are not affected by Underline, Blink or Highlight field attributes; however, these characteristics can be programmed *individually* for Character Attribute Symbols.

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## Cursor Timing a polibooquerros a pad reflud wor das3

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

- 1. a blinking underline easily at equality block a negligible
- 2. a blinking reverse video block
- 3. a non-blinking underline most retoristic a translation
- 4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

## Light Pen Detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enables the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the 8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

Note: Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

## Device Programming of perimerpong ed rea 3353 ed 7

The 8275 has two programming registers, the Command Register (CREG) and the Parameter Register (PREG). It also has a Status Register (SREG). The Command Register can only be written into and the Status Registers can only be read from. They are addressed as follows:

A <sub>0</sub>	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1   1	Read   A O	SREG
1	Write	CREG

The 8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

#### Instruction Set

The 8275 instruction set consists of 8 commands.

COMMAND	NO. OF PARAMETER BYTES
Reset Marian A	nilrebatti e4oM
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	t the 8275 is programmed in t
Enable Interrupt	node, the 8275 FIGO is activated
Disable Interrupt	0
Preset Counters	0

In addition, the status of the 8275 (SREG) can be read by the CPU at any time.

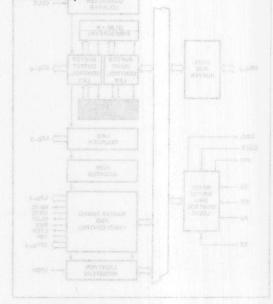


Figure 25. Block Diagram Shewing FIFO





		1	ion	DATA BUS	
	OPERATION	A <sub>0</sub>	DESCRIPTION	MSB	LSB
Command	Write	1/	Reset Command	0 0 0 0 0 0	0 0
0 0 0	0 Write	0	Screen Comp Byte 1	з н н н н	нн
in Flows	Write	0	Screen Comp Byte 2	VVRRRR	RR
Parameters 189	G SofWrite Q	0	Screen Comp Byte 3	0700 U/10 L L	olioli
	Write	0	Screen Comp Byte 4	M F C C Z Z	z z

Action — After the reset command is written, DMA requests stop, 8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter - S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter - HHHHHHH Horizontal Characters/Row

sus H	н	н	н	н	н	Н	NO. OF CHARACTERS PER ROW
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	said 1 2 mW bream
0	0	0	0	0	1	0	No parametins
			arti				ction – Interrupts are dis
1	0	0	1	1	1	1	atus flag is rese 08
1	0	1	0	0	0	0	Undefined
1	1	1	1	1	1	1,60	Smmo Undefined 192914

Parame	ter	- VI	/ Vertical Retrac		Row Count	
	٧	٧	NO. OF ROW COL	JI	NTS PER VRTC	
	0	0	1		parameters	No
	0	1	2			
	1	0 9	gming counters a		- The internal	
	1	101	rdr te noiticed vid	13	a to a screen dis	

Parameter - RRRRRR Vertical Rows/Frame

	R	R	R	R	R	R	NO. OF ROWS/FRAME
	0	0	0	0	0	0	of clustered F.H.T displays o
	0	0	0	0	0	1	2
	0	0	0	0	1	0	3
	1	1	1	1	1	1	64
-				_			

Parameter - UUUU Underline Placement

	U	U	U	U	LINE NUMBER OF UNDERLINE	
STI	0	0	0	0	N AO DESCRIPTION	on
	0	0	0	1	2	
	0	0	1	0	3	
					S BURST SPACE CO	
	1	1	1	1	16 000	
		83	23	JD3	H AMO MEEN DMA H	_

Parameter - LLLL Number of Lines per Character Row

L	L	L	L	NO. OF	LIN	ES/R	wo
0	0	0	0	15	1		
0	0	0	1	82	2		
0	0	1	0	4.7	3		
				55			
				о тишо:	TER		33
1	1	1	1	000000	16	000	

Parameter - M Line Counter Mode

	M	LINE COUNTER MODE
	0	Mode 0 (Non-Offset)
ed :	1	Mode 1 (Offset by 1 Count)

Parameter - F Field Attribute Mode

F	FIELD ATTRIBUTE MODE
0	Transparent
1	Non-Transparent

Parameter - CC Cursor Format Company OTRY base

give	C	C	CURSOR FORMAT	
	0	0	Blinking reverse video block	
	0	1	Blinking underline	
	1	0	Nonblinking reverse video block	
	1	10	Nonblinking underling	

Parameter - ZZZZ Horizontal Retrace Count

09	z	z	z	z	NO. OF CHARACTER COUNTS PER HRTC
	0	0	0	0	cycles of the parameter Segister. Sto
	0	0	0	1	4 bernet
	0	0	1	0	6
		iup			Note: Software correction of light pen post
	1	1	1	1	32

Note: uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).



## 2. Start Display Command:

		1 23 20	1,1712333937			D	AT	A B	US		
	OPERATION	A <sub>0</sub>	DESCRIPTION	M	SB					L	SB
Command	Write	1	Start Display	0	0	1	S	S	s	В	В
Nop	arameters										

#### SSS BURST SPACE CODE

s	s	S		CHARACT EN DMA			S
0	0	0		0			
0	0	119	and I to	nedm7.14			
0	1	0	DRISSING	15			
0	1	1		23			
1	0	0		31			0
1	0	1	1 1	39			
1	1	0	1 A 1 S 1 A 1	47	0		
1	1	1		55			

#### BB BURST COUNT CODE

В	В	NO. OF	DMA CYC BURST	LES PE	R
0	0		1		
0	1	show	200		
1	0	3000	4	3001	
1	1		8	Dahat	

Action-8275 interrupts are enabled, DMA requests begin, video is enabled, Interrupt Enable and Video Enable status flags are set.

## 3. Stop Display Command:

	OPERATION	Ao	DESCRIPTION	M	SB	DA	ATA	BI	US	L	SB
Command	Write	1	Stop Display	0	1	0	0	0	0	0	0
No	parameters									Т	

Action — Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to re-enable the display.

## 4. Read Light Pen Command

	OPERATION		DESCRIPTION			D	ATA	A BI	US	L	SB
Command	Write	1	Read Light Pen	0	1	1	0	0	0	0	0
Parameters	Read Read	10.5	Char. Number Row Number				siti		n A	ow	)

Action — The 8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

Note: Software correction of light pen position is required.

#### 5. Load Cursor Position:

						DA	ATA	BI	JS.		
	OPERATION	A <sub>0</sub>	DESCRIPTION	M	SB					L	SB
Command	Write	1	Load Cursor	1	0	0	0	0	0	0	0
Parameters	Write	0	Char. Number Row Number	100	har.				n R	ow	)

Action — The 8275 is conditioned to place the next two parameter bytes into the cursor position registers. Status flags not affected.

Action - After the reset command is written, DMA re-

# 6. Enable Interrupt Command:

	OPERATION	A <sub>0</sub>	DESCRIPTION	M	SB	D	ATA	ABI	US	L	SB
Command	Write	1	Enable Interrupt	1	0	1	0	0	0	0	0
No	parameters										

Action — The interrupt enable status flag is set and interrupts are enabled.

#### 7. Disable Interrupt Command:

	OPERATION	A <sub>0</sub>	DESCRIPTION	M	SB	D	ATA	B	US	L	SB
Command	Write	1	Disable Interrupt	1	1	0	0	0	0	0	0
No	parameters			0							

Action — Interrupts are disabled and the interrupt enable status flag is reset.

## 8. Preset Counters Command:

	OPERATION	A <sub>0</sub>	DESCRIPTION	M	SB	D	ATA	A B	US	L	SB
Command	Write	1	Preset Counters	1	1	1	0	0	0	0	0
No	parameters										

Action — The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.



	1 . TI (1		BUS LSB	DATA E		OPERATION AO		
uma i seano	status read.		VE OU FO	O IE IR LP IC	Status Word	Read 1	Command	
This flag i	<ul> <li>(Video Enable) This flag indicate operation of the CRT is enabled, set on a "Start Display" comman on a "Stop Display" or "Reset" cor</li> </ul>	V/VE	IE — (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.  IR — (Interrupt Request) This flag is set at the begin-					
A transfers operation i	- (DMA Underrun) This flag is set data underrun occurs during DM Upon detection of DU, the DMA stopped and the screen is blanked	DU -	frame if	row of the	lay of the last t enable flag is	ning of disp	IR -	
henever the	the vertical retrace interval. This after a status read (FIFO Overrun) This flag is set w FIFO is overrun. It is reset on a	6.9 FO -	ave been	LP — This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.				
				efinU	feeT			
				efinU Fig	faeT sHM l = al			

		ethill	Test Conditions
			Test Conditions
			Trest Conditions
			Test Conditions
			GoodiNood (set)
			Englished Test
			enckibnoð (saT





## **ABSOLUTE MAXIMUM RATINGS\***

 \*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## D.C. CHARACTERISTICS (T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5V ±5%)

Symbol	data undernamenter during DM	Min.	Max.	Units	Test Conditions
VIL IIIIU	Input Low Voltage	-0.5	0.8	V 388	the interrupt enable flag is a status read operation.
V <sub>IH</sub> si gail	Input High Voltageer lastings of	2.0	V <sub>CC</sub> +0.5V	nt perVinper	LP - This flag is set when the lig
V <sub>OL</sub>	Output Low Voltage	0.7	0.45	n reg <b>V</b> ers h	I <sub>OL</sub> = 2.2 mA
V <sub>OH</sub>	Output High Voltage	2.4	6 13310 3	V	I <sub>OH</sub> = -400 μA
I <sub>IL</sub>	Input Load Current		±10	μΑ	V <sub>IN</sub> = V <sub>CC</sub> to 0V
I <sub>OFL</sub>	Output Float Leakage		±10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> to 0V
Icc	V <sub>CC</sub> Supply Current		160	mA	

## CAPACITANCE (T<sub>A</sub> = 25°C, V<sub>CC</sub> = GND = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C <sub>IN</sub>	Input Capacitance		10	pF	f <sub>c</sub> = 1 MHz
C <sub>I/O</sub>	I/O Capacitance		20	pF	Unmeasured pins returned to V <sub>SS</sub> .

## A.C. CHARACTERISTICS ( $T_A = 0^{\circ}C$ to $70^{\circ}C$ , $V_{CC} = 5.0V \pm 5\%$ , GND = 0V)

#### **Bus Parameters**

## **READ CYCLE**

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t <sub>AR</sub>	Address Stable Before READ	0		ns	
t <sub>RA</sub>	Address Hold Time for READ	0		ns	
t <sub>RR</sub>	READ Pulse Width	250		ns	
t <sub>RD</sub>	Data Delay from READ		200	ns	C <sub>L</sub> = 150 pF
tor	READ to Data Floating	20	100	ns	C <sub>L</sub> min. = 20 pF; C <sub>L</sub> max. = 150 pF

#### WRITE CYCLE

Symbol	Parameter	Min.	Max.	Units	<b>Test Conditions</b>
t <sub>AW</sub>	Address Stable Before WRITE	0		ns	
t <sub>WA</sub>	Address Hold Time for WRITE	0		ns	
tww	WRITE Pulse Width	250		ns	
t <sub>DW</sub>	Data Setup Time for WRITE	150		ns	
twp	Data Hold Time for WRITE	0		ns	MATERIAL PROPERTY.

#### **CLOCK TIMING**

Symbol	Parameter	Min.	Max.	Units	Test Conditions
tclk	Clock Period	480		ns	
tKH	Clock High	240		ns	
t <sub>KL</sub>	Clock Low	160		ns	
tKR	Clock Rise	5	30	ns	
t <sub>KF</sub>	Clock Fall	5	30	ns	

ST1-373



## A.C. CHARACTERISTICS (Continued)

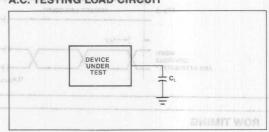
## **OTHER TIMING**

Symbol	Parameter	Min.	Max.	Units	Test Conditions
tcc	Character Code Output Delay		150	ns	C <sub>L</sub> = 50 pF
tHR	Horizontal Retrace Output Delay		200	ns	C <sub>L</sub> = 50 pF
tLC	Line Count Output Delay		400	ns	C <sub>L</sub> = 50 pF
t <sub>AT</sub>	Control/Attribute Output Delay	1111	275	ns	C <sub>L</sub> = 50 pF 3130
tvR	Vertical Retrace Output Delay		275	ns	C <sub>L</sub> = 50 pF
t <sub>RI</sub>	IRQ↓ from RD↑		250	ns	C <sub>L</sub> = 50 pF
two	DRQ↑ from WR↑	T RAJ V	250	anons \/	C <sub>L</sub> = 50 pF
tRQ	DRQ↓ from WR↓	ASTORBAND/	200	ns /\a	C <sub>L</sub> = 50 pF
tLR	DACK↓ to WR↓	Одатол	BOW 1 TO 80 CHAR	ns	9
t <sub>RL</sub>	WR↑ to DACK↑	0		ns	20p
tpR	LPEN Rise		50	ns	JURN STRE
t <sub>PH</sub>	LPEN Hold	100		ns	

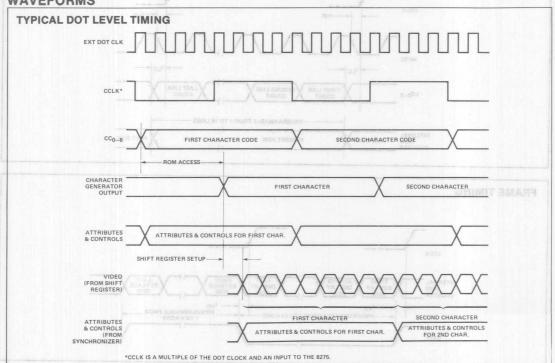
## A.C. TESTING INPUT, OUTPUT WAVEFORM

# 2.4 2.2 TEST POINTS 0.8 A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC: "AND 0.45V FOR A LOGIC: "O. TIMING MEASUREMENTS ARE MADE AT 2.2V FOR A LOGIC: "AND 0.8V FOR A LOGIC: "O. TIMING MEASUREMENTS ARE MADE AT 2.2V FOR A LOGIC: "

## A.C. TESTING LOAD CIRCUIT



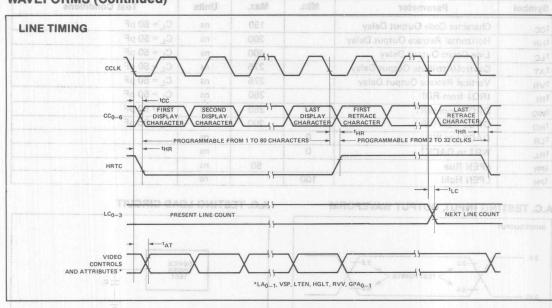
## **WAVEFORMS**

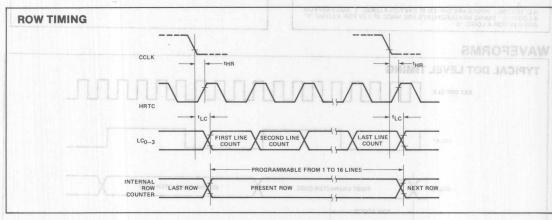


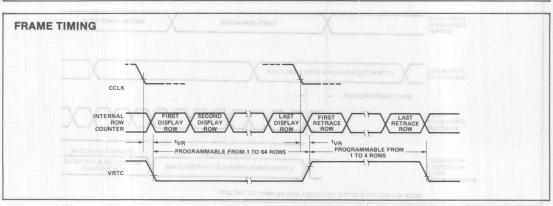




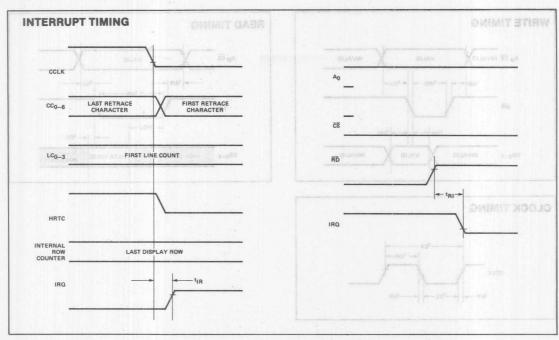


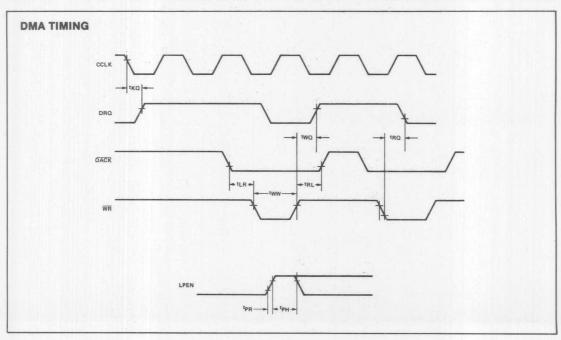






## **WAVEFORMS** (Continued)



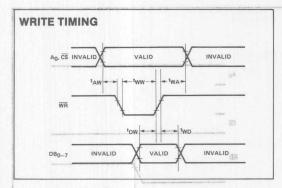


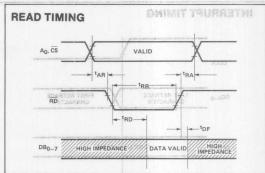


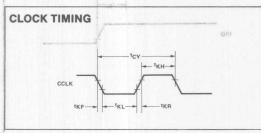


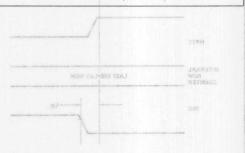
## **WAVEFORMS (Continued)**

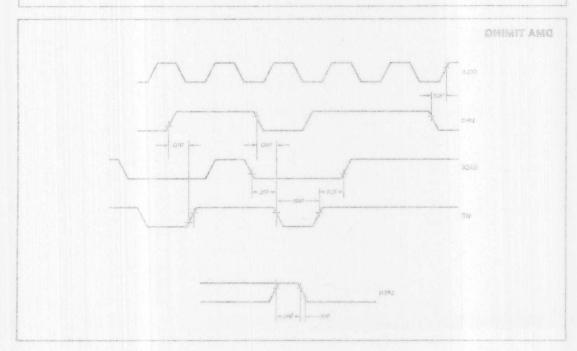
## WAVEFORMS (Continued)













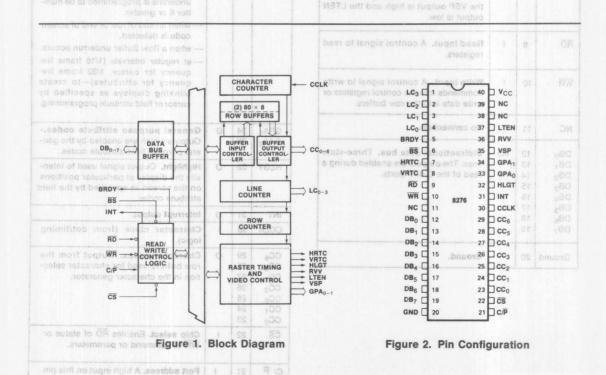
ters and a low input selects the "P" port.

8276

.r eldsT

	-						
JAMS Name and Function	L S	SYS	STEM	CRT CONTROLLER	eqyî	Pin No.	lodniya
+5V power supply.		40	DOV	Line count. Output from the line count-	0		1.03
			NC	or which is used to address the charac-		8	
<ul> <li>Programmable Screen and</li> </ul>	d C	har	acter	■ MCS-51®, MCS-85®, iAPX	86,	and	100
			LTEN	iAPX 88 Compatible			
and TRO ent of langua ceby est aldans beamma port est to sevice at tructuo  6 Independent Visual Field	1 A	ttrib	utes	Buffer ready. Dutout signal indicating that a Ro Buffers and I Bud  Character data.			YORK
Reverse video. Output signal used to	0	36	VVS	■ Single +5V Supply		8	
Cursor Control (4 Types)				■ 40-Pin Package		0	60
cursor is programmed or at the posi- tions specified by the field attribute codes.				Horizontal retrace, Output signal which is active dering the programmed contractal retrace interval. During this	0	7	ЭТЯН

The Intel 8276 Small System CRT Controller is a single chip device intended to interface CRT raster scan displays with Intel microcomputers in minimum device-count systems. Its primary function is to refresh the display by buffering character information from main memory and keeping track of the display position of the screen. The flexibility designed into the 8276 will allow simple interface to almost any raster scan CRT display with a minimum system IC count.



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Table 1. Pin Descriptions

Symbol	Pin No.	Туре	Name and Function
LC <sub>3</sub>	1	0	Line count. Output from the line count-
LC <sub>2</sub>	2		er which is used to address the charac-
LC <sub>1</sub>	3	38	ter generator for the line positions on
LC <sub>0</sub>	4	February	the screen.
BRDY	5	0	Buffer ready. Output signal indicating that a Row Buffer is ready for loading of character data.
BS	6	1	Buffer select. Input signal enabling WR for character data into the Row Buffers.
Scan dis	res		Horizontal retrace. Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
at a the T	an.		
VRTC	8	0	Vertical retrace. Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
RD	9	1	Read input. A control signal to read registers.
WR	10	1	Write input. A control signal to write
VVI	10	D Yee	commands into the control registers or
		314	write data into the row buffers.
NC	11	C CTEN	No connection.
DB <sub>0</sub>	12	1/0	Bidirectional data bus. Three-state
DB <sub>1</sub>	13	J GPA	lines. The outputs are enabled during a
DB <sub>2</sub>	14	D GPA	read of the C or P ports.
DB <sub>3</sub>	15	TO HLOT	
DB <sub>4</sub>	16	TM)	re avea or NW
DB <sub>5</sub>	17	Mao []	NG [11 200
DB <sub>6</sub>	18	600 E	
DB <sub>7</sub>	19	3 CCs	03 Et 🖸 13 25
Ground	20	2 co <sub>3</sub>	Ground.
		,00E	285 [ 17 24
		020[	at Dag Dag
		85 D	SS er D rag

	Symbol	Pin No.	Туре	Name and Function
	Vcc	40		+5V power supply.
	NC	39		No connection.
	NC DE	38	O b	No connection, Idammarporq
	LTEN	37	o IA b	Light enable. Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
	RVV	36	0	Reverse video. Output signal used to activate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
-07	n VSPain m devic	umi	nim r	Video suppression. Output signal used to blank the video signal to the CRT. This output is active:
	nism m Is Hiw 8			during the horizontal and vertical re- trace intervals
				<ul> <li>at the top and bottom lines of rows if underline is programmed to be num- ber 8 or greater.</li> </ul>
				when an end of row or end of screen code is detected.
				when a Row Buffer underrun occurs.      at regular intervals (1/16 frame fre-
	RETO/ PETU	BAHO UOO		quency for cursor, 1/32 frame frequency for attributes)—to create blinking displays as specified by cursor or field attribute programming.
	PRITT	U8 181	in i	
	GPA <sub>1</sub> GPA <sub>0</sub>	34 33	0	General purpose attribute codes Outputs which are enabled by the general purpose field attribute codes.
	HLGT	32	0	<b>Highlight.</b> Output signal used to intensify the display at particular positions on the screen as specified by the field attribute codes.
	INT	31	0	Interrupt output.
	CCLK	30	_	Character clock (from dot/timing logic).
	CC <sub>6</sub> CC <sub>5</sub> CC <sub>4</sub> CC <sub>3</sub> CC <sub>2</sub>	29 28 27 26 25	0	Character codes. Output from the row buffers used for character selection in the character generator.
	CC <sub>1</sub>	24 23		
	CS manga	22	Bloc	Chip select. Enables RD of status or WR of command or parameters.
	C/ P	21	1	Port address. A high input on this pin selects the "C" port or command registers and a low input selects the "P" port or parameter registers.



## FUNCTIONAL DESCRIPTION SOME OT STATE OF THE PROPERTY OF THE PR

## **Data Bus Buffer**

This 3-state, bidirectional, 8-bit buffer is used to interface the 8276 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

C/P	OPERATION	REGISTER
18007	Read R	RESERVED
0	Write	PARAMETER
1	Read	STATUS
office	Write 0	COMMAND

## RD (READ)

A "low" on this input informs the 8276 that the CPU is reading status information from the 8276.

#### WR (WRITE)

A "low" on this input informs the 8276 that the CPU is writing data or control words to the 8276.

## CS (CHIP SELECT)

A "low" on this input selects the 8276 for  $\overline{\text{RD}}$  or  $\overline{\text{WR}}$  of Commands, Status, and Parameters.

#### **BRDY (BUFFER READY)**

A "high" on this output indicates that the 8276 is ready to receive character data.

#### **BS** (BUFFER SELECT)

A "low" on this input enables WR of character data to the 8276 row buffers.

## INT (INTERRUPT)

A "high" on this output informs the CPU that the 8276 needs interrupt service.

C/P	RD	WR	CS	BS	
0	0	1	0	1	Reserved
0	1	0	0	1	Write 8276 Parameter
1	0	1	0	1	Read 8276 Status
1	1	0	0	1	Write 8276 Command
X	1	0	1	0	Write 8276 Row Buffer
X	1	-1	X	X	High Impedance
X	X	X	1	1	High Impedance

## Character Counter MOTTAREGO METRYS

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be derived from the external dot clock.

## **Line Counter**

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Raster Scans) per character row. Its outputs are used to address the external character generator.

## Row Counter mun ent bins wor reg sretogrado

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

## **Raster Timing and Video Controls**

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA<sub>0-1</sub> (General Purpose Attribute) outputs.

## **Row Buffers**

The Row Buffers are two 80-character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

## **Buffer Input/Output Controllers**

The Buffer Input/Output Controllers decode the characters being placed in the row buffers. If the character is a field attribute or special code, they control the appropriate action. (Example: A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)



## SYSTEM OPERATION Telauso Telastation

The 8276 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding and cursor timing.

It is designed to interface with standard character generators for dot matrix decoding. Dot level timing must be provided by external circuitry.

## **General Systems Operational Description**

Display characters are retrieved from memory and displayed on a row-by-row basis. The 8276 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

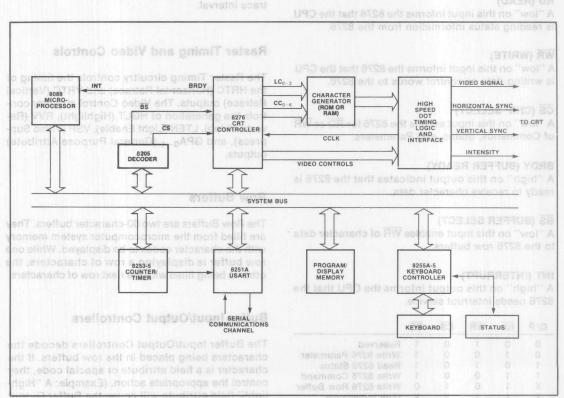
The 8276 uses BRDY to request character data to fill the row buffer that is not being used for display.

The 8276 displays character rows one scan line at a time. The number of scan lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The 8276 provides special Control Codes which can be used to minimize overhead. It also provides Visual Attribute Codes to cause special action on the screen without the use of the character generator. (See Visual Attributes Section.)

The 8276 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is also programmable.

The 8276 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)



Liugiuo T. Did en ela Figure 3. CRT System Block Diagram



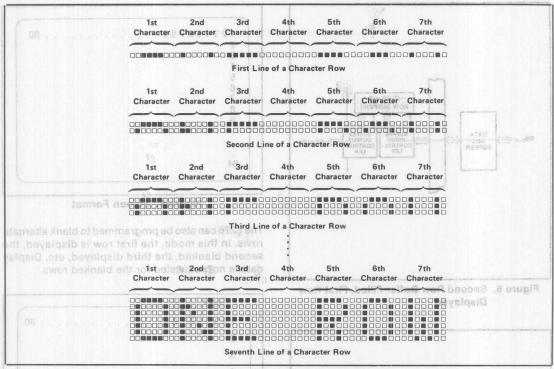


Figure 4. Display Of A Character Row

## **Display Row Buffering**

Before the start of a frame, the 8276 uses BRDY and BS to fill one row buffer with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, the other row buffer is filled with the next row of characters.

After all the lines of the character row are scanned, the buffers are swapped and the same procedure is followed for the next row.

This process is repeated until all of the character rows are displayed.

Row Buffering allows the CPU access to the display memory at all times except during Buffer Loading (about 25%). This compares favorably to alternative approaches which restrict CPU access to the display memory to occur only during horizontal and vertical retrace intervals (80% of the bus time is used to refresh the display.)

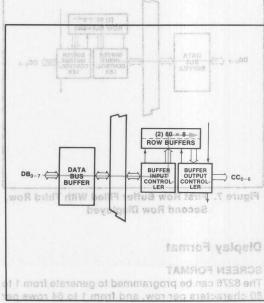


Figure 5. First Row Buffer Filled



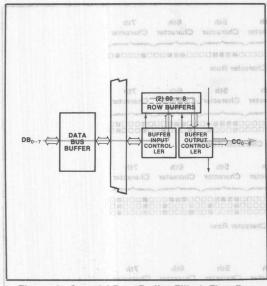


Figure 6. Second Row Buffer Filled, First Row Displayed

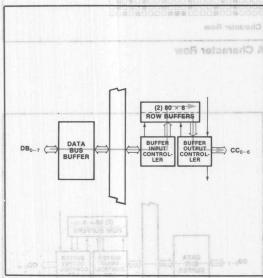


Figure 7. First Row Buffer Filled With Third Row, Second Row Displayed

## **Display Format**

## **SCREEN FORMAT**

The 8276 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.



Figure 8. Screen Format

The 8276 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. Display data is not requested for the blanked rows.

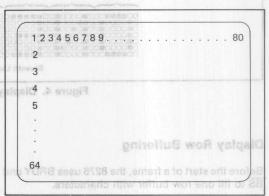


Figure 9. Blank Alternate Rows Mode

## **ROW FORMAT**

The 8276 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the entire character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.



In mode 1, the line counter is offset by one from the line number, no searchs end out extended to be succeed to be a first out to be a fir

Note: In mode 1, while the first line (line number 0) is being displayed, the last count is output by the line counter (see examples).

Line lumber									Line Counter Mode 0	
0					0				0000	111
1									0001	000
2									0010	000
3							0		0011	001
4						0			0.1.00	001
5									0 1 0 1	0 1 0
6		ш.			10.				0110	010
7							111		0111	0 1 1
8							III		1000	0 1 1
9		9		D	0		- 10	0	1001	100
10		0	-0		0				1010	100
11				0					1011	101
12									1100	101
13				0					1101	110
14	 .0		.0			0		P	1110	110
15		0					. 0	0	1111	111

Figure 10. Example of a 16-Line Format

								Counter Mode 0	Counter Mode 1
0								0000	1001
1								0001	0000
2				0		0		0010	0001
3								0011	0010
4					0			0100	0011
- 5								0101	0100
6	0	(=			0	W		0110	0101
-7	10				0	-	0	0111	0110
8	DAGE			0		0	g 🗆	1000	0111
9			0	0	0	0		1001	1000

Figure 11. Example of a 10-Line Format

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number									Counter Mode 0	Counter Mode 1
0	0								0000	1011
1									0001	0000
2					-		0	0	0010	0001
3		00			0				0011	0010
4									0100	0011
5	=								0101	0100
6									0110	0101
7			0	0		0			0111	0110
8						. 0			1000	0111
9							-		1001	1000
10									1010	1001
11		0	0			0			1011	1010

Figure 12. Underline in Line Number 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number								Line Counter Mode 0	Line Counter Mode 1
0								0000	0111
character	00	0					0	0001	0000
aretoared						я.		0010	0001
3		-			- [ ]	-		0011	0010
80). Is then								0100	0011
ensis fi bi	780	-	0	D	0		0	0101	0100
-010 6 5V1	0	(80)	0					0110	0101
dina7anoo	a.Fa					Р.	(88)	0111	0110
									.beised
	Top and Bottom Lines are not Blanked								

Figure 13. Underline in Line Number 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.



#### If the line number of the underline is TAMROT TOO

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

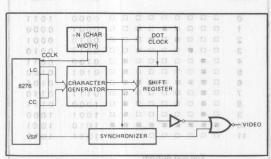


Figure 14. Typical Dot Level Block Diagram

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width, in page and to redmun end to

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

## **Raster Timing**

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This process is constantly repeated.

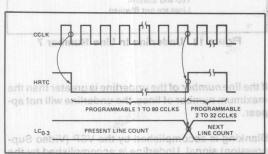


Figure 15. Line Timing 3 (doi.) M3T.

The line counter is driven by the character counter. It is used to generate the line address outputs ( $LC_{0-3}$ ) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

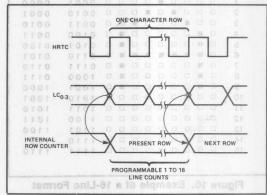


Figure 16. Row Timing

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

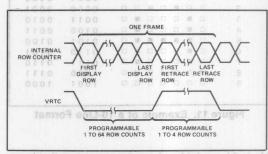


Figure 17. Frame Timing

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.



## **Interrupt Timing**

The 8276 can be programmed to generate an interrupt request at the end of each frame. If the 8276 interrupt enable flag is set, an interrupt request will occur at the beginning of the last display row.

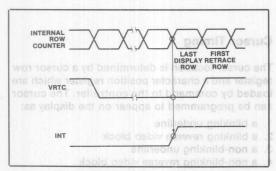


Figure 18. Beginning of Interrupt

INT will go inactive after the status register is read.

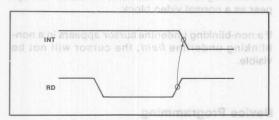


Figure 19. End of Interrupt

A reset command will also cause INT to go inactive, but this is not recommended during normal service.

Note: Upon power-up, the 8276 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the 8276 before system interrupts are enabled.

# VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the 8276 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Field Attribute or Special Code (MSB = 1).

## Special Codes g of bernmangong ed nac 8728 and

Four special codes are available to help reduce bus usage. And to not substant yet because a read as used

## SPECIAL CONTROL CHARACTER

SB 1	enon eni	e are six field attrioure agu
		SPECIAL CONTROL CO
		pression output (VSP). The blint equal to the NOITONUT elresh frequency
	0 0	End of Row SE yd
918	0 1	End of Row-Stop Buffer Loading
Hgh-	1 0	End of Screen inpliced of becuse

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop Buffer Loading (BRDY) Code (01) causes the Buffer Loading Control Logic to stop buffer loading for the rest of the row upon being written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop Buffer Loading (BRDY) Code (11) causes the Row Buffer Control Logic to stop buffer loading for the rest of the frame upon being written. It affects the display in the same way as the End of Screen Code (10).

If the Stop Buffer Loading feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

Note: If a Stop Buffer Loading is not the last character in a row, Buffer Loading is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop Buffer Loading character.

#### **Field Attributes**

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the next field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval



The 8276 can be programmed to provide visible field attribute characters; all field attribute codes will occupy a position on the screen. These codes will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

There are six field attributes:

- 1. Blink-Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
- 2. Highlight-Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
- 3. Reverse Video Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
- 4. Underline—Characters following the code are caused to be underlined by activating the Light of Enable output (LTEN): of reffue and seauso (10)
- 5,6. General Purpose—There are two additional 8276 outputs which act as general purpose, independently programmable field attributes.  $GPA_{0-1}$  are active high outputs.

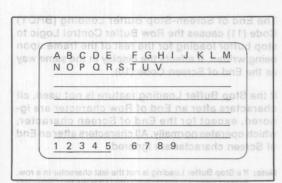
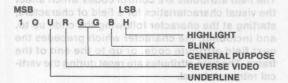


Figure 20. Example of a Visible Field Attribute reference (Underline Attribute)

### FIELD ATTRIBUTE CODE



H = 1 FOR HIGHLIGHTING

B = 1 FOR BLINKING

R = 1 FOR REVERSE VIDEO

U = 1 FOR UNDERLINE Demanapora ed nac 8758 edT

GG = GPA1, GPA0 STI doss to bus ent is temper tour interrupt enable flag is set, an interrupt re

Note: More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

### **Cursor Timing**

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

- 1. a blinking underline
- 2. a blinking reverse video block
- 3. a non-blinking underline
- 4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video cursor appears in a non-blinking reverse video field, the cursor will appear as a normal video block.

If a non-blinking underline cursor appears in a nonblinking underline field, the cursor will not be visible.

### **Device Programming**

The 8276 has two programming registers, the Command Register and the Parameter Register. It also has a Status Register. The Command Register can only be written into and the Status Register can only be read from. They are addressed as follows:

C/P	OPERATION	REGISTER		
0	Read	Reserved		
0	Write	Parameter		
1	Read	Status		
1	Write 83	Command		

The 8276 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.



# Instruction Set MOD TRUBBETH BJBASIC .8

The 8276 instruction set consists of 7 commands.

COMMAND	NO. OF PARAMETER BYTES
Resetti erit bns	citon-Interrutts are disabled
Start Display	nable status flog is reset.
Stop Display	0
Load Cursor	PRESET COUNTERS COMM
Enable Interrupt	PRESET COUNTERS COMMI
Disable Interrupt	0
Preset Counters	Commend Write 1 Press County

In addition, the status of the 8276 can be read by the CPU at any time.

# 1. RESET COMMAND sib neeros s of phionogeomos

of the frame

	OPERATION	C/P	DESCRIPTION	DATA BUS MSB LSB
Command	Write - 11	3/1	Reset Command	00000000
and syn-	Write	0	Screen Comp Byte 1	<b>S</b> Н Н Н Н Н Н
	-	0	Screen Comp Byte 2	VVRRRRRR
Parameters	Write	0	Screen Comp Byte 3	UUUULLL
	Write	0	Screen Comp Byte 4	M1CCZZZZ

Action—After the reset command is written, BRDY goes inactive, 8276 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up

As parameters are written, the screen composition is defined. On Velocif Disable and test with the "Reset" command.

# Parameter—S Spaced Rows

S	FUNCTIONS
0	Normal Rows umetri ent 1
100	Spaced Rows

# (Improper Command) This flag is set when a comma Parameter—HHHHHHHH commo comma Horizontal Characters/Row Horizontal Characters/Row

Н	н	н					12	NO. OF CHARACTERS PER ROW
0 0 0	0 0 0	0	0	0	1	0	AR	operation of the CR set on & "Start Displ on a "Stop Display"
aver	0	0	tet ale	e e	0	1	ain	T (Buffer Underrun) T Row 808 er is not fill till benefindering
ibs is li	ol in	ter u b	li Li			s is	ini ne	Upon activation of ceases, and the son thebenilebnU etrace i

### Parameter---VV Vertical Retrace Row Count

V V	NO. OF RO	WCOUN	ITS	PE	RV	RT	C
0 0	an han ein	1	+3-	7	à.	1.0	-
0 1	2	2			0		
1 0	4	3		0		0	
1 1	- 8	4	0				

### Parameter---RRRRRR Vertical Rows/Frame

	R	R	R	R	R	R	NO. OF ROWS/FRAME
enil	0 0 0		000			1	colneid ion = 0 1be/insid = 1) 2 3
						QN	START DISPLAY COMMA
652	11	1	1	de	1	dome	10830 NO M64A390
5	0 0	0	0 1	0	0	play	Committee 1 Start Dis

### Parameter—UUUU Underline Placement

Vide	one i	de	U	U	U	LINE NUMBER OF DIV. 9VI
	0	)	0	0	0	1
	0	) (	0	0	1	2
	0	) (	0	1	0	3
					. (	STOP DISPLAY. COMMAN
	SUB AT					OPERATION OF DESCRIPT
	000				1	get gove 16 other branch
		_			1	No parameters

# Parameter—LLLL Number of Lines per Character Row

0	"ye	i	916	ųi	Star	NO. OF LINES/ROW	
	.V10	200	2173	AT	ir alı	TENEDITON D	
		0	0	0	0	1	
		0	0	0	1	2	
		0	0	1	0	3	
						OAD CURSOR POSITION	
					1101	OPERATION CIP DESCRIPT	
		1	1	1	1	wand Wms 11 Load Cure	
	nino	har	T U	(KJ)	191	mothers Wines D Under Numb	

### Parameter—M Line Counter Mode

noMia	og ToLINE COUNTER MODE amanag owt
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

### Parameter—CC Cursor Format

5. ENABLE INTERRUPT COMMAND

0 [	C	C	CURSOR FORMAT
	0	0	Blinking reverse video block
	0	1	Blinking underline
	1	0	Non-blinking reverse video block
	1	1	Non-blinking underline dang ens



### Parameter—ZZZZ Horizontal Retrace Count

			Z		CC	CTER V	
	0	0	0	0	3	2	1 0
	0	0	0	1	8	4	
	0	0	1	0	16	6	111
					-		
omi	1	ıdri	ofi	Ito	lineV	AAA 32 A-	Paramoter-

Note: uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

### 2. START DISPLAY COMMAND

	OPERATION	C/P	DESCRIPTION	M	SB		ATA	B	US	LS	SB
Command	Write	1	Start Display	0	0	1	0	0	0	0	0
No p	arameters										

Action—8276 interrupts are enabled, BRDY goes active, video is enabled, Interrupt Enable and Video Enable status flags are set.

### 3. STOP DISPLAY COMMAND

	OPERATION	C/P	DESCRIPTION	м	SB	DA	ATA	В	US	LS	SB
Command	Write	1	Stop Display	0	1	0	0	0	0	0	0

Action—Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to reenable the display.

### 4. LOAD CURSOR POSITION

	OPERATION	C/P	DESCRIPTION	MSB LSB
Command	Write 8	1	Load Cursor	10000000
Parameters	Write Write	0	Char. Number Row Number	(Char. Position in Row) (Row Number)

Action—The 8276 is conditioned to place the next two parameter bytes into the cursor position registers. Status flag not affected.

### 5. ENABLE INTERRUPT COMMAND

	OPERATION	C/P	M	SB	D	ATA	В	US		SB	
Command	Write	09.8	Enable Interrupt	1	0	1	0	0	0	0	C
No p	parameters	Saint .			9			ñ	in its	-	Ī

Action—The interrupt enable flag is set and interrupts are enabled.

### 6. DISABLE INTERRUPT COMMAND

shaama	OPERATION	C/P	DESCRIPTION	M	SB		ATA	B	US	1	SB
Command	Write	1	Disable Interrupt	1	1	0	0	0	0	0	0
No p	parameters		in nu				24	253	64		

Action—Interrupts are disabled and the interrupt enable status flag is reset.

### 7. PRESET COUNTERS COMMAND

	OPERATION	C/P	DESCRIPTION	M	SB	D	ATA	B	US.	LS	SB
Command	Write	1	Preset Counters	1	1	1	0	0	0	0	0
No p	arameters	tres	and the protect	0	a.	1.9	6	0	41		10

Action—The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

# Status Flags | Drammoo lear ent rettA-noito

and the ATC and	OPERATION	C/P	DESCRIPTION	DATA BUS MSB LSB
Command	Read	ad f	Status Word	0 IE IR X IC VE BU X

- IE (Interrupt Enable) Set or reset by command.

  It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.
- IR (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.
- IC (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.
- VE (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.
- BU (Buffer Underrun) This flag is set whenever a Row Buffer is not filled with character data in time for a buffer swap required by the display. Upon activation of this bit, buffer loading ceases, and the screen is blanked until after the vertical retrace interval.



# A.C. CHARACTERISTICS (TA = 0°C to 70°C; VCC = 5.0V ±5%; \*201TAR MUMIXAM 3TUIOSBA

Ambient Temperature Under Bias ....0°C to 70°C Storage Temperature .....-65°C to +150°C Voltage On Any Pin

 \*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Address Stable Before READ Address Hold Time for READ

## D.C. CHARACTERISTICS (TA = 0°C to 70°C; VCC = 5V ±5%)

SYMBOL	PARAMETER an	MIN.	MAX.	UNITS	TEST CONDI	TIONS and
V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	V		
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 0.5V	V	3.	RITE CYC
Vol	Output Low Voltage	37.0.08	0.45	V	I <sub>OL</sub> = 2.2 mA	E ATROPES DE LE COMO
VoH	Output High Voltage	2.4	.971103	V	$I_{OH} = -400  \mu A$	JUGINIS
tic	Input Load Current		±10	μΑ	$V_{IN} = V_{CC}$ to 0V	WA
lofL	Output Float Leakage		±10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> to 0.45	/ AWS
lcc	V <sub>CC</sub> Supply Current		160	mA	MADIN BRIDE PURB WIGHT	M.M.I
	611		UGI	211/199	Data Setup Time for	MG.
	en		0	STIRV	Data Hold Time for V	gwj

# CAPACITANCE (TA = 25°C; VCC = GND = 0V)

CLOCK TIMING

aai

SYMBOL	PARAMETI	RTIMU	MIN.	MAX.	UNITS	TEST CONDITION	ONS
CIN	Input Capacitance	en		10	pF	f <sub>C</sub> = 1 MHz	) JOIN
C <sub>I/O</sub>	I/O Capacitance	ns		20	pF	Unmeasured pins return	ned to V <sub>SS</sub>
		en		car		Clock Low	THE
		an	30	- 5		Clock Rise	
		an.	30	5		Clock Fall	1KF

Note 1: AC timings measured at  $V_{OH}=2.0$ ,  $V_{OL}=0.8$ ,  $V_{IH}=2.4$ ,  $V_{IL}=0.45$ .

### OTHER TIMING

JOSMYS	PARAMETER	MIN	.XAM	UNITS	TEST CONDITIONS
00	Character Code Output Delay			នព	O <sub>L</sub> = 50 pF
	Horizontal Retrace Output Delay		200	an	C <sub>L</sub> = 50 pF
LC	Line Count Output Delay		400	ns	OL = 50 pF
TA	Control/Attribute Output Delay		275	an	C <sub>L</sub> = 50 pF
AV	Vertical Retrace Output Delay			en	
181	INT   from RD†		250		$C_L = 50 \text{ pF}$
OW!	BRDY† from WR†		250	an	- Ct = 50 pF
OR	BRDY! from WRI		200	sn	G <sub>L</sub> = 50 pF
RJ	BSĮ to WRĮ	-0		an	
	WR7 to 851	0		ns	



# A.C. CHARACTERISTICS (T<sub>A</sub> = 0°C to 70°C; V<sub>CC</sub> = 5.0V ±5%; GND = 0V)

# **Bus Parameters (Note 1)**

# READ CYCLE obsessor landitional bins vino golden seems a si

SYMBOL	PARAMETER IN 10 and	MIN.	MAX.	UNITS	TEST CONDITIONS
t <sub>AR</sub>	Address Stable Before READ	0		ns	
t <sub>RA</sub>	Address Hold Time for READ	0		ns	自己的最高。 第二章
t <sub>RR</sub>	READ Pulse Width	250	70°C: Vcc	ns ns	CHARACTERISTICS
t <sub>RD</sub>	Data Delay from READ		200	ns	C <sub>L</sub> = 150pF
tor ewor	READ to Data Floating	20	100	ns 8	TEMARAS JOEMYS

8276

### WRITE CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t <sub>AW</sub>	Address Stable Before WRITE	0		ns	Senson Hills and the Hill
twa	Address Hold Time for WRITE	0		ns	GHBHNAS EBOJ ARQN
tww	WRITE Pulse Width	250		ns	development midno 146
tow	Data Setup Time for WRITE	150	1	ns	mauno Ardos 304 05
twp	Data Hold Time for WRITE	0		ns	

### **CLOCK TIMING**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
tCLK	Clock Period	480		ns	annetinens 2 tunni
tkH	Clock High	240		ns	pagetinean O.U.
t <sub>KL</sub>	Clock Low	160		ns	
t <sub>KR</sub>	Clock Rise	5	30	ns	
tKF	Clock Fall	5	30	ns	

Note 1: AC timings measured at  $V_{OH} = 2.0$ ,  $V_{OL} = 0.8$ ,  $V_{IH} = 2.4$ ,  $V_{IL} = 0.45$ .

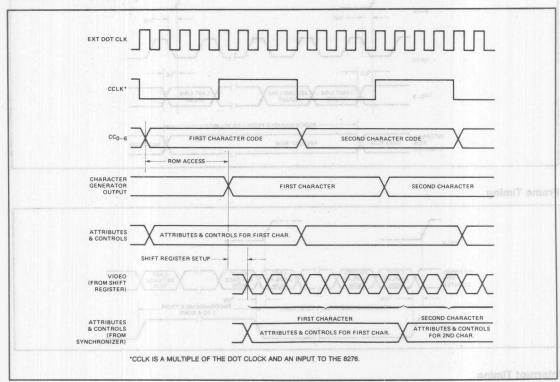
### **OTHER TIMING**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
tcc	Character Code Output Delay		150	ns	C <sub>L</sub> = 50 pF
t <sub>HR</sub>	Horizontal Retrace Output Delay		200	ns	C <sub>L</sub> = 50 pF
tLC	Line Count Output Delay		400	ns	C <sub>L</sub> = 50 pF
t <sub>AT</sub>	Control/Attribute Output Delay		275	ns	C <sub>L</sub> = 50 pF
tvR	Vertical Retrace Output Delay		275	ns	C <sub>L</sub> = 50 pF
t <sub>RI</sub>	INT↓ from RD↑		250	ns	C <sub>L</sub> = 50 pF
twQ	BRDY↑ from WR↑		250	ns	C <sub>L</sub> = 50 pF
tRQ	BRDY↓ from WR↓		200	ns	C <sub>L</sub> = 50 pF
tLR	BS↓ to WR↓	0		ns	
t <sub>RL</sub>	WR↑ to BS↑	0		ns	

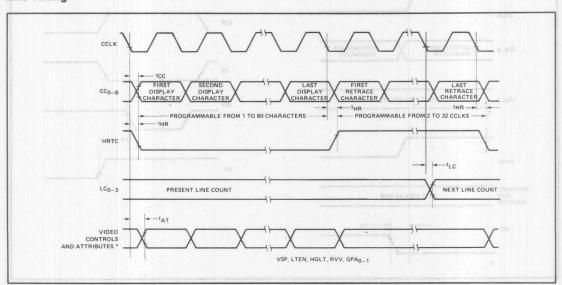


### **WAVEFORMS**

### **Typical Dot Level Timing**

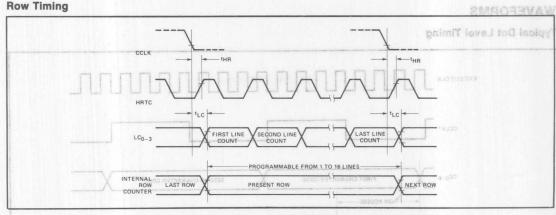


### **Line Timing**

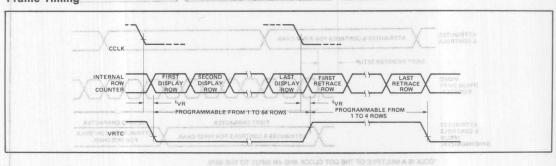


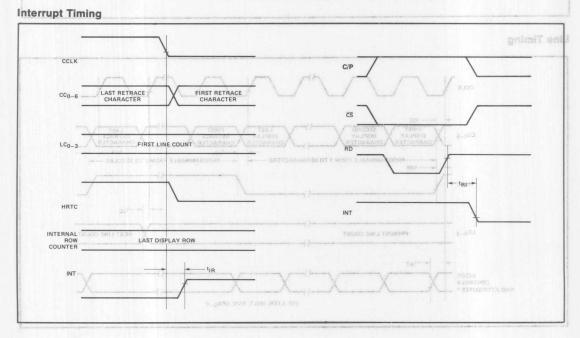






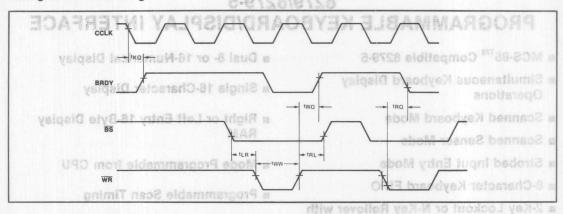
### Frame Timing









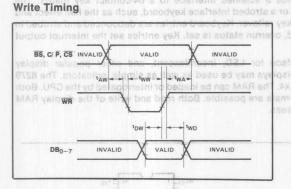


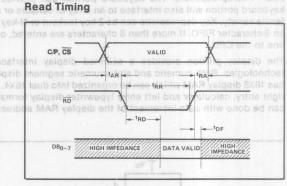
The Intel® 8278 is a general purpose programmable keyboard and display i/O interface device designed for use with

a Interrupt Output on Key Entry

A DOM RUGS

# de a scanned interface to a 64-contact key

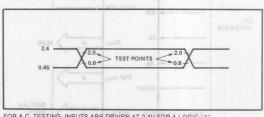




### **Clock Timing**

# NR CL ▼ tKH+→ BE tKR EA TUO !!

### Input and Output Waveforms for A.C. Tests



FOR A.C. TESTING, INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS FOR INPUT AND OUTPUT SIGNALS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

Figure 2. Pin Configuration





# 8279/8279-5

# PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- MCS-85<sup>TM</sup> Compatible 8279-5
- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8-Character Keyboard FIFO
- 2-Key Lockout or N-Key Rollover with Contact Debounce

- Dual 8- or 16-Numerical Display
- Single 16-Character Display
- Right or Left Entry 16-Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- m Interrupt Output on Key Entry

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

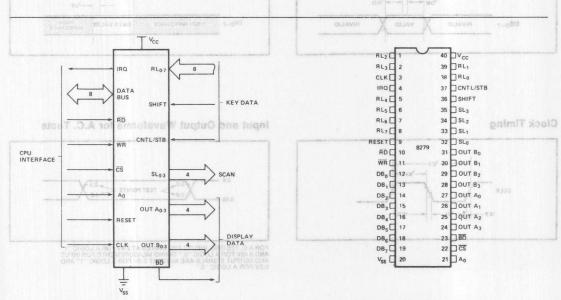


Figure 1. Logic Symbol

Figure 2. Pin Configuration



seboli tuo

### HARDWARE DESCRIPTION

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Table 1. Pin Descriptions viscons motors are available and in before

Symbol		Pin No.	Name and Function
DB <sub>0</sub> -DB <sub>7</sub>	variou	8	<b>Bi-directional data bus:</b> All data and commands between the CPU and the 8279 are transmitted on these lines.
CLK orgol		y <b>1</b> bos	Clock: Clock from system used to generate internal timing.
lete Burte-Tasan that connect the n the chip is not high impedance and output during			Reset: A high signal on this pin resets the 8279. After being reset the 8279 is placed in the following mode:  1) 16 8-bit character display—left entry.  2) Encoded scan keyboard—2 key lockout.  Along with this the program clock
Control	garant	oas	prescaler is set to 31.
cs modes and CPU. The	d by the		Chip Select: A low on this pin enables the interface functions to receive or transmit.
Ao ne ne	and the	1 = ( ed)	Buffer Address: A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
RD, WR	SCNSON	2	Input/Output Read and Write: These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
IRQ	sur		Interrupt Request: In a key- board mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/ Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
V <sub>SS</sub> , V <sub>CC</sub>	CIPIAGO	2	Ground and power supply pins.
SL <sub>0</sub> -SL <sub>3</sub>	JORTA	4	Scan Lines: Scan lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
RL <sub>0</sub> -RL <sub>7</sub>	MAUT 6 A THIST CHITCHES	8 SA	Return Line: Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.

Symbol ×8) 595	Pin No.	Name and Function					
SHIFT SHOP MAN	d in	Shift: The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.					
	1 (siqe hid- mnoi	Control/Strobed Input Mode: For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode.  (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.					
OUT A <sub>0</sub> -OUT A <sub>3</sub> OUT B <sub>0</sub> -OUT B <sub>3</sub>	4 4 1m b 1sib 1	Outputs: These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL <sub>0</sub> –SL <sub>3</sub> ) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8-bit port.					
BD	1	Blank Display: This output is used to blank the display during digit switching or by a display blanking command.					

### **FUNCTIONAL DESCRIPTION**

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit microprocessors.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279. These modes include:

manpalG koel6

### input modes

- Scanned Keyboard with encoded (8 x 8 key keyboard) or decoded (4 x 8 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.
- Scanned Sensor Matrix with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines.
   Key status (open or closed) stored in RAM addressable by CPU.
- Strobed Input Data on return lines during control line strobe is transferred to FIFO.

### Output Modes at bedara lorded

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit (B<sub>0</sub> = D<sub>0</sub>, A<sub>3</sub> = D<sub>7</sub>).
- · Right entry or left entry display formats.

Other features of the 8279 include:

- · Mode programming from the CPU.
- Clock Prescaler
- Interrupt output to signal CPU when there is keyboard or sensor data available.
- An 8 byte FIFO to store keyboard information.
- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.

### PRINCIPLES OF OPERATION

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 3.

### I/O Control and Data Buffers

The I/O control section uses the  $\overline{CS}$ ,  $A_0$ ,  $\overline{RD}$  and  $\overline{WR}$  lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by  $\overline{CS}$ . The character of the information, given or desired by the CPU, is identified by  $A_0$ . A logic one means the information is a command or status. A logic zero means the information is data.  $\overline{RD}$  and  $\overline{WR}$  determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ( $\overline{CS}$  = 1), the devices are in a high impedance state. The drivers input during  $\overline{WR} \bullet \overline{CS}$  and output during  $\overline{RD} \bullet \overline{CS}$ .

### **Control and Timing Registers and Timing Control**

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with  $A_0 = 1$  and then sending a  $\overline{WR}$ . The command is latched on the rising edge of  $\overline{WR}$ .

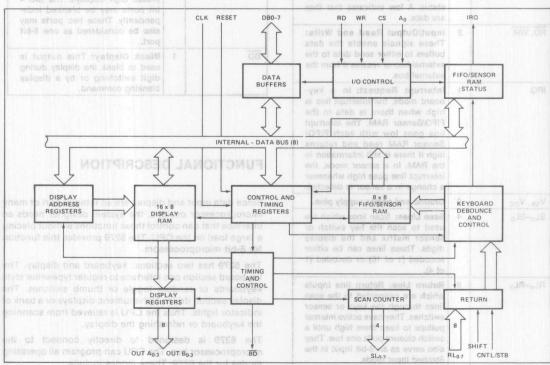


Figure 3. Internal Block Diagram



The command is then decoded and the appropriate function is set. The timing control contains the basic timing counter chain. The first counter is a  $\div$  N prescaler that can be programmed to yield an internal frequency of 100 kHz which gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

### Scan Counter on organ os xelf = BA

The scan counter has two modes. In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display. In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan. Note than when the keyboard is in decoded scan, so is the display. This means that only the first 4 characters in the Display RAM are displayed.

In the encoded mode, the scan lines are active high outputs. In the decoded mode, the scan lines are active low outputs.

# Return Buffers and Keyboard Debounce and Control

The 8 return lines are buffered and latched by the Return Buffers. In the keyboard mode, these lines are scanned, looking for key closures in that row. If the debounce circuit detects a closed switch, it waits about 10 msec to check if the switch remains closed. If it does, the address of the switch in the matrix plus the status of SHIFT and CONTROL are transferred to the FIFO. In the scanned Sensor Matrix modes, the contents of the return lines is directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time. In Strobed Input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

# FIFO/Sensor RAM and Status

This block is a dual function 8 x 8 RAM. In Keyboard or Strobed Input modes, it is a FIFO. Each new entry is written into successive RAM positions and each is then read in order of entry. FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or writes will be recognized as an error. The status can be read by an  $\overline{\text{RD}}$  with  $\overline{\text{CS}}$  low and  $A_0$  high. The status logic also provides an IRQ signal when the FIFO is not empty. In Scanned Sensor Matrix mode, the memory is a Sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix. In this mode, IRQ is high if a change in a sensor is detected.

### Display Address Registers and Display RAM

The Display Address Registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The Display RAM can be directly read by the CPU after the correct mode and address is set. The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU. The A and B nibbles can be entered independently or as one word, according to the mode that is set by the CPU. Data entry to the display can be set to either left or right entry. See Interface Considerations for details.

### SOFTWARE OPERATION

### 8279 commands

The following commands program the 8279 operating modes. The commands are sent on the Data Bus with  $\overline{CS}$  low and  $A_0$  high and are loaded to the 8279 on the rising edge of  $\overline{WR}$ .

# Keyboard/Display Mode Set

	MSI	3							
Code:	0	0	0	D	D	K	K	K	

Where DD is the Display Mode and KKK is the Keyboard Mode.

### DD

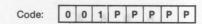
- 0 0 8 8-bit character display Left entry
- 0 1 16 8-bit character display Left entry\* 388 1918
- 1 0 8 8-bit character display Right entry
- 1 1 16 8-bit character display Right entry

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

### KKK

- 0 0 0 Encoded Scan Keyboard 2 Key Lockout\*
- 0 0 1 Decoded Scan Keyboard 2-Key Lockout
- 0 1 0 Encoded Scan Keyboard N-Key Rollover
- 0 1 1 Decoded Scan Keyboard N-Key Rollover
- 1 0 0 Encoded Scan Sensor Matrix
- 1 0 1 Decoded Scan Sensor Matrix
- 1 1 0 Strobed Input, Encoded Display Scan
- 1 1 1 Strobed Input, Decoded Display Scan comeno

### Program Clock



All timing and multiplexing signals for the 8279 are generated by an internal prescaler. This prescaler divides the external clock (pin 3) by a programmable integer. Bits PPPPP determine the value of this integer which ranges from 2 to 31. Choosing a divisor that yields 100 kHz will give the specified scan and debounce times. For instance, if Pin 3 of the 8279 is being clocked by a 2 MHz signal, PPPPP should be set to 10100 to divide the clock by 20 to yield the proper 100 kHz operating frequency.

### Read FIFO/Sensor RAM

Code:	0	1	0	Al	X	A	A	A	X = Don't Care
									the FIFO/Sensor

\*Default after reset.





board Mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read ( $A_0=0$ ) in the same sequence in which the data first entered the FIFO. All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set (AI = 1), each successive read will be from the subsequent row of the sensor RAM.

### Read Display RAM

Code: 0 1 1 Al A A A A

The CPU sets up the 8279 for a read of the Display RAM by first writing this command. The address bits AAAA select one of the 16 rows of the Display RAM. If the AI flag is set (AI = 1), this row address will be incremented after each following read *or write* to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read *or write* address and the sense of the Auto-Increment mode for both operations.

### Write Display RAM

Code: 1 0 0 Al A A A A

The CPU sets up the 8279 for a write to the Display RAM by first writing this command. After writing the command with  $A_0=1$ , all subsequent writes with  $A_0=0$  will be to the Display RAM. The addressing and AutoIncrement functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display or FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next Read location.

### Display Write Inhibit/Blanking

A B A B Code: 1 0 1 X IW IW BL BL

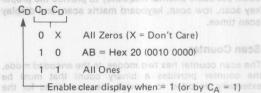
The IW Bits can be used to mask nibble A and nibble B in applications requiring separate 4-bit display ports. By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the Display RAM from the CPU do not affect that port. Thus, if each nibble is input to a BCD decoder, the CPU may write a digit to the Display RAM without affecting the other digit being displayed. It is important to note that bit  $B_0$  corresponds to bit  $D_0$  on the CPU bus, and that bit  $A_3$  corresponds to bit  $D_7$ .

If the user wishes to blank the display, the BL flags are available for each nibble. The last Clear command issued determines the code to be used as a "blank." This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

### Clear

Code: 1 1 0 C<sub>D</sub> C<sub>D</sub> C<sub>D</sub> C<sub>F</sub> C<sub>A</sub>

The C<sub>D</sub> bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows:



During the time the Display RAM is being cleared ( $\sim$ 160  $\mu$ s), it may not be written to. The most significant bit of the FIFO status word is set during this time. When the Display RAM becomes available again, it automatically resets

If the  $C_F$  bit is asserted ( $C_F$ =1), the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

 $C_A$ , the Clear All bit, has the combined effect of  $C_D$  and  $C_F$ ; it uses the  $C_D$  clearing code on the Display RAM and also clears FIFO status. Furthermore, it resynchronizes the internal timing chain.

# End Interrupt/Error Mode Set

Code: 1 1 1 E X X X X X = Don't care.

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset).

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

### Status Word

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when  $A_0$  is high and  $\overline{CS}$  and  $\overline{RD}$  are low. See Interface Considerations for more detail on status word.

### **Data Read**

Data is read when A<sub>0</sub>,  $\overline{CS}$  and  $\overline{RD}$  are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of  $\overline{RD}$  will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

### Data Write

Data that is written with  $A_0$ ,  $\overline{CS}$  and  $\overline{WR}$  low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of  $\overline{WR}$  occurs if AI set by the latest display command.



### INTERFACE CONSIDERATIONS

### Scanned Keyboard Mode, 2-Key Lockout

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. Other depressed keys are looked for during the next two scans. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, IRQ will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

### Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down. If it is, the key is entered into the FIFO. Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

### Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode. If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set). The error flag could be read in this mode by reading the FIFO STATUS word. (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with CF = 1.

### Sensor Matrix Mode

In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure. To make the software easier, the designer should functionally group the sensors by row since this is the format in which the CPU will read them. The IRQ line goes high if any sensor value change is detected at the end of a sensor matrix scan. The IRQ line is

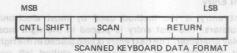
cleared by the first data read operation if the Auto-

Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

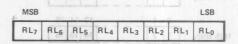
Note: Multiple changes in the matrix Addressed by  $(SL_{0-3} = 0)$  may cause multiple interrupts.  $(SL_{0} = 0)$  in the Decoded Mode). Reset may cause the 8279 to see multiple changes.

### **Data Format**

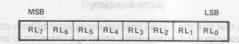
In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines (non-inverted). CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.



In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch postion maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.



In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.



### Display

### Left Entry

Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left most position and filling again proceeds from there



	0 1	14 15
2nd entry	1 2 1871 9	ti ni est ni
	8279 to 1eeonu	ed 14 15
16th entry	1 2	15 16
	mode, tite oha	
17th entry	17 2	15 16
	is the MSB <sub>0</sub> of	
18th entry	17 18	15 16

LEFT ENTRY MODE
(AUTO INCREMENT)

### **Right Entry**

Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.

	2000	14 15 0 ← Display
1st entry	Fught of Vic	1 RAM Address
	2 3 1 0	thing that cant bo cernected
2nd entry	iggeren u e inauss Ei	yn A ebom
	3 4	input ports core of terior dito the r
3rd entry		1 2 3
	0 1	13 14 15
	-	
16th entry	1 2	14 15 16
	1 2	14 15 0 on bedout of
17th entry		from the ret. 15 16 17 the dat
	2 3	edge of a CNTL/STE line pu
18th entry	3 4	26 bear 16 17 18 5 and muler
		inoni

Note that now the display position and register address do not correspond. Consequently, entering a character to ah arbitrary position in the Auto Increment mode may have

RIGHT ENTRY MODE (AUTO INCREMENT)

arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address

0 with sequential entry is recommended.

### Auto Increment not valuable transfer of the Increment and Increm

In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:

	0	1	2	3	4	5	6	7
2nd entry	1	2	10	erij	loc	שר	110	1
assion an along wit	0	1	2	3	4	5	6	7
Command 10010101		2	3.	ani	T	TH	8 13	1
	En	ter	nex	t at	Lo	cati	on !	5 A
losed swit	-	dio	2	3	4	5	6	
3rd entry	1	2	.en	0.8	lett.	3	tac	6
	170773333							
	0	1	2	3		3		7

(AUTO INCREMENT)
In the Right Entry mode, Auto Incrementing and

In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:

1	2	3	4	5	6	7	0-	← Display
	a la la	i,	134	do	8.0	101	1	RAM Address
	TYY	b.	1		1.	1	_	
	3	4						
2010	qal					1	_	
	2	2 3	2 3 4	2 3 4 5	2 3 4 5 6	2 3 4 5 6 7	2 3 4 5 6 7 0	2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 1 2 2 3 4 5 6 7 0 1

	3	4	5	6	7	0	1	2
3rd entry	retr	el b	3	90	170	1	2	ei ei
		ows	9	opi	iod	de	9	T
	4	5	6	1	0	1	2	3

RIGHT ENTRY MODE (AUTO INCREMENT)

Starting at an arbitrary location operates as shown below:

	0	1	2	3	4	5	6	7-	Display
Command 10010101		30	ing fi	10			PHE		RAM Address
	En	tor	nov	+	10	anti	00 6	Auto	Ingramas

4 5 6 7 3 0 1st entry 2 3 4 5 6 7 0 2nd entry 8th entry 8 2 3 9th entry 6 8 9 2 3 4





Entry appears to be from the initial entry point.

# 8/16 Character Display Formats seems a si sidt . solveb

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).

Maximum Ratings" may cause permanent damage to

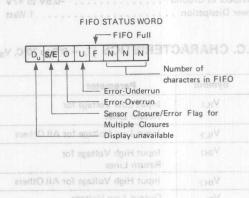
### G. FIFO Status

FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure indication is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.



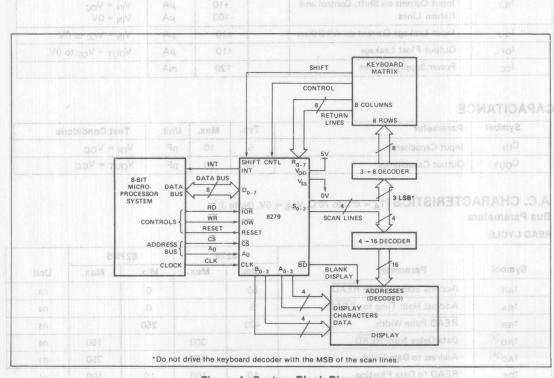


Figure 4. System Block Diagram



### ABSOLUTE MAXIMUM RATINGS\*

Ambient Temperature	17	10						Di	. 0°C to 70°C
Storage Temperature .	110	3	18		et	0	1	-1	65°C to 125°C
Voltage on any Pin with	1								
Respect to Ground .	100		5						-0.5V to +7V
Power Dissipation									1 Watt

\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **D.C. CHARACTERISTICS** $[T_A = 0^{\circ}C \text{ to } 70^{\circ}C, V_{SS} = V_{CC} = +5V \pm 5\%, V_{CC} = +5V \pm 10\% (8279-5)]$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
VIL1 Flag for	Input Low Voltage for Return Lines	-0.5	1.4	un Scourt	FIFO is attempted. Under a to read an empty FIFO.
V <sub>IL2</sub>	Input Low Voltage for All Others	-0.5	0.8	of tide a	a EIEO status word also he
V <sub>IH1</sub>	Input High Voltage for Return Lines	2.2 <sub>0 y</sub>		s ec.V.se a	play RAM was unavailable sar All command had no
V <sub>IH2</sub>	Input High Voltage for All Others	2.0		V	anation.
VOL	Output Low Voltage		0.45	V	Note 1
V <sub>OH1</sub>	Output High Voltage on Interrupt Line	3.5		V	Note 2
V <sub>OH2</sub>	Other Outputs	2.4			
I <sub>IL1</sub>	Input Current on Shift, Control and Return Lines		+10 -100	μΑ μΑ	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = 0V
I <sub>IL2</sub>	Input Leakage Current on All Others		±10	μΑ	V <sub>IN</sub> = V <sub>CC</sub> to 0V
IOFL	Output Float Leakage		±10	μΑ	V <sub>OUT</sub> = V <sub>CC</sub> to 0V
Icc	Power Supply Current		120	mA	

### CAPACITANCE

Symbol	Parameter	Тур.	Max.	Unit	Test Conditions
CIN	Input Capacitance	5	10	pF	VIN = VCC
COUT	Output Capacitance	10	20	pF	V <sub>OUT</sub> = V <sub>CC</sub>

# A.C. CHARACTERISTICS [ $T_A = 0^{\circ}C$ to $70^{\circ}C$ , $V_{SS} = 0V$ , (Note 3)] Bus Parameters

### READ CYCLE

		82	79	827		
Symbol	Parameter XMAIS	Min.	Max.	Min.	Max.	Unit
t <sub>AR</sub>	Address Stable Before READ	50		0		ns
t <sub>RA</sub>	Address Hold Time for READ	5		0		ns
t <sub>RR</sub>	READ Pulse Width	420		250		ns
t <sub>RD</sub> [4]	Data Delay from READ		300		150	ns
t <sub>AD</sub> [4]	Address to Data Valid	sboard decode	450	n où	250	ns
t <sub>DF</sub>	READ to Data Floating	10	100	10	100	ns
tRCY	Read Cycle Time	1		1		μs





### A.C. CHARACTERISTICS (Continued)

### WRITE CYCLE

		82	79	827	SEAD OPE	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t <sub>AW</sub>	Address Stable Before WRITE	50	A STATE OF THE STA	0	DESCRIPTION OF THE PARTY OF THE	ns
tWA	Address Hold Time for WRITE	20		0	X	ns
t <sub>WW</sub>	WRITE Pulse Width	400		250	0.17	ns
t <sub>DW</sub>	Data Set Up Time for WRITE	300		150		ns
t <sub>WD</sub>	Data Hold Time for WRITE	40		0		ns
twcy	Write Cycle Time	1		1/		μS

### **OTHER TIMINGS**

	WHIGH IMPEDANCE	MALIE TALLE	GUAVAT 8279		8279-5	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t <sub>Ø</sub> W	Clock Pulse Width	230		120		nsec
tcy	Clock Period	500		320	MOITA	nsec

Key Scan Time ......80 μsec 

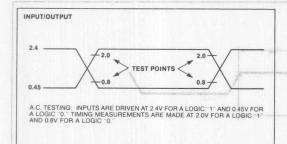
Digit-on Time ...... 480 μsec Blanking Time  $160~\mu sec$  Internal Clock Cycle<sup>[5]</sup>  $10~\mu sec$ 

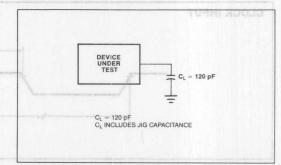
### NOTES:

- 1. 8279,  $I_{OL} = 1.6$ mA; 8279-5,  $I_{OL} = 2.2$ mA. 2. 8279,  $I_{OH} = -100\mu$ A; 8279-5,  $I_{OH} = -400\mu$ A. 3. 8279,  $V_{CC} = +5V \pm 5\%$ ; 8279-5,  $V_{CC} = +5V \pm 10\%$ .
- 4. 8279, C<sub>L</sub> = 100pF; 8279-5, C<sub>L</sub> = 150pF.
- 5. The Prescaler should be programmed to provide a 10 µs internal clock cycle.

### A.C. TESTING INPUT, OUTPUT WAVEFORM

### A.C. TESTING LOAD CIRCUIT





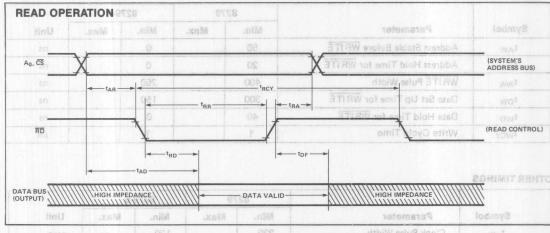


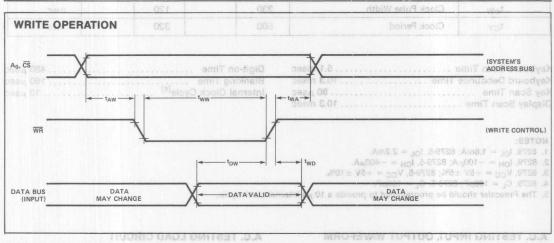


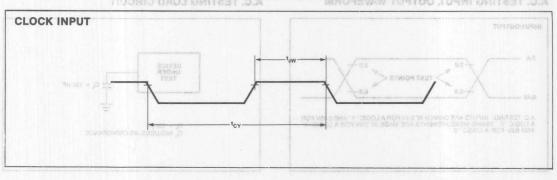
# A.C. CHARACTERISTICS (Continued)

### **WAVEFORMS**



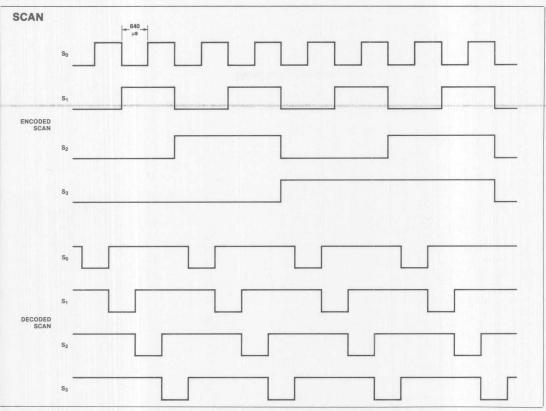


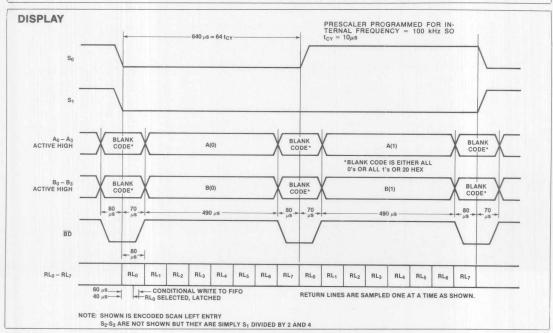




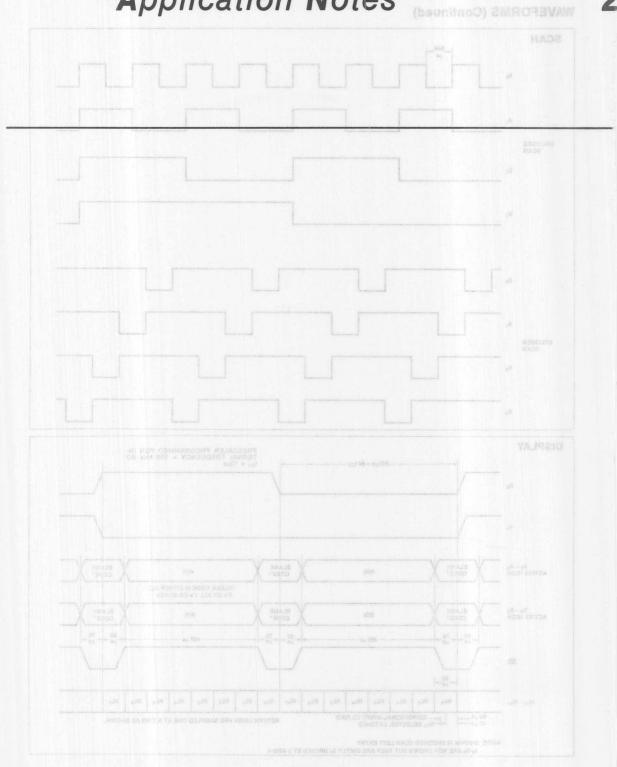


# **WAVEFORMS (Continued)**









# Introduction to suppose the UPLATATM INTRODUCTION 2-2 UPLAT VS. UPLATA 2-2 UPLAT VS. UPLATA 2-3 UPVIMASTER PROTOCOL 2-3 EXAMPLE APPLICATIONS 2-9 8-Digit Multiplexed LED Display 2-10 Combination I/O Device 2-19 DESUG TECHNIQUES 2-27 CONCLUSION 2-30 APPENDIX A 2-31

# Introduction to the UPI-41A™

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### INTRODUCTION TO THE UPI-41ATM

### Introduction

Since the introduction in 1974 of the second generation of microprocessors, such as the 8080, a wide range of peripheral interface devices have appeared. At first, these devices solved application problems of a general nature; i.e., parallel interface (8255), serial interface (8251), timing (8253), interrupt control (8259). However, as the speed and density of LSI technology increased, more and more intelligence was incorporated into the peripheral devices. This allowed more specific application problems to be solved, such as floppy disk control (8271), CRT control (8275), and data link control (8273). The advantage to the system designer of this increased peripheral device intelligence is that many of the peripheral control tasks are now handled externally to the main processor in the peripheral hardware rather than internally in the main processor software. This reduced main processor overhead results in increased system throughput and reduced software complexity.

In spite of the number of peripheral devices available, the pervasiveness of the microprocessor has been such that there is still a large number of peripheral control applications not yet satisfied by dedicated LSI. Complicating this problem is the fact that new applications are emerging faster than the manufacturers can react in developing new, dedicated peripheral controllers. To address this problem, a new microcomputer-based Universal Peripheral Interface (UPI-41A) device was developed.

In essence, the UPI-41A acts as a slave processor to the main system CPU. The UPI contains its own processor, memory, and I/O, and is completely user programmable; that is, the entire peripheral control algorithm can be programmed locally in the UPI, instead of taxing the master processor's main memory. This distributed processing concept allows the UPI to handle the real-time tasks such as encoding keyboards, controlling printers, or multiplexing displays, while the main processor is handling non-realtime dependent tasks such as buffer management or arithmetic. The UPI relies on the master only for initialization, elementary commands, and data transfers. This technique results in an overall increase in system efficiency since both processorsthe master CPU and the slave UPI-are working in parallel.

This application note presents three UPI-41A applications which are roughly divided into two groups: applications whose complexity and UPI code space

requirements allow them to either stand alone or be incorporated as just one task in a "multi-tasking" UPI, and applications which are complete UPI applications in themselves. Applications in the first group are a simple LED display and sensor matrix controllers. A combination serial/parallel/ I/O device is an application in the second group. Each application illustrates different UPI configurations and features. However, before the application details are presented, a section on the UPI/master protocol requirements is included. These protocol requirements are key to UPI software development. For convenience, the UPI block diagram is reproduced in Figure 1 and the instruction set summary in Table 1.

### UPI-41 vs. UPI-41A

The UPI-41A is an enhanced version of the UPI-41. It incorporates several architectural features not found on the "non-A" device:

- Separate Data In and Data Out data bus buffer registers
- User-definable STATUS register bits
- Programmable master interrupts for the OBF and IBF flags
- Programmable DMA interface to external DMA controller.

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The separate Data In (DBBIN) and Data Out (DBBOUT) registers greatly simplify the master/UPI protocol compated to the UPI-41. The master need only check IBF before writing to DBBIN and OBF before reading DBBOUT. No data bus buffer lock-out is required.

The most significant nibble of the STATUS register, undefined in the UPI-41, is user-definable in UPI-41A. It may be loaded directly from the most significant nibble of the Accumulator (MOV STS,A). These extra four STATUS bits are useful for transferring additional status information to the master. This application note uses this feature extensively.

A new instruction, EN FLAGS, allows OBF and  $\overline{\rm IBF}$  to be reflected on PORT 2 BIT 4 and PORT 2 BIT 5 respectively. This feature enables interrupt-driven data transfers when these pins are interrupt sources to the master.

By executing an EN DMA instruction PORT 2 BIT 6 becomes a DRQ (DMA Request) output and PORT 2 BIT 7 becomes DACK (DMA Acknowledge). Setting DRQ requests a DMA cycle to an external DMA controller. When the cycle is granted, the DMA controller returns DACK plus either RD (Read) or WR (Write). DACK automatically forces

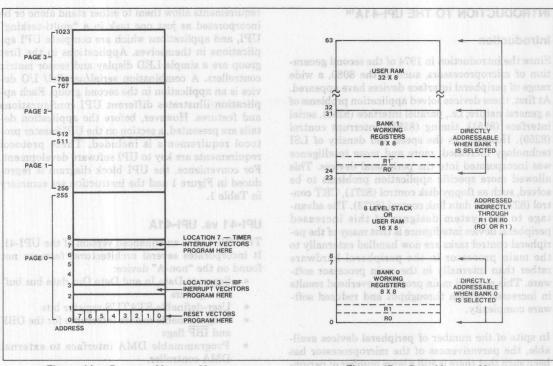


Figure 1A. Program Memory Map

Figure 1B. Data Memory Map

 $\overline{\text{CS}}$  and  $A_0$  low internally and clears DRQ. This selects the appropriate data buffer register (DBBOUT for DACK and  $\overline{\text{RD}}$ , DBBIN for DACK and  $\overline{\text{WR}}$ ) for the DMA transfer.

Like the "non-A", the UPI-41A is available in both ROM (8041A) and EPROM (8741A) Program Memory versions. This application note deals exclusively with the UPI-41A since the applications use the "A"s enhanced features.

### **UPI/MASTER PROTOCOL**

As in most closely coupled multiprocessor systems, the various processors communicate via a shared resource. This shared resource is typically specific locations in RAM or in registers through which status and data are passed. In the case of a master processor and a UPI-41A, the shared resource is 3 separate, master-addressable, registers internal to the UPI. These registers are the status register (STATUS), the Data Bus Buffer Input register (DBBIN), and the Data Bus Output register (DBBOUT). [Data Bus Buffer direction is relative to the UPI]. To illustrate this register interface, consider the 8085A/UPI system in Figure 2.

Looking into the UPI from the 8085A, the 8085A sees only the three registers mentioned above. If the 8085A wishes to issue a command to the UPI, it does so by writing the command to the DBBIN register according to the decoding of Table 2. Data for the UPI is also passed via the DBBIN register. (The UPI differentiates commands and data by examining the A<sub>0</sub> pin. Just how this is done is covered shortly.) Data from the UPI for the 8085A is passed in the DBBOUT register. The 8085A may interrogate the UPI's status by reading the UPI's STATUS register. Four bits of the STATUS register act as flags and are used to handshake data and commands into and out of the UPI. The STATUS register format is shown in Figure 3.

BIT 0 is OBF (Output Buffer Full). This flag indicates to the master when the UPI has placed data in the DBBOUT register. OBF is set when the UPI writes to DBBOUT and is reset when the master reads DBBOUT. The master finds meaningful data in the DBBOUT register only when OBF is set.

The Input Buffer Full (IBF) flag is BIT 1. The UPI uses this flag as an indicator that the master has written to the DBBIN register. The master uses IBF

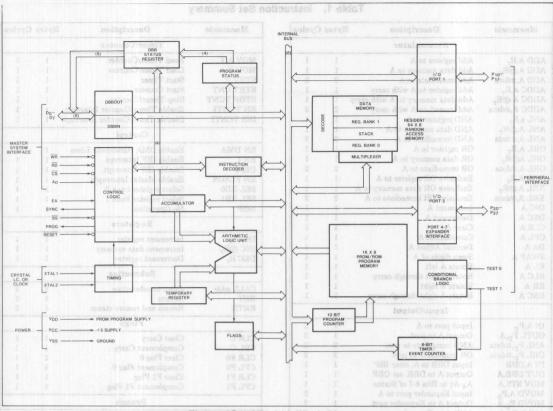


Figure 1C. UPI-41A Block Diagram

to indicate when the UPI has accepted a particular command or data byte. The master should examine IBF before outputting anything to the UPI. IBF is set when the master writes to DBBIN and is reset when the UPI reads DBBIN. The master must wait until IBF=0 before writing new data or commands to DBBIN. Conversely, the UPI must ensure IBF=1 before reading DBBIN.

The third STATUS register bit is  $F_0$  (FLAG 0). This is a general purpose flag that the UPI can set, reset, and test. It is typically used to indicate a UPI error or busy condition to the master.

FLAG 1  $(F_1)$  is the final dedicated STATUS bit. Like  $F_0$  the UPI can set, reset, and test this flag. However, in addition,  $F_1$  reflects the state of the  $A_0$  pin whenever the master writes to the DBBIN register. The UPI uses this flag to delineate between master command and data writes to DBBIN.

The remaining four STATUS register bits are user definable. Typical uses of these bits are as status in-

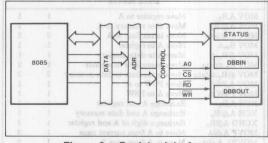


Figure 2. Register Interface

dicators for individual tasks in a multitasking UPI or as UPI generated interrupt status. These bits find a wide variety of uses in the upcoming applications.

Looking into the 8085A from the UPI, the UPI sees the two DBB registers plus the IBF, OBF, and F<sub>1</sub> flags. The UPI can write from its accumulator to DBBOUT or read DBBIN into the accumulator. The UPI cannot read OBF, IBF, or F<sub>1</sub> directly, but these flags may be tested using conditional jump

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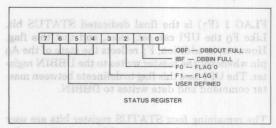
Table 1. Instruction Set Summary

Mnemonic	Description	Bytes C	ycles
	Accumulator		
ADD A,R <sub>r</sub>	Add register to A	1	1
ADD A,@Rr	Add data memory to A	1	1
ADD A,#data	Add immediate to A	2	2
ADDC A,R <sub>r</sub>	Add register to A with carry	1	1
ADDC A @Rr	Add data memory to A with carry		11
ADDC A,#data	Add immed. to A with carry	2	2
ANL a,R <sub>r</sub>	AND register to A	1	1
ANL A,@R <sub>r</sub>	AND data memory to A	1	1
ANL A,#data	AND immediate to A	2	2
ORL A,R <sub>r</sub>	OR register to A	1	1
ORL A@Rr	OR data memory to A	1	1
ORL A,#data	OR immediate to A	2	2
XRL A,Rr	Exclusive OR register to A	1	1
XRL A,@Rr	Exclusive OR data memory to A	1	1
XRL A,#data	Exclusive OR immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap digits of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
	Input/Output	Netro	
IN A P_	Input port to A	1	2
IN A,Pp OUTL Pp,A	Output A to port	1	2
ANI, P. #data	AND immediate to port	2	2
ANL P <sub>p</sub> ,#data ORL P <sub>p</sub> ,#data	OR immediate to port	2	2
IN A,DBB	Input DBB to A, clear IBF	1	1
OUT DBB,A	Output A to DBB, set OBF	1	1
MOV STS,A	A <sub>4</sub> -A <sub>7</sub> to Bits 4-7 of Status	1	1
MOVD A,Pp	Input Expander port to A	1	2
MOVD Pp,A	Output A to Expander port	1	2
ANLD P.A		palo k	2
ANLD P <sub>p</sub> ,A ORLD P <sub>p</sub> ,A	OR A to Expander port	1	2
	Data Moves		
MOV A,R <sub>r</sub>	Move register to A	1	1
MOV A,@R <sub>r</sub>	Move data memory to A	1	1 :
MOV A,#data	Move immediate to A	2	2
MOV R <sub>r</sub> ,A	Move A to register	1	1
MOV @R <sub>r</sub> ,A	Move A to data memory	1	1
MOV R <sub>r</sub> ,#data	Move immediate to register	2 800	2
MOV @R <sub>r</sub> ,#data	Move immediate to data memory	2	2
MOV A,PSW	Move PSW to A	1	1
MOV PSW,A	Move A to PSW	1	1
XCH A,Rr	Exchange A and register	1	1
XCH A,@R <sub>r</sub>	Exchange A and data memory	1	1
XCHD A@R <sub>r</sub>	Exchange digit of A and register	1	1
MOVP A,@A	Move to A from current page	1	2
	Move to A from page 3	1	2

Mnemonic	Description	Bytes	Cycles
	Timer/Counter		
MOV A,T	Read Timer/Counter	1	- 1
MOV T,A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/Counter Interrupt	1	1
DIS TCNTI		2 1	7.5
DIS TUNTI	Disable Timer/Counter Interrupt	1	1
	Control		
EN DMA	Enable DMA Handshake Lines	1	1
ENI	Enable IBF Interrupt	1	1
DIS I	Disable IBF Interrupt	1	1
EN FLAGS	Enable Master Interrupts	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
NOP	No Operation	1	1
	Registers	2000	
INCP		1	4
INC R <sub>r</sub>	Increment register		1
INC @R <sub>r</sub>	Increment data memory	1	1
DEC R <sub>r</sub>	Decrement register	1	1
	Subroutine	T.JATX	ALTERNO 200-203
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
	Flags	cinv	
CLRC	Clear Carry	. 1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear F1 Flag	1	1
CPL F1	Complement F1 Flag	1	1
	Branch		
JMP ADDR		2	2
JMPP @A	Jump indirect	1	2
DJNZ R,addr	Decrement register and skip	2 .	2
JC addr	Jump on Carry=1	201	200
JNC addr	Jump on Carry=0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on A not Zero Jump on T0=1	1 9191	W SOE
JNT0 addr	Jump on T0=0	10	0
JT1 addr	Jump on T1=1	2	0
	Jump on T1=1	2	2
JNT1 addr	Jump on T1=0 Jump on F0 Flag=1		
JF0 addr	Jump on F0 Flag=1	2	2
JF1 addr	Jump on F1 Flag=1 1880 gri		
JTF addr	Jump on Timer Flag=1,Clear Flag	2	2
JNIBF addr	Jump on IBF Flag=0	2	2
	A STATE OF THE STA	3 14 1 1	A ATT
JOBF addr	Jump on OBF Flag=1	2	0.52

Table 2. Register Decoding Authorition sol erotable

CS	AO	RD	WR	REGISTER
0	0	0	1	READ DBBOUT
0	9 1 P	0	110	READ STATUS and grandoo.
0	0	101	0	WRITE DBBIN (DATA)
0	umus umus	acres e acr	0	WRITE DBBIN (COM- MAND)
1	X	X	X	NO ACTION



and test. It is typically used to indicate a UPI error

Figure 3. Status Register Format daniels

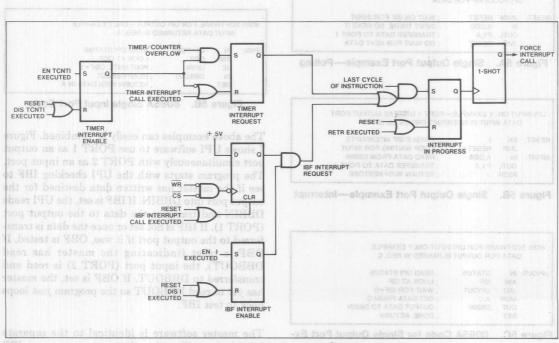
instructions. The UPI should make sure that OBF is reset before writing new data into DBBOUT to ensure that the master has read previous DBBOUT data. IBF should also be tested before reading DBBIN since DBBIN data is valid only when IBF is set. As was mentioned earlier, the UPI uses F1 to differentiate between command and data contents in DBBIN when IBF is set. The UPI may also write the upper 4-bits of its accumulator to the upper 4-bits of the STATUS register. These bits are thus user definable.

The UPI can test the flags at any time during its internal program execution. It essentially "polls" the STATUS register for changes. If faster response is needed to master commands and data, the UPI's internal interrupt structure can be used. If IBF interrupts are enabled, a master write to DBBIN (either command or data) sets IBF which generates an internal CALL to location 03H in program memory. At this point, working register contents can be saved using bank switching, the accumulator saved in a spare working register, and the DBBIN register read and serviced. The interrupt logic for the IBF interrupt is shown in Figure 4. A few observations concerning this logic are appropriate. Note that if the master writes to DBBIN while the UPI is still servicing the last IBF interrupt (a RETR instruction has not been executed), the IBF Interrupt Pending line

is made high which causes a new CALL to 03H as soon as the first RETR is executed. No ENI (Enable Interrupt) instruction is needed to rearm the interrupt logic as is needed in an 8080 or 8085A system; the RETR performs this function. Also note that executing a DIS I to disable further IBF interrupts does not clear a pending interrupt. Only a CALL to location 03H or RESET clears a pending IBF interrupt.

Keeping in mind that the actual master/UPI protocol is dependent on the application, probably the best way to illustrate correct protocol is by example. Let's consider using the UPI as a simple parallel I/O device. (This is a trivial application but it embodies all of the important protocol considerations.) Since the UPI may be either interrupt or non-interrupt driven internally, both cases are considered.

Let's take the easiest configuration first; using the UPI PORT 1 as an 8-bit output port. From the UPI's point-of-view, this is an input-only application since all that is required is that the UPI input data from the master. Once the master writes data to the UPI, the UPI reads the DBBIN register and transfers the data to PORT 1. No testing for commands versus data is needed since the UPI "knows" it only performs one task—no commands are needed.



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Non-interrupt driven UPI software is shown in Figure 5A while Figure 5B shows interrupt based software. For Figure 5A, the UPI simply waits until it sees IBF go high indicating the master has written a data byte to DBBIN. The UPI then reads DBBIN, transfers it to PORT 1, and returns to waiting for the next data. For the interrupt-driven UPI, Figure 5B, once the EN I instruction is executed, the UPI simply waits for the IBF interrupt before handling the data. The UPI could handle other tasks during this waiting time. When the master writes the data to DBBIN, an IBF interrupt is generated which performs a CALL to location 03H. At this point the UPI reads DBBIN (no testing of IBF is needed since an IBF interrupt implies that IBF is set), transfers the data to PORT 1, and executes an RETR which returns program flow to the main program.

Software for the master 8085A is included in Figure 5C. The only requirement for the master to output data to the UPI is that it check the UPI to be sure the previous data had been taken before writing new data. To accomplish this the master simply reads the STATUS register looking for IBF=0 before writing the next data.

```
: UPI INPUT ONLY EXAMPLE—PORT 1 USED AS OUTPUT PORT
: UPI POLLS IBF FOR DATA
: RESET: JNIBF RESET ; WAIT ON IBF FOR INPUT
IN A_DBB ; INPUT THERE, SO READ IT
OUTL P1,A ; TRANSFER DATA TO PORT 1

JMP—RESET ; GO WAIT FOR NEXT DATA
```

Figure 5A. Single Output Port Example—Polling

```
: UPI INPUT ONLY EXAMPLE—PORT 1 USED AS OUTPUT PORT
DATA INPUT IS INTERRUPT-DRIVEN ON IBF
: RESET: EN I ENABLE IBF INTERRUPTS
JMP RESET+1 LOOP WAITING FOR INPUT
IBFINT: IN A,DBB READ DATA FROM DBBIN
OUTL P1,A : TRANSFER DATA TO PORT 1
RETR : RETURN WITH RESTORE
```

Figure 5B. Single Output Port Example—Interrupt

```
8085 SOFTWARE FOR UPLINPUT-ONLY EXAMPLE
      DATA FOR OUTPUT IS PASSED IN REG. C
UPIOUT: IN
             STATUS
                           READ UPI STATUS
       ANI
             IBF
                           LOOK AT IRE
                           WAIT FOR IBF=0
             UPIOUT
       JNZ
       MOV
                           GET DATA FROM C
             DBBIN
                           OUTPUT DATA TO DBBIN
       RET
                          DONE, RETURN
```

Figure 5C. 8085A Code for Single Output Port Example

Figure 6A illustrates the case where UPI PORT 2 is used as an 8-bit input port. This configuration is termed UPI output-only as the master does not write (input) to the UPI but simply reads either the STATUS or the DBBOUT registers. In this example only the OBF flag is used. OBF signals the master that the UPI has placed new port data in DBBOUT. The UPI loops testing OBF. When OBF is clear, the master has read the previous data and UPI then reads its input port (PORT 2) and places this data in DBBOUT. It then waits on OBF until the master reads DBBOUT before reading the input port again. When the master wishes to read the input port data. Figure 6B, it simply checks for OBF being set in the STATUS register before reading DBBOUT. While this technique illustrates proper protocol, it should be noted that it is not meant to be a good method of using the UPI as an input port since the master would never get the newest status of the port.

```
: UPI OUTPUT ONLY EXAMPLE—PORT 2 USED AS INPUT PORT
: PORT DATA IS AVAILABLE IN DBBOUT

RESET: JOBF RESET : LOOP IF OBF=1 (DATA NOT READ)
IN A,P2 : DBBOUT CLEAR, READ PORT
OUT DBB,A : TRANSFER PORT DATA TO DBBOUT

JMP RESET : WAIT FOR MASTER TO READ DATA
```

Figure 6A. Single Input Port Example

```
: 8085 SOFTWARE FOR UPI OUTPUT—ONLY EXAMPLE
: INPUT DATA RETURNED IN REG. A

UPIIN: IN STATUS READ UPI STATUS
ANI OBF LOOK AT OBF
JZ UPIIN WAIT UNTIL OBF= 1
IN DBBOUT READ DBBOUT
RET RETURN WITH DATA IN A
```

Figure 6B. 8085A Single Input Port Code

The above examples can easily be combined. Figure 7 shows UPI software to use PORT 1 as an output port simultaneously with PORT 2 as an input port. The program starts with the UPI checking IBF to see if the master has written data destined for the output port into DBBIN. If IBF is set, the UPI reads DBBIN and transfers the data to the output port (PORT 1). If IBF is not set or once the data is transferred to the output port if it was, OBF is tested. If OBF is reset (indicating the master has read DBBOUT), the input port (PORT 2) is read and transferred to DBBOUT. If OBF is set, the master has yet to read DBBOUT so the program just loops back to test IBF.

The master software is identical to the separate input/output examples; the master must test IBF

```
UPI INPUT/OUTPUT EXAMPLE—PORT 10UTPUT, PORT 2 INPUT
RESET:
      JNIBF OUT1
                          IF IBF=0, DO OUTPUT
             A, DBB
                          IF IBF=1. READ DBBIN
       OUTL P1 A
                          TRANSFER DATA TO PORT 1
OUT 1:
       JOBE
            RESET
                          IF OBF=1, GO TEST IBF
                          IF OBF=0, READ PORT 2
             A P2
       IN
       OUT
                          TRANSFER PORT DATA TO DBBOUT
             DBB. A
                          GO CHECK FOR INPUT
             RESET
```

Figure 7. Combination Output/Input Port Example

and OBF before writing output port data into DBBIN or before reading input port from DBBOUT respectively.

In all of the three examples above, the UPI treats information from the master solely as data. There has been no need to check if DBBIN information is a command rather than data since the applications do not require commands. But what if both PORTs 1 and 2 were used as output ports? The UPI needs to know into which port to put the data. Let's use a command to select which port.

Recall that both commands and data pass through DBBIN. The state of the  $A_0$  pin at the time of the write to DBBIN is used to distinguish commands from data. By convention, DBBIN writes with  $A_0$ =0 are for data, and those with  $A_0$ =1 are commands. When DBBIN is written into,  $F_1$  (FLAG 1) is set to the state of  $A_0$ . The UPI tests  $F_1$  to determine if the information in the DBBIN register is data or command.

For the case of two output ports, let's assume that the master selects the desired port with a command prior to writing the data. (We could just use  $F_1$  as a port select but that would not illustrate the subtle differences between commands and data). Let's define the port select commands such that BIT 1=1 if the next data is for PORT 1 (Write PORT 1=0000 0010) and BIT 2=1 if the next data is for PORT 2 (Write PORT 2=0000 0100). (The number of the set bit selects the port.) Any other bits are ignored. This assignment is completely arbitrary; we could use any command structure, but this one has the advantage of being simple.

Note that the UPI must "remember" from DBBIN write to write which port has been selected. Let's use  $F_0$  (FLAG 0) for this purpose. If a Write PORT 1 command is received,  $F_0$  is reset. If the command is Write PORT 2,  $F_0$  is set. When the UPI finds data in DBBIN,  $F_0$  is interrogated and the data is loaded into the previously selected port. The UPI software is shown in Figure 8A.

```
UPI DUAL OUTPUT PORT EXAMPLE—BOTH PORT 1 AND 2 OUTPUTS
     COMMAND SELECTS DESIRED PORT
     WRITE PORT 1-0000 0010 (02H)
     WRITE PORT 2-0000 0100 (04H)
     FLAG O USED TO REMEMBER WHICH PORT WAS SELECTED
     BY LAST COMMAND. of them 1008 HU beet bed
RESET: JNIBF RESET : WAIT FOR MASTER INPUT
 TO IN ON A, DBB SE A READ INPUT
                       IF F1=1, COMMAND INPUT
      JF1
           CMD
      JF0
           PORT2
                       INPUT IS DATA, TEST FO
                       F0=0, SO OUTPUT TO PORT 1
      OUTL
           P1.A
           RESET
                       WAIT FOR NEXT INPUT
                       F0=1, SO OUTPUT TO PORT 2
PORT2
      OUTL
           P2,A
      JMP
           RESET
                 ; WAIT FOR NEXT INPUT
CMD
      JB1
                       TEST COMMAND BITS (BIT 1)
      JR2
                       TEST BIT 2
           RESET . NEITHER BIT SET, WAIT FOR INPUT
      JMP.
PT1:
                       PORT 1 SELECTED, CLEAR FO
      CLR
                       WAIT FOR INPUT
      JMF
PT2:
      CLR
           FO PORT 2 SELECTED, SET FO
      CPL
                      ; WAIT FOR INPUT
      JMP
           RESET
```

Figure 8A. Dual Output Port Example

Initially, the UPI simply waits until IBF is set indicating the master has written into DBBIN. Once IBF is set, DBBIN is read and  $F_1$  is tested for a command. If  $F_1$ =1, the DBBIN byte is a command. Assuming a command, BIT 1 is tested to see if the command selected PORT 1. If so,  $F_0$  is cleared and the program returns to wait for the data. If BIT 1=0, BIT 2 is tested. If BIT 2 is set, PORT 2 is selected so  $F_0$  is set. The program then loops back waiting for the next master input. This input is the desired port data. If BIT 2 was not set,  $F_0$  is not changed and no action is taken.

When IBF=1 is again detected, the input is again tested for command or data. Since it is necessarily data, DBBIN is read and F<sub>0</sub> is tested to determine which port was previously selected. The data is then output to that port, following which the program waits for the next input. Note that since F<sub>0</sub> still selects the previous port, the next input could be more data for that port. The port selection command could be thought of as a port select flip-flop control; once a selection is made, data may be repeatedly written to that port until the other port is selected. Master software, Figure 8B, simply must check IBF before writing either a command or data to DBBIN. Otherwise, the master software is straightforward.

For the sake of completeness, UPI software for implementing two input ports is given in Figure 9. This case is simpler than the dual output case since the UPI can assume that all writes to DBBIN are port selection commands so no command/data testing is required. Once the Port Read command is input, the selected port is read and the port data is placed in DBBOUT. Note that in this case F<sub>0</sub> is used as a UPI

error indicator. If the master happened to issue an invalid command (a command without either BIT 1 or 2 set), F<sub>0</sub> is set to notify the master that the UPI did not know how to interpret the command. F<sub>0</sub> is also set if the master commanded a port read before it had read DBBOUT from the previous command. The UPI simply tests OBF just prior to loading DBBOUT and if OBF=1, F<sub>0</sub> is set to indicate the error.

All of the above examples are, in themselves, rather trivial applications of the UPI although they could easily be incorporated as one of several tasks in a UPI handling multiple small tasks. We have covered them primarily to introduce the UPI concept and to illustrate some master/UPI protocol. Before moving on to more realistic UPI applications, let's discuss two UPI features that do not directly relate to the master/UPI protocol but greatly enhance the UPI's transfer capability.

In addition to the OBF and IBF bits in the STATUS register, these flags can also be made available directly on two port pins. These port pins can then be used as interrupt sources to the master. By executing an EN FLAGS instruction, PORT 2 pin 4 reflects the condition of OBF and PORT 2 pin 5 reflects the inverted condition of IBF (IBF). These dedicated outputs can then be enabled or disabled via their respective port bit values; i.e., P24 reflects OBF as long as an instruction is executed which sets P24 (i.e. ORL P2,#10H). The same action applies to the IBF output except P25 is used. Thus P24 may serve as a DATA AVAILABLE interrupt output. Likewise for P25 as a READY-TO-ACCEPT-DATA interrupt. This greatly simplifies interrupt-driven master-slave data transfers.

```
8085 SOFTWARE FOR DUAL OUTPUT PORT EXAMPLE
     THIS ROUTINE WRITES DATA IN REG. C TO PORT 1
     (SAME ROUTINE FOR PORT 2-JUST CHANGE COMMAND)
                       READ UPI STATUS
PORT1: IN
           STATUS
      ANI
The SEUNZ
           PORT1
                       WAIT UNTIL IBF=0 100 98 8 90
            A, 00000010B
                       LOAD WRITE PORT 1 CMD
                       OUTPUT TO UPI COMMAND PORT
           UPICMD
      OUT
P11 IN D
                       READ UPI STATUS AGAIN
           STATUS
MISS ANI
                       WAIT UNTIL COMMAND ACCEPTED
      JNZ
           A C GET DATA FROM C
      MOV
      OUT
           DBBIN
                       OUTPUT TO DBBIN
                       DONE, RETURN
```

Figure 8B. 8085A Dual Output Port Example Code

The UPI also supports a DMA transfer interface. If an EN DMA instruction is executed, PORT 2 pin 6 becomes a DMA Request (DRQ) output and P27 becomes a high impedance DMA Acknowledge

```
UPI DUAL INPUT PORT EXAMPLE—BOTH PORT 1 AND 2 INPUTS
      COMMAND SELECTS WHICH PORT IS TO BE READ
      FLAG 0 USED AS ERROR FLAG
RESET: JNIBE RESET
                          WAIT FOR INPUT
                          CLEAR ERROR FLAG
       CLR
             FO
                          READ INPUT (COMMAND)
       IN
             A. DBB
             PT1
                          TEST BIT 1 (PORT 1)
       JB1
       JB<sub>2</sub>
                          TEST BIT 2 (PORT 2)
ERROR: CPL
                          ERROR-COMPLEMENT FO
             FO
                          WAIT FOR INPUT
       JMP
             RESET
PT1:
                          READ PORT 1
                          TEST OBF BEFORE LOADING DBBOUT
       JOBF
             ERROR
       OUT
             DBB. A
                          LOAD PORT 1 DATA INTO DBBOUT
       .IMP
             RESET
                          WAIT FOR INPUT
                          READ PORT 2
PT2
       IN
             A. P2
                          TEST OBF BEFORE LOADING DBBOUT
       JOBE
             ERROR
                          LOAD PORT 2 DATA INTO DBBOUT
       OUT
             DBB, A
             RESET
                          WAIT FOR INPUT
```

Figure 9. Dual Input Port Example

 $(\overline{DACK})$  input. Any instruction which would normally set P26 now sets DRQ. DRQ is cleared when  $\overline{DACK}$  is low and either  $\overline{RD}$  or  $\overline{WR}$  is low. When  $\overline{DACK}$  is low,  $\overline{CS}$  and A0 are forced low internally which allows data bus transfers between DBBOUT or DBBIN to occur, depending upon whether  $\overline{WR}$  or  $\overline{RD}$  is true. Of course, the function requires the use of an external DMA controller.

Now that we have discussed the aspects of the UPI protocol and data transfer interfaces, let's move on to the actual applications.

# EXAMPLE APPLICATIONS AND ALLER OF THE PROPERTY 
Each of the following three sections presents the hardware and software details of a UPI application. Each application utilizes one of the protocols mentioned in the last section. The first example is a simple 8-digit LED display controller. This application requires only that the UPI perform input operations from the DBBIN; DBBOUT is not used. The reverse is true for the second application: a sensor matrix controller. The final application involves both DBBOUT and DBBIN operations: a combination serial/parallel I/O device.

The core master processor system with which these applications were developed is the iSBC 80/30 single board computer. This board provides an especially convenient UPI environment since it contains a dedicated socket specifically interfaced for the UPI-41A. The 80/30 uses the 8085A as the master processor. The I/O and peripheral complement on the 80/30 include 12 vectored priority interrupts (8 on an 8259 Programmable Interrupt Controller and 4 on the 8085A itself), an 8253 Programmable Interval Timer supplying three 16-bit programmable timers (one is dedicated as a programmable baud rate generator), a high speed serial channel provided by a 8251 Programmable USART, and 24 parallel I/O

lines implemented with an 8255A Programmable Parallel Interface. The memory complement contains 16K bytes of RAM using 2117 16K bit Dynamic RAMs and the 8202 Dynamic RAM Controller, and up to 8K bytes of ROM/EPROM with sockets compatible with 2716, 2758, or 2332 devices. The 80/30's RAM uses a dual port architecture. That is, the memory can be considered a global system resource, accessible from the on-board 8085A as well as from remote CPUs and other devices via the MULTIBUS. The 80/30 contains MULTIBUS control logic which allows up to 16 80/30s or other bus masters to share the same system bus. (More detailed information on the iSBC 80/30 and other iSBC products may be found in the latest Intel Systems Data Catalog.)

A block diagram of the iSBC 80/30 is shown in Figure 10. Details of the UPI interface are shown in Figure 11. This interface decodes the UPI registers in the following format:

Register
Read STATUS
Write DBBIN (command)
Pood DPPOUT (data)

Write DBBIN (data)

### **Operations**

IN E5H OUT E5H IN E4H OUT E4H

### 8-Digit Multiplexed LED Display

The traditional method of interfacing an LED display with a microprocessor is to use a data latch along with a BDC-to-7-segment decoder for each digit of the display. Thus two ICs, seven current limiting resistors, and about 45 connections are required for each digit. These requirements are, of course, multiplied by the total number of digits desired. The obvious disadvantages of this method are high parts count and high power dissipation since each digit is "ON" continuously. Instead, a scheme of time multiplexing the display can be used to decrease both parts count and power dissipation.

Display multiplexing basically involves connecting the same segment (a, b, c, d, e, f, or g) of each digit in parallel and driving the common digit element (anode or cathode) of each digit separately. This is shown schematically in Figure 12. The various digits of the display are not all on at once; rather, only one digit at a time is energized. As each digit is energized, the appropriate segments for that digit are turned on. Each digit is enabled in this way, in sequence, at a rate fast enough to ensure that each digit appears to be "ON" continuously. This implies that the display must be "refreshed" at periodic intervals to keep the digits flicker-free. If the CPU had to handle this task, it would have to suspend normal

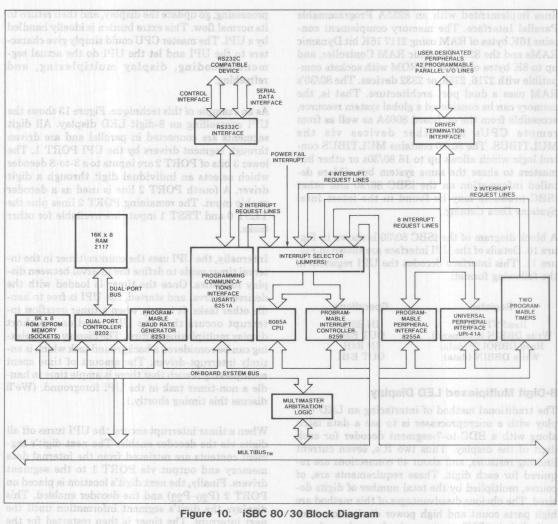
processing, go update the display, and then return to its normal flow. This extra burden is ideally handled by a UPI. The master CPU could simply give characters to the UPI and let the UPI do the actual segment decoding, display multiplexing, and refreshing.

As an example of this technique, Figure 13 shows the UPI controlling an 8-digit LED display. All digit segments are connected in parallel and are driven through segment drivers by the UPI PORT 1. The lower 3 bits of PORT 2 are inputs to a 3-to-8 decoder which selects an individual digit through a digit driver. A fourth PORT 2 line is used as a decoder enable input. The remaining PORT 2 lines plus the TEST 0 and TEST 1 inputs are available for other tasks.

Internally, the UPI uses the counter/timer in the interval timer mode to define the interval between display refreshes. Once the timer is loaded with the desired interval and started, the UPI is free to handle other tasks. It is only when a timer overflow interrupt occurs that the UPI handles the short display multiplexing routine. The display multiplexing can be considered a background task which is entirely interrupt-driven. The amount of time spent multiplexing is such that there is ample time to handle a non-timer task in the UPI foreground. (We'll discuss this timing shortly.)

When a timer interrupt occurs, the UPI turns off all digits via the decoder enable. The next digit's segment contents are retrieved from the internal data memory and output via PORT 1 to the segment drivers. Finally, the next digit's location is placed on PORT 2 (P20-P22) and the decoder enabled. This displays the digit's segment information until the next interrupt. The timer is then restarted for the next interval. This process continues repeatedly for each digit in sequence.

As a prelude to discussing the UPI software, let's examine the internal data memory structure used in this application, Figure 14. This application requires only 14 of the 64 total data memory locations. The top eight locations are dedicated to the Display Map; one location for each digit. These locations contain the segment and decimal point information for each character. Just how characters are loaded into this section of memory is covered shortly. Register R7 of Register Bank 1 is used as the temporary Accumulator store during the interrupt service routines. Register R3 stores the digit number of the next digit to be displayed. R2 is a temporary storage register for characters during input routine. R0 is



the offset pointer pointing to the Display Map location of the next digit. That makes 12 locations so far. The remaining two locations are the two stack locations required to store the return address plus status during the timer and input interrupt service routines. The remaining unused locations, all of Register Bank 0, 14 bytes of stack, 4 in Register Bank 1, and 24 general purpose RAM locations, are all available for use by any foreground task.

The UPI software consists of only three short routines. One, INIT, is used strictly during initialization. DISPLA is the multiplexing routine called at a timer interrupt. INPUT is the character input handler called at an IBF interrupt. The flow charts for these routines are shown in Figures 14A through 14C.

INIT initializes the UPI by simply turning off all segment and digit drivers, filling the Display Map with blank characters, loading and starting the timer, and enabling both timer and IBF interrupts. Although the flow chart shows the program looping at this point, it is here that the code for any foreground task is inserted. The only restrictions on this foreground task are that it not use I/O lines dedicated to the display and that it not require dedicated use of the timer. It could share the timer if precautions are taken to ensure that the display will still be refreshed at the required interval.

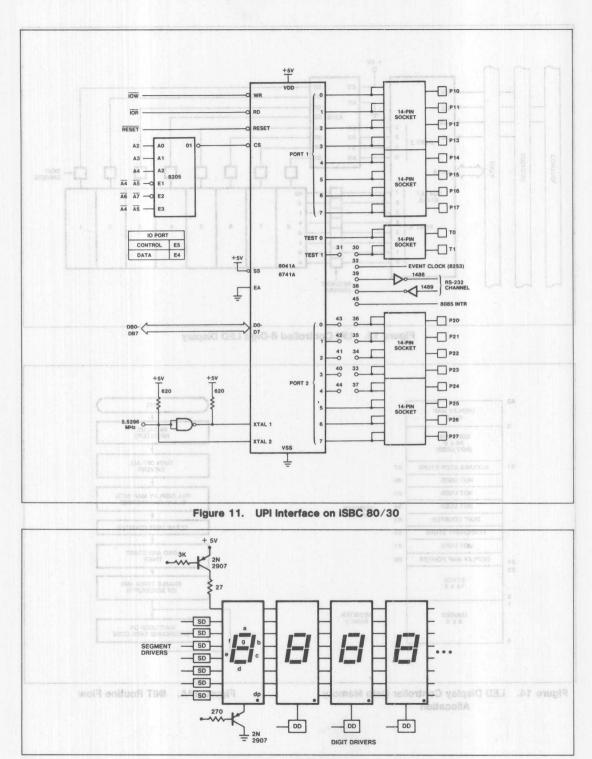


Figure 12. LED Multiplexing

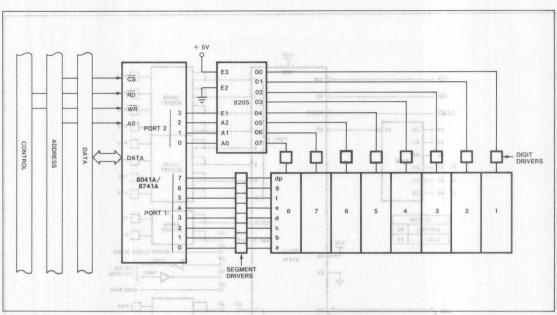
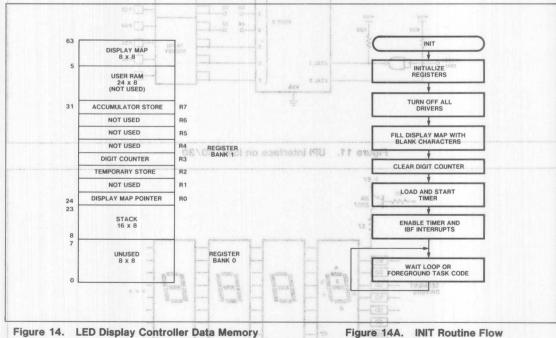


Figure 13. UPI Controlled 8-Digit LED Display



Allocation

Figure 14A. INIT Routine Flow

Figure 12. LED Multiplaxing

gg .....

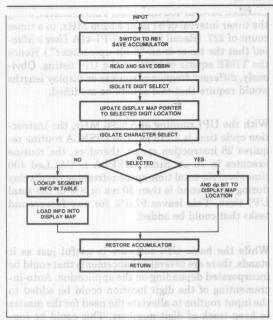


Figure 14B. INPUT Routine Flow

The INPUT routine handles the character input. It is called when an IBF interrupt occurs. After the usual swapping of register banks and saving of the accumulator, DBBIN is read and stored in register Ro. DBBIN contains the Display Data Word. The format for this word. Figure 15, has two fields: Digit Select and Character Select. The Digit Select field selects the digit number into which the character from the Character Select field is placed. Notice that the character set is not limited strictly to numerics. some alphanumeric capability is provided. Once DBBIN is read, the offset for the selected digit is computed and placed in the Display Map Pointer Ro. Next the segment information for the selected character is found through a look-up table starting in page 3 of the program memory. This segment information is then stored at the location pointed at by the Display Map Pointer. If the Character Select field specified a decimal point, the segment corresponding to the decimal point is ANDed into the present segment information for that digit. After the accumulator is restored, execution is returned to the main program, woods tada odd goddaglasgio xittem

The DISPLA routine simply implements the multiplexing actions described earlier. It is called whenever a timer interrupt occurs. After saving pre-

This arrangement of 16 sensors requires only 4 input

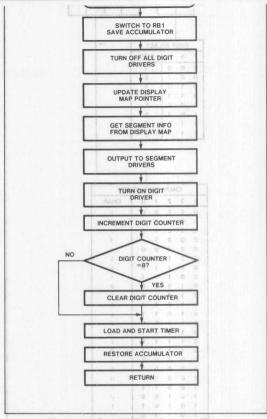


Figure 14C. DISPLA Routine Flow

interrupt status by switching register banks and storing the Accumulator, all digit drivers are turned off. The Display Map Pointer is then updated using the Current Digit Register to point at that digit's segment information in the Display Map. This information is output to PORT 1; the segment drivers. The number of the current digit, R3, is then sent to the digit select decoder and the decoder is enabled. This turns on the current digit. The digit counter is incremented and tested to see if all eight digits have been refreshed. If so, the digit counter is reset to zero. If not, nothing is done, Finally, the timer is loaded and restarted, the Accumulator is restored, and the routine returns execution to the main program. Thus DISPLA refreshes one digit each time it is CALLed by the timer interrupt. The digit remains on until the next time DISPLA is executed.

The UPI software listing is included as Appendix A1. Appendix A2 shows the 8085A test routine used

AFN-01536A

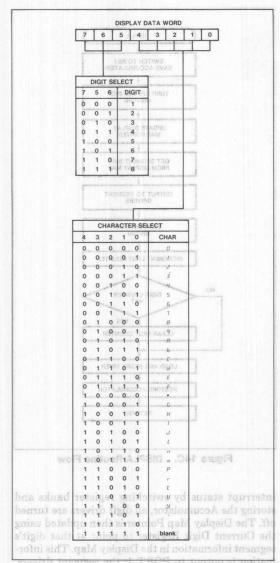


Figure 15. LED Display Controller Display Data Word Format

to display the contents of a display buffer on the display. The 8085A software takes care of the display digit numbering. Since the application is input-only for the UPI, the only protocol required is that the master must test IBF before writing a Display Data Word into DBBIN.

On the iSBC 80/30, the UPI frequency is at 5.5296 MHz. To obtain a flicker-free display, the whole display must be refreshed at a rate of 50 Hz or greater.

If we assume a 50 Hz refresh rate and an 8-digit display, this means the DISPLA routine must be CALLed  $50\times8$  or 400 times/sec. This transfers, using the timer interval of  $87~\mu s$  at 5.5296 MHz, to a timer count of 227. (Recall from the UPI-41A User's Manual that the timer is an "8-bit up-counter".) Hence the TIME equate of 227D in the UPI listing. Obviously, different frequency sources or display lengths would require that this equate be modified.

With the UPI running at 5.5296 MHz, the instruction cycle time is 2.713  $\mu$ s. The DISPLA routine requires 28 instruction cycles, therefore, the routine executes in 76  $\mu$ s. Since DISPLA is CALLed 400 times/sec, the total time spent refreshing the display during one second is then 30 ms or 3% of the total UPI time. This leaves 97.0% for any foreground tasks that could be added.

While the basic UPI software is useful just as it stands, there are several enhancements that could be incorporated depending on the application. Auto-incrementing of the digit location could be added to the input routine to alleviate the need for the master to keep track of digit numbers. This could be (optionally) either right-handed or left-handed entry a la TI or HP calculators. The character set could be easily modified by simply changing the lookup table. The display could be expanded to 16 digits at the expense of one additional PORT 2 digit select line, the replacement of the 3-to-8 decoder with a 4-to-16 decoder, and 8 more Display Map locations.

Now let's move on to a slightly more complex application that is UPI output-only—a sensor matrix controller.

# Sensor Matrix Controller

Quite often a microprocessor system is called upon to read the status of a large number of simple SPST switches or sensors. This is especially true in a process or industrial control environment. Alarm systems are also good examples of systems with a large sensor population. If the number of sensors is small, it might be reasonable to dedicate a single input port pin for each sensor. However, as the number of sensors increase, this technique becomes very wasteful. A better arrangement is to configure the sensors in a matrix organization like that shown in Figure 16. This arrangement of 16 sensors requires only 4 input and 4 output lines; half the number needed if dedicated inputs were used. The line saving becomes even more substantial as the number of sensors increases. sa 19ffA. atuooo tquatatai remit a tavenedw

In Figure 16, the basic operation of the matrix involves scanning individual row select lines in sequence while reading the column return lines. The state of any particular sensor can then be determined by decoding the row and column information. The typical configuration pulls up the column return lines and the selected row is held low. Deselected rows are held high. Thus a return line remains high for an open sensor on the selected row and is pulled low for a closed sensor. Diode isolation is used to prevent a phantom closure which would occur when a sensor is closed on a selected row and there are two or more closures on a deselected row. Germanium diodes are used to provide greater noise margin at the return line input.

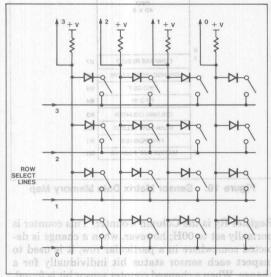
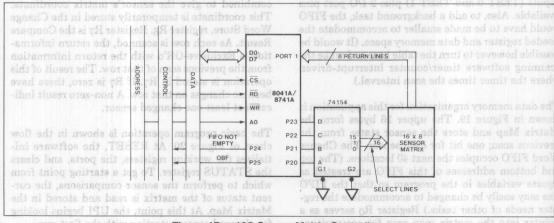


Figure 16. 4×4 Sensor Matrix

If the main processor was required to control such a matrix it would periodically have to output at the row port and then read the column return port. The processor would need to maintain in memory a map of the previous state of the matrix. A comparison of the new return information to the old information would then be made to determine whether a sensor change had occurred. Any changes would be processed as needed. A row counter and matrix map pointer also require maintenance each scan. Since in most applications sensors change very slowly compared to most processing actions, the processor probably would scan the rows only periodically with other tasks being processed between scans.

Rather than require the processor to handle the rather mundane tasks of scanning, comparing, and decoding the matrix, why not use a dedicated processor? The UPI is perfect.

Figure 17 shows a UPI configuration for controlling up to 128 sensors arranged in a 16×8 matrix. The 4to-16 line decoder is used as the row selector to save port pins and provides the expansion to 128 sensors over the maximum of 64 sensors if the port had been used directly. It also helps increase the port drive capability. The column return lines go directly into PORT 1. Features of this design include complete matrix management. As the UPI scans the matrix it compares its present status to the previous scan. If any change is detected, the location of the change is decoded and loaded, along with the sensor's present state, into DBBOUT. This byte is called a Change Word. The Master processor has only to read one byte to determine the status and coordinate of a changed sensor. If the master had not read a previous Change Word in DBBOUT (OBF=1) before a new sensor change is detected, the new Change



worden and this guide Figure 17. 128 Sensor Matrix Controller

Word is loaded into an internal FIFO. This FIFO buffers up to 40 changes before it fills. The status of the FIFO and OBF is made available to the master either by polling the UPI STATUS register, Figure 18A, or as interrupt sources on port pins P24 and P25 respectively, Figure 17. The FIFO NOT EMP-TY pin and bit are true as long as there are changes not yet read in the FIFO. As long as the FIFO is not empty, the UPI monitors OBF and loads new Change Words from the FIFO into DBBOUT. Thus, the UPI provides complete FIFO management.

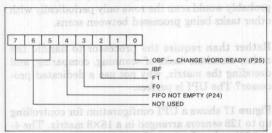


Figure 18A. Sensor Matrix Status Register Format

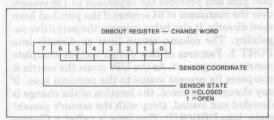


Figure 18B. Sensor Matrix Change Word Format

Internally, the matrix scanning software is programmed to run as a foreground task. This allows the timer/counter to be used by any background task although the hardware configuration leaves only 2 inputs (TEST 0 and TEST 1) plus 2 I/O port pins available. Also, to add a background task, the FIFO would have to be made smaller to accommodate the needed register and data memory space. (It would be possible however to turn the table here and make the scanning software timer/counter interrupt-driven where the timer times the scan interval.)

The data memory organization for this application is shown in Figure 19. The upper 16 bytes form the Matrix Map and store the sensor states from the previous scan; one bit for each sensor. The Change Word FIFO occupies the next 40 locations. (The top and bottom addresses of this FIFO are treated as equate variables in the program so that the FIFO size may easily be changed to accommodate the register needs of other tasks.) Register R0 serves as a pointer into the matrix map area for comparisons

and updates of the sensor status. R<sub>1</sub> is a general FIFO pointer. The FIFO is implemented as a circular buffer with In and Out pointer registers which are stored in R<sub>4</sub> and R<sub>5</sub> respectively. These registers are moved into FIFO pointer R<sub>1</sub> for actual transfers into or out of the FIFO. R<sub>2</sub> is the Row Select Counter. It stores the number of the row being scanned.

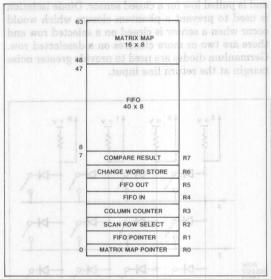


Figure 19. Sensor Matrix Data Memory Map

Register R3 is the Column Counter. This counter is normally set to 00H; however, when a change is detected somewhere in a particular row, it is used to inspect each sensor status bit individually for a change. When a changed counter sensor bit is found, the Row Select Counter and Column Counter are combined to give the sensor's matrix coordinate. This coordinate is temporarily stored in the Change Word Store, register R6. Register R7 is the Compare Result. As each row is scanned, the return information is Exclusive-OR'd with the return information from the previous scan of that row. The result of this operation is stored in R7. If R7 is zero, there have been no changes on that row. A non-zero result indicates at least one changed sensor.

The basic program operation is shown in the flow chart of Figure 20. At RESET, the software initializes the working registers, the ports, and clears the STATUS register. To get a starting point from which to perform the sensor comparisons, the current status of the matrix is read and stored in the Matrix Map. At this point, the UPI begins looking for changed sensors starting with the first row.

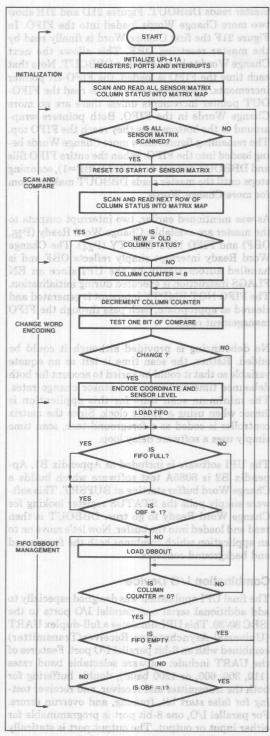


Figure 20. Sensor Matrix Controller Flow Chart

Before delving further into the flow, let's pause to describe the general format of the operation. The UPI scans the matrix one row at a time. If no changes are detected on a particular row, the UPI simply moves to the next row after checking the status of DBBOUT and the FIFO. If a change is detected, the UPI must check each bit (sensor) within the row to determine the actual sensor location. (More than one sensor on the scanned row could have changed.) Rather than test all 8 bits of the row before checking the DBBOUT and FIFO status again, the UPI performs the status check in between each of the bit tests. This ensures the fastest response to the master reading previous Change Words from DBBOUT and the FIFO.

With this general overview in mind, let's go first thru the flow chart assuming we are scanning a row where no changes have occurred. Starting at the Scan-and-Compare section, the UPI first checks if the entire matrix has been scanned. If it has, the various pointers are reset. If not, the address of the next row is placed on PORTs 20 thru 23. This selects the desired row. The state of the row is then read on PORT 1; the column return lines. This present state is compared to the previous state by retrieving the previous state from the matrix map and performing an Exclusive-OR with the present state. Since we are assuming that no change has occurred, the result is zero. No coordinate decoding is needed and the flow branches to the FIFO-DBBOUT Management section.

The FIFO-DBBOUT Management section simply maintains the FIFO and loads DBBOUT whenever Change Words are present in the FIFO and DBBOUT is clear (OBF=0). The section first tests if the FIFO is full. (If we assume our "no-change" row is the first row scanned, the FIFO obviously would not be full.) If it is, the UPI waits until OBF=0, at which point the next Change Word is retrieved from the FIFO and placed in DBBOUT. This "unfills" the FIFO making room for more Change Words. At this point, the Column Counter, R3, is checked. For rows with no changes, the Column Counter is always zero so the test simply falls through. (We cover the case for changes shortly.) Now the FIFO is tested for being empty. If it is, there is no sense in any further tests so the flow simply goes back up to scan the next row. If the FIFO is not empty, DBBOUT is tested again through OBF. If a Change Word is in DBBOUT waiting for the master to read it, nothing can be done and the flow likewise branches up for the next row. However, if the DBBOUT is free and remembering that the previous test showed that the FIFO was not empty, DBBOUT is loaded with the next Change Word and the last two conditional tests automotically acts OEF, OEF remains set unitagen

Now let's assume the next row contains several changed sensors. Like before, the row is selected, the return lines read, and the sensor status compared to the previous scan. Since changes have occurred, the Exclusive-OR result is now non-zero. Any 1's in the result reflect the positions of the changed sensors. This non-zero result is stored in the Compare Result register, R7. At this point, the Column Counter is preset to 8. To determine the changed sensors' locations, the Compare Result register is shifted bit-bybit to the left while decrementing the Column Counter. After each shift, BIT 7 of the result is tested. If it is a one, a changed sensor has been found. The Column Counter then reflected the sensor's matrix column position while the Scan Row Select register holds it row position. These registers are then combined in R6, the Change Word Store, to form the sensor's matrix coordinate section of the Change Word. The 8th bit of the Change Word Store is coded with the sensor's present state (Figure 18). This byte forms the complete Change Word. It is loaded into the next available FIFO position. If BIT 7 of the Compare Result had been zero, that particular sensor had not changed and the coordinate decoding is not performed.

In between each shift, test, and coordinate encode (if necessary), the FIFO-DBBOUT Management is performed. It is the Column Counter test within this section that routes the flow back up to the Change Word Encoding section if the entire Compare Result (row) has not been shifted and tested.

The FIFO is implemented as a circular buffer with IN and OUT pointers (R<sub>4</sub> and R<sub>5</sub> respectively). The operations of the FIFO is best understood using an example, Figure 21. This series of figures show how the FIFO, DBBOUT, and OBF interact as changes are detected and Change Words are read by the master. The letters correspond to sequential Change Words being loaded into the FIFO. Note that the figures show only a 4×8 FIFO however, the principles are the same in the 40×8 FIFO.

Figure 21A shows the condition where no Change Words have been loaded into the FIFO or DBBOUT. In Figure 21B a change, "A", has been detected, decoded, and loaded into the FIFO at the location equal to the value of the FIFO-IN pointer. The FIFO-OUT pointer is reset to the bottom of the FIFO since it had reached the FIFO top. Now that a Change Word is in the FIFO, OBF is checked to see if DBBOUT is empty. Because OBF=0, DBBOUT is empty and the Change Word is loaded from the FIFO location pointed at by the FIFO-OUT pointer. This is shown in Figure 21C. Loading DBBOUT automatically sets OBF. OBF remains set until the

master reads DBBOUT. Figures 21D and 21E show two more Change Words loaded into the FIFO. In Figure 21F the first Change Word is finally read by the master resetting OBF. This allows the next Change Word to be loaded into DBBOUT. Note that each time the FIFO is loaded, the FIFO-IN pointer increments. Each time DBBOUT is read the FIFO-OUT pointer increments unless there are no more Change Words in the FIFO. Both pointers wraparound to the bottom once they reach the FIFO top. The remaining figures show more Change Words being loaded into the FIFO. When the entire FIFO fills and DBBOUT can not be loaded (OBF=1), scanning stops until the master reads DBBOUT making room for more Change Words.

As was mentioned earlier, two interrupt outputs to the master are available: Change Word Ready (P<sub>25</sub>, OBF) and FIFO NOT EMPTY (P<sub>24</sub>). The Change Word Ready interrupt simply reflects OBF and is handled automatically by the UPI since an EN FLAGS instruction is executed during initialization. The FIFO NOT EMPTY interrupt is generated and cleared as appropriate, each pass through the FIFO management code.

No debouncing is provided although it could be added. Rather, the scan time is left as an equate variable so that it could be varied to account for both debounce time and expected sensor change rates. The minimum scan time for this application is 2msec when using a 6MHz clock. Since the matrix controller is coded as a foreground task, scan time simply uses a software delay loop.

The UPI software is included as Appendix B1. Appendix B2 is 8085A test software which builds a Change Word buffer starting at BUFSRT. This software simply polls the STATUS register looking for Change Word Ready to go true. DBBOUT is then read and loaded into the buffer. Now let's move on to an application which combines both the foreground and background concepts.

#### Combination I/O Device

The final UPI application was designed especially to add additional serial and parallel I/O ports to the iSBC 80/30. This UPI simulates a full-duplex UART (Universal Asynchronous Receiver/Transmitter) combined with an 8-bit parallel I/O port. Features of the UART include: software selectable baud rates (110, 300, 600, or 1200 baud), double buffering for both the transmitter and receiver, and receiver testing for false start bit, framing, and overrun errors. For parallel I/O, one 8-bit port is programmable for either input or output. The output port is statically latched and the input port is sampled.

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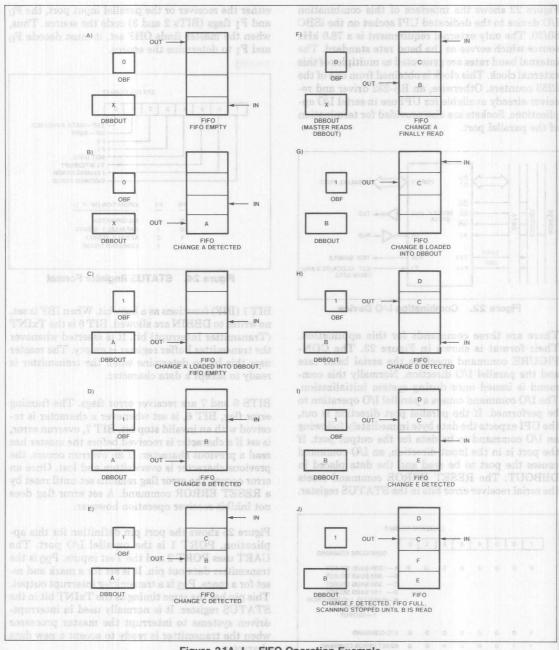


Figure 21A-J. FIFO Operation Example

Figure 22 shows the interface of this combination I/O device to the dedicated UPI socket on the iSBC 80/30. The only external requirement is a 76.8 kHz source which serves as the baud rate standard. The internal baud rates are generated as multiples of this external clock. This clock is obtained from one of the 8253 counters. Otherwise, an RS-232 driver and receiver already available for UPI use in serial I/O applications. Sockets are also provided for termination of the parallel port.

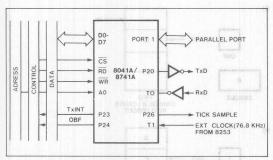


Figure 22. Combination I/O Device

There are three commands for this application. Their format is shown in Figure 23. The CON-FIGURE command specifies the serial baud rate and the parallel I/O direction. Normally this command is issued once during system initialization. The I/O command causes a parallel I/O operation to be performed. If the parallel port direction is out, the UPI expects the data byte immediately following an I/O command to be data for the output port. If the port is in the input direction, an I/O command causes the port to be read and the data placed in DBBOUT. The RESET ERROR command resets the serial receiver error bits in the STATUS register.

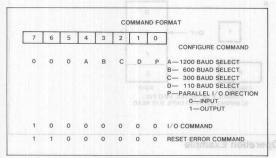


Figure 23. Combination I/O Command Format

The STATUS register format is shown in Figure 24. Looking at each bit, BIT 0 (OBF) is the DATA AVAILABLE flag. It is set whenever the UPI places data into DBBOUT. Since the data may come from

either the receiver or the parallel input port, the  $F_0$  and  $F_1$  flags (BITs 2 and 3) code the source. Thus, when the master finds OBF set, it must decode  $F_0$  and  $F_1$  to determine the source.

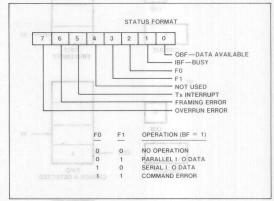


Figure 24. STATUS Register Format

BIT 1 (IBF) functions as a busy bit. When IBF is set, no writes to DBBIN are allowed. BIT 5 is the TxINT (Transmitter Interrupt) bit. It is asserted whenever the transmitter buffer register is empty. The master uses this bit to determine when the transmitter is ready to accept a data character.

BITS 6 and 7 are receiver error flags. The framing error flag, BIT 6, is set whenever a character is received with an invalid stop bit. BIT 7, overrun error, is set if a character is received before the master has read a previous character. If an overrun occurs, the previous character is overwritten and lost. Once an error occurs, the error flag remains set until reset by a RESET ERROR command. A set error flag does not inhibit receiver operation however.

Figure 25 shows the port pin definition for this application. PORT 1 is the parallel I/O port. The UART uses PORT 2 and the Test inputs.  $P_{20}$  is the transmitter data out pin. It is set for a mark and reset for a space.  $P_{23}$  is a transmitter interrupt output. This pin has the same timing as the TxINT bit in the STATUS register. It is normally used in interrupt-driven systems to interrupt the master processor when the transmitter is ready to accept a new data character.

The OBF flag is brought out on  $P_{24}$  as a master interrupt when data is available in DBBOUT.  $P_{26}$  is a diagnostic pin which pulses at four times the selected baud rate. (More about this pin later.) The receiver data input uses the TEST 0 input. One of the PORT 2 pins could have been used, however, the

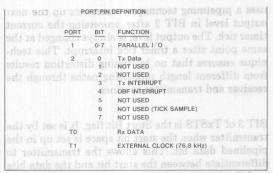


Figure 25. Combination I/O Port Definition

software can test the TEST 0 in one instruction without first reading a port.

The TEST 1 input is the baud rate external source. The UART divides this input to determine the timing needed for the selected baud rate. The input is a non-synchronous 76.8 kHz source.

Internally, when the CONFIGURE command is received and the selected baud rate is determined, the internal timer/counter is loaded with a baud rate constant and started in the event counter mode. Timer/counter interrupts are then enabled. The baud rate constant is selected to provide a counter interrupt at four times the desired baud rate. At each interrupt, both the transmitter and receiver are handled. Between interrupts, any new commands and data are recognized and executed.

As a prelude to discussing the flow charts, Figure 26 shows the register definition. Register Bank 0 serves the UART receiver and parallel I/O while Register Bank 1 handles the UART transmitter and commands. Looking at RB0 first, R3 is the receiver status register, RxSTS. Reflected in the bits of this register is the current receiver status in sequential order. Figure 27 shows this bit definition. BIT 0 is the Rx flag. It is set whenever a possible start bit is received. BIT 1 signifies that the start bit is good and character construction should begin with the next received bit. BIT 1 is the Good Start flag. BIT 2 is the Byte Finished flag. When all data bits of a character are received, this flag is set. When all the bits, data and stop bits are received, the assembled character is loaded into the holding register (R4 in Figure 27) BIT 3, the Data Ready flag, is set. The foreground routine which looks for commands and data continuously, looks at this bit to determine when the receiver has received a character. BITS 4 and 5 signify any error conditions for a particular character.

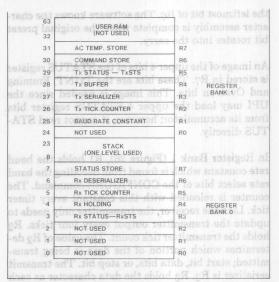


Figure 26. Combination I/O Register Map

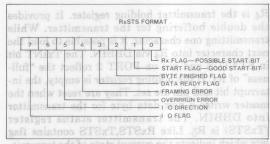


Figure 27. RxSTS Register

The parallel I/O port software uses BITS 6 and 7. BIT 6 codes the I/O direction specified by the last CONFIGURE command. BIT 7 is set whenever an I/O command is received. The foreground routine tests this bit to determine when an I/O operation has been requested by the master.

As was mentioned, R<sub>4</sub> is the receiver holding register. Assembled characters are held in this register until the foreground routine finds DBBOUT free, at which time the data is transferred from R<sub>4</sub> to DBBOUT. R<sub>5</sub> is the receiver tick counter. Recall that counter interrupts occur at four times the baud rate. Therefore, once a start bit is found, the receiver only needs to look at the data every four interrrupts or tick counts. R<sub>5</sub> holds the current tick count.

R<sub>6</sub> is the receiver de-serializing register. Data characters are assembled in this register. R<sub>6</sub> is preset to 80H when a good start bit is received. As each bit is

sampled every four timer ticks, they are rotated into the leftmost bit of R6. The software knows the character assembly is complete when the original preset bit rotates into the carry.

An image of the upper 4 bits of the STATUS register is stored in R7. These bits are the TxINT, Framing and Overrun bits. This image is needed since the UPI may load the upper 4 STATUS register bits from its accumulator; however, it cannot read STATUS directly.

In Register Bank 1 (Figure 26), R1 holds the baud rate constant which is found from decoding the baud rate select bits of the CONFIGURE command. The counter is reloaded with this constant every timer tick. Like the receiver, the transmitter only needs to update the transmitter output every four ticks. R2 holds the transmitter tick count. The value of R2 determines which portion of the data is being transmitted; start bit, data bits, or stop bit. The transmit serializer is R3. R3 holds the data character as each character bit is transmitted.

R<sub>4</sub> is the transmitter holding register. It provides the double buffering for the transmitter. While transmitting one character, it is possible to load the next character into R<sub>4</sub> via DBBIN. The TxINT bit in STATUS and pin on PORT 2 reflect the "fullness" of R<sub>4</sub>. If the holding register is empty, the interrupt bit and pin are set. They are reset when the master writes a new data byte for the transmitter into DBBIN. The transmitter status register (TxSTS) is R<sub>5</sub>. Like RxSTS,TxSTS contains flag bits which indicate the current state of the transmitter. This flag bit format is shown in Figure 28.

TxSTS BIT 0 is the Tx flag. It is set whenever the transmitter is transmitting a character. It is set from the beginning of the start bit until the end of the stop bit. BIT 1 is the Tx request flag. This bit is set by the foreground routine when it transfers a new character from DBBIN to the Tx holding register, R4. The transmitter software uses this flag to tell if new data is available. It is reset when the transmitter transfers the character from the holding register to the serializer.

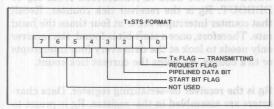


Figure 28. TxSTS Register

BIT 2 is the pipelined Tx data bit. The transmitter uses a pipelining technique which sets up the next output level in BIT 2 after processing the current timer tick. The output level is always changed at the same point after a timer tick interrupt. This technique ensures that no bit timing distortion results from different length processing paths through the receiver and transmitter routines.

BIT 3 of TxSTS is the Start Bit flag. It is set by the transmitter when the start bit space is set up in the pipelined data bit. This allows the transmitter to differentiate between the start bit and the data bits on following timer ticks.

The flow charts for this application are shown in Figures 29A-F. At reset, the INIT routine is executed which initializes the registers and port pins. After initialization, IBF and OBF are tested in MNLOOP. These flags are tested continually in this loop. If IBF is set, F1 is tested for command or data and execution is transferred to the appropriate routine (CMD or DATA). If IBF=0, OBF is checked. If OBF=0 (DBBOUT is free), the Rx data ready and I/O flags in RxSTS are tested. If Rx data ready is set. the received data is retrieved from the Rx holding register and transferred to DBBOUT. Any error flags associated with that data are also transferred to STATUS. If the I/O flag is set and the I/O direction is input, PORT 1 is read and the data transferred to DBBOUT. In either case, Fo and F1 are set to indicate the data source. stormstol resewied helbrad

If IBF is set by a command write to DBBIN, CMD reads the command and decodes the desired operation. If an I/O operation is specified, the I/O flag is set to indicate to the MNLOOP and DATA routines that an I/O operation is to be performed. If the command is a CONFIGURE command, the constant for the selected baud rate is loaded into both Baud Rate Constant register and the timer/counter. The timer/counter is started in the event counter mode and timer/counter interrupts are enabled. In addition, the I/O port is initialized to all 1's if the I/O direction bit specifies an input port. If the command is a RE-SET ERROR command, the two error flags in STA-TUS are cleared.

If the IBF flag is set by a data write, the DATA routine reads DBBIN and places the data in the appropriate place. If the I/O flag is set, the data is for the output port so the port is loaded. If the I/O flag is reset, the data is for the UART transmitter. Data for the transmitter resets the TxINT bit and pin plus sets the Tx request flag in TxSTS. The data is transferred to the Tx holding register, R4.

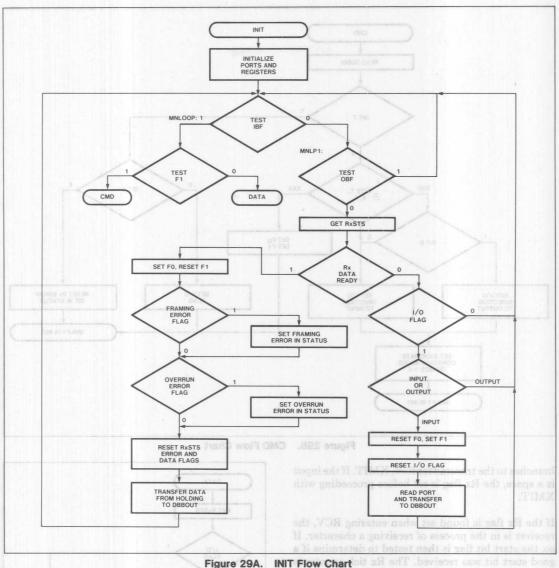


Figure 29A.

Once a CONFIGURE command is received and the counter started, timer/counter interrupts start occurring at four times the selected baud rate. These interrupts cause a vector to the TIMINT routine, Figure 29D. A 76.8 kHz counter input provides a 13.02 µs counter resolution. Since it requires several UPI instruction cycles to reload the counter, the counter is set to two counts less than the desired baud rate and the counter is reloaded in TIMINT synchronous with the second low-going transition after the interrupt. Once the counter is reloaded, an output port (P26) is toggled to give an external indication of internal counter interval. This is a helpful diagnostic feature. After the tick sample output, the pipelined transmitter data in TxSTS is output to the TxD pin. Although this occurs every timer tick, the pipelined data is changed only every fourth tick.

The receiver is now handled, Figure 29E. The Rx flag in RxSTS is examined to see if the receiver is currently in the process of receiving a character. If it is not, the RxD input is tested for a space condition which might indicate a possible start bit. If the input is a mark, no start bit is possible and execution

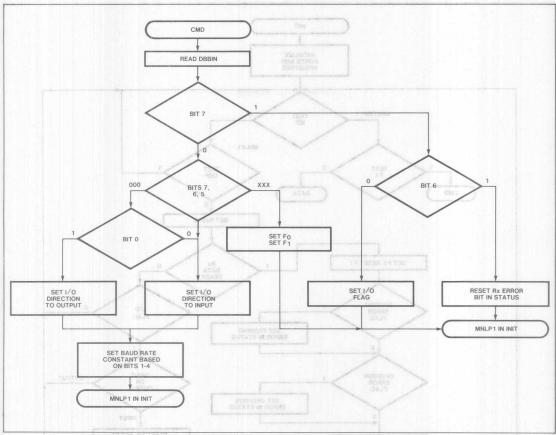


Figure 29B. CMD Flow Chart

branches to the transmitter flow, XMIT. If the input is a space, the Rx flag is set before proceeding with XMIT.

If the Rx flag is found set when entering RCV, the receiver is in the process of receiving a character. If so, the start bit flag is then tested to determine if a good start bit was received. The Rx tick counter is initialized to 4 and the Rx deserializer is set to 80H. A mark indicates a bad start bit; the Rx flag is reset to abort the reception.

If the start bit flag is set, the program is somewhere in the middle of the received character. Since the data should be sampled every fourth timer tick, the tick counter is decremented and tested for zero. If non-zero no sample is needed and execution continues with XMIT. If zero, the tick counter is reset to four. Now the byte finished flag is tested to determine if the data sample is a data or stop bit. If reset, the sample is a data bit. The sample is done and the new bit rotated into the Rx deserializer. If this rotate

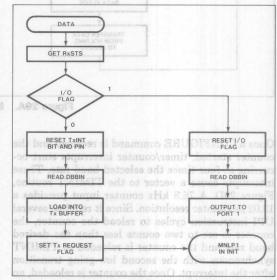


Figure 29C. Data Flow Chart

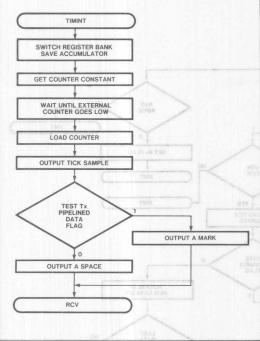


Figure 29D. TIMINT Flow Chart

sets the carry, that data bit was the last so the byte finished flag is set. If the carry is reset, the data bit is not the last so execution simply continues with XMIT.

Had the byte finished flag been set, this sample is for the stop bit. The RxD input is tested and if a space, the framing error flag is set. Otherwise, it is reset. Next, the Rx data ready flag is tested. If it is set, the master has not read the previous character so the overrun error flag is set. Then the Rx data ready flag is set and the received data character is transferred into the Rx holding register. The Rx, start bit, and byte finished flags are reset to get ready for the next character.

Execution of the transmitter routine, XMIT, follows the receiver, Figure 29F. The transmitter starts by checking the start bit flag in TxSTS. Recall that the actual transmit data is output at the beginning of the timer routine. The start bit flag indicates whether the current timer tick interrupt started the start bit. If it is set, the pipelined data output earlier in the routine was the start of the start bit so the flag is reset and the Tx tick counter is initialized. Nothing else is done this timer tick so the routine returns to the foreground.

In the start bit flag is reset, the Tx tick counter is incremented and tested. The test is performed modulo 4. If the counter mod 4 is not zero, it has not been four ticks since the transmitter was handled last so the routine simply returns. If the counter mod 4 is zero, it is time to handle the transmitter and the Tx flag is tested.

The Tx flag indicates whether the transmitter is active. If the transmitter is inactive, no character is currently being transmitted so the Tx request flag is tested to see if a new character is waiting in the Tx buffer. If no character is waiting (Tx request flag=0), the Tx interrupt pin and bit are set before returning to the foreground. If there is a character waiting, it is retrieved from the buffer and placed in the Tx serializer. The Tx request flag is reset while the Tx and start bit flags are set. A space is placed in the Tx pipelined data bit so a start bit will be output on the next tick. Since the Tx buffer is now empty, the Tx interrupt bit and pin are set to indicate the availability of the buffer to the master. The routine then returns to the foreground.

If the tick counter mod 4 is zero and the Tx flag indicates the transmitter is in the middle of a character, the tick counter is checked to see what transmitter operation is needed. If the counter is 28H (40D), all data bits plus the stop bits are complete. The character is therefore done and the Tx flag is reset. If the counter is 24H (36D), the data bits are complete and the next output should be a mark for the stop bit so a mark is loaded into the Tx pipelined data bit.

If neither of the above conditions are met for the counter, the transmitter is some place in the data field, so the next data bit is rotated out of the Tx serializer into the pipelined data bit. The next tick outputs this bit.

At this point the program execution is returned to the foreground.

That completes the discussion of the combination I/O device flow charts. The UPI software listing is shown in Appendix C1. Appendix C2 is example 8085A driver software.

Several observations concerning the drivers are appropriate. Notice that since the receiver and input port of the UPI use the OBF flag and interrupt output, the interrupt and flag are cleared when the master reads DBBOUT. This is not true for the transmitter. There is always some time after a master write of new transmitter data before the transmitter bit and pin are cleared. Thus in an interrupt-driven system, edge-sensitive interrupts should be

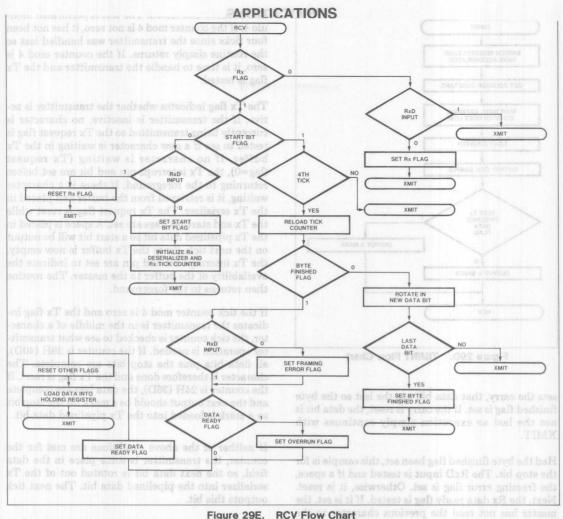


Figure 29E. RCV Flow Chart

used. For polled-systems, the software must wait after writing new data for IBF=0 before re-examining the Tx interrupt flag in STATUS.

Notice that this application uses none of the user data memory above Register Bank 1 and only 361 bytes of program memory. This leaves the door open for many improvements. Improvements that come to mind are increased buffering of the transmit or received data, modem control pins, and parallel port handshaking inputs.

This completes our discussion of specific UPI applications. Before concluding, let's look briefly at two debug techniques used during the development of

these applications that you might find useful in your own designs,

#### **DEBUG TECHNIQUES**

Since the UPI is essentially a single-chip microcomputer, the classical data, address, and control buses are not available to the outside world during normal operation. This fact normally makes debugging a UPI design difficult; however, certain "tricks" can be included in the UPI software to ease this task.

If a UPI is handling multiple tasks, it is usually easier to code and debug each task individually. This is fairly standard procedure. Since each task usually utilizes only a subset of the total number of I/O pins,

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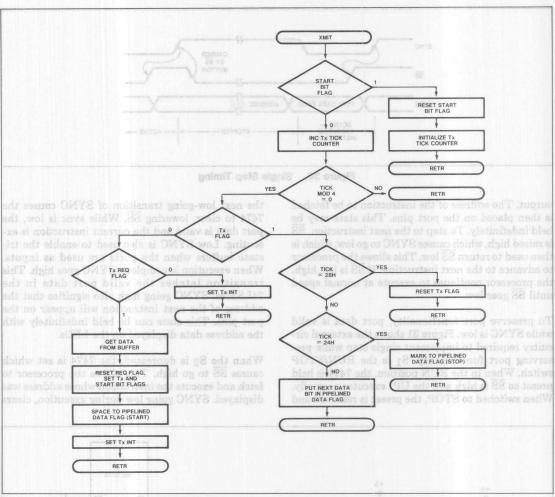


Figure 29F. XMIT Flow Chart

coding only one task leaves some I/O pins free. Port output instructions can then be added in the task code being debugged which toggle these unused pins to determine which section of task code is being executed at any particular time. The task can also be made to "wait" at various points by using an extra pin as an input and adding code to loop until a particular input condition is met.

One example of using an extra pin as an output is included in the combination serial/parallel device code. During initial development the receiver was not receiving characters correctly. Since this could be caused by incorrect sampling, three lines of code were added to toggle BIT 6 of PORT 2 at each tick of the sample clock. This code is at lines 184 and 185 of the listing. Thus by looking at the location of the tick

sample pulse with respect to the received bit, the UPI sampling interval can be observed. The tick sample time was incorrect and the code was modified accordingly. Similar techniques could be applied at other locations in the program.

The EPROM version of the UPI (8741A) also contains another feature to aid in debug: the capability to single step thru a program. The user may step thru the program instruction-by-instruction. The address of the next instruction to be fetched is available on PORT 1 and the lower 2 bits of PORT 2. Figure 30 shows the timing used in the discussion below. When the single step input,  $\overline{SS}$ , is brought low, the internal processor responds by stopping during the fetch portion of the next instruction. This action is acknowledged by the processor raising the SYNC

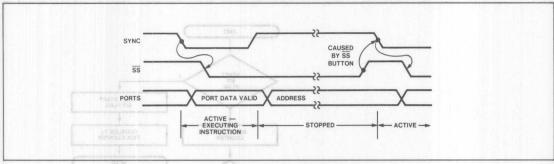


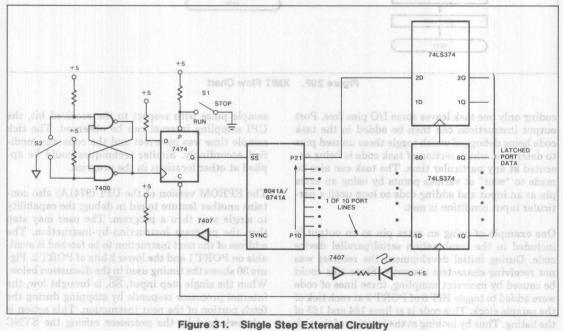
Figure 30. Single Step Timing

output. The address of the instruction to be fetched is then placed on the port pins. This state may be held indefinitely. To step to the next instruction, SS is raised high, which causes SYNC to go low, which is then used to return SS low. This allows the processor to advance to the next instruction. If SS is left high, the processor continues to execute at normal speed until SS goes low.

To preserve port functionality, port data is valid while SYNC is low. Figure 31 shows the external circuitry required to implement single step while preserving port functionality. S1 is the RUN/STOP switch. When in the RUN position, the 7474 is held preset so SS is high and the UPI executes normally. When switched to STOP, the preset is removed and

the next low-going transition of SYNC causes the 7474 to clear, lowering SS. While sync is low, the port data is valid and the current instruction is executing. Low SYNC is also used to enable the tristate buffers when the ports are used as inputs. When execution is complete, SYNC goes high. This transition latches the valid port data in the 74LS374s. SYNC going high also signifies that the address of the next instruction will appear on the port pins. This state can be held indefinitely with the address data displayed on the LEDs.

When the S2 is depressed, the 7474 is set which causes SS to go high. This allows the processor to fetch and execute the instruction whose address was displayed. SYNC going low during execution, clears



the 7474 lowering  $\overline{SS}$ . Thus the processor again stops when execution is complete and the next fetch is started.

All UPI functions continue to operate while single stepping (the processor is actually executing NOPs internally while stopped). Both IBF and timer/counter interrupts can be serviced. The only change is that the interval timer is prescaled on single stepped instructions and, of course, will not indicate the correct intervals in real time. The total number of instruction which would have been executed during a given interval is the same however.

The single step circuitry can be used to step through a complete program; however, this might be a time-consuming job if the program is long or if only a portion is to be examined. The circuitry could easily be modified to incorporate the output toggling technique to determine when to run and stop. If you would like to step thru a particular section of code,

an extra port pin could replace switch S<sub>1</sub>. Extra instructions would then be added to lower the port when entering the code section and raise the port when exiting the section. The program would then stop when that section of code is reached allowing it to be stepped through. At the end of the section, the program would execute at normal speed.

#### CONCLUSION

Well, that's it. Machine readable (floppy disk or paper tape) source listings of UPI software for these applications are available in Insite, the Intel library of user-donated programs. Also available in Insite are the source listings for some of Intel's pre-programmed UPI products.

For information about Insite, write to: Insite Intel Corp. 3065 Bowers Ave. Santa Clara, Ca 95051

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For information about Insite, write to:

entenI

tel Coms

3065 Bowers Ave.

### **APPENDIX A**

LOC OBJ

INE	SOURCE STATEMEN								PIBPLAY	
1	\$MOD41A			****	PALITA					
2	; **********	*****	****	***	****	***	***			
3	* UPI-41A E	-DIGIT LE	D DISP	LAY	CONT	ROLL	ER	*		
4	, *********	****	****	***	****	***	****	**	CHARACT	
5	,	HARACTER								
6	,									
7	1				0					
8	THIS PROGRAM USES THE	UPI-41A	AS A L	ED I	DISPL	AY C	ONTR	OLLER		
9	WHICH SCANS AND REFRE	SHES EIGH	T SEVE	N-SE	EGMEN	T LE	D DI	SPLAYS.		
10	THE CHARACTERS ARE DE	FINED BY	INPUT	FROM	MAM	ASTE	R CP	U IN TH	E	
11	FORM OF ONE EIGHT BIT	WORD PER	DIGIT	-CHA	ARACT	ER S	BELEC	TION.		
12	i		6							
13				1	2	0				
14	i .	65			0	7				
15	; *******	*****	****	***	****	***	***	****	****	-
16	;				0	- 8				
17	REGISTER DEFINITIONS:	11								
18	REGISTER		RB1	0				RBO		
19	;									
20	; RO	DISPLAY	MAP P	DINT	TER			NOT !	USED	
21	; R1	NOT USE	D		8			NOT	USED	
22		DATA WO	RD AND	CHA	ARACT	ER S	STORA	GE NOT		
23		DIGIT C		10				NOT		
24		NOT USE		1			1	NOT		
25		NOT USE			- 0	- 0		NOT		
26		NOT USE	- 17					NOT		
27		ACCUMUL						NOT		
	; *****	****	****	***	****	***	****	****	***	1
29			1	1	1	0				
	PORT PIN DEFINITIONS:	9.	0.	0	0	1	1			
31		PORT 1	FUNCTI	ON	0	P	ORT	2 FUNCT	IUN	
32		OF OWENIE		-	0	. 1				
33		SEGMENT	DKINE	K CC	חאואם	L	IGIT	DRIVER	CONTROL	-
	\$EJECT				I	1	- 2			
30	PEUEU1			0	1		1			
			0	ž	1	1				
		"BILANK"				1				
								TOBLE	S TIDIO	
					40		2.0			
						0	0			

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 PAGE 2 LOC OBJ LINE SOURCE STATEMENT 36;\* 39; 40; 0-4 CHARACTER SELECT
41; 5-7 DIGIT SELECT
42;
43; CHARACTER SELECT: 44 ; D4 D3 D2 D1 D0 CHARACTER 45 ; 0 00 00 274.192.0 141 U-0 0 0 0 0 0 0 0 0 1 0 1 THIS PROPRET USED TO SENSE SE VANDE AND HERKESHES SENSE THE PART CORD THE CHARACTERS ARE DETINED AND TOOR ONE SIGHT BIT GOND TO THE PART OF THE PART O 0 0 47 : 48 ; 0 0 0 49 ; 00 50 ; 51 ; 52 ; 0 0 1 0 53 ; 0 0 0 8 55 ; 0 0 1 0 AB 56 ; 0 0 57 ; 0 0 0 58 ; 0 0 DE 0 60; 0 1 1 0 0 61 ; 0 0 64 ; 00 0 0 0 65 ; 66 ; 0 0 67 ; 68 ; 0 0 69 : 0 0 0 70 ; 71 ; ORTHOD REVIEW 11 00 73 ; 74 ; 0 0 76 i "BLANK" 78 ; DIGIT SELECT: D7 D6 D5 DIGIT NUMBER 0 81 : 0 0 2 82 ; 0 0 3 83 ; 0 84 ;

0 0

0

85 ;

86 :

89 \$EJECT

5

6

8 88 ; \*

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.oc	OBJ	LINE	SOURCE	BTATEMENT		STATEMENT	SOURCE	3011.3	600	on.
		90	; *****					*****		
		91	1	EQU	JATES TUDE YAL			1-901		
		92	THE FOLLOWING	CODE DESIGNA	ATES "TIME" AS	A VARIABLE TH	HIS TROP BIN	T : OAI		
		93	ADJUSTS THE A	MOUNT OF CYCL	ES THE TIMER	COUNTS BEFORE	HE MONU CEN	141 - WC		
		94	A TIMER INTER	RUPT OCCURS #	AND REFRESHES	THE DISPLAY, AF	PROXIMATEL	VID I SAI		
		95	50 TIMES PER	BECOND.	WILL HAVE RE	STRUBBETHE BER	IT THOIS SE	143 : TH		
FF1		96	TIME EQUIPM	-OFH TAJTI	MER VALUE 2:	MSEC AND AT		144 (85)		
		97	*******	*********	******	*******	******	*****		
		98	TER BANK IS HEE	RIGHT REGIS	TERRUPT BRANCE	HING MUDDA BHT	RESET AND	146:18		
		99	THIS PORTION	OF MEMORY IS	DEDICATED FOR	USE OF RESET	AND	147 /		
		100	INTERRUPT BRAI	NCHING WHEN	THE INTERRUPTS	ARE ENABLED 1	HE 198 (A.F	ere pre		0.10
		101	CODE AT THE FO	DLLOWING DESI	GNATED SPOTS	ARE EXECUTED W	HEN A	149		
			RESET OR A IN					002	6048	P40
0000					DO TIGIGA			101	119	
	0409		PRESENTED SAN				180	152	8328	
0002		105					VON		SA	920
	0436	106	GAM . IMP IMP	INPUT	TRE IN	TERRUPT 099 A	1/7/86			650
0005			NOP 3					663		
	00		SOTA JUNIOP				VOM	156		
	041D	109				INTERRUPT				699
,,,,,	0410		; *********							
		111					TEIX	981	7080	
			THE FOLLOWING					061		
			; INTO OPERATION							
			MAP IS FILLED							
			INTERRUPTS ARE							
			I INTERNOT TO PART				TATE	761		
0009	D5		START: SEL	PR1s : MITTON	39079391	A. 87		165	33	
	BAOB		ORL	P2, #08H	TURN D	GIT DRIVERS OF			93	
	B838		MOV							
	23FF		BLKMAP: MOV	A, #OFFH			TOS			
010			MOV			TO DISPLAY MAP				
0011		122	INC	RO		ENT DISPLAY MAP				
012		123	MOV	A, RO		MAP POINTER 1		TOR		
	B20E	124	105	BLKMAP		DISPLAY MAP TIL		ION		
	BBOO	125		R3, #00H		SIT COUNTER TO				
	23F1	126	MOV	A, #TIME	TIMER					
019		127		T. A	LOAD T					
01A		128		T	START					
01B		129	EN			TIMER INTERRUF	т			
01C		130	EN	I		IBF INTERRUPT				
			; ******				******	******		
		132			ER PROGRAM					
			A USERS PROGRA			S POINT THE S	OLL ON THE			
			CODE IS UND CO			O . OINI. INE P	OLLOWING			
			SYNC CHARACTER			TE IMMEDIATELY	PRECEEDS TO	4F		
			FINAL SYNC.						4.46	
			\$EJECT		CONTROLL					

OC OBJ	LINE	SOURCE STATE	MENT	STATEMENT	BORNOS				
	138 ; ****	***	****	****	*****	****	****		
	139 ;		DISPLAY ROUTIN	E AUDB			1.6		
	140 ; THI	S PORTION OF T	HIS PROGRAM IS AN	NTERRUPT ROUTINE	WHICH	IS	56		
	141 ; ACTE	D UPON WHEN TH	E TIMER COUNT IS CO	MPLETED. THE ROL	TINE UP	DATES			
			FROM THE DISPLAY MA						
			NTERRUPTS WILL HAVE						
	144 ; REGI	STER BANK 1 IS	SELECTED AND THE	CCUMULATOR IS SA	VED UPO	V			
			NE. ONCE THE DISPLA						
	146 ; IS R		CCUMULATOR AND PRE-						
	147 ;		A RO SEU NOR GETADI						
01D D5			MANA STANFREGIS						
01E AF	149		A SAVE						
01F 8A0B	150			DIGIT DRIVERS OF					
021 FB	151			COUNTER TO ACCU		cons.			
022 4338		ORL A, #	38H : "OR"	TO GET DISPLAY				9050	
024 AB	153	MOV RO,	A ; DISPL	AY MAP POINTER	180394		601		
025 F0	154								
026 39	155	OUTL P1,		T CHARACTER TO S					
027 FB	156	MOV A, R		COUNTER VALUE 1					
028 3A	157		A COUTPU						
029 1B 02A D307	159		FO7H ; CHECK	IF AT LAST DIG					
02C 9630	160		IME TO CHA LA ; RESET						
02E BB00			#OOH RESET						
030 23F1			TIME TIME						
032 62	163	MOV T. A		TIMER 43 BANS 3					
033 55	164	STRT T							
034 FF	165	MOV A, R				TRATE			
035 93	166		TING TIGIG MIRETUR						
	167 ; ****		***		*****	*****	***		
	168 \$EJEC		PRIMA (Breing)						
			VALISELA DI MESLIAY		VON		121	GA	
			: INCREMENT DISPLA					16	
	ROTA.	TER TO ACCUME.	DISPLAY MAP POIN	OH-A	VOH			FS	
			BLANK DISPLAY NA		486		457		
				HODBAER	VOR		125		
			MULIAV KENKT:	SMITE A					
					VOM		281		
					THIE		861	86	
			SMARKE TIMER INT		1438				
		· · · · · · · · · · · · · · · · · · ·	**************						
		NAME OF TAXABLE PARTY.	NAME OF THE PARTY		manage as				
		ALLE ANTINIA THE	THIS BOINT TA EST						
	The last of	64501000 V	ATGERNA BYTE MUEROE	CNCLUDED WITH					
			ALLISTEL STEL TOWNS						

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LOC	OBJ	LINE	SOURCE STA	TEMENT		TWENTTAYE			USD	2007
	020		0001102 0111							
						<b>经存货的 计自由表示 电电影操</b>				
						*****				
		171 ;				T ROUTINE				
						RRUPT ROUTINE				
						THE ROUTINE GE				
						NES BOTH THE I				
						DONE BY MEANS				
						AP FOR DIGIT A				
						N FOR A DECIMA				
						IN THE DISPLAY				
						IS SAVED UPON		LIMILLATOR		
			THE PRE-INTE			N FULLY DEFINE				
		181 ; AND		RRUPI REGISI	ER BANK 15	RESTURED.				
0036	D5	183 INPU				R BANK 1		SEND ISS SNHO SES		
0036		184		7. A 9		CUMULATOR				
0037		185		DBB	GET DAT					
0039		186	E100	2, A		TA WORD	80			
0037		187		0 0 0 0		DIGIT LOCATION				
003B		188		0 1 1 0	O ; II	DIGIT LOCALION	80			
	5307	189	*****	, #07H	0 ; 1:			22S CHA:		ADEC
	4338	190		#38H	0 .1:			18HD VSE		
0040		191		0, A 0 0		OCATION IN DI				
0041		192		R20 0 1		ATA WORD TO AC				
	531F	193		#1FH 0 0		CHARACTER LOOK				
0044	E3	194	MOVP3 A	A CO	GET CHA		610	- Pag Chill-		
0045	AA	195	MOV	2, A 1	SAVE CH	ARACTER	38.0			
0046	D37F	196	XRL	#7FH 0 0		ACTER DECIMAL	POINT	- 0HB - 6HB -		
0048	C64E	197	JZ I D D	POINT 0	0 111				78	0312
004A	FA	198	MOV	. R2	; SAVED C	HARACTER TO AC	CUMULATOR		878	
004B	AO	199	MOV	RO, A	; CHARACT	ER TO DISPLAY	MAP =		13	0314
0040	0451	200	JMP R	ETURN 0 0	1 : 11					0315
004E		201 DPOI		IR2 DOLL		HARACTER TO AC		240 0701	84	0316
004F		202		@RO		ITH OLD CHARAC				0317
0050		203		RO, A		DISPLAY MAP		:9H5 S1S		BIED
0051		204 RETU		, R7	RESTORE	ACCUMULATOR	. SG			
0052	93	205	RETR	1 0 0 0	0 64	SYM	8.0	THIS ARS		
		206 ; ***		****		****				
		207 \$EJE				910				
								247 CHDA 248 CHBA		
								MAJE FAS		
		481818144		THE RESIDENCE STATES		27770			44	
							Gisti			
									BUDGMY	
			CH3 6363					BLAMAP DOOE		
		CHB DSC								
		DEO HIED							GODO	
									#15D	

2-36

ISIS-II M	1CS-48/UP I	-41 MACRO	ASSEMBLE	R, V3.0		∃ PA	GE	6					RHEGSA C			и-вом	
LOC OF	IJ	LINE	SOURCE	STATEME	NT				79	ratte	TATE	308					
		208 . ***	****	****	****		***										
				*****													
				JP TABLE										M. 3 . (3.7.7)			
				IS USED T													
				POINT FO										1 7477			
				IC IS USE													
				VEN SEGME													
				MA TIOTA													
0000				JAMI DEC I									DONTION				
0300		2007/2	ORG			DP ; DP							IN Y JUNI				
0300 C		218 CHO:				ADTA: 1							EI I RMA				
0301 F				OF9H							0		TTUDA BH				
0302 A4		220 CH2:	DB				0			0 1		the Charles	N BHT OV				
0303 B		221 CH3:	DB	овон		; 1	0	1		0 0		0					
0304 99		222 CH4:	DB			PETETER.		0		1 0				MI BBI			
0305 92		223 CH5:	DB			DOA HUI					1						
0306 83		224 CH6:	DB	82H		ATAC TE				0 0		100		195			
0307 F8		225 CH7: 226 CHB:	DB			TAG BUILD				1 0		0					
0308 80			DB		3 1201	DEFINE D					0 4 0	Olai					
0304 98		227 CH9:		98H		; 1					0 0						
030B 83		228 CHA: 229 CHB:	DB	83H		; 1				1 0 0							
0300 03		230 CHC:		-						0 0		1				4338	
030D A1		231 CHD:		OCAH			0	-	133	7	0 1	0		361			
030E 88				B6H			0	0		0 0	0 0	0					1900
030F 8E		233 CHF:	DB			RAHO TEL				1 401		0					
0310 7F		234 CHDP				O IVE CHA				1 4 1		1		2.9			0045
0311 Ca		235 CHG:		OC2H			1			0 0							
0312 89	,	236 CHH:	DB	89H		; 1	o			1 0		1					
0313 FE		237 CHI:			MERACTE	TAVED OF	1	-	77	1 9 0		1 00					4400
0314 E1		23B CHJ:		OE1H				1		0 0		1 00					
0315 C7	,	239 CHL:	DB	OC7H		; 1	1			0 1		1 9					
0316 A		240 CHN:	POT DB	OABH	ARACTI		0	1		1 0		100					
0317 A3	3	241 CHO:	DB	HEAD ACH	LIO HT	IN TOWN	0				) A 1	1 1					
0318 80		242 CHP:	DB	всн	DIGEL	OT NOM	0	0	0	1 01	0	OVE	Old .				
0319 AF		243 CHR:	DB	OAFH	ACCUM	I ISTORE	0	1	0	1 111	A 1	1 1/6		204 RE			
031A 87		244 CHT:	DB	87H		; 1	0	0	0	0 1	1	1					
031B C1		245 CHU:	DB	OC1H	10000	energy 1	1 1 1	0	0	0 0	0	-1-	******	# 1 805			
0310 91		246 CHY:	DB	91H		; 1	0	0	1	0 0	0	1		30 705			
031D BF		247 CHDA		OBFH		i 1	0		1	1 1	1	1					
031E FI		248 CHAP		OFDH		; 1	1	1		1 1		1					
031F FF		249 BLAN		OFFH		; 1	1			1 1		1					
		250 ; ***		***	****	****	***	***	***	***	***	****	****	****	++		
		251	END														
USER SYME	OL S																
		MAP OOOE	сно	0300	CH1	0301	CH2		030	7	CIT	3	0303	CH4	0304	CHE	0705
	806 CH7		CHB		CH1	0301	CHA		030		CH	APOS	0303	CH4 CHB	0304 030B	CH5 CHC	0305 030C
		ASH 031D	CHDP		CHE	030F	CHE		030		CH		031E	CHB	0308	CHC	0300
	14 CHL		CHN		CHO	0317	CHP		030		CHI		0311	CHT	031A	CHU	0313
CHY 03		PLA 001D	DPOINT		INPUT	0036	RETL	IRN				TIME		START	0009	TIME	
											1000		The same of the sa				

ASSEMBLY COMPLETE, NO ERRORS

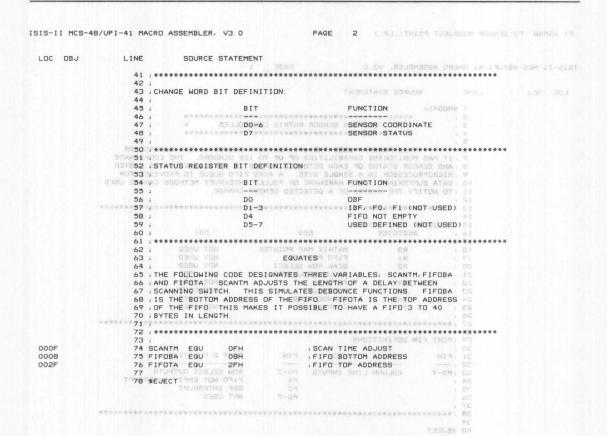
AFRI-01538A

:F1:ASM48 :F3:SENSOR NOOBJECT PRINT(:LP:) % 30A9 0 EV JAEJSM35EA DROAM IA-140ASA-BOM 11-8181

40 SEJECT

PAGE ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 LOC OBJ LINE SOURCE STATEMENT 1 \$MOD41A \*\*\*\*\*\*\*\*\*\*\* STAN \* 19080 UPI-41A SENSOR MATRIX CONTROLLER 3; \*\*\*\*\*\*\*\*\* 5 ; 6;
THIS PROGRAM USES THE UPI-41A AS A SENSOR MATRIX CONTROLLER.
7; IT HAS MONITORING CAPABILITIES OF UP TO 128 SENSORS. THE COORDINATE
8; AND SENSOR STATUS OF EACH DETECTED CHANGE IS AVAILABLE TO THE MASTER
9; MICROPROCESSOR IN A SINGLE SYTE. A 40X8 FIFO GUEUE IS PROVIDED FOR
10; DATA BUFFERING. BOTH HARDWARE OR POLLED INTERRUPT METHODS CAN BE USED 11 ; TO NOTIFY THE MASTER OF A DETECTED SENSOR CHANGE. 12 : 15 : REGISTER DEFINITIONS: RBI RBG 16; REGISTER RBG MATRIX MAP POINTER FIFO POINTER SCAN ROW SELECT 18; R0 19; R1 20; R2 NOT USED NOT USED 20; R2 SCAN ROW SELECT NUT USED
21; R3 COLUMN COUNTER NOT USED
22; R4 FIFO-IN NOT USED
23; R5 FIFO-OUT NOT USED
24; R6 CHANGE MORD NOT USED
25; R7 COMPARE NOT USED NOT USED 26 : 29 ; PORT PIN DEFINITIONS: 30 ; 31 ; PIN PORT 1 FUNCTION PIN PORT 2 FUNCTION 33 : PO-7 PO-3 ROW SELECT OUTPUTS
P4 FIFO NOT EMPTY INTE COLUMN LINE INPUTS 34 ; P4 P5 FIFO NOT EMPTY INTERRUPT OBF INTERRUPT 36 ; P6-7 NOT USED 37 : 

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112 AMOV U.A.R2 ROW SCAN SELECT VALUE TO ACCUMULATOR
113 OUTL P2.A FINITIALIZE PORT 2, BIT 4 FOR "EN FLAGS"

OOIC F5 TARMUSSA 114; TROS MEN SUTA FLAGS 303 TUSMI; ENABLE OBF INTERRUPT PORT 2, BIF 4

MOYALUNDS A 115 JO SAGE STATEMEN STATEMENT OF SAGE SAGE STATEMENT OF SAGE STATEMENT O

0018 B... 001A FA

	LINE	500	RCE STATEMENT					
	117		**********	**********	*******	***********	******	
	118	i						
	119		SC	AN AND COMPARE				
	120	,						
			WING CODE IS T					
			RING THIS SECT					
			SCANNED. IF S					W
			ARE RESET TO TH					
			SNT BEEN SCANNI					
			FOR SCANNING A					~
			OF THE REGIST					,
			E FUNCTION DES					
			TRIX IS SCANNE					
			). A BYTE OF					
	132	AT THE TI	ME THE NEW COL	UMN STATUS IS	COMPARED TO	THE OLD. THE	RESULT IS	
	133	STORED IN	THE COMPARE RI	EGISTER. THE	PROGRAM IS	THEN ROUTED AC	CORDING TO	
			R NOT A CHANGE					BAOF
	135	TOS ASTRICE	MPUT ADDRESS RE	TOTIAL A	BOTT IN OFF			
	136	; *******	*****	******	********	*********	*****	
	137		LIZE FORT 1 HIC					
OID FA			IV A ROLA, R2 BY					
01E 530F	139	AN	Laga A, #OFH at	TI SW ; CHECK	FOR O SCAN	VALUE ONLY, NO	TINTERRUPT	
020 C626	140	ROYALIUMUSZ	C TE RO MADE	MADE: IF O	RESET REGIS	TERS		
023 CA	141	DE DE	C 138 KO MADE	DECRE	MENT SCAN D	MAP PUINTER		
024 0420	142	DE	C HITA R2	DECKE	MATRIX	UW SELECT		
026 BB3F	144	RSETRO MO	V RO, #3FH	PECET	MATRIX MAD	POINTED PECIE	TER TOR ADDR	ECC AT
028 FA			V A.R2					
029 430F			L A, #OFH					
OZB AA								
O2C FA	148	SCANMX: MO	V R2, A V A, R2	SCAN	ROW SELECT	TO ACCUMULATOR		
02D 3A	149	OU	TL P2, A	OUTPU	T SCAN ROW	SELECT TO PORT	2	
OZE BBOF	150	MO	V R3, #SCAN	TM SET D	ELAY FOR OU	TPUT SCAN TIME		
030 EB30	- 20A 151	DELAY2: DJ	NZ R3, #SCAN	2 DELAY				
032 09	152	18 STROIN	T A. P1	BURANT : INPUT	COLUMN STA	TUS FROM PORT	1 TO ACCUMUL	ATOR
033 20	153	XC	H A, @RO	STORE	NEW COLUMN	STATUS SAVE DE	LD IN ACCUMU	LATOR
074 00	154	XR	L A, @RO	COMPA	RE OLD WITH	NEW COLUMN ST	ATUS	
7034 DO			1/ D7 A	CAUE	COMPARE DECI	III T THE COMPARE	DECTED	
0034 D0 0035 AF	155	HU	V R/, A	, SAVE	CUMPARE RES	OLI IN CUMPARE	KEGISTER	
0035 AF 0036 C669	156 157	JZ	L A, eRO V R7, A CHFFUL	; IF TH	E SAME, CHE	CK IF FIFO IS	FULL	

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15-11 MCS-	48/UP1-41 MA	ACRO ASSEMBLER, V3. 0	PAGE 5 0 EV M				
_OC OBJ	LINE	SOURCE STATEMENT	E STATEMENT		BHILL	VED	203
	159	; *******	*************	******	*******		
	160				105		
	161		RD ENCODING				
	162	1					
	163	THE FOLLOWING CODE IS THE CHAN	GE WORD ENCODING SEC	TION THIS			
		SECTION IS ONLY EXECUTED IF A					
		IS SET AND DECREMENTED TO DESI					
		REGISTER IS LOOKED AT ONE BIT					
		THE CHANGE(S). WHEN A CHANGE					
		COORDINATE FOR ITS LOCATION.					
		IN THE ROW SCAN SELECT REGISTE					
		OF THAT SENSOR IS ESTABLISHED					
		THE MATRIX MAP. THIS STATUS I					
		THE CHANGE WORD. THE CHANGE W				ER.	
	173				815		
	174	; ******************	****		*****		
	175						
038 BB08	176	ADDM AMOV STREET NORTH THE	SET COLUMN COUNTER	REGISTER TO	818		0032
ОЗА СВ		RRLOOK: DEC R3				PA	
03B F0	178	MOV A, CRO	COLUMN STATUS TO A	CCUMULATOR	715	33	0004
03C 77	179	LOAD FIFD AT ALFO INTA ADDRESS	ROTATE COLUMN STAT	USRIGHT		IA	6800
O3D AO	180	MOV PRO PRO A TIE	ROTATED COLUMN STA	TUS BACK TO	MATRIX MAP	0165	±500
O3E FF	181	MOV A A R7 OT STIRM	COMPARE REGISTER V	ALUE TO ACCU	MULATOR	9.0	
03F 77	182		ROTATE COMPARE VAL.	UE RIGHT		OSAG	2000
040 AF	183	MOV R7, A MADE WORL	ROTATED COMPARE VA	LUE TO COMPA	RE REGISTER	AR	60058
041 F245	184	JB7 ENCODE AL SVAS	TEST BIT 7 IF CHAN	GE DETECTED	ENCODE CHANG	E WORD	
043 0469	185	JMP CHFFUL MADE HOR	; IF NO CHANGE IS DE	TECTED CHECK	FOR FIFO FU	LL AA	
045 FA	186	ENCODE: MOV A. R2	SCAN ROW SELECT TO	ACCUMULATOR	0000XXXX	2025	
046 530F	187	ANL ANHOFH	ROTATE ONLY SCAN V	ALUE		90	
048 E7	188	IN THE SHAP TEND TENAP THE BE.	ROTATE LEFT		OOOXXXXO	0567	
049 E7	189	NEXT FIED INPAT ADDRESS	ROTATE LEFT		OOXXXXOO		6900
04A E7	190	CHECK FIFT FUA		AMP	OXXXXOOO		0600
04B 4B	191	ORL A.R3	ESTABLISH MATRIX C	OORDINANT	OXXXXXXX	8008	0067
	192	FIFE IMPUT ADDRESS TO ACCUMULAT	; (OR) COLUMN COUNTE	R VALUE WITH	ACCUMULATOR	FC	6900
O4C AE	193	DALE TO MOV HTI ROLAMI BRASHOD	SAVE COORDINANT IN	CHANGE WORD	REGISTER		A400
04D F0	194	MOV A A CRO	COLUMN STATUS FROM	MATRIX MAP	TO ACCUMULAT		
04E 5380	195	ANL A #80H	O ALL BITS BUT BIT	PROBET LONG			
050 4E		ADTA JUNU ORL OT BARGA POT DELE					
051 AE	197	COMPANE TO A 69 BUT EVOM IFO ADD	SAVE CHANGE WORD		XXXXXXXX		
		IF THE SAME RESET FIFO BUTFUL R					
	199	SEJECT RESPROGA TURTUD OFFT TXBM			240		
						64.90	
			R5.WFIFORA	RSFFDT: MOV			
		CHANGE WORD TO ACCUMULATOR			CAS		B700
		CHANGE WORD TO DEBOUT			6AS		
		COLUMN COUNTER TO ACCUMULATOR					
		IF NOT D FINISH CHANGE WORD END				AEAP	
		FIFD BOTTOM ADDRESS TO ACCUMULA	A WEIFORA			8005	

A88210-W38

PAGE 6 0 EV ASSEMBLER, VG C 6 SPA ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 SOURCE STATEMENT 201 ; FIFO-DBBOUT MANAGEMENT 203 204 THE FOLLOWING CODE IS THE FIFO-DBBOUT MANAGEMENT SECTION OF THE 204; THE FOLLOWING CODE IS THE FIFO-DBBOUT MANAGEMENT SECTION OF THE
205; PROGRAM THIS SECTION TAKES AN ENCODED CHANGE WORD AND LOADS IT INTO
206; THE FIFO. THE FIFO NOT EMPTY INTERRUPT IS THEN SET AND THE FIFO-IN
207; PDINTER GETS UPDATED. A FIFO FULL CONDITION IS THEN CHECKED FOR AND
208; ROUTED ACCORDINGLY. IF BOTH THE FIFO AND OBE HAVE CHANGE WORDS THE
209; PROGRAM LOCKS UP UNTIL THIS HAS CHANGED. IF THE FIFO ISNT FULL COLUMN
210; COUNTER= 0, FIFO EMPTY AND OBE CONDITIONS ARE CHECKED. THE FIFO-OUT
211; PDINTER IS SET AND DBBOUT IS LOADED IF THE FIFO ISNT EMPTY AND OBE ISNT
212; SET. IF THIS ISNT THE SITUATION, PROGRAM FLOW IS ROUTED BACK TO THE 213 THE SCAN AND COMPARE SECTION TO SCAN THE NEXT ROW. 214 : 216 217 LOADFF: MOV A, R4 ;FIFO INPUT ADDRESS TO ACCUMULATOR 0052 FC A,R4 ;FIFO INPUT ADDRESS ID ACCUMULATUR
R1.A ;FIFO POINTER USED FOR INPUT
A,R6 ;CHANGE WORD TO ACCUMULATOR
RR1.A ;LOAD FIFO AT FIFO INPUT ADDRESS
A,#10H 3 ;BIT 4 FOR FIFO NOT EMPTY
STS.A ;WRITE TO STATUS REGISTER, FIFO NOT EMPTY MOV 0053 A9 218 0054 FE 219 0055 A1 220 MOV. 221 STATNE: MOV A, #10H ;BIT 4 FUN FIFO SEGISTER, FIFO NOT EMPTY P2.#20H ;FIFO NOT EMPTY INTERRUPT PORT 2-5 HIGH A, R2 ;ROM SCAN SELECT TO ACCUMULATOR A.#20H ;SAVE INTERRUPT, NO CHANGE TO SCAN VALUE R2.A ;ROW SCAN SELECT REGISTER A, #FIFOTA ;FIFO TOP ADDRESS TO ACCUMULATOR A, R4 ;COMPARE WITH CURRENT FIFO INPUT ADDRESS A, R4 ;COMPARE WITH CURRENT FIFO INPUT ADDRESS TO THE SAME RESET FIFO INPUT REGISTER 0056 2310 222 0058 90 MOV 223 INTRHI: ORL 005E FA 224 005C 4320 224 005E AA 226 005E AA 226 005E 232F 227 ADJEIN 0061 DC 0059 BA20 MOV ORL MOV 227 ADJFIN MOV XRL 0/22/229 0062 0667 JZ R4 CHFFUL R4, #FIFOBA NEXT FIFO INPUT ADDRESS 0064 10 230 TNC , NEXT FIRD INPUT ADDRESS
, CHECK FIFO FULL
, RESET FIFO INPUT REGISTER, BOTTOM OF FIFO
, FIFO INPUT ADDRESS TO ACCUMULATOR
, COMPARE INPUT WITH OUTPUT FIFO ADDRESS 0065 0469 000XX 231 JMP 0067 BC08 232 RSFFIN: MOV A, R4 1000 3VAB 0069 FC POTALUS 233 CHFFUL: MOV 006A DD 234 XRL CHCNTR CHOBF1 ; IF NOT SAME CHECK COLUMN COUNTER VALUE
; IF OBF IS 1 THEN CHECK OBF
; FIFO TOP ADDRESS TO ACCUMULATOR
; COMPARE TOP TO OUTPUT FIFO ADDRESS
; IF THE SAME RESET FIFO OUTPUT REGISTER 006B 967D TALKING 235 JNZ 006D 866D 236 CHORE 1 JOBE 006F 232F A, #FIFOTA 237 ADJFOT: MOV 0071 DD 238 A. R5 DIAHO BYAR XRL 0072 C677 239 .17 RSFFOT NEXT FIFO OUTPUT ADDRESS 0074 1D 240 INC R5 0075 0479 241 JMP LOADDB LOAD DBBOUT 242 RSFFOT: MOV R5, #FIFOBA RESET FIFO OUTPUT ADDRESS TO BOTTOM OF FIFO 0077 BD08 OUTPUT FIFO ADDRESS TO ACCUMULATOR 0079 FD 243 LOADDB: MOV A, R5 R1, A 007A A9 244 FIFO POINTER USED FOR OUTPUT 007B F1 245 MOV A. @R1 CHANGE WORD TO ACCUMULATOR DBB, A A, R3 CHANGE WORD TO DBBOUT 007C 02 246 DUT 007D FB 247 CHCNTR: MOV COLUMN COUNTER TO ACCUMULATOR ; IF NOT O FINISH CHANGE WORD ENCODING ; FIFO BOTTOM ADDRESS TO ACCUMULATOR 007E 963A 248 JNZ RRLOOK 249 CHFFEM: MOV A. #FIFOBA 0080 2308 250

251 SEJECT

0085 DC	252	XRL	A, R4 COMPARE FIFO INPUT ADDRESS WITH FIFO BOTTOM ADD
0083 C68C	253	JZ	ADJEM IF THE SAME, ADJUST TO CHECK FOR FIFO EMPTY
0085 FC	254	MOV	A.R4 ; FIFO INPUT ADDRESS TO ACCUMULATOR
0086 07	255	DEC	A DECREMENT FIFO INPUT ADDRESS IN ACCUMULATOR
0087 DD	256	XRL	A.R5 COMPARE INPUT TO OUTPUT FIFO ADDRESSES
0088 C691	257	JZ	STATMT ; IF SAME, WRITE STATUS REGISTER FOR FIFO EMPTY
008A 049C	258	JMP	CHOBF2 CHECK OBF
00BC 232F	259 ADJFEM	MOV	A, #FIFOTA : FIFO TOP ADDRESS TO ACCUMULATOR
OOBE DD	260	XRL	A.R5 ; COMPARE TOP TO OUTPUT FIFO ADDRESS
008F 969C	261	JNZ	CHOBF2 : IF NOT SAME THEN FIFO IS NOT EMPTY, CHECK OBF
0091 2300	262 STATMT	MOV	A, #OOH ; CLEAR BIT O FOR FIFO EMPTY
0093 90	263	MOV	STS, A ; WRITE TO STATUS REGISTER
0094 9ADF	264 INTRLO	ANL	P2, #ODFH ; FIFO EMPTY, INTERRUPT PORT 2-5 LOW
0096 FA	265	MOV	A, R2 ; SCAN ROW SELECT TO ACCUMULATOR
0097 53DF	266	ANL	A, #ODEH SAVE INTERRUPT, NO CHANGE TO SCAN VALUE
0099 AA	267	MOV	R2, A ; SCAN ROW SELECT REGISTER
009A 041D	268	JMP	ADJREG MADDUST REGISTERS
009C 861D	269 CHOBF2:	JOBF	ADJREG : IF OBF=1 THEN ADJUST REGISTERS
009E 046F	270	JMP	ADJFOT ADJUST FIFO OUT ADDRESS TO LOAD DBBOUT
	271		Rewind Operation
	272	END	Abort Operation
SER SYMBOLS			
DJFEM 008C	ADJFIN 005F	ADJFOT OO	6F ADJREG 001D CHCNTR 007D CHFFEM 0080 CHFFUL 0069 CHDBF1 006
HDBF2 009C		ENCODE OO	
NTRLO 0094		LOADFF 00	
CANMX 002C		STATMT OO	

ASSEMBLY COMPLETE, NO ERRORS

An 8741A/8041A Digital Cassette Controller	Contents		NCS-48/UPI-41 NA	0.40
TFO IMPUT ADDRESS WITH PIFO BOTTOM ADD	STANDARD ON COO MINI DEK	igy		2-47
T ADDRESS TO ACCUMULATOR FIFD IMPUT ADDRESS IN ACCUMULATOR	RECORDING FORMAT	VOM 230	254	2-47
NPUT TO DUTPUT FIFD ADDRESSES INTE STATUS REGISTER FOR FIFD EMPTY	STATMI . IF SAME !	JRX 5t.	0 255 691 257 490 256	
ADDRESS TO ACCUMULATOR	THE UPI-41A™ CONTRO	LLER HERODA	965 356	
WHE THEN FIFO IS NOT EMPTY, CHECK ORF TO FOR FIFO EMPTY	THE HARDWARE INTER		74S 098 S4S 000	2-50
TATUS REGISTER  T. INTERRUPT PORT 2-3 LOW SELECT TO ACCUMULATOR	THE CONTROLLER SOF	TWARE	0 263 ADF 264 A 263	
TRRUPT, NO CHANGE TO SCAN VALUE SELECT REGISTER	Write Command	ANL	38F 266 A 267	2-54
PLESTERS THEN ADDRESS TO LOAD DRBOUT	Skin Operation	OHOBEZ JOBE GHOBEZ JOBE JML	41D 256 61D 259 66F 270	2.50
	Rewind Operation Abort Operation	аиз		2-60 2-60
COURT CHEEN CORD CHEEN, CORS CHORES		775 M	BOLS OBC ABJEIN OC	MYE REEL
DOOR FILLMY COOD INTTMY COOD INTRMI	COO CREINT GOOS RELOCK	OF ENCODE  77 LOADEF  OF STAIM	DPC DELAY2 DC	0 52-60

#### INTRODUCTION

The microcomputer system designer requiring a low-cost, non-volatile storage medium has a difficult choice. His options have been either relatively expensive, as with floppy discs and bubble memories, or non-transportable, like battery backed-up RAMs. The full-sized digital cassette option was open but many times it too was too expensive for the application. Filling this void of low-cost storage is the recently developed digital mini-cassette. These mini-cassettes are similar to, but not compatible with, dictation cassettes. The mini-cassette transports are inexpensive (well under \$100 in quantity), small (less than 25 cu. in.), low-power (one watt), and their storage capacity is a respectable 200K bytes of unformatted data on a 100-foot tape. These characteristics make the mini-cassette perfect for applications ranging from remote datalogging to program storage for hobbyist systems.

The only problem associated with mini-cassette drives is controlling them. While these drives are relatively easy to interface to a microcomputer system, via a parallel I/O port, they can quickly overburden a CPU if other concurrent or critical real-time I/O is required. The cleanest and probably

the least expensive solution in terms of development cost is to use a dedicated single-chip controller. However, a quick search through the literature turns up no controllers compatible with these new transports. What to do? Enter the UPI-41A family of Universal Peripheral Interfaces.

The UPI-41A family is a group of two user-programmable slave microcomputers plus a companion I/O expander. The 8741A is the "flag-chip" of the line. It is a complete microcomputer with 1024 bytes of EPROM program memory, 64 bytes of RAM data memory, 16 individually programmable I/O lines, an 8-bit event counter and timer, and a complete slave peripheral interface with two interrupts and Direct Memory Access (DMA) control. The 8041A is the masked ROM, pin compatible version of the 8741A. Figure 2 shows a block diagram common to both parts. The 8243 I/O port expander completes the family. Each 8243 provides 16 programmable I/O lines.

Using the UPI concept, the designer can develop a custom peripheral control processor for his particular I/O problem. The designer simply develops his peripheral control algorithm using the UPI-41A assembly language and programs the EPROM of



Figure 1. Comparison of Mini-Cassette and Floppy Disk Transports and Media.

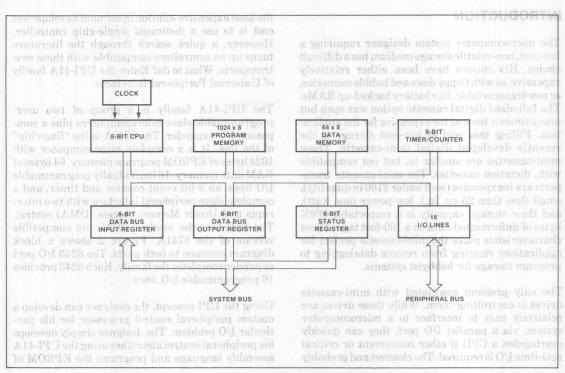


Figure 2. 8741A/8041A Block Diagram

the 8741A. Voila! He has a single-chip dedicated controller. Testing may be accomplished using either an ICE-41A or the Single-step mode of the 8741A. UPI-41A peripheral interfaces are being used to control printers, keyboards, displays, custom serial interfaces, and data encryption units. Of course, the UPI family is perfect for developing a dedicated controller for digital mini-cassette transports. To illustrate this application for the UPI family let's consider the job of controlling the Braemar CM-600 Mini-Dek®.

#### THE CM-600 MINI-DEK®

The Braemar CM-600 is representative of digital mini-cassette transports. It is a single-head, singlemotor transport which operates entirely from a single 5-volt power supply. Its power requirements, including the motor, are 200ma for read or write and 700ma for rewind. Tapes speeds are 3 inches per second (IPS) during read or write, 5 IPS fast forward, and 15 IPS rewind. With these speeds and a maximum recording density of 800 bits per inch (BPI), the maximum data rate is 2400 bits per second (BAUD). The data capacity using both sides the transport occupies only 22.5 cubic inches (3"x3"x2.5").

All I/O for the CM-600 is TTL-compatible and can be divided into three groups: motor control, data control, and cassette status. The motor group controls are GO/STOP, FAST/SLOW, and FORWARD/ REVERSE. The data controls are READ/WRITE, DATA IN, and DATA OUT. The remaining group of outputs give the transport's status: CLEAR LEADER, CASSETTE PRESENCE, FILE PRO-TECT, and SIDE SENSOR. These signals, shown schematically in figure 3 and table 1, give the pin definition of the CM-600 16-pin I/O connector.

#### RECORDING FORMAT

The CM-600 does not provide either encoding or decoding of the recorded data; that task is left for the peripheral interface. A multitude of encoding techniques from which the user may choose are available. In this single-chip dedicated controller application, a "self-clocking" phase encoding scheme similar to that used in floppy discs was chosen. This scheme specifies that a logic "0" is a bit cell with no of a 100-foot tape is 200K bytes. On top of this, transition; a cell with a transition is a logic "1."

		ADDI
Pin	1/0	Function
1	_	Index pin—not used
2	_	Signal ground
2 3	0	Cassette side (0—side B, 1—side A)
4 5	I	Data input (0—space, 1—mark)
5	0	Cassette presence (0—cassette, 1—no cassette)
6	I	Read/Write (0—read, 1—write)
7	0	File protect (0—tab present, 1—tab removed)
8		+5v motor power
9		Power ground
10	_	Chassis ground
11	I	Direction (0—forward, 1—rewind)
12	I	Speed (0-fast, 1-slow)
13	0	Data output (0—space, 1—mark)
14	0	Clear leader (0—clear leader, 1—off
15 16	appror	clear leader) Motion (0—go, 1—stop) +5v logic power

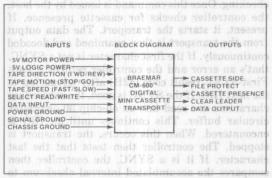


Figure 3. Braemar CM-600™ Block Diagram

Figure 4 illustrates the encoding of the character 3AH assuming the previous data ended with the data line high. (The least significant bit is sent first.) Notice that there is always a "clocking" transition at the beginning of each cell. Decoding is simply a matter of triggering on this "clocking" transition, waiting 3/4 of a bit cell time, and determining whether a mid-cell transition has occurred. Cells with no mid-cell transitions are data 0's; cells with transitions are data 1's. This encoding technique has all the benefits of Manchester encoding with the added advantage that the encoded data may be "decoded by eyeball:" long cells are always 0's, short cells are always 1's.

Besides the encoding scheme, the data format is also up to the user. This controller uses a variable byte length, checksum protected block format. Every block starts and ends with a SYNC character

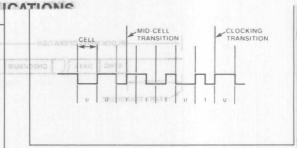


Figure 4. Modified Phase Encoding of Character 3A Hex

(AAH), and the character immediately preceeding the last SYNC is the checksum. The checksum is capable of catching 2 bit errors. The number of data characters within a block is limited to 64K bytes. Blocks are separated by an Inter-Record Gap (IRG). The IRG is of such a length that the transport can stop and start within an IRG, as illustrated in the data block timing, figure 5. Braemar specifies a maximum start or stop time of 150ms for the transport, thus the controller uses 450ms for the IRG. This gives plenty of margin for controlling the transport and also for detecting IRGs while skipping blocks.

#### THE UPI-41A CONTROLLER

The goal of the UPI software design for this application was to make the UPI-41A microcomputer into an intelligent cassette control processor. The host processor (8086, 8088, 8085A, etc.) simply issues a high-level command such as READ-a-block or WRITE-a-block. The 8741A accepts the command, performs the requested operation, and returns to the host system a result code telling the outcome of the operation, eg. Good-Completion, Sync Error, etc. Table 2 shows the command and result code repertoire. The 8741A completely manages all the data transfers for reading and writing.

As an example, consider the WRITE-a-block command. When this command is issued, the UPI-41A expects a 16-bit number from the host telling how many data bytes to write (up to 64K bytes per block). Once this number is supplied in the form of two bytes, the host is free to perform other tasks; a bit in the UPI's STATUS register or an interrupt output will notify the host when a data transfer is required. The 8741A then checks the transport's status to be sure that a cassette is present and not file protected. If either is false, a result code is

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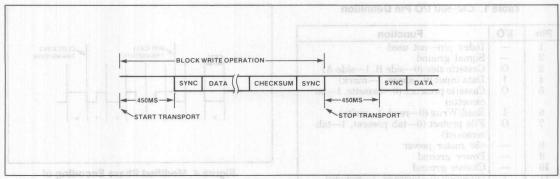


Figure 5. IRG/Block Timing Diagram (not to scale)

Table 2. Controller Command/Result Code Set

Command	Result no goni datas to alded
Read (01H)	Bad Synch1 Error (42H) Bad Synch2 Error (43H)
Rewind (04H)	Good-Completion (00H)
Skip (03H)	Good-Completion (00H) End of Tape Error (47H) Beginning of Tape Error (48H)
Write (02H)	Good-Completion (00H) Buffer Underrun Error (81H) Command Error (82H) End of Tape Error (83H)

returned to the host; otherwise the transport is started. After the peripheral controller checks to make sure that the tape is off the clear leader and past the hole in the tape, it writes a 450ms IRG, a SYNC character, the block of data, the checksum, and the final SYNC character. (The tape has a clear leader at both ends and a small hole 6 inches from the end of each leader.) The data transfers from the host to the UPI-41A slave microcomputer are double buffered. The controller requests only the desired number of data bytes by keeping track of the count internally.

If nothing unusual happened, such as finding clear leader while writing, it returns a Good-Completion result code to the host. If clear leader was encountered, the transport is stopped immediately and an End-of-Tape result code is returned to the host. Another possible error would be if the host is late in supplying data. If this occurs, the controller writes

an IRG, stops the drive, and returns the appropriate Data-Underrun result code.

The READ-a-block command also provides error checking. Once this command is issued by the host, the controller checks for cassette presence. If present, it starts the transport. The data output from the transport is then examined and decoded continuously. If the first character is not a SYNC, that's an error and the controller returns a Bad-First-SYNC result code (42H) after advancing to the next IRG. If the SYNC is good, the succeeding characters are read into an on-chip 30 character circular buffer. This continues until an IRG is encountered. When this occurs, the transport is stopped. The controller then tests that the last character. If it is a SYNC, the controller then compares the accumulated internal checksum to the block's checksum, the second to the last character of the block. If they match, a Good-Completion result code (00H) is returned to the host. If either test is bad, the appropriate error result code is returned. The READ command also checks for the End-of-Tape (EOT) clear leader and returns the appropriate error result code if it is found before the read operation is complete. This gold and its not transmit

The 30 character circular buffer allows the host up to 30 character times of response time before the host must collect the data. All data transfers take place thru the UPI-41A Data Bus Buffer Output register (DBBOUT). The controller continually monitors the status of this register and moves characters from the circular buffer to the register whenever it is empty.

The SKIP-n-blocks command allows the host to skip the transport forward or backward up to 127 blocks. Once the command is issued, the controller expects one data byte specifying the number of

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blocks to skip. The most significant bit of this byte selects the direction of the skip (0=forward, 1=reverse). SKIP is a dual-speed operation in the forward direction. If the number of blocks to skip is greater than 8, the controller uses fast-forward (5 IPS) until it is within 8 blocks of the desired location. Once within 8 blocks, the controller switches to the normal read speed (3 IPS) to allow accurate placement of the tape. The reverse skip uses only the rewind speed (15 IPS). Like the READ and WRITE commands, SKIP also checks for EOT and beginning-of-tape (BOT) depending upon the tape's direction. An error result code is returned if either is encountered before the number of blocks skipped is complete.

The REWIND command simply rewinds the tape to the BOT clear leader. The ABORT command allows the termination of any operation in progress, except a REWIND. All commands, including ABORT, always leave the tape positioned on an IRG.

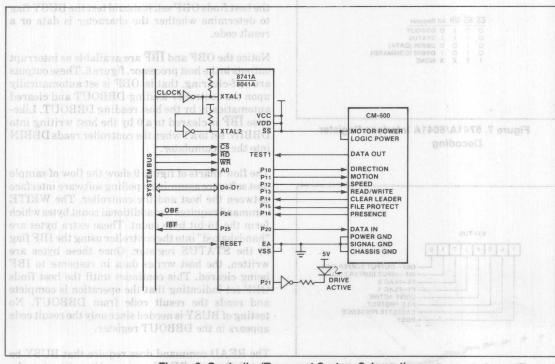
# THE HARDWARE INTERFACE IS A MILE OF THE MILE OF THE HARDWARE INTERFACE IS A MILE OF THE MILE OF THE MI

There's hardly any hardware design effort required for the controller and transport interface in figure 6. Since the CM-600 is TTL compatible, it connects

directly to the I/O ports of the UPI controller. If the two are separated (i.e. on different PC cards), it is recommended that TTL buffers be provided.) The only external circuitry needed is an LED driver for the DRIVE ACTIVE status indicator.

The 8741A-to-host interface is equally straightforward. It has a standard asynchronous peripheral interface: 8 data lines ( $D_0$ - $D_7$ ), read (RD), write (WR), register select (AO), and chip select (CS). Thus it connects directly to an 8086, 8088, 8085A, 8080, or 8048 bus structure. Two interrupt outputs are provided for data transfer requests if the particular system is interrupt-driven. DMA transfer capability is also available. The clock input can be driven from a crystal directly or with the system clock (6MHz max). The UPI-41A clock may be asynchronous with respect to other clocks within the system.

This application was developed on an Intel iSBC 80/30 single board computer. The iSBC 80/30 is controlled by an 8085A microprocessor, contains 16K bytes of dual-ported dynamic RAM and up to 8K bytes of either EPROM or ROM. Its I/O complement consists of an 8255A Programmable Parallel Interface, an 8251A Programmable Communica-



onti affilia de la communitation (Figure 6. Controller/Transport System Schematic along Reliant Bennit

tions Interface, an 8253 Programmable Interval Timer, and an 8259A Programmable Interrupt Controller. The iSBC 80/30 is especially convenient for UPI development since it contains an uncommitted socket dedicated to either an 8041A or 8741A, complete with buffering for its I/O ports. The iSBC 80/30 to 8741A interface is reflected in figure 8. (Optionally, an iSBC 569 Digital Controller board could be used. The iSBC 569 board contains three uncommitted UPI sockets with an interface similar to that in figure 8.)

Looking at the host-to-controller interface, the host sees the 8741A as three registers in the host's I/O address space: the data register, the command register, and the status register. The decoding of these registers is shown in figure 7. All data and commands for the controller are written into the Data Bus Buffer Input register (DBBIN). The state of the register select input. AO, determines whether a command or data is written. (Writes with AO set to 1 are commands by convention.) All data and results from the controller are read by the host from the Data Bus Buffer Output register (DBBOUT).

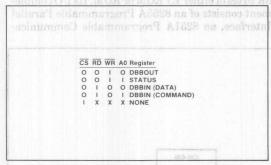
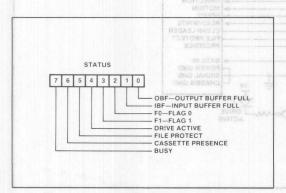


Figure 7. 8741A/8041A Interface Register Decoding



The Status register contains flags which give the host the status of various operations within the controller. Its format is given in figure 8. The Input Buffer Full (IBF) and Output Buffer Full (OBF) flags show the Status of the DBBIN and DBBOUT registers respectively. IBF indicates when the DBBIN register contains data written by the host. The host may write to DBBIN only when IBF is 0. Likewise, the host may read DBBOUT only when OBF is set to a 1. These bits are handled automatically by the UPI-41A internal hardware. FLAG 0 (F<sub>0</sub>) and FLAG 1 (F<sub>1</sub>) are general purpose flags used internally by the controller which have no meaning externally, a groted because one at realities

The remaining four bits are user-definable. For this application they are DRIVE ACTIVE, FILE PRO-TECT, CASSETTE PRESENCE, and BUSY flags. The FILE PROTECT and CASSETTE PRESENCE flags reflect the state of the corresponding I/O lines from the transport. DRIVE ACTIVE is set whenever the transport motor is on and the controller is performing an operation. The BUSY flag indicates whether the contents of the DBBOUT register is data or a result code. The BUSY flag is set whenever a command is issued by the host and accepted by the controller. As long as BUSY is set, any character found in DBBOUT is a result code. Thus whenever the host finds OBF set, it should test the BUSY flag to determine whether the character is data or a result code.

Notice the OBF and IBF are available as interrupt outputs to the host processor, figure 6. These outputs are self-clearing, that is, OBF is set automatically upon the controller loading DBBOUT and cleared automatically by the host reading DBBOUT, Likewise IBF is cleared to a 0 by the host writing into DBBIN: set to a 1 when the controller reads DBBIN into the accumulator.

The flow charts of figure 9 show the flow of sample host software assuming a polling software interface between the host and the controller. The WRITE command requires two additional count bytes which form the 16-bit byte count. These extra bytes are "handshaked" into the controller using the IBF flag in the STATUS register. Once these bytes are written, the host writes data in response to IBF being cleared. This continues until the host finds OBF set indicating that the operation is complete and reads the result code from DBBOUT. No testing of BUSY is needed since only the result code appears in the DBBOUT register.

The READ command does require that BUSY be Figure 8. Status Register Bit Definition tested. Once the READ command is written into the

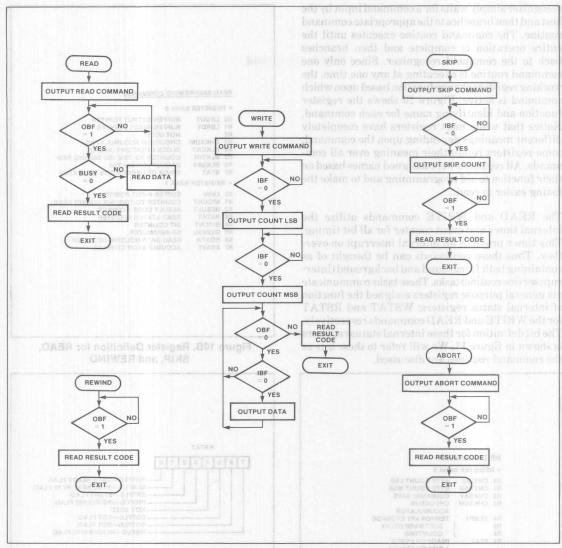


Figure 9. Host CPU Flow Charts for Commands When Polling is Used

controller, the host must test BUSY whenever OBF is set to determine whether the contents of DBBOUT is data from the tape or the result code.

The SKIP command requires the skip count byte. This byte is written into DBBIN after IBF has been cleared following the command. The host then waits until OBF is set indicating the operation is complete and the result code is waiting in DBBOUT. The REWIND and ABORT commands only require that the host test OBF. Once set, the result code is ready in DBBOUT.

The flow charts for an interrupt-driven system are simplified since no testing of OBF or IBF is required. The mere fact that an interrupt occurred implies that the corresponding bit in the STATUS REGISTER is set or cleared.

#### THE CONTROLLER SOFTWARE

The internal UPI-41A software can be divided roughly into the various commands. (This software is discussed as flow charts. The actual program listing is included in Appendix A.) A command

recognizer simply waits for a command input by the host and then branches to the appropriate command routine. The command routine executes until the entire operation is complete and then branches back to the command recognizer. Since only one command routine is executing at any one time, the working registers change function based upon which command is active. Figure 10 shows the register function and identifying name for each command. Notice that while most registers have completely different meanings depending upon the command, some registers retain their meaning over all commands. All registers were assigned names based on their function to aid programming and to make the listing easier to read.

The READ and WRITE commands utilize the internal timer and event counter for all bit timing. This timer provides an internal interrupt on overflow. Thus these commands can be thought of as containing both foreground and background (interrupt service routine) tasks. These tasks communicate via general purpose registers assigned the function of internal status registers: WSTAT and RSTAT for the WRITE and READ commands respectively. The bit definition for these internal status registers is shown in figure 11. We will refer to these bits as the command routines are discussed.

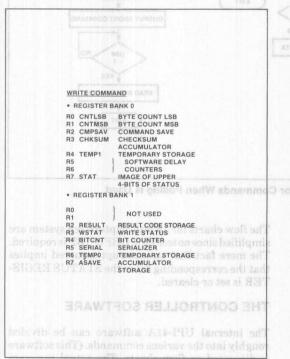


Figure 10A. Register Definition for WRITE

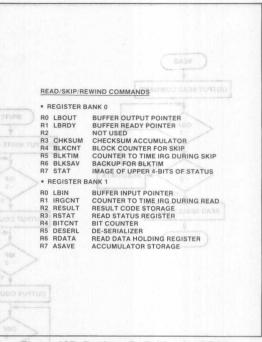


Figure 10B. Register Definition for READ, SKIP, and REWIND

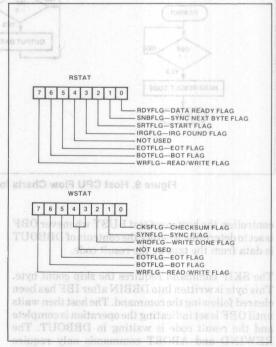


Figure 11. READ and WRITE Internal Status Register Bit Definitions

#### WRITE COMMAND

Let's look at the WRITE command routine first, figure 12. As was mentioned earlier, the WRITE requires two additional data bytes before it can be processed. Once the command recognizer branches to the WRITE routine, the routine waits on IBF until these bytes are written by the host. These count bytes are stored in the CNTLSB and CNTMSB (Count Least and Most Significant Byte) registers. These two registers are concatenated to form the 16-bit byte count. At this point, the routine tests the

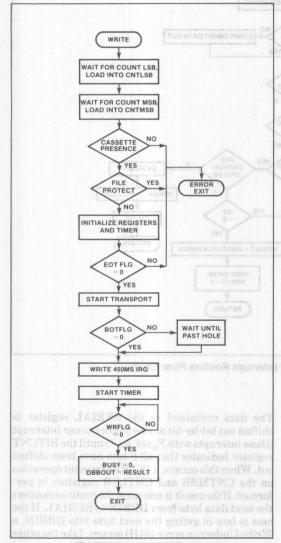
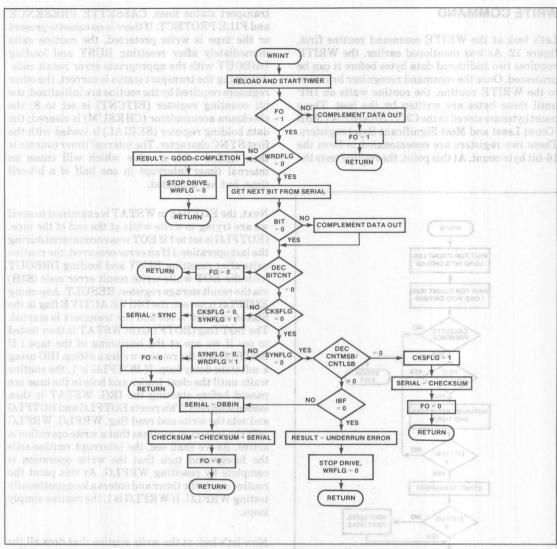


Figure 12. WRITE Command Flow Chart

transport status lines, CASSETTE PRESENCE and FILE PROTECT. If there is no cassette present or the tape is write protected, the routine exits immediately after resetting BUSY and loading DBBOUT with the appropriate error result code Assuming the transport status is correct, the other registers required by the routine are initialized: the bit counting register (BITCNT) is set to 8; the checksum accumulator (CHKSUM) is cleared; the data holding register (SERIAL) is loaded with the first SYNC character. The internal timer counter is then loaded with a value which will cause an internal timer interrupt in one half of a bit-cell time, but not activated.

Next, the EOT flag in WSTAT is examined to see if we are trying to write while at the end of the tape. (EOTFLG is set to 1 if EOT was encountered during the last operation.) If an error occurred, the routine exits after resetting BUSY and loading DBBOUT with the EOT-while-write result error code (83H) via the result storage register, RESULT. Assuming EOTFLG is not set, the DRIVE ACTIVE flag in the Status register is set and the transport is started. The BOT flag (BOTFLG) in WSTAT is then tested to see if we are at the beginning of the tape.) If BOTFLG is 0, the routine writes a 450ms IRG using a software delay loop. If BOTFLG is 1, the routine waits until the clear leader and hole in the tape are passed before starting the IRG. WSTAT is then loaded with 80H. This resets EOTFLG and BOTFLG and sets the write and read flag, WRFLG. WRFLG tells the interrupt routines that a write operation is active. As we shall see, the interrupt routine tells the foreground task that the write operation is complete by resetting WRFLG. At this point the routine starts the timer and enters a loop continually testing WRFLG. If WRFLG is 1, the routine simply loops.

Now let's look at the write routine that does all the work: the write timer interrupt service routine. When the timer interrupt occurs half a bit-cell time later, an automatic vector to the INT routine is performed (location 07H in program memory). INT test WRFLG to see whether it's a read or write operation in progress and branches accordingly. Since we are talking about a write operation, the branch is to the WRINT routine, figure 13. WRINT first reloads the timer to provide the timing for the next half cell (the timer continues to run). The Fo is used to define whether this particular interrupt is for the first or the second half of the bit cell. The phase encoding algorithm used specifies that the beginning of a bit must always have a transition. If Fo is reset, the data output to the transport is simply



SHIPPOT SOLVED JOURN Figure 13. WRINT—Write Timer Interrupt Routine Flow Chart

complemented providing the transition. If set, the interrupt is at the mid-cell position. If the data bit is a 1, complement the data output; otherwise, do not change it.  $F_0$  is complemented every interrupt.

The CLEAR LEADER input from the transport is also tested on every interrupt. If it was encountered, the transport is stopped, the EOTFLG in WSTAT is set, WRFLG is reset, and RESULT is loaded with the EOT-while-write error result code (83H). WRINT returns to the main write loop.

The data contained in the SERIAL register is shifted out bit-by-bit at every other timer interrupt (those interupts with  $F_0$  set to a 1) until the BITCNT register indicates that all 8 bits have been shifted out. When this occurs, a 16-bit decrement operation on the CNTMSB and CNTLSB registers is performed. If the result is non-zero, the routine transfers the next data byte from DBBIN to SERIAL. If the host is late in geting the next byte into DBBIN, a Write-Underrun error (81H) occurs. Like the other error conditions, WRFLG in WSTAT is reset and

the Write-Underrun error result code is loaded into the result holding register, RESULT, before returning to the main write loop. If the data is ready in DBBIN, it is transferred to SERIAL and added to the accumulating checksum. The routine then returns to the write main foreground task. (Remember that the foreground task is doing nothing more than testing WRFLG.)

If the decrement result is zero, all data transfers are complete. The accumulated checksum value is loaded into Serial and the Checksum flag, CKSFLG, is set in WSTAT before exiting the interrupt routine. This causes the checksum value to be written onto the tape. Sixteen timer interrupts later the checksum is complete; it is now time to write the final SYNC. CKSFLG is reset, a SYNC character is loaded into SERIAL, and the SYNC flag (SYNFLG), is set in WSTAT. Sixteen more timer interrupts later the SYNC is written to the tape and the block is almost finished. One more interrupt is needed to finish the last bit. The write done flag (WRDFLG) is set to indicate that this is the last interrupt for this block. WRDFLG is detected as being set to a 1 on the next interrupt and the transport is stopped. WRFLG in WSTAT is reset and the Good-Completion result code is loaded into the RESULT register before exiting to the foreground task.

All this occurs while the foreground task is testing WRFLG. When WRFLG is cleared, the foreground task "knows" that the background task is finished: BUSY is reset and the result code stored in RESULT is loaded into DBBOUT. The program then returns to the command recognizer.

#### READ OPERATION

In the case of the read command, figure 14, the RSTAT register provides the communication between the foreground and background tasks. The read command routine starts out by initializing the registers it requires: the checksum accumulator, CHKSUUM, is cleared; pointers for the circular buffer, DBIN, LBRDY, and LBOUT are set to the start of the buffer; and the bit counter, BITCNT, is set to 8.

The circular buffer has three pointers: LBIN to point to the next free buffer location, LBOUT to point to the next location from which to retrieve data, and LDRTDY to trail LBIN by two locations. LBRDY trails LBIN to ensure that the host does not get the received checksum or last SYNC bytes as data. The buffer is empty whenever LDRDY equals LBOUT. The buffer is full whenever LBOUT minus

loading it into the location pointed at by LBIN and then LBIN is incremented. Data is removed from the buffer at the location pointed at by LBOUT and the LBOUT is incrementd by one. The data memory locations 20H thru 3FH form the circular buffer. Any pointer increment or decrement operation limits the pointers to this range. (If a pointer at 3FH is incremented, the result wraps around to 20H.)

Once the registers have been initialized, the timer is loaded, but not started, with a value that corresponds to 3/4 of a bit-cell time. Next, the EOT test is performed on the EOTFLG in RSTAT. The routine exits with an EOT-while-read error result code if an attempt to read is made while at EOT. If not, the transport is started and the BOTFLG is tested to see if it must move past the clear leader and hole. Once past the clear leader and hole, if necessary, the SYNC-Next-Byte flag (SNBFLG), and the Start flag (SRTFLG), are set in RSTAT. SNBFLG informs the software that the next received byte should be a SYNC. SRTFLG prevents LBRDY from being incremented prematurely.

As soon as a transition from mark (1) to space (0) is detected, the timer is started. The routine enters a loop which tests the data ready flag (RDYFLG), the IRG found flag (IRGFLG), and the EOT detected flag (EOTFLG) in RSTAT. These flags are set by the background task to communicate with the foreground. RDYFLG is set when a character has been assembled and is waiting in the holding register, RDATA. IRGFLG is set when an IRG has been found by the background task. EOTFLG has the same meaning as with the write command; the clear leader at the end of the tape has been found.

If none of these flags are set, the foreground then looks at the circular buffer to see if it contains any data to output to the host. The buffer contains data when LBIN does not equal LBOUT. If these pointers are equal, the buffer is empty and the foreground task just continues to loop. If they are not equal, there is some data left in the buffer. OBF is tested to see if DBBOUT is free to accept more data. If it is free, the character pointed at by LBOUT is transfered to DBBOUT and LBOUT is incremented to the next location. If DBBOUT still contains previously loaded data (OBF set), the foreground continues to test the flags in RSTAT.

When the foreground task finds RDYFLG set, data is available in RDATA. Before transfering this data into the buffer, it first compares LBIN and LBOUT. If LBOUT is one less than LBIN, the buffer is full and no more data can be loaded. This is an error 1 equals LBIN. Data is placed in the buffer by condition; the read operation is aborted and the

> 2-56 AFN-01342A

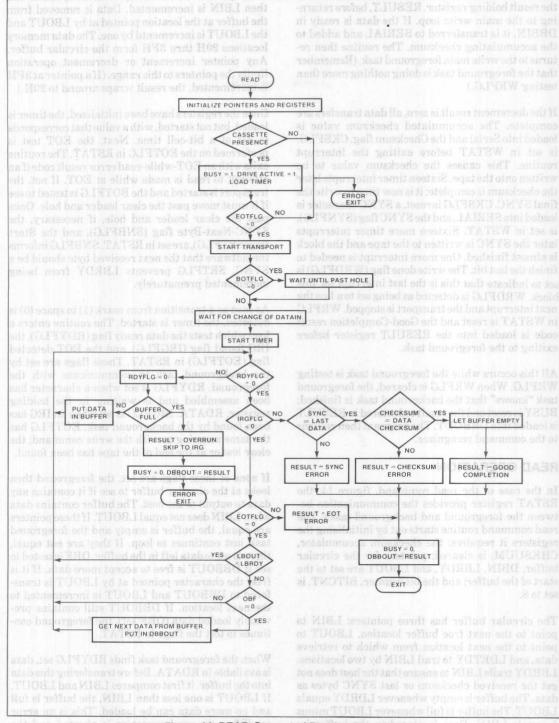


Figure 14. READ Command Routine Flow Chart

transport is moved to the next IRG using the SKIP routine discussed below. Once at the next IRG. BUSY is reset and the Read-Overrun error result. code (41H) is placed in DBBOUT. This terminates the read operation and the routine branches back to the command recognizer. Tol supindost smas adT SKIP command routine. The SKIP command, figure

If the buffer is not full, the data is transfered from RDATA to the location pointed to by LBIN, LBIN is incremented and the RDYFLG in RSTAT is reset. LBRDY is also incremented if LBIN has been incremented twice already. (SRTFLG set prevents LBRDY from being incremented. SRTFLG is reset when LBIN is incremented to the second buffer position.) This ensures that LBRDY will point to the last data byte once an IRG is detected. The data is also added to the accumulated checksum, CHKSUM. The foreground then goes back to test the RSTAT flags. When IRGFLG is found set, the background task has found an IRG and stopped the transport. This indicates that the block read is complete. Since the IRG occurs after the checksum and final SYNC characters, these two bytes are in the circular buffer. To test them the foreground task then decrements LBIN to point at the final SYNC and checks if it is a SYNC character. If not, a Bad-Sync2 error result code (43H) is placed in RESULT and the routine branches to the read exit routine. If it is okay, a SYNC is removed from the accumulated checksum. LBIN is decremented again to point to the received checksum. Since this character is also in the accumulated checksum, it is subtracted out. Now the accumulated checksum reflects only the received data so it is compared with the received checksum. If they are equal, the data is presumed good and a Good-Completion result code (00H) is loaded into result. If not, an error has occured and the RESULT is loaded with the Bad-Checksum result code (44H).

Although the actual read operation is complete with respect to the transport, there may still be data remaining in the buffer of the controller. The read exit routine loops testing LBOUT and LBRDY and transfering data from the buffer into DBBOUT until the buffer is empty. Once the buffer is empty. BUSY is reset and the result code is transferred from RESULT to DBBOUT, completing the read operation.

The timer interrupt routine, RDINT, for the read operation is shown in figure 15. The phase decoding algorithm specifies that the timer start at the beginning transition of the bit cell. It waits for 3/4 of a bit cell before sampling the data input. If the data input is the same as immediately after the beginning transition, the data bit is a 0. If it is different, the same of the Routine Flow Chart

data bit is a 1. The timer interrupt routine compares the present state of the data input to the state immediately following the beginning transition. Fo stores this value and shifts it into the de-serializing register (DESERL), Once 8 bits have been accumulated, the RDYFLG is set to inform the foreground that a character is complete. This character is then transfered from DESERL to the holding register. RDATA

After the interrupt routine has sampled and shifted in the bit, it looks for the beginning transition of the

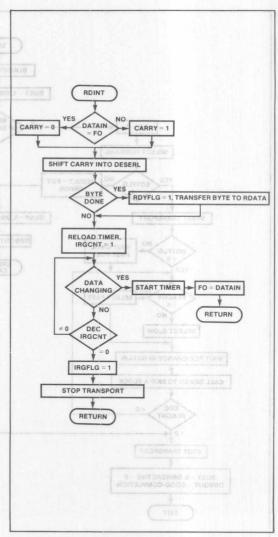


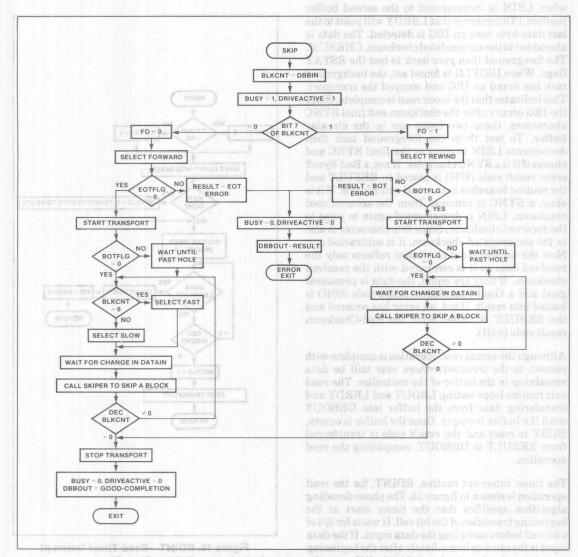
Figure 15. RDINT—Read Timer Interrupt

next bit cell. While looking for this transition, it keeps track of time be decrementing a counter called IRGCNT. If this counter reaches zero, no transition has occured within a certain amount of time (this application used two bit cell times); this is defined as the beginning of an IRG. When an IRG is found, the transport is stopped and the IRGFLG is set in RSTAT before exiting the interrupt service routine. If a transition is found before the counter times out, the routine exits setting  $\mathbf{F}_0$  to the data input state after the transition.  $\mathbf{F}_0$  is used for storing the state while in the foreground. As in the write operation, the CLEAR LEADER input is also

tested every interrupt. If an EOT is found, EOTFLG is set and the transport is stopped.

# SKIP OPERATION (MCI H) handle at (H.14) aboo

The same technique for finding IRGs is used in the SKIP command, figure 16, causes the transport to skip forward or reverse a specified number of IRGs. The number of IRGs to skip is indicated by the byte following the SKIP command byte acceptance (i.e. BUSY has been set and IBF is 0). The SKIP command routine waits, looping on IBF, until the IRG skip count is loaded by



restO wolld and Figure 16. SKIP Command Routine Flow Chart 0 s at the also end, mentioned

APPI ICATIONS

BOI tests are performed to ensure it doesn't skip forward when at EOT or reverse when at BOT. The transport is then started in the direction indicated by bit 7 of the BLKCNT value. (This bit is masked off after the initial direction test.)

For reverse skips, the skipping subroutine, SKIPER, is called. It advances the transport to the next IRG using the IRGCNT technique described above. When SKIPER returns, BLKCNT is decremented and tested for zero. If non-zero, SKIPER is called repeatedly until BLKCNT is zero. Once zero, the transport is stopped and BUSY is reset. DBBOUT is loaded with a Good-Completion result code (00H).

When doing forward skips, the software takes advantage of the fact that the transport can recognize IRGs during fast forward. If the BLKCNT is greater than 8, fast forward is selected instead of slow and SKIPER is called. (The IRGCNT value is modified to take into account the faster tape speed.) When SKIPER returns, BLKCNT is decremented and tested both for being less than 8 or equal to zero. Once BLKCNT is less than 8, the slow speed is selected. Once BLKCNT reaches 0, the operation is terminated like the reverse skips. The transport is stopped and BUSY is cleared. DBBOUT is loaded with a Good-Completion result code.

As with both READ and WRITE commands, the clear leader test is made periodically to ensure that no skips are made past the end or beginning of the tape. The appropriate error result code is issued if CLEAR LEADER is found set. RSTAT is loaded with the appropriate EOTFLG bit set.

#### **REWIND OPERATION**

The REWIND command routine, figure 17, simply sets the transport to fast rewind and loops until clear leader is found for greater than 50ms. (The hole at the ends of the tape is guaranteed not to cause the clear leader input to be active for more than 50ms.) Once the tape's clear leader is found; the transport is stopped; BUSY is reset. A Good-Completion result code is loaded into DBBOUT. Also, since the transport is now at the BOT, the BOTFLG is RSTAT is set.

#### **ABORT OPERATION**

The final command is the ABORT command. It does not have a separate flow chart of its own. All other commands monitor IBF periodically during

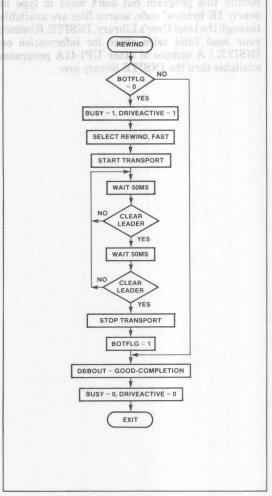


Figure 17. REWIND Command Routine Flow Chart

their execution. If a command is found, the command is compared to the ABORT command code. If it is found, the routine in execution is stopped and BUSY is reset. The Abort-Complete result code is placed in DBBOUT. The aborted routine does ensure that it exits gracefully. An aborted READ or SKIP advances to the next IRG before stopping; WRITE records an IRG before stopping.

#### WRAPPING IT UP

The program listing follows in Appendix A. For more information on the UPI-41A family, see the

Selko printer controller
Olivetti printer controller
LRC printer controller (8295)
Sensor matrix controller
LED display controller
Combination serial/parallel I/O
Programmable keyboard/display controller
GPIB controller (8292)

For reverse skips, the skipping subroutine, SKIPER, is called. It advances the transport to the next IRG using the IRGCNT technique described above. When SKIPER returns, BLKCNT is decremented and tested for zero. If non-zero, SKIPER is called repeatedly until BLKCNT is zero. Once zero, the transport is stopped and BUSY is reset. DBBOUT is loaded with a Good-Completion result code (00H).

When doing forward skips, the software takes advantage of the fact that the transport can recognize IRGs during fast forward. If the BLKCNT is greater than 8, fast forward is selected instead of stoward is selected instead of solve and SKIPER is called. (The IRGCNT value is modified to take into account the faster tape speed.) When SKIPER returns, BLKCNT is decremented and tested both for being less than 8 or equal to zero. Once BLKCNT is less than 8, the slow speed is selected. Once BLKCNT reaches 0, the operation is berminated like the reverse skips. The transport is stopped and BUSY is cleared. DBBOUT is loaded with a Good-Corolletion result code.

As with both READ and WRITE commands, the clear leader test is made periodically to ensure that no slops are made past the end or beginning of the tape. The appropriate error result code is issued if CLEAR LEADER is found set. RSTAT is loaded with the appropriate EOTFLG bit set.

#### REWIND OPERATION

The REWIND command routine, figure 17, simply sets the transport to fast rewind and loops until clear leader is found for greater than 50ms. (The hole at the ends of the tape is guaranteed not to cause the clear leader input to be active for more than 50ms.) Once the tape's clear leader is found; the transport is stopped; BUSY is reset. A Good-Completion result code is loaded into DEBOUT. Also, since the transport is now at the BOT, the BOTFIG is RESTAT is set.

#### MOSTAGRIO TROPA

The final command is the ABORT command. It does not have a separate flow chart of its own. All other commands monitor IBF periodically during

referenced manuals on the cover of this application note. For those readers who would like to use or modify this program but don't want to type in nearly 1K bytes of code, source files are available through the Intel User's Library, INSITE. (Contact your local Intel sales office for information on INSITE.) A sample of other UPI-41A programs available thru the INSITE library are:

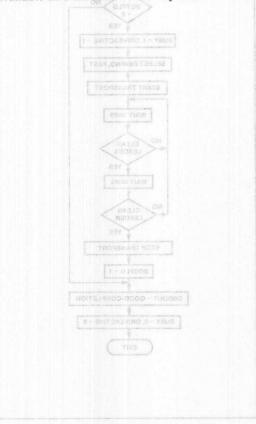


Figure 17. REWIND Command Routine Flow Chart

their execution. If a command is found, the command is compared to the ABORT command code. If it is found, the routine in execution is stopped and BUSY is reset. The Abort-Complete result code is placed in DBBOUT. The aborted routine does ensure that it exits gracefully. An aborted READ or SKIP advances to the next IRG before stopping; WRITE records an IRG before stopping.

#### WEAPPING IT UP

The program listing follows in Appendix A. For more information on the UPI-41A family, see the

ASM48 : F1: DIGCAS. ASM NOOBJECT PRINT(: LP: )

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3 0 DIGITAL CASSETTE CONTROLLER REV 1 0 - 26 MARCH 80

```
LOC OBJ
                         LINE
                                           SOURCE STATEMENT
                                $MACROFILE MOD41A TITLE('DIGITAL CASSETTE CONTROLLER REV 1.0 - 26 MARCH 80')
                                  UPI-41A DIGITAL CASSETTE CONTROLLER FOR THE BRAEMAR CM-600
                                  *****
                                  THIS UPI-41A BASED PROGRAM CONTROLS A BRAEMAR CM-600 MINI-CASSETTE
                            9. THIS UPI-41A BASED PROGRAM CONTROLS A BRAEMAR CM-600 MINI-CASSETTE.

10. THE PROGRAM ALLOWS THE HOST CPU TO SIMPLY ISSUE COMMANDS SPECIFYING

11. READ-A-BLOCK, WRITE-A-BLOCK, SKIP FORWARD OR REVERSE N BLOCKMS.

12. REWIND, AND ABORT THE UPI-41A HANDLES ALL DATA REQUESTS AND MONITORS

13. THE CASSETTE DRIVE FOR ERRORS. EG WRITING TO THE END-0F-TAPE. ETC.

14. EACH COMMAND SETS THE CONTROLLER IN THE BUSY CONDITIONS ONCE THE

15. OPERATION IS COMPLETE, THE UPI-41A RESETS IT'S BUSY FLAG AND LOADS THE

16. OUTPUT DATA BUFFER WITH A RESULT BYTE WHICH INDICATES THE RESULT

17. OF THE REQUESTS OPERATION THE COMMANDS AND RESULT CODES ARE SHOWN

18. IN THE SYSTEMS EQUATES.
                             18 IN THE SYSTEMS EQUATES.
                             20 ; THE CONTROLLER USES A MODIFIED PHASE ENCODING WHERE DATA O'S ARE LONG
                            20 ; HE CUNINCLER OSES A MODIFIED PHASE ENCODING WHERE DATA O'S ARE LUNG
21 ; (FULL BIT TIME) CELLS AND DATA I'S HAVE TRANSITIONS AT THE MID-BIT CELL
22 ; POSITION. WHEN WRITING, ALL BLOCKS ARE PREFACED AND CONCLUDED WITH
23 ; SYNC CHARACTERS (OAAH). A CHECKSUM BYTE IMMEDIATELY PRECEDS THE
24 ; FINAL SYNC WHEN READING, THE CONTROLLER TESTS THE VALIDITY OF
25 ; BOTH SYNC CHARACTERS AND THE CHECKSUM
26 ; INTER-RECORD GAPS (IRC) ARE WRITTEN WITH ALL MARK (DATA OUT = 1).
                            27;
28:THE WRITE-A-BLOCK OPERATION IS DOUBLE BUFFERED WHILE THE READ-A-BLOCK
29:OPERATION USES A 30-CHARACTER CIRCULAR BUFFER TO MINIMIZE CPU
30:RESPONSE TIME REQUIREMENTS
                             32 $EJECT
                             35 REGISTER EQUATES - THE WRITE AND READ/SKIP OPERATIONS ARE DISTINCT
                                 THEREFORE THE SAME PHYSICAL REGISTER MAY BE USED FOR DIFFERENT PURPOSES IN EACH OPERATION. EACH OPERATION USES DIFFERENT REGISTER LABELS FOR CLAPITS.
                                 LABELS FOR CLARITY
                             39
                             40 ; *******************
                             41
                                             WRITE - RBO
                             43
0000
                             44 CNTLSB
                                                                      BYTE COUNTER LSB
0001
                                                                      BYTE COUNTER MSB; COMMAND SAVER
                             45 CNTMSB
                                             FQU
0002
                             46 CMDSAV
                                             EQU
0003
                             47 CHKSUM
                                             FQU
                                                          R3
                                                                      CHECKSUM REGISTER
0004
                             48 TEMP1
                                                                      TEMPORARY STORAGE
                                             EQU
                                                                       DELAY REGISTER
DELAY REGISTER
                             49
                                                         R5
0007
                             51 STAT
                                             EQU
                                                         R7
                                                                      STS IMAGE
                             53
                                             WRITE - RRI
                             54
                                                                       NOT USED
                                                                       NOT USED
                                                          R1
                                                                      RESULT STORAGE
WRITE STATUS REGISTER
0002
                             57 RESULT
                                             EQU
                                                         R2
R3
0003
                             58 WSTAT
                                             EQU
                                                                     WRITE BIT COUNTER
0004
                             59 BITCHT
                                             EQU
                                                         R4
0005
                             60 SERIAL
                                                         R5
                                             EQU
                                                                      TEMPORARY STORAGE
0006
                             61 TEMPO
                                             EQU
                                 ASAVE
                                             EQU
                             63
                             65
                             66 ;
                                             READ/SKIP - RBO
                             67
                             48 LBOUT
                                             EQU
                                                         RO
                                                                     NEXT BYTE OUTPUT POINTER
0001
                            69 LBRDY
70 ;
                                             EQU
                                                         R1
                                                                      NEXT BYTE AVAILABLE POINTER
                                                         R2
                             71 CHKSUM FOU
                                                         R3
                                                                       CHECKSUM REGISTER (SAME FOR WRITE)
                             72 BLKCNT
                                                                     ; BLOCK COUNTER FOR SKIP
; BLOCK IRG TIMER FOR SKIP
; BLOCK IRG TIMER SAVE
; STS IMAGE (SAME FOR WRITE)
0004
                                             EQU
                                                         R4
0005
                            73 BLKTIM
74 BLKSAV
                                             EQU
                                                         R5
0006
                                             EQU
                                                         R6
                             75 ; STAT
                                             EQU
                             76 ;
                                             READ/SKIP - RB1
                             78 ;
0000
                             79 LBIN
                                                                      NEXT BYTE INPUT POINTER
0001
                            80 IRGCNT
                                            EQU
                                                         R1
                                                                     ; IRG TICK TIMER
; RESULT STORAGE (SAME FOR WRITE)
                             81
                                RESULT EQU
                                                         R2
0003
                             82 RSTAT
                                             EQU
                                                         R3
                                                                      READ STATUS REGISTER READ BIT COUNTER (SAME FOR WRITE)
                             83 ; BITCHT EQU
0005
                             84 DESERI
                                                                      READ DE-SERIALIZER
                                            FOU
                                                         R5
0006
                             85 RDATA
                                                                      READ DATA BUFFER
                             86 ; ASAVE
                                             FOU
                                                                     ACCUMULATOR SAVE (SAME FOR WRITE)
```

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 DIGITAL CASSETTE CONTROLLER REV 1.0 - 26 MARCH 80 LINE SOURCE STATEMENT 88 ;\* 99; STATUS REGISTER BIT DEFINITIONS:
91; THE MAJOR OPERATIONS. WRITE AND READ, USE THE TIMER TO DETERMINE
92; ALL BIT-CELL TIMING AND TO PERFORM THE SERIAL-TO-PARALLEL CONVERSIONS.
93; THE TIMER INTERRUPT SERVICE AND MAIN ROUTINES COMMUNICATE VIA
4 CENTERAL PURPOSE REGISTERS USED AS STATUS REGISTERS. GENERAL PURPOSE REGISTERS USED AS STATUS REGISTERS. 95 ; STAT IS THE STS REGISTER IMAGE SINCE THE UPI CAN'T READ STS DIRECTLY (ONLY THE HIGH ORDER 4-BITS OF STAT ARE USED.)

THE LOWER 4-BITS ARE NOT USER-DEFINABLE. 96 172 HRCHT EGU 0804 : HRITE DIT CONSTRERATES RECISION SUTTRE STATUS : WASTAT - WRITE STATUS REGISTER CONSTREMA CUT EGU -444 HRITE STATUS REGISTER CONSTRUCT REGISTER REGISTE WSTATO CHECKSUM FLAG (CKSFLG) - CHECKSUM BYTE BEING SENT

1 SYNC FLAG (SYNFLG) - FINAL SYNC BYTE BEING SENT

2 WRITE DONE FLAG (WRDFLG) - FINAL SYNC IS BEING SENT

(ENSURES LAST BIT IS COMPLETE)

3 NOT USED

4 NOT USED 107 3 NOT USED
4 NOT USED
5 END OF TAPE FLAG (EOTFLG) - EOT WAS FOUND, TAPE IS NOW AT EOT
6 BEGINNING OF TAPE FLAG (BOTFLG) - BOT WAS FOUND, TAPE IS NOW AT BOT
7 WRITE/READ FLAG (WRFLG) - WRITE OR READ OPERATION IS ACTIVE 109 : 111 : 113 : 114 ;RSTAT - READ STATUS REGISTER 117 PRINTED ATACL 113 RSTATO DATA READY FLAG (RDYFLG) - NEXT BYTE IS READY IN RDATA

1 SYNC NEXT BYTE FLAG (SNBFLG) - NEXT BYTE SHOULD BE A SYNC

2 START FLAG (SRTFLG) - BEGINNING OF READ, DON'T INC LBRDY

UNTIL LBIN=22

3 IRG FOUND FLAG (IRGFLG) - IRG WAS FOUND BY TIMER INTERRUPT ROUTINE

4 NOT USED 116 ; 117 118 ; 119 120 ; 121 122 ; 123 : 125 : 126 ; STAT - STS IMAGE 127 ; 1 1BF - INPUT BUFFER FULL
2 FO - GENERAL PURPOSE FLAG (USED INTERNALLY)
3 F1 - COMMAND/DATA FLAG
4 DRIVE ACTIVE - MOTOR ON
5 FILE PROTECT - DRIVE STATUS
6 CASSETTE PRESENCE - DRIVE STATUS
7 BUSY - CONTROLLER PERFORMING OPERATION 129 : 130 ; 131 : 133 : 135 ; 137 \$F. IECT 139 140 ; PORT DEFINITION: 143 144 ; PORTIO - DIRECTION (O-FORWARD, 1-REWIND) 83000 TJURBS STIRM, ISS T10 - DIRECTION (O-FORWARD, 1-REWIND)

11 - MOTION (O-GO, 1-STOP)

12 - SPEED (O-FAST, 1-SLOW)

13 - READ/WRITE (O-READ, 1-WRITE) CHAPMON HIS US ASOMOW HIS

14 - CLEAR LEADER (O-OFF LEADER, 1-ON LEADER)

15 - FILE PROTECT (O-TAB PRESENT, 1-NO TAB

16 - PRESENCE (O-TAPE IN WITH DOOR CLOSED, 1-NO TAPE)

17 - NOT USED

18 - MURSING SSS 145 146; 147 148 ; 149 150 ; 151 152 ; 192; PORT2O - DATA DUT TO CASSETTE (O-SPACE; 1-MARK) 154; 21 - DRIVE ACTIVE LED (O-ON; 1-OFF) 155; 22 - NOT USED 23 - NOT USED
24 - OBF INTERRUPT OUTPUT
25 - IBF/ INTERRUPT OUTPUT
26 - NOT USED
27 - NOT USED 157 158 ; 159 160 ; 161 161; 162; TEST1 - DATA IN FROM CASSETTE
163;
164 \*EJECT! MOITIEMART OM - TWATEMOD TWUDD SHI MOUSE.
TWATEMOD THUOD SAI TRATE
9188 MOT TWUCD SAI GMINESS. ABORT COMMAND: READ FROM TAPE COMMAND: WRITE TO TAPE COMMAND: REMIND COMMAND SKIP BLOCK COMMAND RESET COMMAND

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 DIGITAL CASSETTE CONTROLLER REV 1.0 - 26 MARCH 80

```
LINE
                               SOURCE STATEMENT
                   167 : SYSTEM EQUATES:
                    168
                    170
                    171 ; WRITE SYSTEM EQUATES:
                    172
                   173 CKSFLG EQU
174 SYNFLG EQU
                                                  CHECKSUM FLAG IN WRITE STATUS
0001
0002
                                          02H
0004
                    175 WRDFLG
                                          04H
                                                   WRITE DONE FLAG IN WRITE STATUS
                                                  ; EOT FLAG
; BOT FLAG
0020
                    176 EOTFLG
                                EQU
                                          20H
0040
                    177 BOTFLG
                                EQU
                                          40H
                                                  ; READ/WRITE FLAG IN WRITE STATUS
; WRITE BIT CONSTANT
; WRITE TIMER CONSTANT
0080
                    178 WRFLG
                                EQU
                                          80H
                    179 WRCNT
                                 EQU
FFFC
                    180 WRTIM
                                EQU
                                          -4H
                    181 ;
                    182 ; PORT EQUATES
                    183
0001
                   184 REWIND EQU
185 FORWD EQU
                                                ; DIRECTION MASKS
OOFE
                                          OFEH
0002
00FD
                    186 STP
                                 EQU
                                                  START/STOP MASKS
                    187 SRT
                                          OFDH
                                 EQU
0004
00FB
                    188 SLOW
                                 EQU
                                          04H
                                                  SPEED MASKS
                                          OFBH
                    189 FAST
                                 EQU
0008
                    190
                        WR
                                 EQU
                                                   WRITE/READ MASKS
00F7
                    191 RD
                                          OF7H
                                 EQU
0001
                    192 DOHI
                                 EQU
                                          01H
                                                  DATA OUTPUT TO DRIVE MASKS
                                                 DRIVE ACTIVE LED MASKS
OOFE
                    193 DOLOW
                                 EQU
                                          OFEH
                    194 DAOFF
                                 EQU
                    195 DAON
OOFD
                                EQU
                                         OFDH
                    196
                    197 ; READ SYSTEM EQUATES:
                    198
                                                   ; DATA READY FLAG IN READ STATUS
                    199 RDYFLG FQU
0001
                                          01H-
                                                  SYNC NEXT BYTE FLAG IN READ STATUS
START INC READY POINTER FLAG IN READ STATUS
IRG FOUND FLAG IN READ STATUS
0002
                    200 SNBFLG
                                EQU
                                          02H
                   201 STRFLG
202 IRGFLG
0004
                                EQU
                                          04H
                                EQU
                                          08H
                                                  READ TIMER CONSTANT
0008
                    203 RDCNT
                                FQU
                                          OBH
                    204 RDTIM
                               EQU
                                          -6H
                    205 :
                    206 ; STS REGISTER EQUATES:
                   207 ;
208 BUSY
                                          80H
                                                   BUSY BIT
                                                   DRIVE ACTIVE BIT
0010
                   209 DRACT
210 TAPIN
                                EQU
                                          10H
40H
                                                   FILE PROTECT BIT
0020
                    211 FILPRT EQU
                                          20H
                    212 SEJECT
                    213 ; GENERAL RESULT CODES
                    214 ;
0001
                    215 ABTCMP EQU
                                                   ABORT COMPLETE CODE
0000
                   216 GOOD
217 CMDERR
                                EQU
                                          00H
                                                   GOOD RESULT CODE
COMMAND ERROR CODE
NO TAPE ERROR CODE
0002
0003
                    218 NTAPE
                                 EQU
                                          03H
0004
                    219 NWR EQU
                                                  FILE PROTECT ERROR CODE
                    220 ;
                    221 ; WRITE RESULT CODES
                    222
                                                   UNDERRUN ERROR CODE
0081
                    223 UNDERW EQU
0082
                    224 WCMDER EQU
                                          82H
                                                COMMAND/DATA ERROR CODE
0083
                    225 EOTERR EQU
                                          83H
                    226
                    227
                        READ RESULT CODES
                   228
0041
                    229 OVERUN EQU
                                                  UNDERRUN CODE FOR BUFFER
                   230 SYNC1
0042
                                EQU
                                          42H
43H
                                                  BAD SYNC1 ERROR CODE
BAD SYNC2 ERROR CODE
0043
                    231 SYNC2
                                EQU
0044
                   232 BADCHS EQU
                                          44H
                                                   BAD CHECKSUM ERROR CODE COMMAND/DATA ERROR CODE
0045
                    233 RCMDER
                                EQU
                                          45H
0046
                    234 REOTER
                                EQU
                                          46H
                                                  EOT AT READ ERROR CODE
EOT AT SKIP ERROR CODE
BOT AT RSKIP ERROR CODE
0047
                    235 SKPEOT
                                EQU
                                          47H
0048
                   236 SKPBOT EQU
                                          48H
                    237
                   238 ; MISC EQUATES
                    239
                                                  ; SYNC BYTE ; SLOW IRG COUNT CONSTANT - NO TRANSITION IN 2 BIT TIMES ; FAST IRG COUNT CONSTANT ; REWIND IRG COUNT FOR SKIP
DOAA
                   240 SYNC
                                          DAAH
0033
                    241 SLWIRG EQU
                                          51D
0020
                   242 FASTRG FOU
                                          32D
                    243 RWDIRG EQU
                                         32D
                   244
                    245 ; COMMANDS
                   246 ;
247 ABORT
0005
                                EQU
                                                  ABORT COMMAND
0001
                   248 RDCMD
249 WRCMD
                                EQU
                                         01H
02H
                                                   READ FROM TAPE COMMAND
0002
                                                  REWIND COMMAND
SKIP BLOCK COMMAND
RESET COMMAND
0004
                   250 RUCMD
                                EQU
                                         04H
0003
                    251 SKCMD
                                EQU
                                         03H
0000
                   252 RESCMD
                                EQU
                                         ООН
                    253
                   254 SEJECT
```

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```
256
                                        START OF PROGRAM - JUMPS FOR COLD START (RESET) AND TIMER INTERRUPTS
                                  257
                                  257 ; *************************
                                  260
                                  260 ;
261 RESET: JMP BEGIN
                                                                                                     JUMP OVER TIMER VECTOR LOCATION
0000 0409
                                                                   7H TIMER INTERRUPT VECTOR LOCATION
                                                     ORG
0007
                                  263
                                  264
                                  264 ;
265 TIMINT. JMP INT JUMP TO TIMER INTERRUPT SERVICE ROUTINE
0007 6400
                                  266
                                         267
                                  DAR
                                  269 ; PROGRAM START - INITIALIZE STATUS REGISTERS, DRIVE OUTPUTS, AND
                                  270 ; WAIT FOR A COMMAND. MOTE DE ATAG E TIA
                                  A INITIALIZE THINGS
                                  274 BEGIN CLR
0009 27
                                                        CLR
                                                                       REO CLEAR STS IMAGE
000B C5
                                  276
                                                        SEL
0000
                                                        MOV
                                                                       STS, A CLEAR STS
0000 90
                                  278
                                                        MOV
                                                                      STS: A
RB1
WSTAT. A
CLEAR STATUS
WSTAT. A
CLEAR STATUS
P1. #FD PR SLOW : STOP DRIVE AND SELECT SLOW FOR STARTERS
P1. #FORHD AND RD. SELECT FORWARD AND READ
P2. #DAOFF
; TURN OFF DRIVE ACTIVE LED
FLAGS
; ENABLE FLAG INTERRUPT DUTPUTS
                                  279
                                                        SEL
OOOF AB
                                  280
                                                        MOV
0010 8906
                                  281
                                                        ORL
0012 99F6
                                  282
                                                        ANL
0016 F5
                                  284
                                                        EN
                                  285 ; 286 ; COMMAND RECOGNIZER MAIN LOOP | DELITION | DECEMBER OF THE PROPERTY                                                                                                 COMMAND PROCESSING IN RBO
                                                       SEL NO
                                                                      RBO
0017 C5
                                  288 B1
                                 289 St. KBO COMMAND PROCESSING IN RBO
289 JNIBF B2 ITEST IF IBF INPUT
290 JF1 CMDIN YES THERE IS AN INPUT, SO TEST IF ITS A COMMAND
291 IN A.DBB NOPE. ITS DATA SO IGNORE IT
292 JMP B1 JUST GO BACK TO TEST IBF
293 B2: CALL STSUP IND INPUT, UPDATE STS WITH DRIVE STATUS
294 JMP B1 OO BACK TO TEST IBF
0018 D61F
001A 7623
0010 22
001D 0417
001F 14AD
                                  295 ;
                                 297;
298 :COMMAND PROCESSOR - TESTS VALIDITY OF INPUT AND BRANCHES TO THE APPROPRIATE
299 :ROUTINE. ILLEGAL COMMANDS ARE FLAGGED AS COMMAND ERRORS.
                                  302
                                                                       A, STAT ; GET STS IMAGE
A, #BUSY ; SET BUSY FOR ALL COMMAND INPUTS
STAT. A ; RESTORE IMAGE
STS. A ; UPDATE STS
READ COMMAND FROM DBBIN
                                  303 CMDIN:
0023 FF
0024 4380
                                  304
                                                        ORL
0026 AF
                                  305
                                                        MOV
                                                                       STS, A JUPDATE STS
A, DBB JREAD COMMAND FROM DBBIN
CMDSAV, A JSAVE IT IN CMDSAV
0027 90
                                  306
                                                        MOV
                                  307
0028 22
                                                        IN
                                                                       CMDSAV.A ; SAVE IT IN CMDSAV
TEMP1. #6H ; INITIALIZE ILLEGAL COMMAND COUNTER
0029 44
                                  308
                                                        MOV
                                  309
                                                                                                     ; INITIALIZE ILLEGAL COMMAN, ; GET COMMAND FROM CMDSAV
002A BC06
                                                        MOV
002C FA
002D 17
                                  310 CMDIN1:
                                                                       A, CMDSAV
                                                        MOV
                                                        INC
                                                                       A
A, TEMP1 ; TEST IF VALID
CMDIN2 ; VES. INDIRECT JUMP TO IT
TEMP1, CMDIN1 ; NO MATCH YET, TRY AGAIN
; NO MATCH, COMMAND ERROR
OOSE DC
                                  312
                                                        XRL
        C63A
002F
                                  313
                                                         JZ
0031 FC2C
                                                        DJN7
                                  314
                                  315
                                  316 ;
317 CMDIN3: CALL
                                                                       NDRACT : RESET DRACT AND BUSY (DRACT WAS NEVER SET)
A, #CMDERR ; COMMAND ERROR CODE
DBB, A ; OUTPUT ERROR CODE
B1 ; QO BACK TO TEST FOR IBF
0033 5404
0035 2302
                                  318
                                                        MOV
0037 02
0038 0417
                                  319
                                                        OUT
                                  320
                                                        JMP
                                 321;
322 CMDIN2: MOV A.CMDSAV. ;IT'S A GOOD COMMAND, GET IT FROM CMDSAV.
323 ADD A.*(LOW CMDJMP) ;ADD OFFSET
324 JMPP &A ;INDIRECT JUMP TO THE COMMAND ROUTINE THRU TABLE;
325 ;COMMAND JUMP TABLE
003A FA
003B 033E
003D B3
                                  326 ;
                                  327 CMDJMP:
                                                                       (LOW RESJMP)
                                                        DR
003E 44
                                                                       (LOW RESUMP)
(LOW RETUMP)
(LOW SKPJMP)
(LOW SKPJMP)
(LOW SKPJMP)
(LOW SKPJMP)
003F 46
                                                        DB
0040 48
                                  329
                                                        DR
0041 4A
                                  330
                                                        DB
0042 40
                                  331
332
                                                       DB
                                                                        (LOW REWJMP)
                                  333 ;
                                  334 ARTJMP:
335 RESJMP: JMP
0044 044E
                                                                        RESCOM
0046 2400
0048 0455
                                                       JMP
                                  336 REDJMP
                                                                        READ
                                  337 WRTJMP
                                                                        WRITE
                                  338 SKPJMP: JMP
339 REWJMP: JMP
0044 4414
004C 4494
                                                                       REWND
                                  340;
341; IT'S A ABORT COMMAND WHILE IN COMMAND RECOGNIZER LOOP
                                  342
                                   343 RESCOM: CALL
                                                                                                     RESET BUSY AND DRACT (DRACT NEVER WAS SET)
004E 54C4
                                                                        A, #ABTCMP
DBB, A
                                                                                                     GET ABORT COMPLETE CODE OUTPUT IT
0050 2301
                                  344
                                                        MOV
                                   345
                                                        OUT
                                                                                                      GO START OVER
0053 0400
                                  346
                                                        JMP
                                                                        RESET
                                  348 SEJECT
```

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```
LOC OBJ
                     LINE SOURCE STATEMENT
                       349 ;***********************************
                       351 ; WRITE TO TAPE ROUTINE
                       354
                       355 WRITE: SEL
0055 C5
                                                        CLEAR INT COUNT FLAG
                                      CLR
0056 85
                       356
                                               FO ;CLEAR INT COUNT FLAG
TCNT ;BE SURE THAT THE TIMER IS STOPPED
TCNTI ;DISABLE TIMER INTS
CLETF ;BE SURE THAT THE TIMER FLAG IS CLEARED
WRI ;WAIT FOR BYTE COUNT LSB
A, DBB ;READ COUNT LSB FROM DBBIN
CMDIN3 ;TEST IF COMMAND - ERROR
0057 65
                       357
                                      STOP
0058 35
                       358
                                     DIS
0059 1659
                       359 CLRTF
                                      JNIBF
005B D65B
                       360 WR1:
005D 22
                       361
                                      JF1
005E 7633
                       362
                                                CNTLSB, A ; IT'S DATA SO STORE IT AWAY
                                      MOV
                                                                    ; WAIT FOR BYTE COUNT MSB
; READ COUNT MSB FROM DBBIN
0061 D661
                       364 WR2
                                      JNIBE
                                                WR2
A, DBB
0063 22
                                      IN
                       365
                                                                   READ COUNT MSB FROM DBBIN
: TEST IF COMMAND - ERROR
:IT'S DATA SO STORE IT AWAY
:GET COUNT LSB
:INC IT TO ACCOUNT FOR SYNC
                                               CMDIN3
CNTMSB, A
0064 7633
                       366
                                      IE 1
0066 A9
                       367
                                      MOV
                                                A, CNTLSB
0067 FB
                       368
                                      MOV
0068 17
                       369
                                      INC
                                                A
CNTLSB, A
                                                                    ; SAVE IT ; NO OVERFLOW, DON'T INC COUNT MSB
0069 AB
                       370
                                      MOV
                                               NINMSB
CNTMSB
006A 966D
                                                                    ; NO OVERFLOW, DON'T INC COUNT MSB
; OVERFLOW, SO INC COUNT MSB
; GET DRIVE STATUS
                       371
                                      JN7
006C 19
                       372
                                      INC
                                               A, P1
DRIVER
DRIVER
                       373 NINMSB
00AD 09
                                      IN
                                                                    TEST IF NO TAPE
TEST IF NO TAPE
TEST IF FILE PROTECTED
EXIT WITH ERROR IF EITHER
CLEAR CHECKSUM REGISTER
0070 B2C5
                       375
                                      JB5
                                                CHKSUM, #OOH
                                      MOV
0072 BB00
                       377
                                                RB1
BITCNT, #WRCNT
                                                                    ; INITIALIZE WRITE BIT COUNTER
0075 BC08
0077 BDAA
                       379
                                      MOV
                                                SERIAL, #SYNC
                                                                    ; INDITIONAL WRITE SHIT COUNTER
; LOAD SYNC INTO SERIAL FOR 1ST BYTE
; GET WRITE TIMER CONSTANT (1/2 CELL TIME)
; LOAD TIMER BUT DON'T START IT YET
                       380
                                      MOV
                                                A, #WRTIM
T, A
A, WSTAT
WEDTER
RBO
DRACTS
0079 23FC
                       381
                                      MUA
007B 62
                       382
                                      MOV
                                                                   GET WRITE STATUS
; IF EOTFLG SET, STILL AT END OF TAPE - ERROR
007C FB
                       383
                                      MOV
007D B2A9
                       384
                                      JB5
007F C5
                       385
                                      CEI
                                                                   NOT AT EOT SO SET DRIVE ACTIVE AND CONTINUE
0080 54BC
                       386
                                      CALL
                                               RB1
P1. **WR OR SLOW OR STP ; SETUP PORT FOR SLOW WRITE
P1. **SRT AND FORWD ; START DRIVE IN FORWARD
A. WSTAT
COMP FOR O TEST
WR3
; TEST BOTFLE - WRITE OVER HOLE IF SET
0082 D5
                       387
                                      SEL
0083 890E
                       388
                                      ORL
0085 99FC
                       389
                                      ANL
0087 FB
                       390
                                      MOV
0088 37
                       391
                                      CPL
0089 D28D
                       392
                                      JB6
                                                PASHOL ;GET OFF CLEAR LEADER AND PAST HOLE IN TAPE WSTAT, #80H ;SETUP WRITE STATUS WITH WRFLG SET
008B 54DC
                       394 WR3
008D BB80
                                      MOV
008F C5
                                                RBO
DEL150
                       395
                                      SEL
                                                                   WAIT 450 MS IRG BEFORE WRITING DATA
0090 1401
                                                DEL150 ; WAIT 450 MS 1
DEL150
DEL150
DEL150
T ; START TIMER
TCNTI ; ENABLE TIMER
                       396
                                      CALL
0092 1401
                                      CALL
0094 1401
                       398
                                      CALL
0096 55
                       399
                                      STRT
                                                                   ; START TIMER
; ENABLE TIMER INTERRUPTS
0097 25
                       400
                                      EN
                       401 /
402 ; TIMER INTERRUPT ROUTINE DOES ALL THE WORK SO WAIT UNTIL IT RESETS WRFLG
                       403
0098 C5
0099 14AD
                       404 WR4
                                      SEL
                                                RBO STOP STOPPARE STS WHILE WAITING RB1
A. WSTAT SET WRITE STATUS
WR4 STEST IF WRITE DONE (WRFLG RESET)
                       405
                                      CALL
009B D5
                       406
                                      SEL
009C FB
                       407
                                      MOV
009D F298
                       408
                                      JB7
                       409
                       410 ; WRFLG IS RESET SO WRITE OPERATION MUST BE COMPLETE - DUTPUT RESULT
                       411
009F C5
                       412 WR5
                                      SEL
00A0 54C4
                                                NDRACT RESET DRACT AND BUSY
                       413
                                      CALL
                                                RB1
A, RESULT GET RESULT CODE
00A2 D5
                       414
                                      SEL
OOA3 FA
                       415
                                               DBB.A ; OUTPUT IT
DELISO ; WAIT FOR DRIVE TO STOP
00A4 02
                       416
                                      OUT
00A5 14C1
                                      CALL
                                                                    ; FULLY BEFORE ACCEPTING NEW COMMAND ; DONE, RETURN TO COMMAND RECOGNIZER LOOP
                       418
00A7 0417
                                      JMP
                       419
                       420 ;
                       421 ; TAPE IS AT EOT WHEN WRITE COMMAND ISSUED - EXIT WITH ERROR
                                                RESULT, #EOTERR ; EOT ERROR RESULT CODE
00A9 BA83
                       423 WEDTER: MOV
00AB 049F
                       424
                                                                    GO RESET BUSY AND OUTPUT RESULT
                       425 :
                       426 SEJECT
```

```
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                    LINE
                                 SOURCE STATEMENT
                      427 ; *************************
                      429 ; STS UPDATE SUBROUTINE - UPDATES THE CASSETTE PRESENCE AND FILE PROTECT
                      430 ; BIT IN STS. (ENTER AND EXIT IN RBO)
                      432 ; ****
                      433
                      433 ;
434 STSUP: MOV A, STAT ; GET STS IMAGE
 00AE 4360
00BO AF
                                           A, #TAPIN OR FILPRT ; SET BOTH PRESENCE AND FILE PROTECT
STAT, A ; RESTORE IMAGE
A, P1 ; READ INPUT
                      435
                      436
                                   MUA
  00B1 09
                                   ORL MO
                                           A.P1 ;READ INPUT
A. WHOT(TAPIN OR FILPRT) ;SET BITS TO CORRECT STATE
A.STAT
STAT, A ;RESTORE IMAGE
STS, A ;UPDATE STS
                      438
439
440
  00B2 439F
 00B4 5F
00B5 AF
                                   ANL
                                   MOV
                                   MOV
  00B7 83
                      442
                      443 ;
                      444 ; *************************
                      445 :
                      446 ; DELAY ROUTINES- ENTER/EXIT IN RBO
                      449
                     449;
450 DEL50: MOV R5,#36D , 50MS DELAY ROUTINE
451 DEL1: MOV R6, #0FFH
 OOBS BD24
 OOBA BEFF
                     451 DEL1:
452 DEL2:
                                  MOV Ro. WUFFE DUNZ RG. DEL2 STATE BASE TSD. TATER A DUNZ RS. DEL1 STATE BASE TSD. TATER A DUNZ RET
  OOBC EEBC
  OOBE EDBA
                                DUNZ
                      453
 0000 83
                      454
                     455 .
456 DEL150: MOV R5.#108D ;150MS DELAY ROUTINE
457 JMP DEL1
458 .
 00C3 04BA
                      461 ; DRIVE ERROR EXIT - NO TAPE OR FILE IS PROTECTED FOR WRITE
                      0005 05
                     465 DRIVER SEL
                                           PRO
                                           RBO
NDRACT , RESET DRACT AND BUSY
A, P1 , READ DRIVE STATUS
NT , TEST IF TAPE IS THERE
A, #NWR , TAPE IS THERE SO ERROR MUST BE FILE PROTECT
DBB. A ; OUTPUT ERROR CODE
B1 , RETURN TO COMMAND LOOP
A, #NTAPE ; NO TAPE ERROR
DRI
  0006 5404
                     466 CALL
467 IN
 0008 09
                                  IN
JB6
  00C9 D2D0
                     468
                                  MOV
 OOCB 2304
                     469
 00CD 02
                      470 DR1:
 00CE 0417
                                  JMP
MOV
                     471
 00D0 2303
 00D2 04CD
                     473
                                  JMP
                     476 , .
476 , .
                     477; READ ERROR WITH ADVANCE TO IRG BEFORE STOPPING DRIVE.
478; WAIT FOR OBF TO BE FREE BEFORE RESETTING BUSY THEN OUTPUT RESULT.
479; RDERR3 LABEL IS EXIT POINT FOR OTHER ROUTINES NEEDING TO WAIT FOR 480; OBF TO BE FREE BEFORE OUTPUTTING RESULT.
                     481 ; ROUTINE EXITS IN RBO.
                     482 ;
                      484
                                           RBO Tan - and
                     485 RDERR
                                  SEL
                                           RBO
BLKCNT, #1H SET SKIP COUNTER TO ADVANCE TO NEXT IRG
BLKTIM, #SLWIRG SETUP IRG COUNTER
BLKSAV, #SLWIRG
SKIPF TO NEXT IRG
                     486
 00D5 BC01
00D7 BD33
                                   MOV
                     487
                                  MOV
 00D9 BE33
                     488
                                  MOV
                                                             DO SKIP TO NEXT IRG
 OODB 5400
                     489
                                  CALL
                                           SKIPER
RDERR2
                                                             ; TEST IF EOT FOUND
; STOP DRIVE WHEN DONE
; TURN OFF DRIVE ACTIVE LED
 00DD F6F1
                     490 JC
491 RDERR3: ORL
 OODF
                                           P1, #STP
P2, #DAOFF
       8902
 00F1 8A02
                     492
                                  ORL
                                           RDERRS TEST IBF WHILE WAITING FOR OUF
RDERR6 TEST OF TEST INPUT
RDERR4 TEST OBF LOOP IF 1. CONTINUE IF 0
RB0
NDRACT RESET DRACT AND BUSY
 00E3 D6E7
                     493 RDERR4: JNIBF
 OOFS OAFR
                     494
 00E7
                     495 RDERR5:
                                  JOBF
      86E3
 00E9 C5
                     496
                                   SEL
                                                           RESET DRACT AND BUSY
 00EA 54C4
                     497
                                  CALL
                                           RB1
A, RESULT GET RESULT MAYING SHU LVING SEC
 OOEC D5
                     498
 OOED FA
                     499
                                  MOV
 00EE 02
00EF 0417
                     500
501
                                           DBB, A
                                  OUT
                                                            DUTPUT RESULT
                                                             GO BACK TO COMMAND LOOP
                                  JMP
                                           B1
                                           RB1 . EOT FOUND WHILE SKIPPING
RESULT. #REDTER . RESET RESULT VALUE TO EOT ERROR
RSTAT. #EOTFLG . SET EOTFLG IN RSTAT
RDERR3 . GO DUTPUT NEW RESULT
                     502
                     503 RDERR2:
                                  SEL
                     504
505
 00F2 BA46
                                  MOV .
 00F4 BB20
                                                                                         186
188
Vali
 00F6 04DF
                     506
                     507 ;
 00F8 22
                     508 RDERR6:
                                                           TEST IF ABORT
                                           A, #ABORT
 00F9 D305
                     509
                                  XRL
                                           RDERR5
RESCOM
 00FB 9AF7
                     510
 00FD 044E
                     511
                                  JMP
                                                             ; IT'S AN ABORT, GO RESET
                     513 SEJECT
```

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 DIGITAL CASSETTE CONTROLLER REV 1.0 - 26 MARCH 80

0	The second second		220		DATECLIER REV 1.0 - 24 MARCH 80
	514 515		ORG	100H	
			******	******	**************************************
	517	1			
	518	READ F	ROM TAP	E ROUTINE	
	520 521				**********
0 C5		READ:	SEL	RBO	newscand despite the second consideration of the SCA
1 65	523		STOP	TCNT	BE SURE THE TIMER IS STOPPED
2 35	524		DIS		
3 1603 5 85	525 526	RCLRTF:	CLR		
6 2320	527				CLEAR LAST DATA FLAG GET POINTER START LOCATION
B AB	528		MOV	LBOUT, A	
9 A9	529		MOV		
A BB00 C D5	530 531		MOV	CHKSUM, #OOH	CLEAR CHECKSUM LOCATION
0 A8	532		MOV		; INITIALIZE LBIN
E BCOB					; INITIALIZE READ BIT COUNTER
0 0 9	534		IN	A, P1	READ DRIVE STATUS
1 D24F	535		JB6		TEST IF TAPE IS THERE TO READ
3 C5 3 54BC	536 537		CALL	RBO	SET DRIVE ACTIVE
5 23FA	538		MOV	A, #RDTIM	;SET DRIVE ACTIVE ;GET READ TIMER CONSTANT (3/4 CELL TIME)
8 62	539		MOV	T. A SUITE NO.	LOAD TIMER BUT DON'T START IT YET
7 25	540		EN	TCNTI	; ENABLE TIMER INTERRUPTS
A D5	541 542		SEL	RB1	
B24B	543		JB5	REOT	TEST IS AT ENT - EPPNP IS SO
8904	544		ORL	P1, #SLOW	; SELECT SLOW
99F4	545		ANL	P1, #RD AND FORWD	AND SRT ; START DRIVE, FORWARD AND REA
2 37 3 D227	546 547		CPL		COMP A FOR O TEST (STILL HAVE RSTAT)
5 54DC	547 548		JB6 CALL	RD1 PASHOL	; TEST FOR AT BOT, IF NOT JUST LOOK FOR MARK ; IF BOT, WAIT UNITL PAST CLEAR LEADER AND HOLI
BB06		RD1:	MOV	RSTAT, #06H	SETUP READ STATUS - SNBFLG AND STRFLG SET
14C1	550		CALL	DEL150	LET DRIVE START UP
3 462B	551		INT		; AND WAIT OVER WRITE STOP LOCATION
562D		RD1A:	JT1	RD1A RD2	; WAIT FOR TRANSITION TO SPACE
55	554		STRT	T	START TIMER
3 24D5 5 FB 5 1251	560 561 562	RD4:	JNIBF JMP MOV JBO	A. RSTAT	:TEST FOR IBF EVEN WHEN READING ;IMPUT DURING READ - GO TEST IT :GET READ STATUS :TEST DATA READY FLAG (RDYFLG)
7291	563		JB3	IRGFND	; TEST IRG FLAG (IRGFLG)
3 7291	563 564			IRGFND	
3 7291	563 564 565	********	JB5	IRGFND REDT	;TEST IRG FLAG (IRGFLG) ;EOT FOUND DURING READ (EOTFLG SET) - ERROR
3 7291 A B24B	563 564 565 566 567	NOTHIN	JB5 G FROM	IRGFND REOT TIMER INTERRUPT RO	;TEST IRG FLAG (IRGFLG) ;EOT FOUND DURING READ (EOTFLG SET) - ERROR UTINE SO GO HANDLE CIRCULAR BUFFER
3 7291 A B24B	563 564 565 566 567 568	NOTHIN	JB5 G FROM SEL	IRGEND REOT  TIMER INTERRUPT RO RBO	; TEST IRG FLAG (IRGFLG) ; EOT FOUND DURING READ (EOTFLG SET) - ERROR BUTINE SO GO HANDLE CIRCULAR BUFFER
3 7291 A B24B C C5 D F9	563 564 565 566 567	; NOTHIN	JB5 G FROM	IRGFND REOT TIMER INTERRUPT RO RBO A, LBRDY A, LBRDY	:TEST IRG FLAG (IRGFLG) :EOT FOUND DURING READ (EOTFLG SET) - ERROR  IUTINE SO GO HANDLE CIRCULAR BUFFER  :GET READY POINTER :COMPARE TO OUT POINTER
3 7291 A B24B	563 564 565 566 567 568 569 570	; ; NOTHIN ;	JB5 G FROM SEL MOV XRL JZ	IRGFND REOT TIMER INTERRUPT RO RBO A, LBRDY A, LBOUT	; TEST IRG FLAG (IRGFLG) ; EOT FOUND DURING READ (EOTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER-  ; GET READY POINTER ; COMPARE TO GUT POINTER
2 C5 2 F9 5 D8 6 C630	563 564 565 566 567 568 569 570 571	NOTHIN	JB5 G FROM SEL MOV XRL JZ	IRGEND REOT  TIMER INTERRUPT RO RBO A, LBRDY A, LBRDY RD3	; TEST IRG FLAG (IRGFLG) ; EOT FOUND DURING READ (EOTFLG SET) - ERROR  UTINE SO GO HANDLE CIRCULAR BUFFER- ; GET READY POINTER ; COMPARE TO OUT POINTER ; EMPTY IF THE SAME SO JUST LOOP ; NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT
2 C.5 2 F9 3 D8 5 C630	563 564 565 566 567 568 569 570 571 572 573	NOTHIN	JB5 G FROM SEL MOV XRL JZ JOBF	IROFND REOT TIMER INTERRUPT RO RBO A. LBRDY A. LBOUT RD3	; TEST IRO FLAG (IROFLG) ; EOT FOUND DURING READ (EOTFLG SET) - ERROR  UTINE SO GO HANDLE CIRCULAR BUFFER ; GET READY POINTER ; COMPARE TO OUT POINTER ; EMPTY IF THE SAME SO JUST LOOP ; NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT ; TEST DBBOUT - FULL, LOOP
3 7291 A B24B C C5 D F9 E D8	563 564 565 566 567 568 569 570 571 572 573	NOTHIN	SEL MOV XRL JZ JOBF MOV	IRGFND REOT TIMER INTERRUPT RO A.LBRDY A.LBRDT RD3 RD3 RD4 A.ELBOUT DB8.A	; TEST IRG FLAG (IRGFLG) ; EOT FOUND DURING READ (EOTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER- ; GET READY POINTER ; COMPARE TO OUT POINTER ; MATERIAL SO SEE IF NEXT BYTE CAN BE OUTPUT ; TEST DBBOUT - FULL, LOOP ; DBBOUT FREE - GET DATA ; OUTPUT IT
3 7291 3 824B C C5 D F9 E D8 C C630 1 8630 3 F0 4 02 5 F8	563 564 565 566 567 568 569 570 571 572 573 574 575	NOTHIN	SEL MOV XRL JZ JOBF MOV OUT MOV	IRGFND REOT TIMER INTERRUPT RO A.LBRDY A.LBRDT RD3 RD3 RD4 A.ELBOUT DB8.A	; TEST IRG FLAG (IRGFLG) ; EOT FOUND DURING READ (EOTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER- ; GET READY POINTER ; COMPARE TO OUT POINTER ; MATERIAL SO SEE IF NEXT BYTE CAN BE OUTPUT ; TEST DBBOUT - FULL, LOOP ; DBBOUT FREE - GET DATA ; OUTPUT IT
3 7291 3 824B C C5 D F9 E D8 F C630 1 8630 3 F0 4 02 5 F8 5 5 F8	563 564 565 566 567 568 569 570 571 572 573 574 575	NOTHIN TO SECOND	SEL MOV XRL JZ JOBF MOV OUT MOV CALL	IROFND REOT  TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3  RD3 A.@LBOUT DBB, A A.LBOUT BUMPIT	; TEST IRG FLAG (IRGFLG) ; EOT FOUND DURING READ (EOTFLG SET) - ERROR  ULTINE SO GO HANDLE CIRCULAR BUFFER- ; GET READY POINTER ; COMPARE TO OUT POINTER ; EMPTY IF THE SAME SO JUST LOOP ; NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT ; TEST DBBOUT - FULL, LOOP ; DBBOUT FREE - GET DATA ; OUTPUT IT ; GET OUT POINTER ; BUMP POINTER
7291 8248 C.5 F9 E D8 C.630 8630 8 F0 4 O2 5 F8 A8	563 564 565 566 567 568 569 570 571 572 573 574 575 576	NOTHIN NO	SEL MOV XRL JZ JOBF MOV CALL MOV	IROFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 A.@LBOUT DBB.A A.LBOUT BUMPIT LBOUT.A	; TEST IRG FLAG (IRGFLG); ;EOT FOUND DURING READ (EOTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER-  ;GET READY POINTER; ;COMPARE TO GOUT POINTER; ;EMPTY IF THE SAME SO JUST LOOP; NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT; TEST DBBOUT - FULL, LOOP; ;DBBOUT FREE - GET DATA; ;OUTPUT IT; GET GUT POINTER; ;BUMP POINTER; ;BUMP POINTER;
7291 8248 C.5 F9 E D8 C.630 8630 8 F0 4 O2 5 F8 A8	563 564 565 566 567 568 569 571 571 573 574 575 576 577 578	NOTHIN	G FROM SEL MOV XRL JZ JOBF MOV OUT MOV CALL MOV JMP	IROFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 A.ELBOUT DBB.A A.LBOUT BWHPIT LBOUT.A RD3	; TEST IRG FLAG (IRGFLG); ;EOT FOUND DURING READ (EOTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER-  ; COET READY POINTER; ;COMPARE TO OUT POINTER ;EMPTY IF THE SAME SO JUST LOOP; NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT; TEST DBBOUT - FULL, LOOP; ;DBBOUT FREE - GET DATA ;OUTPUT IT; GET OUT POINTER; ;BUMP POINTER; ;RETURN IT; ;LOOP
7291 8248 C.5 F9 E D8 C.630 8630 8 F0 4 O2 5 F8 A8	563 564 565 566 567 569 570 571 572 573 574 575 576 577 580	NOTHIN	G FROM SEL MOV XRL JZ JOBF MOV OUT MOV CALL MOV JMP	IROFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 A.@LBOUT DBB.A A.LBOUT BUMPIT LBOUT.A	; TEST IRG FLAG (IRGFLG); ;EOT FOUND DURING READ (EOTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER-  ;GET READY POINTER ;COMPARE TO OUT POINTER ;CMPTY IF THE SAME SO JUST LOOP ;NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT ;TEST DBBOUT - FULL, LOOP ;DBBOUT FREE - GET DATA ;OUTPUT IT ;GET OUT POINTER ;BUMP POINTER ;BUMP POINTER ;RETURN IT ;LOOP  SSUED - ERROR
7291 824B 6 C5 9 F9 1 D8 6 C630 8 630 8 600 8 600 8 600 8 600 8 600 8 600 8 600 8 60	563 564 565 566 567 568 569 570 571 572 573 576 577 578 579 580 581	NOTHIN TO THE A	G FROM SEL MOV XRL JZ JOBF MOV CALL MOV TEOT WITH TEOT W	IROFND REOT TIMER INTERRUPT RO RBO A. LBRDY A. LBOUT RD3 RD3 A. ELBOUT DBB, A A. LBOUT BUMPIT LBOUT, A RD3 HEN READ COMMAND I	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EOTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER  GET READY POINTER FOTO THE FIRE SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT FEST DBBOUT - FULL, LOOP DBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER RETURN IT LOOP  SSUED - ERROR
3 7291 824B 1 C5 9 F9 1 D8 1 C630 8630 3 F0 4 02 5 F8 5 54CC 3 AB 2 2430	563 564 565 566 567 568 569 570 571 572 573 576 577 578 579 580 581	NOTHIN TO THE A REOT:	JB5 G FROM 'SEL MOV XRL JZ JOBF MOV OUT MOV CALL MOV JMP T EOT WI	IROFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 RD3 RD3 A.&CLBOUT DBB.A A.LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT.#REDTER	FEST IRG FLAG (IRGFLG) FOUND DURING READ (EOTFLG SET) - ERROR  ULTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOUND FOUNT FUND FOUNT FO
3 7291 8 824B C C5 D F9 E D8 C C630 8 8630 B F0 4 02 B F0 B F8 B 5 54CC B AB B 2430	563 564 565 566 567 568 569 570 5711 572 573 576 577 578 579 580 581 582 583 584	TAPE A	JB5 G FROM ' SEL MOV XRL JZ JOBF MOV OUT MOV JMP T EOT WI MOV JMP	IROFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 A.@LBOUT DBB,A A.LBOUT BUMPIT LBOUT,A RD3 HEN READ COMMAND I RESULT, #REOTER RDERR3	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EDTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOTH IF THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT TEST DBBOUT - FULL, LOOP DBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER BUMP POINTER RETURN IT LOOP  SSUED - ERROR FOTH THE SAME SO JUST LOOP SSUED - ERROR FOTH THE SAME SO JUST LOOP SSUED - ERROR FOTH THE SAME SO JUST LOOP SSUED - ERROR FOTH THE SAME SO JUST LOOP FOTH THE SAME S
3 7291 824B 1 C5 9 F9 1 D8 1 C630 8630 3 F0 4 02 5 F8 5 54CC 3 AB 2 2430	563 564 565 566 567 577 572 573 574 575 576 576 577 580 581 582 583 584 585 586	TAPE A REOT:	JB5 G FROM ' SEL MOV XRL JZ JOBF MOV OUT MOV JMP T EOT WI MOV JMP	IROFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 RD3 RD3 A.&CLBOUT DBB.A A.LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT.#REDTER	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EOTFLG SET) - ERROR  UTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOR THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT FEST DBBOUT - FULL, LOOP DBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER RETURN IT LOOP  SSUED - ERROR FOR THE SAME SO JUST LOOP FOR THE SAME SO JUST LOOP SSUED - ERROR FOR THE SAME SO JUST LOOP  SSUED - ERROR FOR THE SAME SO JUST LOOP FOR THE SAME SO JUST LOOP  SSUED - ERROR FOR THE SAME SO JUST LOOP FOR THE SAME SAME SO JUST LOOP  SUEDT AT READ ERROR CODE FEXIT
3 7291 8 24B 1	563 564 565 366 367 569 570 571 572 573 575 576 577 580 581 582 583 584 585 586	TAPE A REOT:	G FROM SEL MOV XRL JZ JOBF MOV CALL MOV JMP PAGE JI	IROFND REOT  TIMER INTERRUPT RO RBO A. LBRDY A. LBOUT RD3  RD3 A. ELBOUT DBB, A A. LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT, #REOTER RDERNS JUMP FOR DRIVE ERRO	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EOTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER  GET READY POINTER FOR THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT TEST DBBOUT - FULL, LOOP JOBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER BUMP POINTER RETURN IT LOOP  SSUED - ERROR FOR THE SAME SO JUST LOOP FOR THE SAME SO JUST LOOP SSUED - ERROR FOR THE SAME SO JUST LOOP  SSUED - ERROR FOR THE SAME SO JUST LOOP  SSUED - ERROR FOR THE SAME SO JUST LOOP  JUST LOOP  SSUED - ERROR FOR THE SAME SAME SO JUST LOOP  JUST LOOP  SELOT AT READ ERROR CODE FEXIT
3 7291 8 24B 1	563 564 565 366 367 569 570 571 572 573 575 576 577 580 581 582 583 584 585 586	TAPE A REOT:	JB5 G FROM ' SEL MOV XRL JZ JOBF MOV OUT MOV JMP T EOT WI MOV JMP	IROFND REOT  TIMER INTERRUPT RO RBO A. LBRDY A. LBOUT RD3  RD3 A. ELBOUT DBB, A A. LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT, #REOTER RDERNS JUMP FOR DRIVE ERRO	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EDTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOTHY IF THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT TEST DBBOUT - FULL, LOOP DBBOUT FREE - GET DATA DUTPUT IT GET OUT POINTER BUMP POINTER RETURN IT LOOP  SSUED - ERROR FOTH THE SAME SO SUST LOOP  SSUED - ERROR FOTH SAME SO SUST LOOP SSUED - ERROR FOTH SAME SO SUST LOOP FOTH SAME SAME SO SUST LOOP FOTH SAME SAME SAME SAME SAME SAME SAME SAME
3 7291 8 24B C C5 D F9 E D8 E D8 D F9 E D8 D F0 D F	563 564 565 366 367 568 570 571 572 573 574 575 576 577 580 581 582 583 584 587 588 587 588	TAPE A REOT:	JB5  G FROM ' SEL MOV XRL JZ  JOBF MOV OUT MOV JMP  T EQT WILL MOV JMP  PAGE JI JMP	IROFND REOT  TIMER INTERRUPT RO RBO A. LBRDY A. LBOUT RD3  RD3 A. ELBOUT DBB, A A. LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT, #REOTER RDERNS JUMP FOR DRIVE ERRO	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EOTFLG SET) - ERROR  UTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FORMARE TO OUT POINTER FEMPTY IF THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT TEST DBBOUT - FULL, LOOP DOBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER RETURN IT LOOP  SSUED - ERROR FEOT AT READ ERROR CODE FEXIT
3 7291 3 7291 3 824B C C5 D F9 E DB E DB	563 564 565 366 367 577 571 572 573 574 577 580 581 582 583 584 589 589 589 590 591	TAPE A REOT: OUT OF DRIVJ:	JB5  G FROM ' SEL MOV XRL JZ  JOBF MOV CALL MOV JMP  PAGE JI JMP  ROUTINE	IRGFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3  RD3 A.ELBOUT DBB.A A.LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT.#REOTER RDERR3 UMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R	; TEST IRO FLAG (IROFLG) ; EOT FOUND DURING READ (EOTFLG SET) - ERROR  IUTINE SO GO HANDLE CIRCULAR BUFFER-  ; COMPARE TO OUT POINTER ; COMPARE TO OUT POINTER ; MATTER PTY SO SEE IF NEXT BYTE CAN BE OUTPUT ; TEST DBBOUT - FULL, LOOP ; DBBOUT FREE - GET DATA ; OUTPUT IT ; GET OUT POINTER ; BUMP POINTER ; BEUMP POINTER ; ECTURN IT ; LOOP  SSUED - ERROR ; EOT AT READ ERROR CODE ; EXIT
3 7291 8 248 3 7291 8 8248 3 7291 8 8248 3 7291 8 8230 8 72430 8 8240 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	563 5645 566 567 577 571 571 577 576 577 578 579 580 581 582 583 584 585 587 588 587 589 590 591	TAPE A REOT: OUT OF DRIVJ: TIMER GETDAT:	JB5 G FROM ' SEL MOV XRL JZ JOBF MOV OUT MOV CALL MOV JMP T EOT WI MOV JMP PAGE JI JMP ROUTINE	IROFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 RD3 RD3 A.&CLBOUT DBB.A A.LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT, #REOTER RDERR3 JMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A. #NOT RDYFLG	FESET DATA READY FLAG (RDYFLG)  FOR THE PARTY PROPERTY OF THE PARTY PARTY PROPERTY OF THE PARTY PROPERTY OF THE PARTY PART
3 7291 3 8248 3 7291 4 8248 3 7291 4 8248 3 7291 4 8248 3 7291 4 82430 4 82430 4 82430 4 82430 4 82430 6 8 8446 6 9 2430 6 9 8 8446 6 9 2430 6 9 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	563 5645 366 367 568 569 570 571 572 573 574 575 575 576 577 580 581 582 583 584 585 587 589 590 591 592 593 592 593 592 593 593 593 593 593 593 593 593 593 593	TAPE A REOT: OUT OF DRIVJ: TIMER GETDAT:	JB5 G FROM ' SEL MOV XRL JZ JOBF MOV OUT MOV CALL MOV JMP T EOT WI MOV JMP PAGE JI JMP ROUTINE	IROFND REOT  REOT  REO REO REO A. LBRDY A. LBOUT RD3 A. ELBOUT DBB, A A. LBOUT BUMPIT LBOUT, A RD3 HEN READ COMMAND I RESULT, #REOTER RDERRS JUMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A. #NOT RDYFLG RSTAT. A	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EDTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER  GET READY POINTER FOR THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT JEST DBBOUT - FULL, LOOP JOBBOUT FREE - GET DATA JOUTPUT IT JOUTPUT IT JOUTPUT IT JECT OUT POINTER RETURN IT JLOOP  SSUED - ERROR JECT AT READ ERROR CODE JEXIT  JECT AT READ ERROR CODE JEXIT  JECT OF STORE READ STATUS
3 7291 3 8248 3 7291 4 8248 5 C.5 5 F.9 5 F.9 5 D.5 6 S.5 6	563 5645 367 368 367 371 372 373 374 375 376 377 378 377 380 381 383 383 384 385 387 387 387 387 387 387 387 387 387 387	TAPE A REOT: OUT OF DRIVJ. TIMER GETDAT:	JB5  G FROM 'SEL MOV XRL JZ JOBF MOV OUT MOV CALL MOV JMP PAGE JI JMP PROUTINE ROUTINE MOV JMP ROUTINE MOV JMP PAGE JI JMP	IROFND REOT TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 A.@LBOUT DBB.A A.LBOUT BUMPIT LBOUT, A RD3 HEN READ COMMAND I RESULT, #REOTER ROERR3 UMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A. #NOT RDYFLG RSTAT. A SNBTST	FEST IRG FLAG (IRGFLG) FOUND DURING READ (EDTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOUND FOR THE SOME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT TEST DBBOUT - FULL, LOOP JOBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER JECT OUT POINTER JECT OUT POINTER JECT AT READ ERROR CODE JEXIT  JECT AT READ STATUS JECT AT READY FLAG (RDYFLG) JECT AT READY FLAG (RDYFLG) JECT AT READY STATUS JECT AT
3 7291 3 7291 4 8248 5 C.5. 5 P.F. 5 D.F. 6 D.F. 6 D.F. 7 C.630 1 8630 3 F.0 1 0.2 3 F.0 3 F.0 4 0.2 3 F.0 4 0.2 5 F.8 5 F.8 6 D.F. 7 2430 6 D.F. 7 2430 6 D.F. 8 D	563 564 565 566 567 577 572 573 577 576 577 580 581 582 583 589 590 591 592 593 593 594 595 595 597 597 597 597 597 597 597 597	TAPE A REOT: OUT OF DRIVU: TIMER GETDAT:	JB5  G FROM ' SEL MOV XRL JZ  JOBF MOV DUT MOV JMP  T EOT WI MOV JMP  ROUTINE  ANL MOV JB1 SEL MOV JB1 SEL MOV JB1 SEL	IRGFND REOT  TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 A.ELBOUT DBB.A A.LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT, #REOTER ROERR3 UMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A. #NOT RDYFLG RSTAT.A SNBTST RBO A.LBOUT	FEST IRG FLAG (IRGFLG) FOR FOUND DURING READ (EDTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOR
3 7291 3 7291 4 8248  C C5 6 F9 E D8 3 F0 4 02 3 F0 4 02 5 F8 3 A8 9 2430  B BA46 0 04DF  F 04C5  I SJFE 3 AB 4 3282 5 C5 F F8 3 D5 F F8	563 5645 565 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 587 587 589 590 591 592 593 593 594 595 595 595 595 595 595 595 595 595	TAPE A REOT: OUT OF DRIVJ: TIMER GETDAT:	JB5  G FROM 'SEL MOV XRL JZ JOBF MOV OUT MOV JMP  T EOT WI MOV JMP  PAGE JI  JMP  ROUTINE  ANL MOV JB1  SEL MOV SEL	IRGFND REOT TIMER INTERRUPT RO RBO A. LBRDY A. LBOUT RD3 RD3 A. ELBOUT DBB. A A. LBOUT BWMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT, #REOTER RDERR3 JMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A. #NOT RDYFLG RSTAT. A SNBTST RBO ALBOUT	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EDTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER  GET READY POINTER FOMPY IF THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT TEST DBBOUT - FULL, LOOP JOBBOUT FREE - GET DATA JOUTPUT IT JOUTPUT IT JOUTPUT IT JOUTPUT IT JECT OUT POINTER RETURN IT LOOP  SSUED - ERROR JECT AT READ ERROR CODE JEXIT  JECT AT READ ERROR CODE JEXIT  JECT AT READ ERROR CODE JEXIT  JECT AT READ STATUS JECT AT READY FLAG (RDYFLG) JESTORE READ STATUS JEST JET DATA SHOULD BE SYNC (SNBFLG SET) JND. TRY TO PUT IN BUFFER JOUTPUTNER JOUTPUT JOUTPUT JUDITER JUDIT
3 7291 3 7291 4 8248 5 C.C.5 6 F.P. 5 D.F.P. 5 D.F.P. 6 D.F. 6 D.F	563 564 565 568 569 570 571 572 573 575 577 578 577 580 581 582 583 584 584 587 590 591 592 593 593 594 595 597 597 597 597 597 597 597 597 597	TAPE A REOT: OUT OF DRIVJ: TIMER GETDAT:	JB5 G FROM ' SEL MOV XRL JZ JDBF MOV DUT MOV CALL MOV JMP T EOT WI MOV JMP ROUTINE ANL JDBF MOV JMP ROUTINE ANL JDBF MOV JMP SEL MOV JMP CALL MOV JMP	IROFND REOT  TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3 A.@LBOUT DBB,A A.LBOUT BUMPIT LBOUT,A RD3 HEN READ COMMAND I RESULT, #REOTER ROERR3  JMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A.#NOT RDYFLG RSTAT.A SNBTST RBO A.LBOUT RBI INMEDIT	FEST IRC FLAG (IRCFLG) FOT FOUND DURING READ (EDTFLG SET) - ERROR  UUTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOTO THE THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT TEST DBBOUT - FULL, LOOP BBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER RETURN IT LOOP  SSUED - ERROR FOTO THE FOULT FOR THE SEME SO FOTO THE SEME SEME SEME SEME SET FOTO THE SEME SEME SEME SEME SEME SEME SET FOTO THE SEME SEME SEME SEME SEME SEME SEME SE
3 7291 3 7291 4 8248  C C5 D F9 E D8 D F8 D	563 5645 565 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 587 587 589 590 591 592 593 593 594 595 595 595 595 595 595 595 595 595	TAPE A REOT: OUT OF DRIVU: TIMER GETDAT:	JB5 G FROM 'SEL MOV XRL JZ JOBF MOV OUT MOV JMP T EOT WI MOV JMP PAGE JI JMP ROUTINE ANL MOV JB1 SEL MOV SEL CALL XRL	IROFND REOT  TIMER INTERRUPT RO RBO A.LBRDY A.LBOUT RD3  RD3 A.@LBOUT DBB.A A.LBOUT BUMPIT LBOUT.A RD3  HEN READ COMMAND I  RESULT, #REOTER RDERR3  UMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A. #NOT RDYFLG RSTAT.A SNBTST RBO A.LBOUT RB1 DUMPIT A.LBIN NDFULL	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EDTFLG SET) - ERROR  ULTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOTO SET IN THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT ITEST DBBOUT - FULL, LOOP JOBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER RETURN IT LOOP  SSUED - ERROR FOTO AT READ ERROR CODE FEXIT  RETURN IT  GET OUT POINTER FOR SEET DATA READY FLAG (RDYFLG) RESTORE READ STATUS RESTORE READ STATUS TEST IF DATA SHOULD BE SYNC (SNBFLG SET) NO. TRY TO PUT IN BUFFER GET OUT POINTER JOUMP IT FOR FULL TEST COMPARE IT TO IN POINTER
3 7291 3 8248 3 7291 4 8248 3 6248 3 6248 3 625 3 63 63 3 63 63 63 3 63 63 63 3 64 62 3 64 62 3 64 62 3 64 62 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 65 64 64 64 3 65 64 64 5 65 64 64 5 65 64 64 5 66 64 64 5 66 64 64 5 66 64	56.3 56.4 56.6 56.7 56.8 56.9 57.7 57.8 57.7 57.8 57.7 58.8 57.9 58.0 58.1 58.2 58.3 58.4 58.5 58.6 58.7 59.3 59.3 59.4 59.5 59.5 59.5 59.5 59.5 59.5 59.5	TAPE A REOT: OUT OF DRIVJ: TIMER GETDAT:	JB5  G FROM 'SEL MOV XRL JZ  JOBF MOV OUT WO CALL MOV JMP  T EOT W MOV JMP  PAGE JI JMP  ROUTINE  ANL MOV JB1 SEL MOV SEL CALL XRL JNZ MOV	IRGFND REOT  TIMER INTERRUPT RO  RBO A. LBRDY A. LBOUT RD3  RD3 A. ELBOUT DBB, A A. LBOUT BUMPIT LBOUT, A RD3  JHEN READ COMMAND I RESULT, #REOTER ROERRS JMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A, #NOT RDYFLG RSTAT. A SNBTST RBO A. LBOUT RBI DUMPIT A. LBOUT RBI NOFULL BESULT, #REOTER ROERRS A, #NOT RDYFLG RSTAT. A SNBTST RBO A. LBOUT RBI DUMPIT A. LBIN NOFULL BESULT, #RUFRIN	FEST IRG FLAG (IRGFLG) FOUND DURING READ (EDTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER-  JUTINE SO SEE IF NEXT BYTE CAN BE OUTPUT SEED TO SEE IF NEXT BYTE CAN BE OUTPUT SEED SOUT - FULL, LOOP  JUDIPUT IT  JUTINE SUMP POINTER  JUTINE SUMP SUMP SUMP SUMP SUMP SUMP SUMP SUMP
3 7291 3 8248 3 7291 4 8248 5 C5 5 F9 5 D F9 5 D B 6 D B 7 C630 1 8630 3 F0 1 02 5 F8 5 5 AC 6 D F9 6 D B 7 C630 1 8630 6 D C400	563 564 565 565 568 569 570 571 572 573 575 575 577 580 581 582 583 584 585 589 590 591 592 593 594 595 594 595 596 597 597 597 598 597 598 598 599 599 591 599 591 592 593 594 595 596 597 597 597 597 597 597 597 597 597 597	TAPE A REOT: OUT OF DRIVJ: TIMER GETDAT:	JB5 G FROM ' SEL MOV XRL JZ JDBF MOV DUT MOV CALL MOV JMP T EOT WI MOV JMP ROUTINE ANL MOV JB1 SEL MOV SEL XRL JNZ MOV JMP	IRGFND REOT  TIMER INTERRUPT RO  RBO A. LBRDY A. LBOUT RD3  RD3 A. ELBOUT DBB, A A. LBOUT BUMPIT LBOUT, A RD3  JHEN READ COMMAND I RESULT, #REOTER ROERRS JMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A, #NOT RDYFLG RSTAT. A SNBTST RBO A. LBOUT RBI DUMPIT A. LBOUT RBI NOFULL BESULT, #REOTER ROERRS A, #NOT RDYFLG RSTAT. A SNBTST RBO A. LBOUT RBI DUMPIT A. LBIN NOFULL BESULT, #RUFRIN	FEST IRG FLAG (IRGFLG) FOUND DURING READ (EDTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER-  JUTINE SO SEE IF NEXT BYTE CAN BE OUTPUT SEED TO SEE IF NEXT BYTE CAN BE OUTPUT SEED SOUT - FULL, LOOP  JUDIPUT IT  JUTINE SUMP POINTER  JUTINE SUMP SUMP SUMP SUMP SUMP SUMP SUMP SUMP
3 7291 3 7291 4 8248 6 C5 6 F9 5 D8 6 G30 6 G3	563 564 565 565 568 569 570 571 572 573 575 575 577 580 581 582 583 584 585 589 590 591 592 593 594 595 596 597 597 598 597 597 598 599 599 599 599 599 599 599 599 599	TAPE A REOT: OUT OF DRIVJ: TIMER GETDAT:	JB5  G FROM 'SEL MOV YRL JZ  JOBF MOV OUT WO WO YMP  T EOT W MOV JMP  PAGE JI JMP  ROUTINE ANL MOV JB1 SEL MOV JB1 SEL YRL JNZ MOV JMP	IRGFND REOT  TIMER INTERRUPT RO  RBO A. LBRDY A. LBOUT RD3  RD3 A. ELBOUT DBB, A A. LBOUT BUMPIT LBOUT, A RD3  JHEN READ COMMAND I RESULT, #REOTER ROERRS JMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A, #NOT RDYFLG RSTAT. A SNBTST RBO A. LBOUT RBI DUMPIT A. LBOUT RBI NOFULL BESULT, #REOTER ROERRS A, #NOT RDYFLG RSTAT. A SNBTST RBO A. LBOUT RBI DUMPIT A. LBIN NOFULL BESULT, #RUFRIN	FEST IRG FLAG (IRGFLG) FOT FOUND DURING READ (EDTFLG SET) - ERROR  ULTINE SO GO HANDLE CIRCULAR BUFFER-  GET READY POINTER FOTO SET IN THE SAME SO JUST LOOP NOT EMPTY SO SEE IF NEXT BYTE CAN BE OUTPUT ITEST DBBOUT - FULL, LOOP JOBBOUT FREE - GET DATA JOUTPUT IT GET OUT POINTER RETURN IT LOOP  SSUED - ERROR FOTO AT READ ERROR CODE FEXIT  RETURN IT  GET OUT POINTER FOR SEET DATA READY FLAG (RDYFLG) RESTORE READ STATUS RESTORE READ STATUS TEST IF DATA SHOULD BE SYNC (SNBFLG SET) NO. TRY TO PUT IN BUFFER GET OUT POINTER JOUMP IT FOR FULL TEST COMPARE IT TO IN POINTER
3 7291 3 8248 3 7291 4 8248 3 6248 3 6248 3 625 3 63 63 3 63 63 63 3 63 63 63 3 64 62 3 64 62 3 64 62 3 64 62 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 64 63 3 65 64 64 64 3 65 64 64 5 65 64 64 5 65 64 64 5 66 64 64 5 66 64 64 5 66 64	56.3 56.4 56.7 56.8 56.9 57.7 57.8 57.9 57.7 57.8 57.9 58.0 58.1 58.1 58.2 58.3 58.4 58.5 58.6 59.7 59.8 59.3 59.1 59.2 59.3 59.1 59.2 59.3 59.1 59.2 59.3 59.1 59.2 59.3 59.1 59.2 59.3 59.3 59.4 59.5 59.6 60.6 60.1	TAPE A REOT: OUT OF DRIVU: TIMER GETDAT:	JB5  G FROM 'SEL MOV YRL JZ  JOBF MOV OUT WO WO YMP  T EOT W MOV JMP  PAGE JI JMP  ROUTINE ANL MOV JB1 SEL MOV JB1 SEL YRL JNZ MOV JMP	IRGFND REOT TIMER INTERRUPT RO RBO A. LBRDY A. LBOUT RD3 RD3 A. ELBOUT DBB. A A. LBOUT BUMPIT LBOUT.A RD3 HEN READ COMMAND I RESULT. #REOTER RDERR3 JUMP FOR DRIVE ERRO DRIVER FLAGGED DATA IS R A. #NOT RDYFLG RSTAT. A SNBTST RBO A. LBOUT RB1 DUMPIT A. LBUN RDERR A. #NOT RDYFLG RSTAT. A SNBTST RB0 A. LBOUT RB1 DUMPIT A. LBUN RDERR A. ROATA RDATA RBO	FEST IRG FLAG (IRGFLG) FOUND DURING READ (ECTFLG SET) - ERROR  JUTINE SO GO HANDLE CIRCULAR BUFFER-  JUTINE SO SEE IF NEXT BYTE CAN BE OUTPUT SENTY BENDT - FULL LOOP  JOBBOUT FREE - GET DATA  JOUTPUT IT  JOUTPUT IN BUFFER  JOUTPUT IT  JOUTP

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AFN-01342A

100 00 1			26 MARCH BO					
LOC OBJ	LINE	SOURCE	STATEMENT					
0167 FE	608	MOV	A, RDATA	GET DATA AGAIN		701 RDIBE		
0168 A0 0169 F8	609 610	MOV	@LBIN, A	PUT IT IN BUFFER TERM				
016A 54CC	611	CALL	DIIMDIT	DUMP IT	16X			
016C A8	612	MOV	LBIN, A	; RETURN IT ; GET READ STATUS ; TEST IF LBRDY SHOULD BE				pard
016D FB	613 00 Tal	MOV	A, RSTAT	GET READ STATUS				
016E 5277	614	JB2	LBTST BAW TI	TEST IF LBRDY SHOULD BE			8/200	0310
0170 C5	615			; BUMPED TOO (SRTFLG RESET)				
0170 C5	616	SEL	RBO A, LBRDY	SRTFLG IS RESET SO GET LBR	DV			
0172 54CC	618	CALL	BUMPIT	BUMP IT	090			
0174 A9	619	MOV	LBRDY, A	RETURN IT				
0175 2430	620	JMP	RD3	GO BACK TO LOOK FOR DATA		STATE OF THE PERSON		
	621 ;	T FLAC IS	GET CEE IE I D	IN HAS ADVANCED FAR ENDUGH TO	CTART	THE LEDDY		
	623 ;	I I LAG 13		IN DERVIEW				
0177 F8	624 LBTST		A, LBIN	GET IN POINTER		716 1 CARRY		
0178 D322	625	XRL	A, #22H	TEST IF READY POINTER SHOU	LD BE	BUMPED		
017A 9630 017C FB	626	JNZ	RD3	; NO, GO BACK FOR DATA ; YES, GET READ STATUS				
017D 53FB	628	ANL						
017F AB	629	MOV	RSTAT, A	RESTORE STATUS		VEL SKIPER.		
0180 2430	630	JMP	RD3	RESTORE STATUS GO BACK TO LOOK FOR DATA				
	631 ;							
	632 ; DATA	SHOULD B	E SYNC - TEST IT					
0182 FE	634 SNBTS	T MOV	A, RDATA	GET DATA VASAUE.A				
0183 D3AA	635	XRL	A, #SYNC	COMPARE TO SYNC A MITALE				
0185 C68B	636	JZ H	RSNB	COMPARE TO SYNC				
0187 BA42 0189 04D4	637 638	MOU	RESULT #SYNC1	TT'C NOT A CVNC DAR FIRET	SYNC	ERROR CODE		
0189 04D4 018B FB	639 PCNP	MOU	A RSTAT	EXIT READ ERROR, ADVANCE T	O NEXT	IRG OLV		
018C 53FD	640	ANL	A, #NOT SNRFLG	RESET SNR FLAG	STATUS			
018E AB	641	MOV	RSTAT, A	RESET SNB FLAG RESTORE STATUS GO BACK TO LOOK FOR DATA				
018F 2430	642	JMP	RD3	GO BACK TO LOOK FOR DATA				
	643 .	COUNTRACT						
	645 ;	FUUND - I	EST FUR SYNC, CUI	RECT AND TEST CHECKSUM				
0191 C5	646 IRGEN	D: SEL	RBO - 10 ABUNUM	SI BIVE ATAC TRUE - SMITUSE				
0192 FF	647	MOV	A, STAT	GET STS IMAGE				
0193 53EF	648	ANL	A, #NOT DRACT	RESET DRIVE ACTIVE	****			
0195 AF 0196 90	649	MOV	STAT, A	RESTORE IMAGE				
0197 BA02	650 651	MOV	515, A	UPDATE STS				
0199 D5	652	SEL	RB1	; UPDATE STS ; TURN OFF DRIVE ACTIVE LED				
019A F8	000	MOV			LIAD	est		
019B 54D3	654	CALL				IAS SYNC	1 B904	
019D AB 019E F0	655	MOV	LBIN, A	DEC IT TO POINT AT LAST DA RETURN IT GET LAST DATA COMPARE TO SYNC NOT EQUAL - ERROR		747		
019F D3AA	656 657	YRI	A #SYNC	GET LAST DATA				
01A1 96BA	658	JNZ	IRGF1	NOT EQUAL - ERROR				
01A3 F8	659	MOV	A, LBIN	GET POINTER AGAIN				
01A4 54D3	660	CALL	DUMPIT					
01A6 A8	661 662	MOV	LRIN. A BUTATE	; TO LAST DATA, ALIAS CHECKS ; RETURN IT	UM			
01A7 C5	663	SEL		SKIPE STATUS SA				
01A8 FB	664	MOV		GET ACCUMULATED CHECKSUM				
01A9 0356 01AB AB	665	ADD	A, #56H	RESTORE CHECKSUM				
OIAC D5	666 667	SEL	DD1					
O1AD FO	668	MOV	A, @LBIN	GET RECEIVED CHECKSUM				
01AE C5						Tot SKIPR		
01AF 37	670	CPL	A TENS TUDBA YE	SUBTRACT IT OUT - MAKE IT	MINUS		PAGE 7	
01B0 17 01B1 6B	671 672	ADD	A CURCUMPT TOTAL	Opine take a makin w				
01B2 D5	673	SEL	RB1	SUBTRACT FROM ACC CHECKSUM				
01B3 D0	674		A. OLBIN	COMPARE RESULT TO RECEIVED				
01B4 96BE	675	JNZ	CKSER	NOT FOLIAL THEM SHEET STATES	2427794			
01B6 BA00	676	MOV	RESULT, #GOOD	FOUND THEN COOD RESULT		768		
01B8 24C0 01BA BA43	677	JMP	BUFFER		OUTPL	JTTING RESULT		
O1BC O4DF	678 IRGF1	JMP	RDERR3	2ND SYNC ERROR CODE				
OIBE BA44	680 CKSER		RESULT, #BADCHS	EXIT				
	681 ;		WEDGE 17 #BHDCHS	, BAD CHECKSON ERROR CODE BU				
	682 ; DONE	WITH REAL	- LET BUFFER EM	PTY BEFORE OUTPUTTING RESULT				
01C0 C5	003 ,							
01C1 F8	684 BUFFER	R: SEL MOV	RBO A, LBOUT	TOTAL POLITICAL STATES				
01C2 D9	686	XRL	A, LBRDY	GET OUT POINTER COMPARE TO READY POINTER				
0103 9607	687	JNZ				- 779 SKIPLE		
01C5 04DF	688	JMP	TINE THE	, BUFFER IS EMPIY - GU UUIPU	RESUL	T 087		
01C7 D6CB 01C9 24D5	689 BUF1:	JNIBF	BUF2	, IEST FUR INPUT	0.31	287		
01CB 86C7	690 691 BUF2	JMP JOBF	RDIBF BUF1	IF INPUT, GO TEST IT				
O1CD FO	692	MOV	A, @I BOUT	TEST OBF		VB4		
01CE 02	693	OUT	DBB. A	; OBF FREE, GET DATA FROM BUF ; OUTPUT IT ; GET OUT POINTER	PER			
01CF F8 01D0 54CC	694	MOV				798		
	695	CALL	BUMPIT	BUMP IT TO POINT AT NEXT DA	ATA			
			LBOUT, A	RETURN IT				
01D2 A8	696 697	MOV		OD TEST IT DONE				
	696 697 698 ;	JMP	BUFFER	GO TEST IT DONE		790 SKIP13.		

				MARCH BO			
DC OB1	LINE		SOURCE S	STATEMENT			
1D5 22		RDIBF:		A, DBB MIAGA			
1D6 76DA 1D8 2430	702		JF1 JMP	ABISI 9333	MUST BE DATA, IGNORE IT		
1DA D305		ABTST:	XRL	A, #ABORT	COMPARE TO ABORT COMMAND		
1DC 9630	705		JNZ		; COMPARE TO ABORT COMMAND ; NOT EQUAL, IGNORE IT		
1DE BA01 1E0 04D4	706 707	ABTST1:	JMP	RESULT, #ABTCMP	; IT IS AN ABORT, ABORT COMP ; EXIT LIKE IT WAS AN ERROR,	ADVANCE TO IRG	
	708 709	\$EJECT		( CERTIFILD RESET)			
200	710		ORG	200H	A LBRDY SERVICE IS		
	711					- VQM 918	
	713	i			<del>获</del>		
	715	SPEED	PASSED	IN BLKTIM.	TO NEXT IRG BASED ON DIRECTIO	IN AND TRATE, SSA	
	716 717	; CARRY=	AND EXI	OT ENCOUNTERED.	CARRY=1, EOT ENCOUNTERED		
	/10	,		ON FOR DATA	A	258 058	
	720					JAA 85a	
200 97	721	SKIPER:	CLR	C PUTAT	CLEAR EDT INTERNAL FLAG		
201 09	722		IN	A.P1 NOW ADD A	READ DRIVE STATUS		
202 9212	723		JB4	SKIPR3	TEST FOR CLEAR LEADER	TANDUT TO UTOU	
204 4600 206 560C	724 725	SKIPR1:	JNT1	SKIPR2	READ DRIVE STATUS TEST FOR CLEAR LEADER NO CLEAR LEADER WAIT UNTI WHILE INPUT IS HIGH, DEC B INPUT WENT LOW, RESET BLKT	I KTIM COUNTER	
208 FE	726	SKII KI.	MOV	A, BLKSAV	INPUT WENT LOW, RESET BLKT	IM COUNTER	
209 AD	727		MOV	BLKTIM, A			
20A 4400	728		JMP	SKIPER	GO WAIT UNTIL INPUT IS HIG	H AGAIN	
200 09							
20D 9212 20F ED06	730 731		JB4	SKIPR3	TEST CLEAR LEADER - ERROR	IF TRUE	0400
211 83	731		RET	BLK I III, SKIPKI	; INPUT STILL HIGH, DEC BLKT	THE COUNTER AND A PER	
212 A7		SKIPR3:		C SUTAT	RETURN WHEN AT IRG		
213 83	734 735			O LOOK FOR DATA	RETURN		
			*****	****	*************		
	737	1					
	738 739	SKIP C	DMMAND		ATA BYTE IS NUMBER OF IRG'S T		
			*****		***	647	
	741	,	,				
214 D614	742	SKIP:	JNIBF	SKIP	WAIT FOR SKIP COUNT INPUT		
216 7692			JF1	CMDINJ	TEST IF COMMAND INSTEAD -	EXIL IF YES	
218 85 218 54BC	744		CLR	FO	CLEAR DIRECTION FLAG - DEF	AULT FORWARI)	
219 54BC 21B 8904	745		CALL	P1. #SLOW	START OUT SLOW		
21D 22	747		IN	A, DBB	START OUT SLOW READ SKIP COUNT INPUT		
21E AC	748		MOV	BLKCNT, A	SAVE IT IN BLOCK COUNTER	VON CEA	
21F F262	749		JB7	RSKIP	, IF BIT 7 SET, IT'S A REVER	74.7	
	751	FORWAR	D SKIP		THE BIT 7 SET, IT'S A REVER		
221 D5	752 753		SEL	RB1		LLAND DEG	
555, LB	754		MOV	A, RSTAT	GET READ STATUS	VOH 188	
223 B278	755		JB5	SKIPB	STATUS SAYS WE'RE AT EOT -	EXIT WITH ERROR	
225 99F4	756		ANL	P1. #FORWD AND	SRT AND RD ; IT'S GO -	FORWARD	
227 C5 228 37	757		SEL	RBO		695 [ ADD	
228 3/ 229 D22D	758 759		CPL JB6	A MUSAUSH SKIP2	; COMP A FOR O TEST	O SKIP	
22B 54DC		SKIP1:		PASHOL	AT BOT SO GET PAST CLEAR L		
22D 14C1	761	SKIP2:	CALL	DEL 150	; WAIT OUT JUNK AT BEGINNING	OF EACH BLOCK	
22F B644	762	SKIP3:	JF0	SKIP6	DON'T WORRY ABOUT FAST OR		
231 FC 232 03F8	763 764		ADD -	A, BLKCNT	GET BLOCK COUNT		
34 F63E			JC	SKIP4	; SEE IF COUNT IS >B ; YES, USE FAST IRG TIMING		
236 BD33	766		MOV	BLKTIM, #SLWIRG	COUNT IS <8, USE SLOW IRG	TIMING	
38 BE33	767		MOV	BLKSAV, #SLWIRG			
3A 8904	768		ORL	P1, #SLOW	SELECT SLOW		
3C 4444 3E BD20		SKIP4:	JMP MOV	SKIPA	GO DO SKIP	TIMING	
40 BE20	771		MOV	BLKSAV, #FASIRG	COUNT IS >8, USE FAST IRG		
242 99FB	772		ANL	P1, #FAST SKIP7	SELECT FAST WAIT FOR SPACE TO START IR	680 CKSER LNDL	
44 464B	773	SKIP6:	JNT1 IN	A.PI	READ DRIVE STATUS	G FIND	
47 9278	775		JB4	SKIPS	READ DRIVE STATUS	F FOUND	
49 4444	776		JMP	CKID4	CONTINUE TO HATT FOR CRACE		
		SKIP7:		SKIP12	TEST IBF WHILE SKIPPING IBF SET, GO TEST IT DO SKIP TO IRG		
4B D64F	778	SKIPIO		SKIP11	IBF SET, GO TEST IT		
24B D64F 24D 4487	780	JAIF12	JC 100	SKIPE	DO SKIP TO IRG		
24B D64F 24D 4487 24F 5400		T.	DJNZ	BLKCNT, SKIP2		AMP BB4	
24B D64F 24D 4487 24F 5400 251 F678 253 EC2D	781		JF0	SKIP13	DELAY A LITTLE IF REVERSE	SET BUFT JUE 198	
24B D64F 24D 4487 24F 5400 251 F678 253 EC2D 255 B65E	781 782		SEL	RB1	Tipode Procure (SUE		
24B D64F 24D 4487 24F 5400 251 F67B 253 EC2D 255 B65E 257 D5	781 782 783	SKIP14:	MOL	DECLU T			
24B D64F 24D 4487 24F 5400 251 F67B 253 EC2D 255 B65E 257 D5	781 782 783 784			PSTAT #00U	CLEAR READ STATUS	AV1 BUFE JUBE	
24B D64F 24D 44B7 24F 5400 251 F67B 253 EC2D 255 B65E 257 D5 258 BA00	781 782 783		MOV	PSTAT #00U	CLEAR READ STATUS		
24B D64F 24D 44B7 24F 5400 251 F67B 253 EC2D 255 B65E 257 D5 258 BA00	781 782 783 784 785 786 787	į	MOV JMP	RSTAT, #OOH RDERR3	CLEAR READ STATUS USE READ EXIT TO COMPLETE		
257 4448 D64F 24B D64F 24F 5400 251 F67B 253 EC2D 255 B65E 257 D5 258 BA00 258 BA00 250 BB00	781 782 783 784 785 786 787 788	; ; REVERSI	MOV JMP	PSTAT #00U	COUNT EXPIRED		
24B D64F 24D 44B7 24F 5400 251 F67B 253 EC2D 255 B65E 257 D5 258 BA00	781 782 783 784 785 786 787 788 789	; ; REVERSI	MOV JMP	RSTAT, #00H RDERR3	CLEAR READ STATUS USE READ EXIT TO COMPLETE		

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 DIGITAL CASSETTE CONTROLLER REV 1.0 - 26 MARCH 80 LOC OBJ LINE SOURCE STATEMENT 793 REVERSE SKIP IS DESIRED - SETUP DRIVE AND DIRECTION FLAG 794 FO ,SET DIRECTION FLAG
A.#7FH ,MASK OFF DIRECTION
BLKCNT. A ,RESTORE BLKCNT
BLKTIM. #RMDIRG ,SET REWIND BLOCK TIMER
BLKSAV.#RWDIRG 795 RSKIP 0263 537F 796 ANI 0265 AC MOV 0266 BD20 79B MOV 0268 BE20 MOV BLKSAV. #RWDIRG
RB1
A.RSTAT ; GET READ STATUS
SKIPB ; AT BOT SO EXIT WITH ERROR
P1. #REWIND ; SELECT REVERSE 026A D5 800 SEL 026B FB 801 MOV 026C D278 802 .IBA 026E 8901 803 ORL 0270 9955 804 RBO 0272 C5 805 SEL A , COMP A FOR O TEST
SKIP2 ; NOT AT EOT SO JUST DO SKIP
SKIP1 ; AT EOT SO WAIT PAST CLEAR LEADER AND HOLE 0273 37 0274 B22D 806 807 JB5 0276 442B 808 JMP 809 810 ; CLEAR LEADER FOUND DURING SKIP OR TAPE ALREADY AT EOT OR BOT WIND MICE. 811 0278 D5 812 SKIPB: SEL TEST DIRECTION
TYS FORWARD SO IT'S EOT
SET EOT FLAG
GO EXIT SKIPP 0279 BAB1 813 JEO RESULT, #SKPEOT 027B BA47 814 MOV RESULT. #SNPBOT SET EOT FLAG
RDERR3
RSULT. #SNPBOT SET EOT FLAG
RSULT. #SNPBOT SET BOT FLAG
RSTAT. #BDTFLG
RSTAT. #BDTFLG
RSTAT. #BDTFLG 027D BB20 815 MOV 027F 04DF 0281 BA48 817 SKIPS MOV 0283 BB40 818 MOV 0285 04DE 819 IMP RDERR3 GO EXIT 821 ; IBF FOUND SET DURING SKIP - TEST INPUT READ INPUT
TEST IF ABORT
JONORE IT IF NOT
STOP DRIVE
TURN OFF DRIVE ACTIVE LED
YES - EXIT WITH RESULT A, DBB SI SI SI A, #ABORT 823 SKIP11: IN 0287 22 0288 D305 XRL 028A 964F 825 JN7 SKIP12 P1,#STP 0280 8902 826 ORL 028E 8A02 827 ORI P2, #DAOFF ABTST1 0290 24DE 828 829 : OUT OF PAGE JUMP FOR CMDIN 831 832 CMDINJ: JMP CMDIN3 0292 0433 833 ; 834 ; \*\*\* 835 836 REWIND COMMAND - STOP WHEN CLEAR LEADER IS FOUND FOR >50MS. 837 839 SELTITO RB1 \*\*\* PROTECTION OF STREET CONTRACTOR CONTRAC 840 REWND: 0294 D5 A, RSTAT ; GET READ STATUS
REWND4 ; TEST IF ALREADY AT BOT - EXIT IF YES 841 MOV 0296 D2B8 842 JB6 SEL 843 RBO
DRACTS ; SET DRIVE ACTIVE
P1.#RD AND FAST ; SELECT RD AND FAST
P1.#REWIND ; SELECT REWIND
P1.#SRT ; START DRIVE 0299 54BC 844 CALL 845 029D 8901 846 ORL 029F 99FD ANL 02A1 14B8 848 REWND1: CALL 02A3 09 IN 02A4 92A8 850 JRA 02A6 44A1 851 JMP 02A8 14B8 852 REWND2: CALL 02AA 09 853 IN 02AB 92AF JRA 854 02AD 44A1 JMP 02AF 8906 856 REWNDS ORI 02B1 99FE ANL 02B3 14B8 858 CALL RE11
RSTAT.\*BOTFLG AND (NOT EOTFLG) ; SET UP READ STATUS
RESULT.\*BODD ; GOOD RESULT
RDERR3 ; GO OUTPUT RESULT 02B5 D5 859 SEL 02B6 BB40 860 MOV 02BB BA00 861 REWND4: 02BA 04DF 862 JMP 863 ; 864 \$EJECT

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ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0
DIGITAL CASSETTE CONTROLLER REV 1.0 - 26 MARCH 80
  LOC OBJ
                            SOURCE STATEMENT
                   LINE
                    865 ; ****************************
                    866 ; DRIVE ACTIVE STATUS SUBROUTINE - ENTER/EXIT IN RBO
868 ; DRIVE ACTIVE BIT IN STATUS IS SET AND DRIVE ACTIVE LED IS TURNED ON
                    870; **********************
                    871
                    872 DRACTS: MOV
                                        A, *DRACT , SET DRIVE ACTIVE BIT
STAT, A , RESTORE IMAGE
STS, A , UPDATE STS
  02BD 4310
                    873
                                ORL
  02BF AF
                    874
  0200 90
                    875
                                MOV
                                                   TURN ON DRIVE ACTIVE LED
  02C1 9AFD
                    876
                                ANL
                                        P2. #DAON
  0203 83
                    877
                                RET
                                                         RETURN
                    878 ;
                    880 ;
                    881 ; DRIVE INACTIVE STATUS SUBROUTINE - ENTER/EXIT IN RBO
882 ; BOTH DRIVE ACTIVE AND BUSY BITS IN STATUS ARE RESET, DRIVE ACTIVE LED IS OFF
                    883 ;
                                        A, STAT GET STS IMAGE
A, WNOT (BUSY OR DRACT) RESET DRACT AND BUSY
STAT, A RESTORE IMAGE
STS. A UPDATE STS
P2. #DAOFF TURN OFF DRIVE ACTIVE LED
                    885 ;
                    886 NDRACT:
  02C4 FF
  02C5 536F
02C7 AF
                    887
                                ANL
                                MOV
  0208 90
                    889
                                MOV
  02C9 8A02
                    890
                                ORL
  02CB 83
                    891
                                RET
                    893 ; ***********************
                    894 ; BUMPIT - POINTER MANAGEMENT - VALUE IN A IS INCREMENTED AND TESTED 896 ; FOR OVERFLOW. IF OVERFLOW OCCURS, SET A TO BOTTOM OF BUFFER.
                    898 ; ***************************
                    899
                    899 ;
900 BUMPIT: INC A ; INC A
901 JB6 OVFLOW ; TEST F
                                                         02CC 17
  OSCD DSDO
                    901 JB6
902 RET
903 OVFLOW: MOV
                                                        NO OVERFLOW, RET
  02CF 83
  05D0 5350
                                        A, #20H
                                                                     CADINAL UNP CHOINS
  02D2 83
                    904
                                RET
                                                         RETURN
                    905
                    906 $EJECT
907 ; *****
                        908;
                    908;
909 :DUMPIT - POINTER MANAGEMENT - VALUE IN A IS DECREMENTED AND TESTED
910 :FOR UNDERFLOW IF UNDERFLOW OCCURS, SET A TO TOP OF BUFFER.
                    911
                    912 ; *************************
                                        A TOS TA VOASILA ; DEC A
                    913 :
                    914 DUMPIT: DEC
  02D4 37
                    915
                                CPL
JB5
                                       A UNFLOW TEST IF UNDERFLOW A NO. COMP BACK
A RETURN
A.#3FH UNDERFLOW SO RESET A RETURN
  02D5 B2D9
                    916
  02D7 37
                    917
                                CPL
  02D8 83
                                RET
                    919 UNFLOW: MOV
  02D9 233F
  02DB 83
                    921 ;
                        ; ******************************
                    923 ;
                    924 ; SUBROUTINE TO GET PAST HOLE IN TAPE
                    926 ; **************************
                                                  ,READ DRIVE STATUS
WAIT UNTIL OFF CLEAR LEADER
READ DRIVE STATUS AGAIN
COMP A FOR O TEST
WAIT UNTIL HOLE
READ DRIVE STATUS
                    927
                                        A, P1
PASHOL
  05DC 03
                    928 PASHOL: IN
                    928 FAL...
929 JB4
930 PAS1: IN
CPL
  02DD 92DC
                                        A. P1
  02DF 09
                                                   WAIT UNTIL HOLE
  02E1 92DF
                    932
                                 JB4
                                        PAS1
  02E3 09
                    933 PAS2
                                 IN
                                                         ; WAIT UNTIL PAST HOLE
  02E4 92E3
                    934
                                JR4
                                        PAS2
  02E6 83
                    936
                    937 $EJECT
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ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3. 0 DIGITAL CASSETTE CONTROLLER REV 1. 0 - 26 MARCH 80

1988   DRG	SITAL CASS	ETTE CONTRO	LLER REV	1.0 - 2	6 MARCH 80	SOURCE STATEMENT
939   940	OC OBJ	LINE		SOURCE S	TATEMENT	
940   941   942   1   942   1   942   1   942   1   942   1   942   1   943   943   943   943   943   944   945   945   945   945   946   947   948	300	938		DRG	300H	
941   942   THER INTERRUPT ROUTINES - FIRST DECIDE IF IT'S READ OR WRITE   943   945						
942   TIMER INTERRUPT ROUTINES - FIRST DECIDE IF IT'S READ OR WRITE 943   943   944   947   947   947   948   948   949				******	******	*************
1943				INTERRUP	T POUTINES - FIR	ST DECIDE IE IT'S READ OR WRITE
1945   1945   1946   1947   1947   1947   1948		943	, The same	THILKNON	THAT EMOD SHIT	TAIN TAD MERTE NOT THE
100   100		944	; ****	*****	******	***
101 AF 947 MOV ASAVE A SAVE ACCUMULATOR 947 MOV ASAVE A SAVE ACCUMULATOR 948 MOV A RESTAT SERIOISTER 15 948 MOV A RESTAT SERIOISTER 15 PAGE 15	200 DE			051	TABLETONNE TONO	
100 F 29		946	INT:			
103   F25E						GET CURRENT STATUS REGISTER
950   OTHERNISE, IT'S A READ   973   973   973   973   974   975	303 F25E	949			WRINT	: IF RD/WR FLAG SET, IT'S A WRITE
952   953						OTHERWISE, IT'S A READ
953 ; READ INTERRUPT ROUTINE 955 ; 954 ; READ INTERRUPT ROUTINE 955 ; 956 ; 957 958 RDINT: CLR C CLEAR SHIFTER 955 ; 956 ; 957 958 RDINT: CLR C CLEAR SHIFTER 956 ; 950 JFO RDI2 INPUT=0. TEST LAST 100 S6612 960 JFO RDI2 INPUT=0. LAST-0. SHIFT IN O CLEAR SHIFTER 956 JFO RDI2 INPUT=0. LAST-0. SHIFT IN O CLEAR SHIFTER 956 JFO RDI2 INPUT=0. LAST-0. SHIFT IN O CLEAR SHIFTER 956 JFO RDI2 CLEAR SHIFTER 956 JFO RDI2 CLEAR SHIFT IN O						
994 READ INTERRUPT ROUTINE 955 : 956 : 957   958   958   958   959   959   951   951   952   953   953   954   957   958   951   957   958   958   958   959   950   950   951   951   951   951   952   953   954   954   954   954   954   954   954   954   954   954   954   954   955   954   954   954   955   954   954   955   954   954   954   955   954   955   954   955   954   955   954   955   954   955   954   955   954   955   954   955   956   957   958   957   958   958   959   959   950				****	*****	*******
955; 957; 958; 959; 957; 958; 959; 968; 9612; 969; 971; 971; 971; 972; 973; 974; 975; 975; 976; 976; 976; 977; 977; 978; 979; 970; 970; 971; 971; 971; 971; 971; 971; 971; 971				NTERRUPT	ROUTINE	
997   998 RDINT: CLR						
0.5   977   998 RDINT:   CLR   C   CLEAR SHIFTER     0.6   36012   960				*****	*****	**
100   250						TATION TO THE TATION OF THE PROPERTY OF THE PR
100 B016				CLR	C	CLEAR SHIFTER
100 B016				JEO	PDI2	TAPLITED TEST LAST
100 B016				JMP	SHIFIN	INPUT=0, LAST=0, SHIFT IN 0
10   6416   765   766   767   768   767   768   767   768	OC B616	962	RDI1:	JFO	RDI3 A7	; INPUT=1, TEST LAST
10   6416   765	OE A7	963			C	; INPUT=1, LAST=0, SHIFT IN 1
10   10   10   10   10   10   10   10						
13 99					SHIFIN	
14 416   968	13 95				FO	SET FO TO CURRENT VALUE OF DATA IN
117 67   971		968			SHIFIN	RIA ANL RA- NDOLON
117 67   971						; INPUT=1, LAST=1, SHIFT IN 0
19 AD   972				MOV	A, DESERL	GET CURRENT VALUE OF DATA BYTE
19 EC22 973 D.NZ BITCNT.RD14 , TEST IF BYTE DDNE 18 AE 974 MOV RDATA, A ; IT'S DDNE, BUFFER IT IN RDATA 16 B608 975 MOV BITCNT.**RDCNT ; RESET BIT COUNTER 1F 4301 976 MOV A. RSTAT ; GET READ STATUS 1F 4301 977 MOV RSTAT. A ; RESTORE STATUS 22 AS 978 MOV RSTAT. A ; RESTORE STATUS 22 AS 979 RD14. STOP TCNT ; STOP COUNTER 23 2374 980 MOV A. **RDTH ; GET TIMER CONSTANT (3/4 CELL TIME) 25 A2 981 MOV T. A ; LOAD TIMER 26 B933 982 MOV IRGCNT.**SLWING ; LOAD TIMER 28 OP 983 RD17: IN A.PI ; READ DRIVE STATUS 28 OP 983 RD17: IN A.PI ; READ DRIVE STATUS 29 9254 984 JB4 RD19 ; TEST IF CLEAR LEADER FOUND - ERROR 29 9254 985 JTI RD15 ; TEST INPUT LODKING FOR EDGE 29 B650 986 JFO RD16 ; INPUT-0.0 TEST LAST 21 B902 986 BD RD. PI, #STP ; COUNT EXPIRED, AT IRG. STOP DRIVE 23 BAO2 989 DRL PI, #STP ; COUNT EXPIRED, AT IRG. STOP DRIVE 23 BAO2 989 DRL PI, #STP ; COUNT EXPIRED, AT IRG. STOP DRIVE 25 F9 990 MOV A. RSTAT ; GET READ STATUS 26 AS 991 DRL A. #IRGFLG ; SET IRG FOUND FLAG 27 P95 ; 29 P25 MOV A. RSTAT ; GET READ STATUS 29 P3 INTEXT: MOV A. PSW ; RESTORE STATUS 29 P3 INTEXT: MOV A. PSW ; GET IRG FOUND FLAG 25 F9 990 MOV A. RSTAT ; GET READ STATUS 26 P3 P3 RD INTEXT: MOV A. PSW ; RESTORE STATUS 27 P3 RL A ; PST RESTORE STACK POINTER ONLY 28 DAGA P3 P3 RD				RRC	A DECERI A	SHIFT IN NEW BIT
18 AE 974 MOV RDATA, A ; IT'S DONE, BUFFER IT IN RDATA   16 F68 975 MOV BITCHT, #RDCHT   16 F68 976 MOV BITCHT, #RDCHT   16 F68 976 MOV BITCHT, #RDCHT   17 A301 977 ORL A #RDYPLG   18 AB 978 MOV RSTAT, A ; RESTORE STATUS   19 A201 977 ORL A #RDYPLG   19 A201 977 ORL A #RDYPLG   10 A2 SET TIMER COMSTANT (3/4 CELL TIME)   19 A22 AS 978 MOV A #RDTIM ; GET TIMER COMSTANT (3/4 CELL TIME)   19 A23 980 MOV T. A   10 A201 MOV T. A   10					BITCHT, RD14	TEST IF BYTE DONE
1C BCOB					RDATA, A	IT'S DONE, BUFFER IT IN RDATA
1E FB				MOV	BITCHT, #RDCHT	RESET BIT COUNTER
21 AB 978 MOV RSTAT.A RESTORE STATUS 22 255 979 RD14: STOP TCNT STOP COUNTER 23 23FA 980 MOV A, #RDTIM GET TIMER CONSTANT (3/4 CELL TIME) 25 62 981 MOV TA LOAD TIMER 26 8933 982 MOV IRGENT.#SLHIRG LOAD IRGE COUNT (READ USES SLOW SPEED) 27 9254 984 JB4 RD19 TEST IF CLOAD IRGE COUNT GREAD USES SLOW SPEED) 28 985 JT1 N A,P1 TEST IF CLOAD IRGE COUNT GREAD USES SLOW SPEED) 28 564 985 JT1 RD15 TEST INPUT.LOANING FOR EDGE 28 18 564 985 JT1 RD15 TEST INPUT.LOANING FOR EDGE 29 8650 986 JF0 RD16: JNNZ IRGENT.RD17 INPUT/LAST SAME, DEC IRG COUNT 21 8902 988 ORL P1.**STP COUNT ESTLAST 21 8902 989 ORL P2.**BDADFF TURN OFF DRIVE ACTIVE LED 23 8A02 989 ORL P2.**BDADFF TURN OFF DRIVE ACTIVE LED 24 8A 9791 ORL A.**IRGFLG SET IRG COUNT GREAD STATUS 25 8A 9792 ORL A.**IRGFLG SET IRG COUNT GREAD STATUS 26 8A 9793 TORL A.**IRGFLG SET IRG COUNT GREAD STATUS 27 974 INTERRUPT EXIT ROUTINE - UPDATES FO IN STACK TO PRESERVE IT OVER RETR 27 975 NAL A.**O77H LOOM AT STACK POINTER ONLY 28 AD 1001 ADD A.**O8H ADD OFFSET FOR POINTER ONLY 29 979 RL A PRIVING TO GET PSW ON TOP OF STACK 29 1004 JF0 EXIT GROWN A.**ORPH SET OF THE STACK POINTER 42 F1 1003 MOV A.**ORPH ADD OFFSET FOR POINTER 42 F1 1003 MOV A.**ORPH ADD OFFSET FOR POINTER 43 B649 1004 JF0 EXIT GROWN A.**ORPH SET OF THE SET OF THE STACK 44 BA 1008 EXITE MOV A.**ASAVE FEB ON TO SEE WHAT TO SET FO TO 45 30DF MOV A.**ASAVE FEB ON TO SEE WHAT TO SET FO TO 46 A 3 BCAP 1001 RETR 46 B62F 1012 RD15: JF0 RD18 INFECT A.**RESTORE STACK 46 FF 1009 MOV A.**ASAVE FEB ON TO SEE WHAT TO SET FO TO CURRENT IN 50 26 4039 1010 RETR 50 4030 NOV A.**ASAVE FEB ON TO SEE WHAT TO SET FO TO CURRENT IN 50 26 4039 1010 RETR 50 40 50 FINALLY DIFFERENT. SET FO TO CURRENT IN 50 50 40 1017 RD19: MOV A.**RSTAT GET READ STATUS 50 50 1013 RD16: CPL F0 FINALLY DIFFERENT. SET FO TO CURRENT IN 50 50 1013 RD16: CPL F0 FINALLY DIFFERENT. SET FO TO CURRENT IN 50 50 40 1019 MOV STAT.A. RESTORE STATUS 50 50 1013 RD16: CPL F0 FINALLY DIFFERENT. SET FO TO CURRENT IN 50 50 40 1019 MOV STAT.A. RESTORE STATUS 50 50 1010 ORL P1.**S				MOV	A. RSTAT	GET READ STATUS
23 23FA 980 MOV A, #RDTIM GET TIMER CONSTANT (3/4 CELL TIME) 25 62 981 MOV TA LOAD TIMER 26 8933 982 MOV IRCCNT.#SLWIRG LOAD TIMER 27 9254 984 JB4 RD19 LOAD TIMER 28 99 983 RD17: IN A,P1 READ DRIVE STATUS 28 99 983 RD17: IN A,P1 REST IF CLEAR LEADER FOUND - ERROR 29 9254 984 JB4 RD19 TEST IF CLEAR LEADER FOUND - ERROR 29 9254 985 JT1 RD15 TEST INPUT-LODKING FOR EDGE 20 8650 986 DR16 JND2 IRCCNT.RD17 INPUT-LOAD TIME FOR EDGE 27 6928 987 RD18: DJNZ IRCCNT.RD17 INPUT-LOAT SAME, DEC IRC COUNT 28 18902 988 ORL P1: #STP COUNT EXPIRED, AT IRC, STOP DRIVE 29 989 ORL P2: #DADFF TURN DFF DRIVE ACTIVE LED 33 FB 990 MOV A, #STAT GET READ STATUS 36 4308 991 ORL A, #IRGFLG SET IRG FOUND FLAG 38 AB 992 MOV RSTAT, A RESTORE STATUS 39 C7 994 INTERRUPT EXIT ROUTINE - UPDATES FO IN STACK TO PRESERVE IT OVER RETR 39 C7 996 IN A, #OFH LOOK AT STACK POINTER ONLY 30 O7 998 DEC A TRYING TO GET PSW ON TOP OF STACK 30 E7 999 RL A 2 BYTES PER STACK ENTRY 31 GOT 999 RL A 2 BYTES PER STACK ENTRY 32 GOT 999 RL A 2 BYTES PER STACK ENTRY 32 GOT 999 RL A 2 BYTES PER STACK ENTRY 33 GOT 999 RL A 2 BYTES PER STACK ENTRY 34 OND INC A 1 POINTER TOR DINTER 35 GOT 990 MOV A, #OBH ADD DEFFSET FOR POINTER 36 AS 300 MOV A 2 ERGCNT, A TLOAD POINTER TOR DINTER 37 GOOD MOV A, #OBH ADD OFFSET FOR POINTER 38 AB 999 MOV A 2 ERGCNT, A RESTORE STACK 39 C7 999 RL A 1 BYTE PROTECT FOR POINTER 39 GOOD MOV A STACK OF PSW 40 A BASAVE RECOVER A 1 RECOVER A 1 RESTORE 40 BASAP MOV A ASAVE RECOVER A 1 RESTORE STACK 40 PO 1010 RETR 40 BASAP MOV A ASAVE RECOVER A 1 RESTORE STACK 40 PO 1014 STATE TO THE STACK AND THE ST				ORL	A, #RDYFLG	SET DATA READY FLAG
23 23FA 980 MOV A, #RDTIM GET TIMER CONSTANT (3/4 CELL TIME) 25 62 981 MOV TA LLOAD TIMER 26 8933 982 MOV IRCCNT.#SLWIRG LLOAD TIMER 27 9254 984 JB4 RD17: IN A,P1 , READ DRIVE STATUS 28 99 983 RD17: IN A,P1 , READ DRIVE STATUS 29 9254 984 JB4 RD19 , TEST IF CLEAR LEADER FOUND - ERROR 29 9254 985 JT1 RD15 , TEST INPUT LODRING FOR EDGE 20 8650 986 JF0 RD16 , INPUT-0, TEST LAST 27 E928 987 RD18: DJNZ IRCCNT.RD17 ; INPUT-1.AST SAME, DEC IRC COUNT 28 18 8002 988 ORL P1: #STP ; COUNT EXPIRED, AT IRC, STOP DRIVE 30 8A02 989 ORL P2: #BDADFF ; TURN OFF DRIVE ACTIVE LED 31 8A02 989 ORL A, #STAT GET READ STATUS 32 FB 990 MOV A, STAT GET READ STATUS 33 BA02 991 ORL A, #IRGFLG ; SET IRC FOUND FLAG 34 A308 991 ORL A, #IRGFLG ; SET IRC FOUND FLAG 35 FB 992 MOV RSTAT, A ; RESTORE STATUS 36 A303 991 ORL A, #OTH LOOK AT STACK POINTER ONLY 37 994 ; INTERRUPT EXIT ROUTINE - UPDATES FO IN STACK TO PRESERVE IT OVER RETR 38 C7 996 IN EXT. MOV A, PSW , GET CURRENT PSW FOR STACK POINTER 39 C7 999 RL A ; ZEBYTES PER STACK ENTRY 39 DEC A ; TRYING TO GET PSW ON TOP OF STACK 39 FO 300 1001 ADD A, #08H ADD OFFSET FOR POINTER 41 A9 1002 MOV IRCCNT, A ; LOOK AT STACK ENTRY 42 F1 1003 MOV A, 21RGCNT, A ; LODD POINTER TOR DINTER 43 8649 1004 JF0 EXIT1 ; TEST FO TO SEE WHAT TO SET FO TO 445 530F 1005 ANL A, #00FH ; FO=0 THEREFORE RESET IT 446 BA1 1006 JMP EXIT2 447 4320 1007 EXIT1 ORL A, #20PH ; FO=1 THEREFORE SET IT 448 A1 1008 EXITE: MOV A, ASAVE ; RECOVER A 449 4320 1007 EXIT1 ORL A, #20PH ; FO=0 THEREFORE SET IT 45 BA2F 1012 RD15: JF0 RD18 ; INPUT=1, TEST LAST, SAME 46 FF 1009 MOV A, ASAVE ; RECOVER A 47 6448 1006 JMP EXIT2 48 BA2F 1012 RD15: JF0 RD18 ; INPUT=1, TEST LAST, SAME 50 95 1013 RD16: CPL F0 ; FINALLY DIFFERENT, SET FO TO CURRENT IN 51 55 4320 1018 ORL A, #ESTORE STATUS 54 FB 1017 RD19: MOV A, RSTAT , RESTORE STATUS 55 4330 1019 MOV STAT, A ; RESTORE STATUS 55 4330 1021 ORL P2, #BDADFF ; DUTO OFF DRIVE LED	22 AB	978	PDIA	STOP	TONT	CTOP COUNTER
25 62 981 MOV T, A		980	ND14.	MOU	A #PDTTM	CET TIMED CONSTANT (2/4 CELL TIME)
28 09 983 RDI7: IN A,PI ,READ DRIVE STATUS 29 7254 984 JB4 RDI9 ,TEST IF CLEAR LEADER FOUND - ERROR 28 564E 985 JT1 RDI5 ,TEST IF DLEAR LEADER FOUND - ERROR 28 564E 985 JT1 RDI5 ,TEST IF DLEAR LEADER FOUND - ERROR 29 886 JF0 RDI6 ,INPUT=0, TEST LAST 28 F828 987 RDI8: DJN2 IRGCNT,RDI7 ,INPUT=0, TEST LAST 28 F828 987 RDI8: DJN2 IRGCNT,RDI7 ,INPUT=0, TEST LAST 28 F828 987 RDI8: DJN2 IRGCNT,RDI7 ,INPUT=0, TEST LAST 28 F828 987 RDI8: DJN2 IRGCNT,RDI7 ,INPUT=0, TEST LAST 29 CR				MOV	TA SMOO - OFF	LOAD TIMER
128 09   983 RDI7: IN	26 B933			MOV	IRGCNT, #SLWIRG	; LOAD IRG COUNT (READ USES SLOW SPEED)
128   544E   985				IN	A, P1	READ DRIVE STATUS
Sept		984		JB4	RDI9	TEST IF CLEAR LEADER FOUND - ERROR
131 8902   988		986		JFO	RDIA	: INPUT=0. TEST LAST
131 8902   988		987	RDIB:	DJNZ	IRGCNT, RDI7	INPUT/LAST SAME, DEC IRG COUNT
SAO2   989		988		ORL	P1, #STP	COUNT EXPIRED, AT IRG, STOP DRIVE
38 AB 992		989			P2, #DAOFF	TURN OFF DRIVE ACTIVE LED
992   993   994   995   993   994   INTERRUPT EXIT ROUTINE - UPDATES FO IN STACK TO PRESERVE IT OVER RETR   995   993   994   INTERRUPT EXIT ROUTINE - UPDATES FO IN STACK TO PRESERVE IT OVER RETR   995   995   996   INTEXT: MOV						CET THE FOUND FLAG 179
993   994   INTERRUPT EXIT ROUTINE - UPDATES FO IN STACK TO PRESERVE IT OVER RETR 995   995   996   INTEXT: MOV					A, #IRGFLG	SET IRG FOUND FLAG
975	00 110	993	,			
995, 139 C7 996 INTEXT: MOV A, PSW , GET CURRENT PSW FOR STACK POINTER 13A 5307 997 ANL A, #07H ; LOOK AT TACK POINTER ONLY 13C C7 998 DEC A ; TRYING TO GET PSW ON TOP DF STACK 13D E7 999 RL A ; 2 BYTES PER STACK ENTRY 13E 13E 17 1000 INC A ; PDINT AT PSW ENTRY 13F 1030 1001 ADD A, #08H ; ADD OFFSET FOR POINTER 14I A9 1002 MOV IRGCNT. A ; LOAD POINTER TOR POINTER 14I A9 1002 MOV A: **ERGCNT GET PSW ENTRY 142 F1 1003 MOV A: **ERGCNT GET PSW ENTRY 1445 5305 1005 ANL A. **GOSH ; FOO THEREFORE RESET IT 145 5305 1005 ANL A. **GOSH ; FOO THEREFORE RESET IT 1449 4320 1007 EXITI CRL A. **BOSH ; FOO THEREFORE SET IT 148 A1 1008 EXIT2: MOV & IRGCNT, A RESTORE STACK 144		994	; INTERF	RUPT EXIT	ROUTINE - UPDAT	TES FO IN STACK TO PRESERVE IT OVER RETR
33 3307 997 ANL A, #07H ;LOOK AT STACK POINTER ONLY 33C 07 998 DEC A ;TRYING TO GET PSW ON TOP OF STACK 33D 27 999 RL A ;2 BYTES PER STACK ENTRY 33F 0308 1001 ADD A, #08H ;ADD OFFSET FOR POINTER 341 A9 1002 MOV IRGENT. A ;LOAD POINTER - USE IRGENT REGISTER 342 F1 1003 MOV A: REGENT. A ;LOAD POINTER - USE IRGENT REGISTER 343 B649 1004 JF0 EXIT1 ;TEST F0 TO SEE WHAT TO SET F0 TO 345 53DF 1005 ANL A, #00DFH ;F0=0 THEREFORE RESET IT 346 448 1006 JMP EXIT2 347 6448 1006 JMP EXIT2 348 A1 1008 EXIT2: MOV @IRGENT, A ;RESTORE STACK 348 A1 1008 EXIT2: MOV @IRGENT, A ;RESTORE STACK 340 93 1010 RETR 341 1011; 342 B62F 1012 RDI5: JF0 RDI8 ;INPUT=1, TEST LAST, SAME 343 B649 1014 STRT T ;START TIMER 344 B647 1017 RDI9: MOV A, RSTAT ;EXIT 354 S430 1015 JMP INTEXT ;EXIT 355 4320 1018 ORL A, #EOTORE STATUS 356 B702 1020 ORL P1. #STP ;ECT SO STOP DRIVE 367 AB 1019 MOV RSTAT. A ;RESTORE STATUS 368 B702 1020 ORL P1. #STP ;ECT SO STOP DRIVE	00.07	995	,			
1	34 5307				A, PSW	GET CURRENT PSW FOR STACK POINTER
3D E7 999 RL A 2 BYTES PER STACK ENTRY 3E 17 1000 INC A POINT AT PSW ENTRY 3F 0308 1001 ADD A, #08H ADD OFFSET FOR POINTER 4L A9 1002 MOV IRCCNT, A LOAD POINTER - USE IRGCNT REGISTER 42 F1 1003 MOV A, EIRGCNT GET PSW 43 B649 1004 JF0 EXIT1 TEST FO TO SEE WHAT TO SET FO TO 45 53DF 1005 ANL A, #00FH F0-0 THEREFORE RESET IT 47 6448 1006 JMP EXIT2 47 4448 1006 JMP EXIT2 48 A1 1008 EXIT2: MOV @IRCCNT, A RESTORE STACK 48 A1 1008 EXIT2: MOV @IRCCNT, A RESTORE STACK 40 F7 1009 MOV A, ASAVE RETURN WITH RESTORE 40 93 1010 RETR 41 1011 TEST FO TO SEE WHAT TO SET FO TO 41 THEREFORE SET IT 42 F0-1 THEREFORE SET IT 43 F0-1 THEREFORE SET IT 44 F0-1 THEREFORE SET IT 45 F0-1 THEREFORE SET IT 46 F0-1 THEREFORE SET IT 47 F0-1 THEREFORE SET IT 48 F0-1 THEREFORE SET IT 49 F0-1 THEREFORE SET IT 49 F0-1 THEREFORE SET IT 40 F0-1 THEREFORE SET IT 41 F0-1 THEREFORE SET IT 41 F0-1 THEREFORE SET IT 42 F0-1 THEREFORE SET IT 43 F0-1 THEREFORE SET IT 44 F0-1 THEREFORE SET IT 45 F1 F1 THEREFORE SET IT 45 F1 F1 THEREFORE SET IT 45 F1 THEREFORE SET IT 45 F1 THEREFORE SET IT 46 F1 THEREFORE SET IT 47 F0-1 THEREFORE SET IT 48 F1 THEREFORE SET IT 49 F0-1 THEREFORE SET IT 40 F1 THEREFORE SET IT 40 F0 THEREFORE SET IT 41 F0-1 THEREFORE SET IT 42 F0 THEREFORE SET IT 44 F0 THEREFORE SET IT 45 F0 THER					A	TRYING TO GET PSW ON TOP OF STACK
3E 17 1000 INC A POINT AT PSW ENTRY 3F O3F O3D 1001 ADD A, #008H ADD OFFSET FOR POINTER 41 AP 1002 MGV IRCCNT.A LOAD POINTER - USE IRCCNT REGISTER 42 F1 1003 MGV A, #1 RCCNT. A LOAD POINTER - USE IRCCNT REGISTER 43 8649 1004 JFO EXIT1 TEST FO TO SEE WHAT TO SET FO TO 45 TO THEREFORE SET IT TO TO SEE WHAT TO SET FO TO THEREFORE SET IT TO TO SEE WHAT TO SET FO TO THEREFORE SET IT TO TO SEE WHAT TO SET FO TO THEREFORE SET IT TO TO SEE WHAT TO SET FO TO THEREFORE SET IT TO TO SEE WHAT TO SET FO TO THEREFORE SET IT TO TO SEE WHAT TO SET FO TO THEREFORE SET IT TO TO SEE WHAT TO SET FO TO THEREFORE SET IT TO TO SEE WHAT TO SET FO TO THEREFORE SET IT THEREFORE SET IT TO THEREFORE SET IT TO THEREFORE SET IT TO THE SET THE THERE THE SET TO TO THEREFORE SET IT TO THE SET THE TO THE SET TO THE SET TO THE SET TO THE SET TO TO THE SET	3D E7	999			A FEST JATOTHE	2 BYTES PER STACK ENTRY
## 41 A9 1002 MOV IRCCNT.A , LOAD POINTER - USE IRCCNT REGISTER ## 42 F1 1003 MOV A. & PIRCCNT. GET PSW ## 43 B649 1004 JF0 EXIT1 ; TEST F0 TO SEE WHAT TO SET F0 TD ## 45 53DF 1005 ANL A. ## 40DFH ; F0=0 THEREFORE RESET IT ## 47 4320 1007 EXIT1: ORL A. ## 201	3E 17			INC	A BUTATE	POINT AT PSW ENTRY
## 88-49 ## 1004	3F 0308				A, #08H	ADD OFFSET FOR POINTER
## 8849   1004	41 A9				IRGCNT, A	LOAD POINTER - USE IRGCNT REGISTER
45 53DF 1005 ANL A.#ODFH ;F0=0 THEREFORE RESET IT 47 644B 1006 JMP EXIT2					FXIT1	TEST EN TO SEE WHAT TO SET EN TO
47 6448						FO=O THEREFORE RESET IT
1009	47 644B	1006		JMP		
1009		1007	EXIT1:	ORL	A, #20H	FO=1 THEREFORE SET IT
## 1010 RETR						RESTORE STACK
4E 862F 1012 RDI5: JFO RDI8 ;INPUT=1, TEST LAST, SAME 50 95 1013 RDI6: CPL FO ,FINALLY DIFFERENT, SET FO TO CURRENT IN 51 55 1014 STRT T ,START TIMER 52 6439 1015 JMP INTEXT ,EXIT 1016; 54 FB 1017 RDI9: MOV A,RSTAT ,GET READ STATUS 55 4320 1018 ORL A, #EDTFLG ,SET EOT FLAG 57 AB 1019 MOV RSTAT,A ,RESTORE STATUS 58 8902 1020 ORL P1. #STP ,EDT SO STOP DRIVE 58 8002 1021 ORL P2. #DAOFF ;TURN OFF DRIVE LED					A, ASAVE	RECUVER A
4E 862F 1012 RDI5: JFO RDI8 ;INPUT=1, TEST LAST, SAME 50 95 1013 RDI6: CPL FO ,FINALLY DIFFERENT, SET FO TO CURRENT IN 51 55 1014 STRT T ,START TIMER 52 6439 1015 JMP INTEXT ,EXIT 1016; 54 FB 1017 RDI9: MOV A,RSTAT ,GET READ STATUS 55 4320 1018 ORL A, #EDTFLG ,SET EOT FLAG 57 AB 1019 MOV RSTAT,A ,RESTORE STATUS 58 8902 1020 ORL P1. #STP ,EDT SO STOP DRIVE 58 8002 1021 ORL P2. #DAOFF ;TURN OFF DRIVE LED	/3			REIR		RETURN WITH RESTURE
1013 RDI6   CPL   FO	4E B62F	1012	RDI5:		RDIS	
52 4439 1015 JMP INTEXT FEXIT 1016; 54 FB 1017 RDI9: MOV A,RSTAT GET READ STATUS 1018 55 4320 1018 ORL A,WEDTFLG SET EDT FLAG STATUS 1019 MOV RSTAT. A RESTORE STATUS 1020 ORL P1.WESTP FOOT SO STOP DRIVE 1020 ORL P2.WDADFF STURN OFF DRIVE LED 1021 ORL P2.WDADFF STURN OFF DRIVE ACTIVE ACTI	50 95	1013	RDI6:		FO	FINALLY DIFFERENT, SET FO TO CURRENT INP
54 FB 1017 RDI9: MOV A,RSTAT ,GET READ STATUS 55 4320 1018 ORL A, WEDTFLG ,SET EDT FLAG 57 AB 1019 MOV RSTAT.A ,RESTORE STATUS 58 8702 1020 ORL P1. WSTP ;EDT SO STOP DRIVE 58 8A02 1021 ORL P2. WDADFF ;TURN OFF DRIVE LED	51 55				T	START TIMER
54 FB 1017 RDI9: MOV A,RSTAT ,GET READ STATUS 55 4320 1018 ORL A, WEDTFLG ,SET EDT FLAG 57 AB 1019 MOV RSTAT.A ,RESTORE STATUS 58 8702 1020 ORL P1. WSTP ;EDT SO STOP DRIVE 58 8A02 1021 ORL P2. WDADFF ;TURN OFF DRIVE LED	52 6439			JMP	INTEXT	PEXIT SERIE SUMPLE TOWN A SAN EUR
55 4320 1018 ORL A. #EDTFLG ; SET EDT FLAG 57 AB 1019 MOV RSTAT. A ; RESTORE STATUS 58 8902 1020 ORL P1. #STP ; EDT SD STOP DRIVE 54 8402 1021 ORL P2. #DAOFF ; TURN OFF DRIVE ACTIVE LED	54 FR	1016	PDTO.	MOU		
57 AB 1019 MOV RSTAT.A RESTORE STATUS 58 8902 1020 ORL P1.#STP FOT SO STOP DRIVE 5A 8A02 1021 ORL P2.#DADFF ; TURN OFF DRIVE ACTIVE LED		1017	ND17.			
5A BA02 1021 ORL P2, #DAOFF ; TURN OFF DRIVE ACTIVE LED	57 AB				RSTAT, A	RESTORE STATUS
5A 8A02 1021 ORL P2, #DAOFF ; TURN OFF DRIVE ACTIVE LED		1020			P1. #STP	; EOT SO STOP DRIVE
					P2, #DAOFF	TURN OFF DRIVE ACTIVE LED
5C 6439 1022 JMP INTEXT ; EXIT	5C 6439	1022		JMP	INTEXT	FYITHIBE LEDWIN DUCKER OF THE VOICE OF THE
1023 ; 1024 \$EJECT						
1024 SEJECT BYING STIRL STORY JRD		1024	PEOEC I			BVIRG MOTE STEELING JACK

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 DIGITAL CASSETTE CONTROLLER REV 1.0 - 26 MARCH 80

```
LOC OBJ
                   LINE
                                 SOURCE STATEMENT
                   1026
                   1027
                        ; WRITE INTERRUPT ROUTINE
                   1028 ;
                          *************************
                   1029
                   1030
                                                            , GET WRITE TIME CONSTANT (1/2 CELL TIME)
,LOAD TIMER (IT'S STILL RUNNING)
;TEST IF SECOND INT — DO NEXT BIT IF IT IS
;FIRST INT — COMPLEMENT DATA OUT
035E 23FC
                   1031 WRINT:
                                  MOV
                                           A. #WRTIM
0360 62
                                           T.A
WRINT1
                   1032
                                  MOV
0361 B672
                   1033
                                  JFO
0363 OA
                   1034
                                  IN
                                           A, P2
0364 126A
                   1035
                                           P2, #DOHI
0366 8A01
                   1036
                                  ORL
0368 6460
                   1037
                                  JMP
                                           WRI2
                                           P2, #DOLOW
036A 9AFF
                   1038 WRI1
                                  ANI
0360 95
                   1039 WRI2:
                                  CPL
                                           FO
                                                             SET SECOND INT FLAG
                                           A, P1
                                                             HANDLE IT IF IT'S FOUND
0340 09
                   1040
                                  IN
036E 92DC
                   1041
                                           CLRLED
                                  JB4
0370 6439
                   1042
                                  JMP
                                           INTEXT
                                                             GO EXIT
                   1043
                   1044 ; SECOND INTERRUPT FOR THIS BIT - GO GET NEXT BIT
                   1045
0372 FB
                   1046 WRINT1:
                                  MOV
                                           A. WSTAT
                                                         GET WRITE STATUS
0373 52BA
                                                             ; TEST WRITE DONE FLAG - DONE IF YES
                   1047
                                  JB2
                                           WRD4
0375 FD
                   1048
                                  MOV
                                           A, SERIAL
                                                              GET DATA REMAINDER
                                                              ROTATE NEXT BIT INTO CARRY
0376 67
                   1049
                                  RRC
                                           SERIAL, A
0377 AD
                    1050
                                                              RESTORE DATA
                                                             TEST NEXT BIT

IF 0 - NO CHANGE IN OUTPUT

IF 1 - COMPLEMENT OUTPUT
                                           WRI3
A, P2
WRI4
0378 E683
                   1051
                                  JNC
037A 0A
                   1052
                                  IN
037B 1281
                   1053
                                  JBO
037D 8A01
                   1054
                                  ORL
                                           P2, #DOHI
                                           WRI3
P2, #DOLOW
037F 6483
                   1055
                                  JMP
                                                            RESET SECOND INT FLAG
EXIT IF CHR NOT DONE
CHR IS DONE SO RESET BIT COUNTER
GET WRITE STATUS
FEGT CHECKSUM FLAG
0381 9AFE
                   1056 WRI4
                                  ANL
0383 85
                   1057 WRI3
                                  CLR
                                           FO
                                           BITCHT, INTEXT
                   1058
                                  DJNZ
                                  MOV
MOV
                                           BITCNT, #WRCNT
A, WSTAT
0386 BC08
                   1059
0388 FB
                   1060
0389 1244
                   1061
                                  JRO
                                           WRD2
038B 32B3
                                           WRD3
                                                             TEST SYNC FLAG
                   1062
                                  JB1
                                  SEL
038D C5
                   1063
                                           RBO
                   1064 ;
                   1065 : NO SPECIAL CHR BEING DONE - DEC BYTE COUNTER AND TEST IF DONE
                   1066;
                                           CNTLSB.WRI5 ,DEC LSB - IF NON-ZERO GET NEXT BYTE
A.CNTMSB ;IF ZERO, GET MSB AND TEST IT
WRD1 ;IF MSB IS ZERO - DONE. GO WRITE CHECKSUM
CNTMSB ;MSB IS NON-ZERO SO DEC IT
038F F894
                   1067
                                  D. JN7
0390 F9
                   1068
                                  MOV
0391 C6A1
                   1069
                                  JZ
                                  DEC
                   1070
0394 D6CA
                   1071 WRI5
                                  JNIBE
                                           WRURUN
                                                             ; NOT DONE WITH ALL BYTES,
; IS THE NEW DATA IN DBBIN YET? NO - UNDERRUN
                   1072
                                                            ; YES, READ IT
; SAVE IT
; BE SURE IT WASN'T A COMMAND
; IT'S DATA, ADD TO CHECKSUM
0396 22
                   1073
                                  IN
                                           A. DRR
0397 AC
                                           TEMP1, A
                   1074
                                  MOV
0398 76CF
                   1075
                                  JF1
                                           WCOMD
A, CHKSUM
039A 6B
                                  ADD
                   1076
039B AB
                   1077
                                  MOV
                                           CHKSUM, A
                                                      RESTORE CHECKSUM
                   1078
                                  MOV
                                           RB1
SERIAL, A
039D D5
                   1079
                                  SEL
                                                       PUT DATA IN SERIALIZER
039E AD
039F 6439
                   1081
                                  JMP
                                           INTEXT
                                                             GO EXIT
                   1082
                   1083 ; BYTE COUNT DONE - WRITE CHECKSUM
                   1084
                                                     GET CHECKSUM
03A1 FB
                   1085 WRD1
                                  MOV
                                           A, CHKSUM
03A2 D5
                                           RB1
                   1086
                                  SEL
                                                     ; PUT IT IN SERIALIZER
; GET WRITE STATUS
; SET CHECKSUM FLAG
; RESTORE STATUS
; CO. FYLT
                                           SERIAL, A
O3A3 AD
                   1087
                                  MOV
                                           A, WSTAT
A, #CKSFLG
03A4 FB
                   1088
                                  MOV
03A5 4301
                   1089
                                  ORL
                                           WSTAT, A
03A7 AB
                                MOV
03AB 6439
                                                             GO EXIT
                   1091
                                  JMP
                                           INTEXT
                   1092
                   1093 ; CHECKSUM BYTE DONE - DO SYNC
03AA 53FE
                   1095 WRD2
                                  ANL
                                           A, #NOT CKSFLG , RESET CHECKSUM FLAG
03AC 4302
                   1096
                                           A, #SYNFLG
                                                       SET SYNC FLAG
                                  ORL
                                                            RESTORE STATUS
OBAE AB
                   1097
                                  MOV
                                           WSTAT, A
SERIAL, #SYNC
OBAF BDAA
                   1098
                                  MOV
03B1 6439
                   1099
                                  IMP
                                           INTEXT
                                                             GO EXIT
                   1100
                   1101 ; SYNC DONE - SET WRITE DONE FLAG
                   1102
                                           A, #NOT SYNFLG , RESET SYNC FLAG
A, #WRDFLG ; SET WRITE DDNE FLAG
03B3 53FD
                   1103 WRD3
                                  ANI
03B5 4304
                   1104
                                  ORL
O3B7 AB
                   1105
                                  MOU
                                           WSTAT, A RESTORE WRITE STATUS
03B8 6439
                                  JMP
                                           INTEXT
                                                            GO EXIT
                   1107
                   1108 ; WRITE DONE FLAG FOUND SET - COMPLETELY DONE SO STOP AND RESET BUSY
                   1109
                                                             GOOD RESULT
03BA BA00
                   1110
                         WRD4
                                           RESULT, #GOOD
                                  MOV
                                                             SET OUTPUT TO 1
STOP TIMER
STOP DRIVE
03BC 8A01
                   1111 WRDON
                                  ORI
                                           P2, #DOHI
03BE 65
                                  STOP
                                           TCNT
                   1112
                                           P1. #STP
03BF 8902
                   1113
                                  DRI
                                           P2, #DAOFF
                                                             TURN OFF DRIVE ACTIVE LED
                                  ORL
03C3 D5
                   1115
                                  SEL
                                           RR1
                                           A, WSTAT
03C4 FB
                                                             GET WRITE STATUS
                   1116
                                  MOV
                                           A, #NOT (WRFLG OR SYNFLG) ; RESET WR/RD FLAG
WSTAT, A ; RESTORE STATUS
03C5 537D
                   1117
                                  ANI
03C7 AB
                   1118
                                  MOV
```

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Using the 8295 Dot Matrix

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0 DIGITAL CASSETTE CONTROLLER REV 1.0 - 26 MARCH 80 SOURCE STATEMENT 0308 6439 1119 JMP INTEXT GO FXIT 1120 ; 1121 ; UNDERRUN OCCURRED 1122 03CA D5 1123 WRURUN: SEL RR1 OSCB BAB1 1124 MOV RESULT, #UNDERW ; UNDERRUN ERROR CODE 03CD 64BC 1125 JMP WRDON EXIT 1126 1127 ; COMMAND FOUND WHEN DATA EXPECTED - CHECK IF ABORT 1128 OSCF D5 1129 WCOMD: SEL 03D0 D305 A, #ABORT COMPARE TO ABORT
WC1 COMPARE TO ABORT
YES, THEN ABORT
RESULT, #WCMDER NO, DATA ERROR RESULT CODE 1130 XRL 03D2 C6D8 1131 JZ 03D4 BA82 1132 MOV 03D6 64BC WRDON ; EXIT
RESULT, #ABTCMP ; ABORT COMPLETE RESULT COE 1133 JMP 1134 WC1 03D8 BA01 MOV 03DA 64BC 1135 JMP WRDON 1136 1137 ; CLEAR LEADER FOUNMD DURING WRITE 1138 RESULT. #EDTERR ; CLEAR LEADER ERROR CODE
A, WSTAT ; GET WRITE STATUS
A, #EDTFLG ; SET EDT FLAG OSDC BA83 1139 CLRLED: MOV 03DE FB 03DF 4320 03E1 AB 1140 MOV 1141 ORL 1142 MOV WSTAT, A 03E2 64BC EXIT 1143 JMP WRDON 1144 1145 END USER SYMBOLS ABORT 0005 BADCHS 0044 ABTCMP 0001 ABTST 01DA BITCNT 0004 ABTST1 01DE ARTJMP 0044 ASAVE 0007 001F BLKSAV 0006 BOTFLG 0040 BUF1 BLKTIM 0005 BEGIN 0009 0107 BLKCNT 0004 BUF2 OICB BUFFER 01CO BUMPIT 02CC BUSY 0080 CHKSUM 0003 CKSER 01BE CKSFLG 0001 CLRLED 03DC CLRTF 0059 CMDERR 0002 CMDIN CMDIN1 002C CMDJMP 003E 0023 CMDIN2 003A CMDIN3 0033 CMDINJ 0292 CMDSAV 0002 CNTLSB 0000 CNTMSB 0001 DAOFF DAON OOFD DEL1 00BA DRACT 0010 DEL 150 00C1 DEL2 OOBC DEL50 OOBB DESERL 0005 DUMPIT 02D3 DOLOW DRIVER OOC5 DOHI 0001 OOFE DR1 OOCD DRACTS 02BC DRIVJ 014F FILPRT 0020 EOTERR 0083 EDTFLG 0020 EXIT1 0349 EXIT2 FASIRG 0020 FAST OOFB IRGF1 FORWD OOFE GETDAT 0151 GOOD 0000 INT 0300 INTEXT 0339 IRGCNT 0001 01BA IRGFLG 0008 IRGFND 0191 LBOUT 0000 LBRDY 0001 LBTST 0177 NDRACT 02C4 NINMSB 006D PAS1 NT 00D0 RCLRTF 0103 NTAPE NWR RD OVFLOW 02D0 PAS2 NOFULL 0162 0003 0004 **DVERUN 0041** 02DF 02E3 PASHOL 02DC RCMDER 0045 00F7 RD1 0127 RD1A 012B RD2 0120 RD3 0130 RDCNT 0008 RDFRR 00D4 RD4 0135 RDATA 0006 RDCMD 0001 RDERR2 OOF1 RDERR3 OODF RDERR4 OOE3 RDERRS OOE7 RDERR6 00F8 0300 RDI2 0312 RDI3 RDINT 0316 RDI4 0322 RDTIM FFFA RDI5 034E RDI6 RDYFLG 0001 RDI8 REOT RDIBF RDI7 0328 032F RDI9 0354 0105 0305 READ 0100 REDJMP 0046 REDTER 0046 RESCMD 0000 RESCOM 004E RESET 0000 RESJMP 0044 RESULT 0002 REWIND 0001 REWJMP 004C REWND 0294 REWND1 02A1 REWND2 02AB SERIAL 0005 REWND3 OZAF REWND4 02BB RSKIP 0262 RSNB 0188 RSTAT RWCMD RWDIRG 0020 SHIFIN 0316 SKCMD 0003 SKIP1 022B SKIP11 0287 SKIP12 024F SKIP13 025E SKIP14 0257 SKIP2 022D SKIP3 022F SKIP4 023E SKIP6 SKIP7 SKIPB 0278 SKIP9 0281 SKIPER 0200 SKIPR1 0206 SKIPR2 0200 SKIPR3 0212 SKPBOT 0048 SKPEOT 0047 SKPJMP 004A SLOW 0004 SLWIRG 0033 SNBFLG 0002 SNBTST 0182 SRT OOFD

SYNC

WR2

WRD3

WSTAT

UNDERW 0081

0061

03B3

0003

SYNC1

WR3

WRD4

WRI5

UNFLOW 02D9

ОЗВА

0394

SYNC2

WC1 WR4

WRDFLG 0004

WRINT 035E

0308

0098

SYNFLG 0002

WCMDER 0082

WRINT1 0372

009F

озвс

WR5

WRDON

ASSEMBLY COMPLETE, NO ERRORS

STP TEMPO

WRI1

WEDTER OOA9

WRCNT 0008

WRTIM FFFC

0002

0006

036A

STRFLG 0004

TEMP1 0004

WRTJMP 0048

WRD1

0008

03A1

STSUP

WR1 WRD2

TIMINT 0007

WRURUN 03CA

005B

OBAA

0383

0007

0040

03CF

0002

0080

TAPIN

WCDMD WRCMD

WRFIG

WRITE 0055

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#### INTRODUCTION

Many microprocessor systems require the real-time control of a peripheral device such as a printer, keyboard, or alpha-numeric display, etc. These medium speed but still real-time tasks can be rather mundane, time-consuming, and require a fair amount of system software overhead. Of course, any time spent by the main processor in servicing these I/O devices is unavailable for other, possibly more important, tasks. This processor burden can largely be removed by isolating the real-time portion of the task to a dedicated peripheral-control processer.

Until recently, this approach was usually not cost effective due to the large number of components required by the dedicated processor: CPU, RAM, ROM, I/O, etc. To help make the approach more cost effective, Intel borrowed the I/O processing concepts found in many mainframe and minicomputers; put all the hardware in one package; and introduced a family of Universal Peripheral Interface controllers—the UPI-41ATM family. The basic family consists of the 8041A and the 8741A. These two devices are essentially single-chip microcomputers with a standard microprocessor bus interface. They have onchip RAM, ROM (8041A) or EPROM (8741A), CPU, timer/counter, and I/O. Using one of the UPI family, the designer simply codes his custom or proprietary peripheral control algorithm into the UPI device itself rather than the main system software. The UPI device then takes over the peripheral control task while the host processor simply issues commands and transfers data. More information on the UPI family is available in the documents referenced opposite the table of contents.

Illustrating the UPI concept as both design examples and actual products, a number of pre-programmed 8041As are available. These devices are the 8278 Keyboard/Display Controller, the 8294 Data Encryption Unit, the 8292 GPIB Controller, and the 8295 Dot Matrix Printer Controller. Data sheets for these devices are found in the Peripheral Design Handbook and their source listings (except for the 8294) are available in Insite, Intel's User's library. This application note deals with the 8295.

#### **THE 8295**

The 8295 Dot Matrix Printer Controller is a device specifically designed to interface microprocessors to the LRC 7040 Series of dot matrix impact printers. It offers complete solenoid and motor drive timing and contains an on-chip 7×7 character generator accommodating 64 ASCII characters. An on-chip FIFO buffers up to 40 ASCII characters before printing. Character density, width, and print intensity are all programmable. Three programmable tabulations and two general purpose outputs are also provided. Four data transfer methods are possible: polling, interrupt-driven, and Direct Memory

Access (DMA) are available when in parallel data transfer mode and asynchronous serial is available in serial mode. The data transfer mode is hardware selectable.

Let's first look at the LRC printer itself and its interface to the 8295.

# THE LRC 7040 PRINTER OF SIRINGOINGER SE Abionsion

The LRC Model 7040 printer is manufactured by LRC, Inc. of Riverton, Wyoming. Capable of printing 40 columns of characters at a speed of 1.25 lines/sec, the 7040 is mechanically simple and is ideal for point-of-sale or data logging terminals.

It is an impact printer whose print head consists of seven solenoids which each drives a stiff wire to impact the paper through an inked ribbon. While the wires are arranged in a circular fashion at the solenoid end, they form a vertical column at the ribbon impact point, Characters are formed by firing the solenoids to form a  $5\times7$  or  $7\times7$  matrix of "dots" (impacts of the wires). Figure 1 shows how the character A is formed using a  $7\times7$  matrix. The columns are labeled C1 thru C7 and the rows R1 thru R7. The print head moves left to right across the paper so at time T1, the head is over column C1. If the correct solenoids are activated at each time Tx for each column Cx, the character is formed.

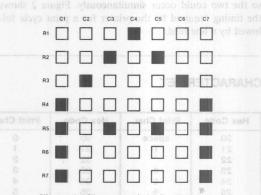


Figure 1. Character A in 7×7 Format

The print head is moved across the paper by the main motor drive. The main motor drive consists of a 24-pole synchronous motor which drives a rotating plastic drum. The drum has a spiral groove molded into it and a pin on the print head rests in the groove so that the print head traverses the paper as the drum rotates. Characters are printed by firing the solenoids during the left-to-right traverse. At the end of the print area, the spiral groove reverses the direction of the print head returning it to its home position.

A HOME microswitch riding on a cam attached to the plastic drum provides the only feedback as to the print head position. When the print head is in its home resting position the HOME switch is inactive. To start a print cycle, the main motor drive is activated which starts the print head motion. As the print head reaches the beginning of the print area, the cam activates the HOME switch as a signal to the printer controller to commence firing the solenoids. The controller then activates the solenoids as appropriate for each character in the line. The print area is defined as the 310ms immediately after HOME goes active. Solenoid timing is the responsibility of the controller; the printer mechanism supplies no character-position information.

After the line is printed and the print head has traversed right to left, the HOME switch is deactivated. This transition signals the controller to turn off the main motor drive since the home position has been reached. A new print cycle may start immediately if data is ready.

Paper feed is accomplished with a second synchronous motor and a PFEED (Paper Feed) microswitch. In the quiescent state, the PFEED switch is inactive. Activating the paper feed motor drive starts the line feed cycle. The switch becomes active at some point during the cycle (typically about 48ms later) and is deactivated when the cycle is complete. The controller uses the active-to-inactive transition to remove the paper feed motor drive. The paper feed operation is independent of the print cycle so the two could occur simultaneously. Figure 2 shows the timing required by the printer for a print cycle followed by a line feed.

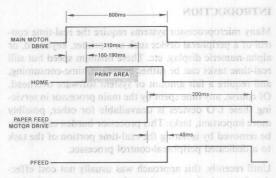


Figure 2. LRC 7040 Motor Drive Timing

Solenoid timing determines the location of any given "dot" and its intensity. The LRC 7040 printer specification states a 400 µs maximum solenoid "ON" time and a 1.3ms typical period. Since the print area is 310ms "long," this timing allows a total of 240 dots (310ms/1.3ms per dot) in one row or 40 characters on a 5 × 7 matrix with a one dot space between characters. While  $5 \times 7$  characters have acceptable readability, their distinctness and format can be improved with a  $7 \times 7$  matrix, however, 40  $7 \times 7$ characters translate to 320 dots per row or a 0.97ms solenoid period. This violates the solenoid duty cycle spec if the solenoids are fired for every column. The best way to get around this dilemma and still retain the improved readability of the  $7 \times 7$  format is to simply fire the solenoid every other column. The 8295 uses this technique and the "every-other" column spacing is reflected in Figure 1. The 8295 character set is included in Figure 3.

width, and print intensity are all programmable. Three

#### CHARACTER SET

Hex Code	Print Char.	Hex Code	Print Char.	Hex Code	Print Char.	Hex Code	Print Char.
20	space	30	0	.40 m s	daliav@na (AQ	8 adr 50 rgaox	ource i <b>R</b> tings (c
21	m m	31	ac 1	deals 44h	ston Anitealle	gs sin51 vacad	ntel's Oser's t
22		32	2	42	В	52	Bock on
23	# #	33	3	43	C	53	S
24	\$	34	4	44	D	54	T
25	%	35	5	45	E	55	U
26 Interes	& A 79	36 1 3703	6	46	F	56	.V.
27	,	37	7	47	G	57	w
28	(	38	8	48	ContHoller is	58	the SOX's Dot
29	across the pap	beyon 39	ming 9at	49	Language of	59 5A	pecific Yly desi
2A	dod ant contra	3A	mind on a	4A	ce microproces impacyprinter	5A	Z
	tor drive consi-		motor driv	4B	impacyprinter	SB D To a	RC 7070 Serie
anuth 2C and 8	drives a cotatic	down ASC TOWN ST	onen/ <iv< td=""><td>Er4C noo b</td><td>drive tigning an</td><td>1010 5C 15 51</td><td>omple¢ solend</td></iv<>	Er4C noo b	drive tigning an	1010 5C 15 51	omple¢ solend
no nig2Done ti	we molded into	ong SD as as	f musheuff	4D nix bo	rator Mcomm	5D 5D	n on-chip 7 x
oned 2Eg ed	groove so that	ent ni 3E er bas	d intre>nds	4E	FIFONbuffers	JE A SE	mesed ID2
2F	chara conste	4F	?	4F	0	5F	mereda 1102/

Figure 3. 8295 Character Set

#### 8295/Printer Interface

It's the job of the 8295/Printer interface to convert the TTL-compatible outputs of the 8295 to the motor and solenoid drive levels. Since the printer side of the 8295 is independent of the system side, this same 8295/Printer interface is used for all examples discussed in the later sections.

For solenoid drive, the 8295 supplies seven solenoid outputs,  $\overline{S1}$  thru  $\overline{S7}$ , plus a solenoid strobe, STB. STB modulates the SI-S7 outputs externally to supply the actual solenoid "ON" time. This time is software programmable. Figure 4 shows the recommended SI-S7/STB gating.

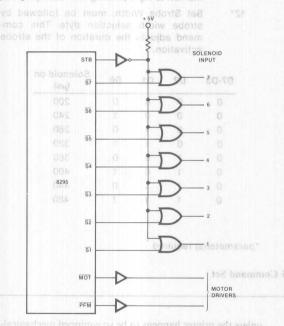
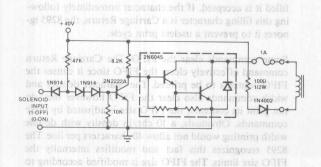


Figure 4. Solenoid and Motor Gating



sidsming && vin Figure 5. Solenoid Driveria dibiw signiz

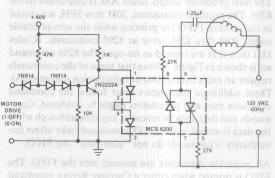
The solenoids must be driven from a  $40^{\circ} \pm 10\%$  volt source. The peak current is approximately 3.6A, the average current is approximately 0.5A. A circuit providing the required drive is shown in Figure 5. The output stage, consisting of the 2N6045 Darlington transistor, the 1N4002 catching diode, and the 100-ohm damping resistor, is the one suggested by the manufacturer. The input stage is a discrete implementation of a DTL gate. Note that the base-emitter junction of the 2N6045 protects the 2N2222A transistor from overvoltage on its collector. This circuit has several features which are important to the printer interface:

- 1.4 All solenoid power (including the power used to drive as the base of the power transistor) is derived from the 40-volt supply.
- 2. Disconnecting the drivers from the 8295 or the loss of the 5-volt supply to the 8295 results in the solenoids turning off,

The first feature of the drivers minimizes the impact of the printer and its interface on the 5-volt supply. The second feature prevents the activation of the solenoids erroneously during power on/off cycles or during system checkout. This an important point since the solenoids will be damaged if left activated continuously. The fuses is series with the solenoids help protect them from mishap.

The two motors can each be driven as shown in Figure 6. The Monsanto MCS-6200 is an optically-coupled TRIAC which is ideal for driving the small synchronous motors in the printer. Coupled with a buffer this part provides a simple means of controlling the motors without sacrificing the isolation required for safe and reliable operation.

These driver circuits were borrowed from the Intel application note AP-27 "Printer Control With the UPI-41." (The 8295 development was inspired by the success of the AP-27 design.) Other solenoid and motor driver circuits are described in the LRC Interface Guide available from the manufacturer.



bool and other Figure 6. Motor Driver position at OHIA

#### COMMAND SET north and training abienalog and

lex Code	Description	H
00	Clear GP1. This command brings the GP1 pin to a logic low state. After power on it is automatically set high.	
01	Clear GP2. Same as the above but for GP2.	
02 JTC	Set GP1. Sets GP1 pin to a logic high state, inverse of command 00.	
03	Set GP2. Same as above but for GP2. Inverse command 01.	
	Software Reset. This is a pacify command. This command is not effective immediately after commands requiring a parameter, as the Reset command will be interpreted as a parameter.	
05	Print 10 characters/in. density.	
06	Print 12 characters/in. density.	
70 By The sec- legolds er-	Print double width characters. This command prints characters at twice the normal width, that is, at either 17 or 20 characters per line.	
08* Historian	Characters to be retched. Least significant	
09	Tab character.	
OA	The Monsento MCS-6200 and DisamoMonT	
0B*	Multiple Line Feed; must be followed by a byte specifying the number of line feeds.	
0C	Top of Form. Enables the line feed output until the Top of Form input is activated.	

Hex Code	or section is Description to do and att
0D	Carriage Return. Signifies end of a line and enables the printer to start printing.
0E*	Set Tab #1, followed by tab position byte.
0F*	Set Tab #2, followed by tab position byte. Should be greater than Tab #1.
10*019	Set Tab #3, followed by tab position byte. Should be greater than Tab #1.
ply the ac- c program- SUST/STB	Print Head Home on Right. On some printers the print head home position is on the right. This command would enable normal left to right printing with such printers.
12*	Set Strobe Width; must be followed by strobe width selection byte. This command adjusts the duration of the strobe activation.

D7-D3	D2	D1	D0	Solenoid on (µs)
0	0	0	0	200
0	0	0	1	240
0	0	1	0	280
0	0	1	1	320
0	1	0	0	360
0	1	0	1	400
0	1	1	0	440
0	1	1	1	480

<sup>\*</sup>parameter(s) required

Figure 7. 8295 Command Set

#### 8295 Command Software

The software control of the 8295 is very straightforward. The host processor simply issues ASCII characters to the 8295. The printable characters, 20H thru 5FH, are stored in the on-chip FIFO for printing while the non-printable codes, 00H thru 12H, serve as 8295 commands. (Codes 13H thru 1FH are treated as no-ops.) The 8295 command set is shown in Figure 7. Note that some of the commands require an extra byte or two of information (parameters). These additional parameters must follow the command otherwise data and parameters might be confused. Commands and data may be mixed at any time although while the data is stored in the FIFO, commands take effect immediately. Commands do not "pass-thru" the FIFO.

All printable characters are entered into the FIFO. The FIFO is printed when either a Carriage Return command is received or the FIFO becomes full. In either case, the FIFO is printed, however there is no automatic line feed

unless the printer happens to be so equipped mechanically. Thus, a Line Feed command should be issued after each Carriage Return or after the last character to fill the FIFO. The FIFO is printed as soon as the character that filled it is accepted. If the character immediately following this filling character is a Carriage Return, the 8295 ignores it to prevent a useless print cycle.

Some commands clear the FIFO. The Carriage Return command effectively clears the FIFO since it causes the FIFO contents to be printed. The character density and width commands also clear the FIFO however they do not print its contents; the FIFO size is adjusted by these commands. Obviously, a 10 chr/in density with double width printing would not allow 40 characters per line. The 8295 recognizes this fact and modifies internally the FIFO size limits. The FIFO size is modified according to the table below. For example, if the density is 10 char/in, single width printing, the 8295 accepts only 33 printable

characters before starting a print cycle. Since these commands take effect as soon as they are accepted, this prevents mixing different character densities or widths on a given line. Any such commands must precede the data for a line.

		BUFFER SIZE
		e, use the 04:95 DMA is
Her. W11h suc	DOUBLE	oparible v02n the 8257 I
or rd0 soore	SINGLE VI	rface all 86st's necessa
enindo nem	DOUBLE	DMA C51troller with

The Software Reset command clears the FIFO, resets the density to 12 chr/in and selects single width printing. It does not effect the solenoid strobe width, the tab positions, or the general purpose outputs. This command should be issued only when the 8295 is expecting a command or data. Issuing it when the 8295 is expecting a parameter causes it to be interpreted as the parameter and not the intended software reset.

A hardware reset causes the 8295 to default into the following states:

- 1. Clears the FIFO of qu for wolfer allowed parameters allowed the property of the control of th
- 2. GP1 and GP2 set high
- 3. 12 chr/in density
- 4. single width prining
- 5. 320μs strobe width
- 6. tab positions indeterminate.

#### Parallel Interfaces

The 8295 has the option of using serial or parallel communication with the main processor. The choice must be

made early in the design cycle since it is a hardware, not a software, selection. Let's look at the parallel options first.

In parallel mode, the 8295 has the traditional microprocessor bus interface: data, control, etc. The parallel mode is selected by not grounding the IRQ/SER pin. To the main processor, the 8295 in parallel mode appears as two registers: the Input Data register and the Output Status register. The main processor writes commands and data into the Input Data register while it reads the 8295 status from the Output Status register.

The Output Status register format is shown in Figure 8. The Input Buffer Full bit (IBF) indicates whether the 8295 has accepted the previous command or data byte. IBF is automatically set when the host processor writes to the 8295 and it is reset when the 8295 accepts the data or command. If IBF = 1, no writes to the Input Data register are allowed. Only when IBF = 0 may a Input Data register write be done. The DMA Enable bit (DE) is set whenever the 8295 is performing DMA data transfers. When the specified number of transfers has been made, the DE bit is cleared. Since DMA cycles are usually transparent to the main processor, the DE bit tells the processor when the DMA block transfer is complete.

The processor does not always have to read the Output Status register, checking IBF, before loading the Input Data register. An interrupt output (IRQ) pin is available to interrupt the processor whenever the 8295 is ready to receive new data or commands. The fact that IRQ is set implies that IBF = 0, so it's not necessary for the processor to read the 8295 status when interrupted; it can just write the next byte.

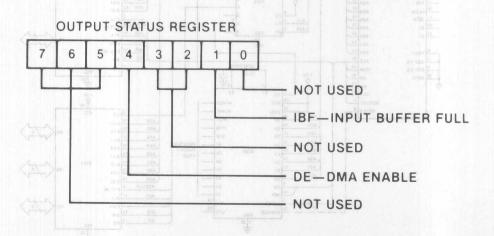


Figure 8. Output Status Register Format

Figure 9 shows the system schematic for using the 8295 in polled-parallel mode in an 8085A system; ie the IRQ line is not used. The 8085A/8295 interface is standard as for any Intel peripheral.  $\overline{CS}$  is decoded from the high-order address lines.  $\overline{RD}$  and  $\overline{WR}$  are the 8085A read and write control lines.  $\overline{RESET}$  is the system reset.

Example 8085A polling software is shown in Figure 10. This routine simply outputs the print buffer starting at the location pointed to in PRTSRT. The system software builds the buffer, terminates it with a 0FFH character, and loads PRTSRT before calling PRINT.

PRINT is not very efficient with respect to processing time. Since the 8295 does not accept data while in a print or line feed cycle, if the buffer contained more printable characters than the FIFO size, the processor would sit in the PRT2 loop during the 800ms print and 200ms line feed cycles. That is obviously not too efficient. The obvious way around this problem is to restrict the buffer size to less than that of the FIFO however this could complicate the system software since more buffer building is required. A better approach is to use interrupts.

By connecting the 8295's IRQ output to one of the 8085A RST interrupt inputs (dotted line in Figure 9), the pro-

cessor is interrupted only when the 8295 is able to take another character. Figure 11 shows such interrupt-driven software assuming the RST 6.5 interrupt input is used for IRQ.

To further enhance the bus efficiency and processor overhead at the expense of slightly more complex hardware, use the 8295 DMA interface. This DMA interface is compatible with the 8257 DMA Controller. With such an interface all that's necessary is for the processor to load the DMA Controller with the print buffer starting address and write the Enable DMA command and length parameters into the 8295. The 8295 does the rest by requesting data directly from memory thru the DMA Controller. It keeps track of the number of characters to request. As long as there are characters remaining to be transferred, the DE bit in the Output Status register is set. After the last byte is transferred into the 8295, the DE bit is reset and the IRQ is made active. Either event is used to tell the processor that DMA is complete and the 8295 is ready for the next block. It is not necessary to restrict the DMA block size to 40 characters, the Enable DMA command parameters allow for up to 65k byte block sizes. The block size given the 8295 must reflect both data plus commands and parameters.

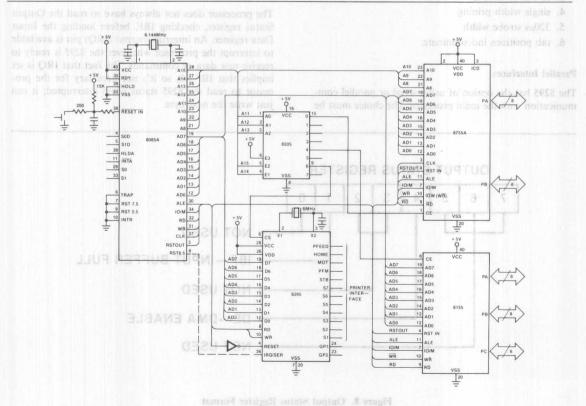


Figure 9. 8295 Parallel Interface

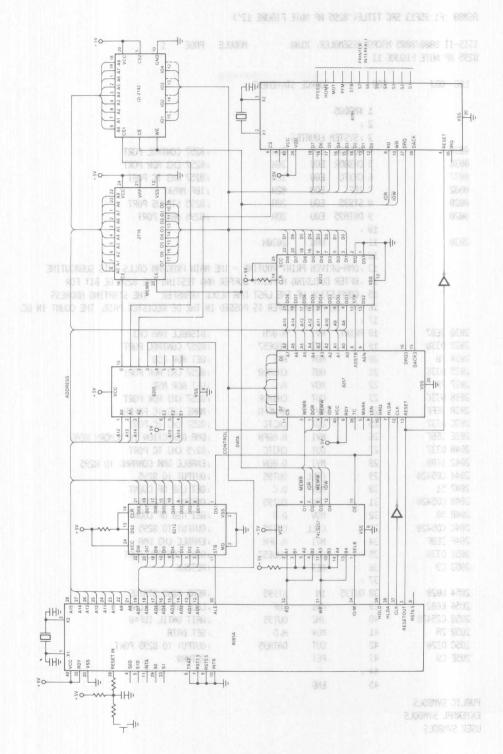
ASM80 :F1:95F10. SRC TITLE(18295 AP NOTE FIGURE 101) ISIS-II 8080/8085 MACRO ASSEMBLER, X108 MODULE 8295 AP NOTE FIGURE 10 LOC OBJ SEQ SOURCE STATEMENT 1 \$M0D85 2; 3 : SYSTEM EQUITES - BENEFITE RETRIEVE - HEARS - LIGHT TRETSH & 2000H POINTER STORAGE 4 PRISRT EQU 2000 02H FERG MASK 5 1BF EQU-0002 6 STS95 EQUIPMENT 31H 1034 HTML 2: 8295 STATUS REGISTER FORT 2 CHING V 0031 31H :8295 DATA REGISTER FORT 7 DATA95 EQU 0031 8 : 2030H OT OF THE SECOND POPULATION TO SECOND TO SECOND 2030 9 10 ; 11 : PRINT BUFFER OUTPUT SUBROUTINE - THIS ROUTINE PRINTS THE BUFFER 12 / STARTING AT THE POINTER STORED AT PRISKY. THE ROUTINE RETURNS WHEN 13 ) A OFFH IS FETCHED FROM THE BUFFER. 14; SAVE HL SAVE BC 2030 E5 15 PRINT: PUSH H В 2031 05 16 PHSH GET BUFFER POINTER 2032 2RD020 17 LHLD PRISRI. 18 PRT1: R, M B, R GET CHARACTER FROM BUFFER SAVE IT IN B 2035 7E MOY 2036 47 19 20 MOY WEFH IS IT THE BUFFER END? 2037 FEFF CPI 21 PEXIT FYES, GO EXIT JZ 2039 CA4A20 STS95 22 PRT2: : NO. REND 8295 STATUS 203C DB31 IN 23 LOOK AT IBF FLAG 203E E602 ANI IBE 24 JNZ 25 MOV 26 OUT PRT2 2040 C23C20 : WAIT UNTIL IBF=0 A. B. 2043 78 RECOVER CHARACTER : OUTPUT TO 8295 H :BUMP BUFFER POINTER 2044 D331 2046 23 27 INX. JMP PRT1 ; GET NEXT CHARACTER 28 2047 033520 29 ; B RESTORE BC 30 PEXIT: POP 204A C1 31 204B E1 POP H RESTORE HL RETURN 2040 09 32 RET 33 ; 34 PUBLIC SYMBOLS 1415 EXTERNAL SYMBOLS USER SYMBOLS DATA95 A 0031 IBF A 0002 PEXIT A 204A PRINT A 2030 PRT1 H 2035 PRT2 R 2030 PRISRT R 2000 STS95 A 0031

Figure 10. 8085A/8295 Polling Subroutine

ASSEMBLY COMPLETE, NO ERRORS

ASM80 :F1:95F11 SRC TITLE(18295 AP NOTE FIGURE 111) ISIS-II 8080/8085 MACRO ASSEMBLER, X108 MODULE 8295 AP NOTE FIGURE 11 SEQ SOURCE STATEMENT LOC OBJ 1 \$MOD85 2; 3 / SYSTEM EQUATES 4 PRTSRT EQU 2000H POINTER STORAGE STANDOS METEVOS 2000 5 IBF EQU 02H 18F FLAG MASK 0002 31H #8295 STATUS REGISTER PORT 0031 6 STS95 EQU 7 DATA95 EQU 31H ;8295 DATH REGISTER PORT 0031 10 : RST6. 5 INTERRUPT VECTOR LOCATION - JUMP TO PRINTER SUBROUTINE 12 STECH ORG TO 34Hg SMITHOS STRT - SMITHOSPHIC THRIND SEPTIDE THIS TO LET 13 Jan 248013 GO 10 PRINT ROUTINE 0034 C33020 14 RST65: JMP 15 ; 16; 2030 19 ; PRINTER OUTPUT SUBROUTINE FOR INTERRUPT-DRIVEN SYSTEM - OUTPUTS 20 ; CHR POINTED AT BY PRISRI. 1F CHR IS OFFH, THE BUFFER 15 COMPLETE 21 ; AND THE RST6. 5 INTERRUPT IS MASKED. THE MAIN PROGRAM MUST UNMASK 22 : RST6. 5 AFTER IT BUILDS A NEW BUFFER. PRINT BUFFER STATUS IS REFLECTED 23 ; TO THE MAIN PROGRAM BY THE RST6.5 MASK BIT IN RIM INSTRUCTION. 24; H 0017 781 76 200 SAVE HL 25 PRINT: PUSH 2030 E5 2031 F5 26 PUSH PSW 27 28 2032 2AD020 LHLD A. M GET NEXT CHR 2035 7E MOV 28 MOV 29 CPI 30 JZ 31 OUT 32 INX 33 SHLD TEST IF BUFFER COMPLETE 2036 FEFF 2038 CA4520 EXIT YES, GO EXIT WITH RST MASKED NO, OUTPUT CHR TO 8295 203B D331 DATR95 BUMP POINTER 203D 23 H RESTORE POINTER 203E 22D020 PRTSRT RESTORE PSW 2041 F1 34 PRT1: POP PSW 2042 E1 35 POP RESTORE HL 2043 FB 36 EI RE-ENABLE INTERRUPTS 2044 C9 37 RET 38; 2045 3E0A 39 EXIT: MVI MASK RST6. 5 2047 30 49 SET INTERRUPT MASK SIM 41 2048 C34120 JMP PRT1 GO EXIT WITH MASK IN PLACE 42 ; 43 END PUBLIC SYMBOLS EXTERNAL SYMBOLS USER SYMBOLS DATA95 A 0031 EX11 A 2045 IBF A 0002 PRINT A 2030 PRT1 A 2041 PRTSRT A 2000 RST65 A 0034

Figure 11. 8085A/8295 Interrupt-Driven Software



igure 12. 8295/DMA Interface

liques 13. 3295 DMA Subroutine

ASM80 :F1:95F13. SRC TITLE('8295 AP NOTE FIGURE 13')

LOC OBJ	SEQ	SOURCE	STRIEMENT	
	1 \$MOD85			
	2 ;			
	3 ; SVSTE	M FOLIATI	5	
0038	4 MODE57		38H	;8257 CONTROL PORT
1036	5 CH3ADR		36H	8257 CH3 ADR PORT
1037	6 CH3TC		37H	8257 CH3 TC PORT
1002	7 IBF		02H	IBF MASK
020	8 STS95		20H	8295 STATUS PURT
020	9 DATA95	-	28H	8295 DHTA PORT
020	10	Luo	Con	7 OESO DINII TOKI
939	11	ORG	2030H	
-	12		2 8	
	7 7 7 8 9 8	RIVEN P	RINT ROUTINE -	THE MAIN PROGRAM CALLS THIS SUBROUTINE
				FER AND TESTING THE 8295 DE BIT FOR
				BLOCK TRANSFER. THE STARTING ADDRESS
				SED IN THE DE REGISTER PAIR, THE COUNT IN
	17 ;	C TREAT	DOTTER 15 THS	SED IN THE DE REGISTER THIRD THE COOK! IN
030 3E07	18 PRINT	MUT	A, 07H	; DISABLE DMA CH3
032 D338	19	OUT	MODE57	8257 CONTROL PORT
034 7B	20	MOY	A, E	GET ADR LSB
035 D336	21	OUT	CH3ADR	8257 CH3 ADR PORT
037 7A	22	MOV	A, U	GET ADR MSB
038 D336	23	OUT	CH3HDR	8257 CH3 ADR FORT
03A 3EFF	24		A, UFFII	MAKE CH3 1C FFFFH
03C D337	25	OUT	CH3TC	: 8257 CH3 1C PORT
03E 3EBF	26	MYI	A, ØBFH	DMA DIRECTION IS MEMORY READ
040 D337	27	OUT	CH3TC	8275 CH3 TC PORT
042 1608	28	MVI	D. 08H	ENABLE DMA COMMAND 10 8295
044 CD5420	29	CALL	0UT95	OUTPUT 10 8295
047 51	30	MOV		GET LSB OF COUNT
048 CD5420	31	CALL	00195	OUTPUT TO 8295
04B 50	A 32	MOV	D. B	GET MSB OF COUNT
04C CD5420	33	CALL	0UT95	OUTFUT TO 8295
04F 3E0F	34	MVI	A, ØFH	ENABLE CH3 DMR
051 D338	35	OUT	MODE57	8257 CONTROL PORT
053 C9	36	RET	Lwit	RETURN
	37 :			
	38 OUT95	IN	51595	READ 8295 STATUS
054 DB20	39	RNI	IBF	LOOK AT IDE FLAG
	V 5 0	JNZ	0UT95	WAIT UNTIL 18F=0
056 E602	40			
056 E602 058 C25420	40 41	MOV	H, D	GET DATA
054 DB20 056 E602 058 C25420 058 7A 05C D320		MUY	H, D DATH95	OUTPUT TO 8295 PORT

PUBLIC SYMBOLS EXTERNAL SYMBOLS USER SYMBOLS

Figure 13. 8295 DMA Subroutine

Figure 12 illustrates an 8257/8295 interface and Figure 13 shows example software for handling the system. This software assumes that the 8295 is doing the counting of the transfers hence the Terminal Count of the 8257 DMA channel is loaded with the maximum value while the 8295 receives the actual block size. The 8295 simply stops making requests once the requested number of transfers have been made.

## Serial Interface

In addition to the parallel interface options, the 8295 supports a "stand-alone" serial interface. In this mode, the only communication with the main processor is via a serial link. This configuration is perfect for remote printer applications; only three wires are required compared to 12 or 13 for the parallel interfaces.

The serial mode is envoked by simply grounding the IRQ/ $\overline{SER}$  pin. See Figure 14. The internal 8295 software interrogates this pin upon power-on and reconfigures the function of several pins if it's grounded. The  $\overline{DACK}/SIN$  pin becomes the serial data input (SIN) and the DR-Q/ $\overline{CTS}$  pin becomes the hardware data holdoff, Clear-to-Send. The lower three Data Bus pins become the Baud Rate Select inputs. Note that it is necessary to ground  $\overline{CS}$  and  $\overline{WR}$ , and pull  $\overline{RD}$  high. This enables the "input" direction of the Data Bus pins so that the 8295 may read the baud rate. All standard baud rates from 110 to 4800 baud are accommodated.

After power-on the 8295 looks at IRQ/SER and if it's grounded, the data bus pins are read to determine the baud rate. Data from the serial input is requested by lowering CTS. CTS stays low until during the eight bit of the serial data character at which point it goes high (inactive). After the character is assembled and interpreted, CTS again goes active to request the next character. The 8295 does not check for parity and characters with invalid start bits or framing errors (stop bit wrong polarity) are ignored. CTS is normally connected to the UART'S CTS input. An inactive CTS holds off the UART transmitter from transmitting characters.

In serial mode, the command and data definitions still apply as in parallel mode. Commands and data may be mixed although commands take effect immediately when received.

Figure 15 shows example software to drive an 8251A Programmable Serial Interface when connected to an 8295. This software is similar to Figure 10 except it assumes that the 8251A has the same I/O port addresses as the 8295 had in Figure 9. Note that the TXE (Transmitter Empty) flag is used to load data into the 8251A transmitting both characters in the transmitter (the transmitter is double buffered) if CTS goes inactive. The TXE flag allows only one character at a time in the transmitter so CTS going inactive simply finishes off the current character. The 8295 accepts only one character at a time.

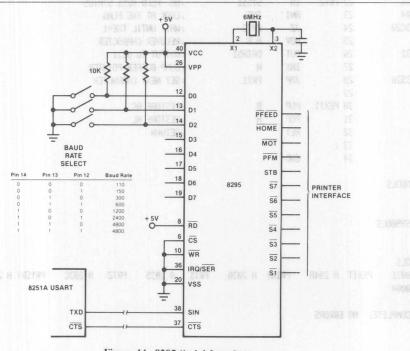


Figure 14. 8295 Serial Interface

		d rate. Data from	software assumes that the 8295 is doing the counting of ban
ISIS-II 8080/8085	MACRO ASSEME	BLER X108 MC	the transfers hence the Terminal Count of the 8257 INVA 3269 3 1000
8295 AP NOTE FIGU	RE 15 on will	serial data character	channel is loaded with the maximum value while the 8295 the
ed and interpreted,	er is assembl		receives the actual block size. The 8295 simply stops mak-
aul FocateRip tyse	2/5F0/201221 0	SOURCE STATEMENT	
characters with in-	bris ying and	5 does not check to	
		d start bits or framiq	
		ignored. CTS is nor	
ds off the UART	tod Stauer	M COLOTEC MINING M	
2000	4 PRTSRT	EQU 200H	
0004	5 TXE	EQU 04H	only communication with the main processory ARM BRIT 3XI : In
	6 STS51 7 DATA51		38251 STHTUS REGISTER PORTAL MONSTAGEMENT SMILL SMILL BUSS
1500 0031	7 DH1851	H1E UQ3	18251 DHIR RESISTER PURTOUS DOWN COLD SCHOOLSONGE COLLEGE
		house	
2030	9	ORG 2030H	The serial mode is envoked by sumply grounding the
	10		
	11 PRINT	BUFFER OUTPUT SUBKO	JULINE - THIS KUULINE PKINIS THE BUFFER
	75 / 21HH	THE THE POTHICK 3	DIUKEL HI FRIDRI. THE KUUTINE KETUKNO WHEN
	13 / A 0FF	H IS FETCHED FROM TH	pin becomes the serial data input (SIN) and the DR- REFINE
	14 ;	t in Figure 9. Note th	
2030 E5	15 PRINT:	PUSH H DORN ALS	
2031 C5	16	PUSH B	Rate Select inputs. Note that it is necessary granted depart 719.
2032 2AD020	17	LHLD PRTSRT	JULI DUFFER FULNIER SHOWS SHOT WAS A STATE OF THE PARTY O
2035 7E	18 PRT1:	MOV A, M	GET CHARACTER FROM BUEFFR
2036 47	19	MOV B, A	SAVE IT IN B
2037 FEFF	20	CPI OFFH	IS IT THE BUFFER END?
2039 CA4A20	21	JZ PEXIT	band are accommodated. TIX3 00 734;
- 203C DB31	22 PRT2:	IN 5TS51	NO, READ 8251 STRTUS
203E E604	23	ANI TXE	LOOK AT TXE FLAG
2040 CA3C20	24	JZ PRT2	; WAIT UNTIL TXE=1
2043 78	25	MOV A.B	RECOVER CHARACTER
2044 D331	26	OUT DRTA51	DOV DUTPUT TO 8251
2046 23	27	INX H	BUMP BUFFER POINTER
2047 033520	28	JMP PRT1	GET NEXT CHARACTER
	29 )		90 SI
204A C1	30 PEXI1:	PUP B	RESTORE BC
2048 E1	31	POP H	RESTORE HL
2040 09	32	RET SMOH	RETURN
	33 ;	100	
	34	END-1 MER	
		sta	
PUBLIC SYMBOLS			
TOTAL STREET	PRINTER		
EXTERNAL SYMBOLS			Le van de la
LATERIAL STABULS		54	un i con i c
			20
USER SYMBOLS			1 no   11
	EVIT 0 2040	DDTN7 0 0000	120g (8C )
DATA51 A 0031 P	EA11 H 204H	PKINI H 2030	PRT1 A 2035 PRT2 A 203C PRISRI H 2000 SIS51 A 0031
TXE A 0004			BSSTA USART
OCCEMBLIT COMPLICE	NO PROFES		my 105
ASSEMBLY COMPLETE,	NO ERRORS		
			275

Figure 15. 8251A Subroutine

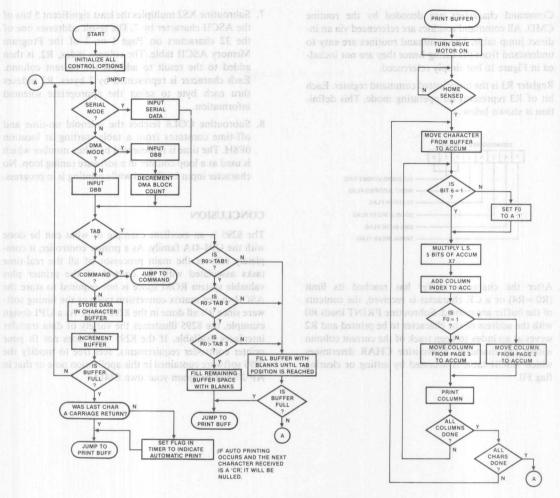


Figure 16. 8295 Flow Chart

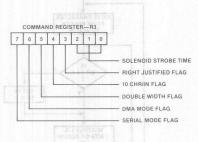
## **8295 SOFTWARE**

For those readers using the 8295 as a design example for UPI software, the flow charts for the program are shown in Figure 16 and the 8295 source listing is included as Appendix A. (Machine readable source listings are available through Insite, the Intel User's Library.) As an aid to understanding this software, the following observations can be made:

- The 8295 uses only Register Bank 0. The function of registers R6 and R7 is determined by the mode. In parallel mode they are concantenated to form the 16 bit DMA count register. In serial mode, R6 is a counter during character reception.
- 2. Characters and commands are input from the Input Data register via the INPUT subroutine. The routine defines the input mode, fetches the data, and stores it in R2. If the DMA mode is enabled, the block count in R6 and R7 is decremented by the DECR routine each time a data transfer occurs until the count is exhausted.
- Characters are decoded by routine P6A which also detects any illegal characters by the INPUT routine.
   R0 is assigned as the character buffer pointer and R4 is designated as the buffer size limit. The commands which affect the buffer size will affect R0 and R4.

AFN-00875A

- 4. Command characters are decoded by the routine CMD. All command routines are referenced via an indirect jump table. The command routines are easy to understand from the listing hence they are not included in Figure 16 but simply referenced.
- Register R3 is the bit-oriented command register. Each bit of R3 represents an operating mode. This definition is shown below.



6. After the character buffer has reached its limit (R0=R4) or a CR character is received, the contents of the buffer are printed. Subroutine PRINT loads R0 with the address of the character to be printed and R2 serves as an index to keep track of the current column within the character. Subroutine CHAR determines which ASCII table is accessed by setting or clearing flag F0.

- 7. Subroutine XS2 multiples the least significant 5 bits of the ASCII character by 7. The result addresses one of the 32 characters on Page 1 or 2 of the Program Memory ASCII table. The column index, R2, is then added to the result to address the current column. Each character is represented by 7 bytes. R2 indexes thru each byte to select the appropriate solenoid information.
- 8. Subroutine COL8 fetches the solenoid on-time and off-time constants from a table starting at location 0F8H. The time is represented by a hex number which is used as a loop counter in a software timing loop. No character input is allowed while printing is in progress.

## CONCLUSION

The 8295 is an excellent example of what can be done with the UPI-41A family. As a printer controller, it completely relieves the main processor of all the real-time tasks associated with the control of the printer plus valuable system ROM space is not required to store the ASCII-to-dot matrix conversion table or the timing software since it's all done in the 8295 itself. As a UPI design example, the 8295 illustrates the variety of data transfer interfaces available. If the 8295 itself does not fit your printer controller requirements, feel free to modify the 8295 software contained in this application note or that in AP-27 and program your own 8741A.



Figure 16. 8295 Flow Chart

Characters and commands are input from the input Data register via the INPUT subroutine. The routine defines the input mode, fetches the data, and stores it in R2. If the DMA mode is enabled, the block count in R5 and R7 is decremented by the DECR routine cach time a data transfer occurs until the count is exhausted.

Characters are decoded by routine P6A which also detects any illegal characters by the IMPUT routine. R0 is assigned as the character buffer pointer and R4 is designated as the buffer size limit. The content and R4 is designated as the buffer size limit. The content is designated.

For those readers using the 8295 as a design example for UP1 software, the flow charts for the program are shown in Figure 16 and the 8295 source listing is included as Appendix A. (Machine readable source listings are available through Insite, the Intel User's Library.) As an aid to understanding this software, the following obser-

The 8295 uses only Register Bank 0. The function of registers R6 and R7 is determined by the mode. In parallel mode they are concamenated to form the 15 bit DMA count register. In serial mode, R6 is a counter during character reception.

CORTES IN

15-11 MCS-40/UP)-41 MCDD RESEMBLER, V2 0 C 70-00 SERIES PRIMTER CONTROLLER SOURCE CODE

## APPENDIX A

```
ASM48 :F1:8295. SRC
ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V2. 0
                                               PAGE 1
LRC 7040 SERIES PRINTER CONTROLLER SOURCE CODE
 LOC OBJ
                SEQ
                          SOURCE STATEMENT
                  1 $MOD42 TITLE('LRC 7040 SERIES PRINTER CONTROLLER SOURCE CODE')
                  3 ; ***************************
                  4 ;** 8295 - LRC 7040 SERIES PRINTER CONTROLLER
                                                                       okak
                  5 ; ** REV. 0 FOR 7X7 CHARACTER MATRIX
                                                                       **
                  6 ; ********************************
                  8
                  9
                 10 ; COPYRIGHT (C) 1978
                 11 ; INTEL CORPORATION
                 12 ; 3065 BOWERS AVE.
                 13 ; SANTA CLARA, CA. 95051
                 14
                 15
                 16
                 17 ; **********************
                 18 ;** PAGEO CONTAINS THE INITIALIZATION SEQUENCE, THE OUTPUTING **
                 19 ; ** OF DATA TO THE SOLENIODS, THE SERIAL INPUT ROUTINE, THE **
                 20 :** PAPER FEED ROUTINE, AND THE SOLENIOD FIRETIME ROUTINE
                 21 ; *****************************
                 22
                 23 SEJECT
ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V2 0
                                               PAGE 2
LRC 7040 SERIES PRINTER CONTROLLER SOURCE CODE
 LOC OBJ
               SEQ
                         SOURCE STATEMENT
                 24
                 25
                 26
                 27 ; ***********************
                 28; **
                 29; **
                                 REGISTER ASSIGNMENT TABLE
                                                                       **
                 30 ; **
                                                                       **
                 31 ;********************
                 32 ; **
                                                                       **
                 33 ; **
                                 RØ
                                     INPUT BUFFER POINTER
                                                                       **
                 34 ; **
                                 R1
                                     TEMPORARY STORAGE
                                                                       **
                 35 ; **
                                 R2
                                       TEMPORARY STORAGE
                                                                       **
                 36; **
                                 R3
                                       COMMAND REGISTER
                 37 ; **
                                 R4
                                       BUFFER SIZE
                 38; **
                                 R5
                                        TEMPORARY STURAGE FOR DELAY ROUTINE
                 39 ; **
                                 R6
                                       LOW ORDER DMA COUNTER
                                                                       **
                 40 ; **
                                 R7
                                       HIGH ORDER DMA COUNTER
                                                                       **
                 41 ; **
                                 TIMER TEMPORARY STORAGE
                                                                       skak
                 42 ; **
                 43 ;**********************
```

44 45 46 \$EJECT

1362-53M 11-5151 ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V2.0 PAGE LRC 7040 SERIES PRINTER CONTROLLER SOURCE CODE SOURCE STATEMENT LOC OBJ SER 47 : \* 49 ; \*\* RAM ASSIGNMENT TABLE 50 ; \*\* akak 51 ; \* 52 ; \*\* FUNCTION 53 ; \*\* RAM ADDRESS \*\* 54;\*\* alcale 55 ; \*\* 00-07H REGISTER BANK 1 56 ; \*\* 08-14H PROGRAM STACK 57 ; \*\* 15-17H TAB POSITION STORAGE \*\* 58 ; \*\* 18-40H CHARACTER BUFFER 59 ; \*\* \*\* 60 ; \* STIRM 61 LINITIRE L HUNE DY STUDIO 62 \$EJECT TUB SAVE ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V2 0 PAGE LRC 7040 SERIES PRINTER CONTROLLER SOURCE CODE LOC OBJ SEQ SOURCE STATEMENT JEC DR CHECK FOR RIGHT JUST KIDEND BUT 163 PT THE WALL WALL ON #U.SUUS 3030 U.64 ;\* THE BY 65 ; \*\* INC. SMOHN INC. SHOWN SOI BORN SOR 66 ; \*\* COMMAND REGISTER DEFINITION 68 ; \* 69 ; \*\* 70 ; \*\* BIT 7 SERIAL MODE FLAG akak 71 ; \*\* BIT 6 DMA MODE FLAG \*\* 72 ; \*\* BIT 5 DOUBLE WIDE FLAG \*\* ELERT SETERAGE HOTIGI 231 73 3 \*\* 04 0 0 BIT 4 0 32 COLUMNS/LINE \*\* 74 ; \*\* BIT 3 RIGHT JUSTIFIED PRINT 冰水 BITS 2,1,0 INDICATE SOLENOID ON TIME 75 ; \*\* 76;\*\* 77 ; \* 78 \$EJECT

				22400	o somble a	LRC 7040 SERIES PRINTER CONTROLLE
LOC	OBJ	SEQ		SOURCE	STATEMENT	TOC 081 SEG SO
0000				ORG.	000H	
	AND STATE	80		CANDERSON.	*****	44. 05
		81	ior ruch		NISG.	**: 04
9999	02	82	INIT:	OUT	DBB, A	; SET OBF
0001	ØA .	28		IN	F, P2	CHECK SERIAL STRAP
0002	B208	84		JB5	PARA	** 07
9994	BB83	T 1987 35		VOM	R3, #83H	
9996	040E	86		JMP	CLP1	56 . 88
8000	9ABF	otnog 87	PARA:	ANL	P2, #0BFI	55 : 88
		gange 88		EN	FLAGS	
900B	E5	g ggr 89		EN	- DMR	57 : **
				MOA	R3, #03H	at 52
000E	27	91	CLR1	CLR	A	CLEAR DMA BUSY FLAG
000F	90	92	****	MOV	STS. A	Production : 83
				MOA		; INITIALIZE BUFFER
0012	B818	94	AGAIN:	MOV	RØ. #18H	· INITIALIZE POINTER
9914	27	95		CLR	A	RESET STACK TO SAVE TABS
0015	07	96		MOV	PSW, A	STACK = 0.ALL FLAGS = 0
9916	3414	97	DECO	CALL	INFLIT	
0013	3428	98		CALL	PGA .	DECODE DATA
0018	FC	99		MOV	R- R4	
9918	08	100		YPL .	A, P0	
0010	9616	101		JNZ 0	SDECO	ISIS-11 MOS-48/JP1-41 MMORD RESE
		182				LRC 7049 SERIES PRINTER CONTROLLS
001E	FE	103	PRINT	MOV	A, R3	
001F	C8	104		DECIME	TARRE BORLE	LOCATE LAST CHRACTER INPUT IF R. J.
		105			ON	CHECK FOR RIGHT JUST.
		196				PRINT FROM THE ORIGIN
						WAIT FOR HOME SWITCH
						67 ; **
			WER.			
						CHECK FOR RJ
						; RJ TRUE 05
						FETCH CHARACTER
						F0 DETERMINES WHICH CHARACTER TABLE
						24 ; 45
						**: 67
						FETCH COL. FROM TRBLE
						; CHECKITFOR D. W.
			NOTE			FØ INDICATES D. W. MODE
			NU15:			DDING COL
						PRINI COL.
						; CHECK RJ
						EDINI NEUT OO
						FRINT NEXT COL.
0048		132		JMP	LSTCOL	
994D			RJP:	CLR	A	CHECK RJ. FIRE COLS. IN REVERSE ORDER
	9000 9001 9001 9002 9004 9008 9008 9008 9010 9015 9016 9016 9016 9016 9016 9016 9016 9018 9018 9018 9020 9020 9020 9020 9020 9020 9020 902	0000 02 0001 0A 0002 B208 0004 BB83 0006 040E 0008 9ABF 000A F5 000B E5 000C BB03 000E 90 0010 BC40 0012 BS18 0014 27 0015 07 0016 3414 0013 3428 001A FC 001B D8 001C 9616  001E FE 001F C8 0020 7224 0022 BS18 0024 9AEF 0026 4626 0028 2340 0021 S488 0020 BR06 002E FB 002F 7233 0031 BA00 0033 B500 0033 B538	8000 79 8000 81 8000 82 8001 86 83 8002 8208 84 80004 8883 85 80006 840E 86 8008 988F 87 8008 E5 89 8000 8803 90 8000 87 8000 8803 90 8000 87 8000 8000 8000 90 8010 8040 93 8012 8818 94 8014 27 95 8015 D7 96 8016 3414 97 8013 3428 98 8017 FC 93 8018 U8 100 8018 U8 100 8018 U8 100 8017 FC 93 8018 U8 100 8	8000   79   80   81   81   82   82   83   84   8001   86   86   86   86   86   86   86   8	0000	

		ES PRINTER CONTRO					
LOC	0BJ	SEQ	SOURCE !	STATEMENT	932		
004E	DA	11770 <b>134</b> 7 dga (	XRL	A, R2	189	8314	
004F	CA JO	SUBTATE SELVIOUS	DEC .II	R2		53	0,718
0050	9633	2001/136 3782	JNZ	CHAR	191	39	
0052	B656	136 3/92 137 LSTCOL	JF0	84	591	- 62	
0054	1480	138	CALL	COL8	CLEAR STB & DATE		
	237F	139 84	MOV	A. #7FH	CLEAR STR & DATE	A PINS	
		140	OUTI	P1. A	201		
0059	2719	141	MUA	A. #19H	sawa : 201		
		GERTZENIA PER					
		OF MI 9143 BHT 30					
		144					
9920	CC	4.45	MON NO.	0.04	000 		
0000	40	143	TNIC	DO NA	THEO DOTHTED		
0061	18	C30937146 F	INC	KO MAR	INCR PUINTER		
0062	0467	147 900	JMP	CK MI	380 792	110	
0064	2317	148 RJ2:	MUV	H, #17H	; INCR POINTER	YHSH	
0066	C8	RESERVED NEG	DEC	R0	DECR POINTER		FIFE
NAP.	08	130 CK	AKL	H, KU		-61255354	
0068	9620	151 CATA	JNZ A	XFER	RETURNS FOR NEXT	CHAR.	
006A	566A	3.070 152 HOME:	JT1	HOME	SENSE HOME LOW?	74E8	
006C	2320	MATE 9153 (3940)	MOV	A, #20H	; SENSE HOME LOW? ; STALL OS		
006E	54F8	18 T9R 1549/09W.	CALL	WAIT	STOP DRIVE MOTOR		288
0070	8A10	155	ORL	P2/#10H	STOP DRIVE MOTOR	SEE 5	
0072	0412	156	JMP	AGAIN	; NEXT LINE 212 CONT	9833	
	8115	THOTE 157 090J	R2.LOAD	SMUC	212 CONT-	3083	
0074	FB	158 DMAIN	VOM	A, R3	EXIT IF SERIAL I	HODE	
0075	F27A	159 2818	JB7	SERROR	SERIAL CMD EKROL WAIT FOR DMA PA	R 3038	086
0077	D677	160 INBUF	JNIBF	INBUF	; WAIT FOR DMA PAI	RAMS	
0079	22	161	IN	A) DBB			
007A	93	161 162 SERROR	RETR		24.7	7458	
		163	9.0	163		Ag	
		163 T18 9016403H0				55	
		T18 90365W9W			220	CDCS	
997R	B67F	166 FIRE	IEQ.9	SRIF	100	92	230
9970	09	167	IN A	9. P10	D. M. RIND PREVIOU	IS COL	ona
	59	169	I/ONE D	9. P4		SSAE	
997E	79	169 COLE:	DUT	D4 A	OUTPUT TO SOL.		
aaoa	ED	170 COLO.	MOU	0.07	O CETCON TIME	1363	
9904	120	174 COLO.	UDI	D #ULON	A GETS ON TIME		
0001	A3	172	MOUD	D GO	000		
	530F	1/2	ONU	n) en	228 LGR0:	2000	
0004	320F	23373 17 SM32N :	OPICE	DA WOOL	CTROPE COLENOYD	0.387	
99999	8980	1/4	UKL	P17 #80H	STROBE SOLENOID	5 (8:38·V	
	54F8				228		
	997F	176	ANL		DISABLE SOL. STI		
008C		177	MOV		A GET OFF TIME		
		1 JAPU 871 ER JAPLE	ORL	A, #0F8H			
008F		179 X20M :		A. PA	234		
		8 2001/180 GGR		A.190	235		Adat
	530F	181	ANLA	A, #OFH	226		808
0093	2B	182	XCH	A, R3		69	3000
0094	9299	S01183 IMI 7:	JB4	C10			
0096		184	XCH	H, R3	239		
0097	049C	TOM 39 185 H	JMP	CON	249 PF	SAFE	700
0099	2B	186 C10:	XCH	A, R3	241		
009A	0306	187	ADD	AJ #06H	INCREASE BIAS FO		
	B6A3	188 CON:			SKIP IF SINGLE		

LOC	0BJ	SEQ		SOURCE S	STATEMENT				
009E	0314	189 190		ADD	A, #14H	; ADD 7	TO OFFT	IME IF C	. W
00A0	29	190		XCH	A, R1	SAVE	PREVIOUS	COL.	
00A1	39	191		OUTL	P1. A	SAVE	<b>PREVIOUS</b>	COL	
00A2	29	192		XCH	A, R1				
00A3	44F8	193	SING:	JMP.	WAIT				
		194 195							
				******					
				RIAL ROUT RIAL INPU					
				*****					
		200			YOM				
00A5	9ABF	200 201	CTS:	ANL	P2; #0BFI	Н	REQUE	ST /CTS	
aga7	AB .	202	ONF .	TN	A. P2	: I DOP	HNTTI ST	ART RIT	FOLIND
00A8	F2A7	203		MJB7	ONE	- fists	148	2317	
00AA	B900	203 204 205 206	9090 t	MOV	R17#0	RESET	TEMP RE	G 83	2868
00AC	BR09	205		MOY A	R2, #09H	SET	NDEX		79867
00AE	09	206		IN	A, P1	BIAS	121		
00AF	74E0	207		CALL	HBIT	, WAIT	1/2 CYCL	E Maas	8966
00B1	0A	208		IN	8, P2	CHECK	FOR STA	RT BIT	
90B2	F287	209		JB7	ONE	. WRONG	STHRT B	SAFE II	3966
00B4	BE03	210 211		MOV	R6, #03H				
0086	EEB6	211	LZ	DJNZ	R6, LZ				
00B8	EACE	212 AIGE 213	CONT:	DJNZ	R2, LOAD	LOAD	THE EIGH	T BITS	
00BA	8A40	AIA 213	TIXE	ORL	P2, #46H	DISAB	BLE /CTS		
00BC	BE06	213		MOV	R6, #06H	BIAS	159		
CODE	CEDE	213	MT4	DAME	R6. W14	WAIT			
00C0	74E0	216		CALL	HBIT				
00C2	74E0	217 218 219 220		CALL	HBIT				
00C4	0A	218		IN	H. P2		(9)T		
00C5	37	219		CPL	A	CHECK	STOP BI	T	
<b>00</b> C6	F2A7	220		JB7	ONE	; WRONG	STOP BI	T	
00C8	F9	221 17377 222		140V	A, R1				
9 <b>0</b> C9	.F7) 200	222	10.01	RLC	A MI		107		
00CA	537F	223 302 0 224		ANL	A, #7FH		395		
00CC	AA	224		MOW	R2. A	SILE			
00CD	93	225		RETR			178		
		226		P. #66/3H R. 66					
		227		190 (8)	TYON		172		5889
DOUCE	74E0	228 1012 10 229	LOAD:	CALL	HBIT	; DELAY	1 CYCLE		
BODO	74E0	229		CHLL	HBIT				
2000	BER?	230	NO. 0	MUV	R6, #03H			2468	
ANDA	EED4	231 232 233	L1	DJNZ	R6, L1				
3007	00	232		NUP	2.50	*********	177	01	
7000	EZOO	233		IN	H, P2	INPUT	SERIHL	BILE	
	5380				A, #80H	MHSK	PII	DIXC S	
99DA	67	235		ORL	H, K1	HOD F	REVIOUS	B112	NO.
	67 89	236		RRC	A.				
	04B8	237		MOV	R1. A CONT	CTNIC	TU TOD		
OOOU	0900	238 239		JMP 3			81	28	
BODF	9AFE	240	PF:	ANL	P2, #0FE	H 8	PF MO	TOR ON	
00E1	B90A	241		MOY	R1, #0AH				6683
90E3	2388	242	P30:	MOY	A, #088H		187		R680
	FAFO	243		COLLE	HOTT				

LOC	0BJ	SEQ		SOURCE	STATEMENT			THEMENUT	309,405				
00E7	E9E3	244		DJNZ	R1, P3C				181			22	
00E9			ITO:	YOM	A, R0	DELAY	CONTANT =BUFF PO		TO 40H			537F	
2000	26EA		IT1:	JNT0	IT1				VON		197		
	54F8	247		CALL	MAIT	DELAY	=1MS TO 2.5MS		LIRO				
	36E9	248		JT0	IT0		DATA STORED IN A		VOH				
	23F3	249		MOV			NET & RESTORE FLAN		RETR		660		
	54F8	250		CALL			SCRIME DRE SERIAL			- 1996	385		
	8A01	251		ORL	P2, #91H								
00F6			P3F:	RETR			CHECK FOR SPECIAL			030			
0010		253	1.51	1.6		J Jenu	anayanc nun Ayana						
00F8		254		ORG	0F8H	: 501 0	N TIME CONSTANTS		381				
00F8		255		DB	0D4H		ON TIME	ATHO				9259	
00F9		256		DB	0C5H	; 248	2011				318		
00FA		257		DB	0B6H	; 280			SHI		112	9696	
00FB		258		DB	987H	; 320	DEFAULT						
oord oord		259		DB				F2. #83H			Eff		
00FD		260		DB	98H	; 360	BRT XIDEHO		YOM				951
				DB	89H	; 400							
00FE		261		2.77	7AH	; 440							
00FF	6B	262		DB	6BH	480			140				
		263									348		
		264						69 .H.	gga				
							******		** 1/3//			17	
							EXECUTES COMMANDS	Contract delighboring			122	E645	35
			; *****	*****	*****	*****	******	ekskakakakakakakak	**				141
		268						R2. P6BB					
0100		269		ORG	100H	MI 111	FXCEED BLL TAB. F		YOM		324		
9100		270		NOP				R2.F		19934		NR.	
0101		271		DB			ADDRESS FOR SET	OUTPUT 1	YOM	SATE			
0102		272		DB	(502 AN			89	DMI			18	
0103		273		DB	(RO1 AN	D OFFH)	; R01		VON		328		149
0104		274		DB	(RO2 AN								RA.
0105		275		DB	(RESET	AND OFF	H) RESET	SATS	300				
0106	A8	276		DB	(B32 AN	D ØFFH)	; B32			10993T	121		
0107	E4	277		DB	(B40 AN	0 9FFH	; B40						
0108		278		DB			D) , DWDE			CHECKS			
0109	C9	279		DB	(SDMA A	ND OFFI	D ; SDMA	SA.A		RTRO			
010A	HØ	280		DB	(SSOL A	ND OFFH	i) ; 550L	A .890		*HEIRS	555		
010B	88	281		DB.	(SLF AN	0 OFFH)			361				
010C	81	282		08	(MLF AN	OFFH)	AMERICAN TRE		JURG			5460	
010D	84	283		DB	(TOF AN	O OFFH)	; TOF		HELLS	-01/32			
010E	DE	284		DB	(CR AND	0FFH)	; CR						
010F	72	285		DB	(TI AND	0FFH)	RI ED INDEX IT:		1/109				
9119	72	286		DB	(T2 AND	0FFH)	T2 ONO STED A						
9111	72	287		DB	(T3 AND		; T3		VOH				
3112	F9	288		DB	(RJ AND		; RJ	R	3MI		342	17	
3113	R0	289		DB			) : SCOI	19.81				60	
		290					NOTE S. HOTER		27		344		
		291						RL P7C	ZMFG				
		292							ST3R		346	56	
3114	FB		INPUT:	MOV	A, R3						347		
	F226	294	210 271	JB7				6, 81	VON	COUND			
9117		295		CPL	A SMITH	HOR ON	JUMP INDIRECT TO						
	D21C	296		JB6	NODECR						SET .		
	8A40	297		ORL		: SET I	RQ FOR DMA		VOM				Sau
	D61C		NODECR:				D BY PARALLEL & DM	LARS of	JNZ			9678	
		570	weeren.	ALATEN.	INCIDENCE	1 THE RE	V VI TIMITILLEL & VI	N 81 87			253	46	

	S PRINTER CONTROL						
LOC OBJ	SEQ	SOURCE 9	STATEMENT				UBO 0
311E 22	299	IN	A, DBB		N ZHLO	244	
911F 537F	300	ANL	A, #7FH	199 - PUS CONTANT - PUSE POI	HOY R	245 178:	
3121 AA	301	MOV	R2. A		1 971/0	246 171:	
122 3462	302	CALL	DECR	DEC DMA COUNT FOR DMA & PARALL	FI LIRO		
3124 FA	303	MOV		DATA STORED IN A & R2			
3125 93	304	RETR	10112	KET & RESTORE FLAGS			
3126 04A5	305 YME:	JMP	CTS	SERIAL USE SERIAL INPUT ROUTT			
120 0403	306	211	012	730 9010N 341 H209 S	The		
0128 74ED	307 P6A:	COLL	SPCR				
		CALL		CHECK FOR SPECIAL CASE CR			
312A D24E	308	JB6	CHECK5	CHECK FOR VOLID CHAP	9 2570		
012C B250	309	JB5		CONTROL FOR THEIR OFFICE			
012E D309	310	XRL		118 ? BMIT NO 2000S: HAD			
9656	311	JNZ	CMD	COMMAND			
0132 B915	312 TRB:	MOV		R1 GETS TRB[]]			
0134 BA03	313	MOV	R2: #03H				
9136 F1	314 P688:	MOM	A, GR1	CHECK TRB 600 HB			
9137 F24D	315	JB7	TERROR	LIMIT THE TO EMAX 984			
0139 D24D	316	JB6	TERROR	RH : 446			
913B 37	317	CPL	А		80		
9130 17	318	INC	А				
313D 68	319	ADD	H, K0				
313E F1	320	MOV		A GET TAB LOC.	CHEST 4 8 8 8	sanneka 200	
				FIND WHICH TAB		1999 - 22C	
013F E645	321	JNC DIC	P6AA	FIND WHICH THE			
9141 19	322	1140					
3142 EA36	323	DJNZ	R2, P6BB				
0144 FC	324 SPRL	MOV	A, R4	EXCEED ALL TAB, FILL IN BLANKS			
0145 AA	325 P6AH:	MOV	R2, A				
0146 B020	326 RTAB:	MOV	@R0, #201	SOL AND BITH) : ADDRESS FOR SETH			
9148 18	327	INC	RØ				
0149 FA	328	MOV	H, R2	ROL AND GEFH) - ROL			
014A D8	329	XRL	A. R0	FILL IN BLANKS			
314B 9646	330	JNZ	RTAB				
014D 93	331 TERROR	RETR		\$28; (HFFFF) (HF \$28			
	332			DAR RND GFFH) DAR			
914E B255	333 CHECK5:	JB5	SEND	BONG. (NRTHE OWN BONG			
9150 FR	334 DATA	MOV	A) R2	SDMB RND GFFH) ; SDMR			
9151 AØ	335	MOV	0R0. A	SSOL RIED BEFREY : 550L			
152 18	336	INC	RØ	SLF RID DEFEND I SLF			
153 54ED	337	CALL	PEON	SET SPECIAL FLAG FOR LAST DATA	CHODOCTE		
155 93			FLON	SET SPECIAL PLAG FOR LAST DATA	CHIRACTE	283	
1100 93	338 SEND:	KETR					
MEE 5014	339	14511		T1 000 96FW : 11			
0156 B914	340 CMD:	MOV	K1, #14H	R1 EQ INDEX TO GHTS GROUP IT			
3158 FA	341 P7C:	MOV	A, R2	A GETS CMD			
159 17	342	INC	A				
815A D9	343	XRL	A, R1	ES: CHIRD SHEET IN			
015B C660	344	JZ	FOUND	MATCH ? JOSE CHARGE CHAR JOSE			
915D E958	345	DJNZ	R1, P70				
15F 93	346	RETR					
	347						
160 F9	348 FOUND:	140V	A, R1				
161 B3	349	JMPF	@A	JUMP INDIRECT TO CMD ROUTINE			15 F226
RIPH H	350			The state of the Root Inc.			
162 FE	351 DECR:	MOV	A, R6	93200		296	
163 9670	351 DECK.	JNZ	LARS	; DEC R6, R7 AS REG. PAIR, RET ON	100		

_OC	0BJ	SEQ	SOURC	E STATEMENT			
3466	966F	354	JNZ	NEST HOTELA			
3168		355	XCH	8. R3			
	53BF	356	ANL	A, #OBFH			
916B				A, R3			
		357	XCH MOV				
016C		358		STS, A P2, #20H ; ENASUE	INTERIET	414 872	
	8A20	333	UNL	LIGHT A	intektier .	415	
016F		360 NF		R7			
0170		361 LF		R6	VOM	417	
0171	93	362	RETR	RAL #39H J. 33 CHRR			
		363				419	
		364				659	
				******	i90:		
				OK UP TABLE.			
			*****	*****	*		
		368		P2. NDRH . SET ORG		424 505	
		369					
		370 T1		ADDR OF CMD JUMP I	N CMD TABLE	426	
		371 Ta		F.1 OR 0		427 902	
0172	17	372 T3	3: INC	A : A=0, 1,	OR 2H		
	5303	373	ANL	A. #03H - MASK S	IGNIFICANT	BITS	
0175	0315	374	ADD	A #15H ACCUM	= 15, 16, OR	17H - (RAM L	OCATIONS FOR TA
0177	62	375 51	TAB: MOY	T.A TEMP S	TORAGE FOR	TAB	
0178	3414	376	CALL	INPUT	X1.5%	411	
017A	0318	377	ADD	A. #18H			
0170	A9	378	MOV				
0170	42	379	MOV	A. T.			
017E	29	380	XCH	A, R1			
017F	A1	381	MOV	9R1, R		436	
0180	93	382	PETR	R) #87H			
		383					
0181	85	384 ML	F: CLR	FØ , MULTIP	LE LINE FEE	ED 823	
0182	248A	385	JMP	LF. MIRING		448 SDM	
		386	ECONNERS.	AND GROTE BEST		<b>大</b> 科中	
0184	97	387 T0	OF: CLR	C TOP OF	FORM	442	81CC 1474
0185	87	388	CPL	F2. #99FH 3			
0186	248A	389	JMP	LF : LFUTF		466	
		390					
0188	85	391 SL	F: CLR	FØ SINGLE	LINE FEED		
0189		392	CPL	F0 9030	4,380	447	91D4 3462
018A	F69C	393 LF	JC_	P12B LFUTOF			
018C	B693	394	JF0	P12A SINGLE	LF		
018E	3414	395	CALL	INPUT			
0190		396	MOV	R2. A	-908		
	C69B	397	JZ	P12C A 212			
	14DF	398 P1					BE OGIĐ
	F690	399	JC	P12B			
	B69B	400		P12C			810E 42
	EA93	400	DJNZ	END DE LUTER O	F OF LINES		
019B		492 P1			" OF CITACO		81E1 9644
0190		403 P1		A. P2			
	3293	404	JB1	P129		459	
019F		405	RETR				
- 231			an te said				
9199	3414	407 59	OL: CALL	INPUT FETCH	SOL. ON TIM	462 3	
	- 1 de 1	101 2	OILL	0 P7	- Ott 111	163	

LKL 704	40 SERIES PRINT	ER CUNTRU								
LOC	OBJ SE	3	SOURCE	STATEMENT	THIERE					
01A3	53F8 4	99	ANL	A. #0FSH				Espe		
01A5	6B 4	10	ADD	A, R3	10.8					
01A6	2B 4	11	XCH	A. R3		H3X				
01A7	93 4	12	RETR		30# .A			385		
	4	13			FR. RE					
01A8	FB 4	14 B32:	MOV	A, R3	32 CH	ARACTER	BUFFER			
		15	ORL	A, #10H						
		16	ANL	A, #ODFH						
01AD	AB 4	17	MOV	R3, A						
01AE	BC39 4	18	MOV	R4, #39H	33 CH	AR. /LIN	E			
01B0	0412 4	19	JMP	AGAIN						
	4	20								
01B2	8R04 4	21 502:	ORL	P2, #04H	SET G	02				
0184		22	RETR							
		23		122223222222			eteres.			
01B5	8A08 4	24 501:	ORL	P2, #08H	SET G	01				
0187		25	RETR							
		26	n dun i							
01B8	9AFB 4	27 RO2:	ANL	P2. #0FBH	1 9G 1	RESET	GD2			
01BA		28	RETR				302			
		29	GITENU.							
9188		30 RO1	ANL	P2, #0F7H	Die die	RESET	GO1			
01BD		31	RETR	C BUSE			18815	375		
		32								
01BE	89FF 4	33 RESET:	ORL	P1, #0FFH		RESET	PORT 1			
01C0		34	MOY	A, #ØBFH	A .19	ACAL	10111 1			
01C2		35	OUTL		RESET	PORT 2				
01C3	FB 4	36	MOY				EPT FOR	SERIAL &	SOL SS	
01C4	5387 4	37	ANL	A, #87H						
0106	AB 4	38	MOY	R3. A		RETR				
<b>01</b> C7	040E 4	39	JMP	CLR1	CLEAR	STS & R	ESET ST	ACK		
0109	1474 4	40 SDMA:	CALL	DMRIN						
01CB	RE 4	41	MOY	R6, A	LOAD I	DMA COUN	TERS			
01CC	1474 4	12	CALL	DMAIN						
01CE	9ADF 4	43	ANL	P2, #0DFH		CLEAR	INT PI	N		
0100	AF 4	14	MOY	R7. A						
91D1	4E 4	45	ORL	A, R6						
<b>01D2</b>	C662 4	46	JZ	DECR						
01D4	3462 4	47	CALL	DECR						
01D6	2B 4	48	XCH	A, R3		71				
01D7	4340 4	49	ORL	R, #40H	SET DI	MA FLAG		394		
01D9		50	XCH							
		51	MOY	A, #10H	SET FI	AG FOR	TELL HO	ST DMA ON		
01DC		52	MOA	STS, A						
01DD	93 4	53	RETR				ASER			
		54								
01DE		55 CR:	MOY			BMAX+1	LHU			
		56 234			IF BU	F PRIN	TED HUT	O, NO CR.		
		57	JNZ	SPRL		RETR				
01E3		58	RETR							
		59								
0454		50	Mari	0.55	10.5	9739				
01E4		51 B49:	MOV		40 CH	ARACTER I	DIECED			
		52		A, #OCFH	THPU					
01E7	no 4	53	MOV	R3, A	A. R3					

	40 SER								
LOC	0BJ	SEQ	9	OURCE	STATEMENT				
01E8	0410	464	8	JMP	CLEAR				
		465							
		466							
189 H		467	ex own Ti	TE ME					
01EA	2320	468	DWDE	MOY	A, #20H	DOUBLE I	WIDE PRINT MOD	E	
01E0	4B	469		ORL	A, R3	SET DW E	SZ4 TIE		
01ED	AB	479		MOV	R3, A				
01EE	B818	471	uton a o	100		CLEAR BI	UFFER POINTER		
01F0					A. R4	VON	527		
	D2F6	473		JB6	X0 8				
	BC2A	474		MOY		; 32 CHAR.			
01F5		475		RETR	IA A	132 CHIN.	DOTTER		
	7// 1//	11.5	VO.			40 01100	DIFFED		
	BC2C		X0:	MOV		; 40 CHAR.	BUFFER		
01F8		477		RETR					
	831 ON 98		M40700		91.92	03R			
01F9			RJ:	YOM	A, R3		BIT IN CMD		
01FA	4308	480		ORL	A, #08H				
01FC	AB	481		MOY	R3 / A				
01FD	93	482		RETR					
		483							
		484							
		485							
			: alcalcalcalcalcalcalcal	enderskrakenbaskrakenb			48.71	alestestestestestestestes	1308
					*******	*****	*********		
		407					******		
			; HBIT	SUBR.	AND THE DA	TA CONSTA	ANTS ARE IN PA	GE 3	12F4
		488	; HBIT	SUBR.	AND THE DA	TA CONSTA		GE 3	PRE
0250		488 489	; HBIT ;******	SUBR. OKKNON	AND THE DA	TA CONSTR	ANTS ARE IN PA	GE 3 ***********************************	SF4
03E0		488 489 490	; HBIT ;******	SUBR.	AND THE DA **********	TA CONSTR	HITS ARE IN PA	GE 3 *********	12F4 * 82F5
		488 489 490 491	; HBIT ;*****	SUBR. ******** ORG	AND THE DA ************************************	TA CONSTR	HITS ARE IN PA	GE 3 **********	82F4 82F5 82F6
03E0	22	488 489 490 491 492	; HBIT ;******	SUBR. ******** ORG IN	AND THE DA **********  ZEOH A, DBB	TR CONSTR	HITS ARE IN PA	GE 3 ***********************************	32F4 32F5 32F6 32F6
03E0		488 489 490 491	; HBIT ;*****	SUBR. ******** ORG	2E0H A, DBB A, #0F8H	TA CONSTR ************************************	HITS ARE IN PA	GE 3 **********	32F4 32F5 32F6 32F6
03E0	22 43F8	488 489 490 491 492	; HBIT ;************************************	SUBR.  CORG  IN  ORL	2E0H A, DBB A, #0F8H	TA CONSTA	HITS ARE IN PA	GE 3 ***********************************	92F4 12F5 32F6 32F6 32F8
03E0 03E1	22 43F8 A3	488 489 490 491 492 493	; HBIT ;************************************	SUBR.  CORG  IN  ORL	2E0H A, DBB A, #0F8H	TA CONSTR ************************************	HNTS ARE IN PA	GE 3	32F4 32F6 32F6 32F8 32F8
03E0 03E1 03E3 03E4	22 43F8 A3	488 489 490 491 492 493 308 30494 495	; HBIT ;************************************	SUBR.  *******  ORG  IN  ORL  MOVP	AND THE DA ************************************	TA CONSTA	ANTS ARE IN PA	GE 3	\$284 \$285 \$286 \$287 \$288 \$288
03E0 03E1 03E3 03E4 03E5	22 43F8 A3 AE	488 489 490 491 492 493 008 70 494 495 496	; HBIT; ********  HBIT:  CO 325 2	SUBR. *******  ORG  IN ORL MOVP MOV MOV	2E0H A, DBB A, #0F8H A, 0A R6, A P7, #03H	TA CONSTR ************************************	ANTS ARE IN PA	GE 3 ***********************************	12F4 12F5 12F6 12F7 12F8 12F8
03E0 03E1 03E3 03E4 03E5	22 43F8 A3 AE BF03	488 489 490 491 492 493 308 494 495 496 497	; HBIT; ************************************	SUBR. *******  ORG  IN ORL MOVP MOV MOV DUNZ	2E0H  A, DBB  A, #8F8H  A, 0A  R6, A  P7, #83H  R7, L00P2	THE CONSTR ************ CHECK DS	ANTS ARE IN PA	GE 3 ***********************************	12F4 12F5 12F6 12F7 12F8 12F8
03E0 03E1 03E3 03E4 03E5 03E7 03E9	22 43F8 A3 AE BF03 EFE7 EEE5	488 489 490 491 492 493 008 494 495 496 497 498	; HBIT; ********  HBIT:  CO 325 2	SUBR. **********  ORG  IN ORL *** MOVP MOV DJNZ DJNZ	2E0H A, DBB A, #0F8H A, 0PB A, #0F8H A, 0PA R6, A P7, #03H R7, L00P2 R6, L00P1	THE CONSTR ************ CHECK DS	ANTS ARE IN PA	GE 3 ***********************************	92F4 82F5 92F6 92F8 92F9 92F9
03E0 03E1 03E3 03E4 03E5 03E7 03E9	22 43F8 A3 AE BF03 EFE7 EEE5 0A	488 489 490 491 492 493 308 494 495 496 497 498 499	; HBIT; ********  HBIT:  CO 325 2	SUBR.  ORG  IN ORL MOVP MOV MOV DJNZ DJNZ IN	2E0H  A, DBB  A, #8F8H  A, 0A  R6, A  P7, #83H  R7, L00P2	THE CONSTREE TO SERVICE TO SERVIC	ANTS ARE IN PA	GE 3 ***********************************	12F4 12F5 12F6 12F7 12F8 12F8
03E0 03E1 03E3 03E4 03E5 03E7 03E9	22 43F8 A3 AE BF03 EFE7 EEE5 0A	488 489 490 491 492 493 308 494 495 496 497 498 499 500	; HBIT : HBIT : L00P1 : L00P2 :	SUBR.  ORG  IN ORL MOVP MOV MOV DINZ DJNZ IN RETR	2E0H A, DBB A, #8F8H A, 0P R6, R P7, #83H R7, L00P2 R6, L00P1 A, P2	TA CONSTR ************************************	ANTS ARE IN PA	GE 3 ***********************************	12F4 12F5 12F6 12F7 12F8 12F8
03E0 03E1 03E3 03E4 03E5 03E7 03E9 03E8	22 43F8 A3 AE BF03 EFE7 EEE5 0A 93	488 489 490 491 492 493 494 495 496 497 498 499 500	; HBIT : HBIT : L00P1 : L00P2 :	SUBR.  ORG  IN ORL MOVP MOV MOV DINZ DJNZ IN RETR	2E0H  A. DBB A. #0F8H A. 0A R6. A P7. #03H R7. L00P2 R6. L00P1 A. P2	TA CONSTR ************************************	ANTS ARE IN PA	GE 3 ***********************************	12F4 12F5 12F6 12F7 12F8 12F8
03E0 03E1 03E3 03E4 03E5 03E7 03E9 03EB 03EC	22 43F8 A3 AE BF03 EFE7 EEE5 0A 93	488 489 490 491 492 493 494 495 496 497 498 499 500 501	; HBIT ; ******** HBIT : L00P1 : L00P2 :	SUBR. *******  ORG  IN ORL MOVP MOV MOV DJNZ DJNZ IN RETR  XRL	AND THE DA *********  ZEOH  A. DBB A. #0F8H A. 0A R6. A P7. #03H R7. LOOP2 R6. LOOP1 A. P2  A. #0DH	TA CONSTR ************************************	ANTS ARE IN PA	GE 3 ***********************************	12F4 12F5 12F6 12F7 12F8 12F8
03E0 03E1 03E3 03E4 03E5 03E7 03E9 03EB 03ED 03ED	22 43F8 A3 AE BF03 EFE7 EEE5 0A 93 D39D 96F5	488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503	; HBIT ; ******** HBIT : L00P1 : L00P2 :	SUBR. *******  ORG  IN ORL MOVP MOV MOV DJNZ DJNZ IN RETR  XRL JNZ	AND THE DA *********  2E0H  A. DBB  A. #0F8H  A. 0A R6. A P7. #03H  R7. LOOP2 R6. LOOP1 A. P2  A. #0DH  XCR	TA CONSTR ********** ; CHECK DE ; 25US PER	ANTS ARE IN PA	GE 3 ***********************************	12F4 12F5 12F6 12F7 12F8 12F8
03E0 03E1 03E3 03E4 03E5 03E7 03E8 03EC	22 43F8 A3 AE BF03 EFE7 EEE5 0A 93 D39D 96F5 34DE	488 489 490 491 492 493 338 494 495 496 497 498 499 500 501 502 503 504	; HBIT ; ********  HBIT : 100P1 : 100P2 : 100P	SUBR. ******* ORG IN ORL HOVP MOV DINZ DINZ IN RETR XRL JNZ CALL	2E0H  A, DBB A, #0F8H A, 0A R6, A P7, #03H R7, L00P2 R6, L00P1 A, P2  A, #0DH XCR CR	TA CONSTE	ANTS ARE IN PA	GE 3 ***********************************	12F 3 12F 3 12F 7 12F 7 12F 11 12F 11
03E0 03E1 03E3 03E4 03E5 03E7 03E8 03EC 03ED 03EF 03F1 03F3	22 43F8 A3 AE BF03 EFE7 EEE5 0A 93 D39D 96F5 34DE BAFF	488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504	; HBIT ; ********  HBIT : 100P1 : 100P2 : 100P	SUBR. *******  ORG  IN ORL MOVP MOV DJNZ DJNZ IN RETR  XRL JNZ CALL MOV	AND THE DA *********  2E0H  A. DBB  A. #0F8H  A. 0A R6. A P7. #03H  R7. LOOP2 R6. LOOP1 A. P2  A. #0DH  XCR CR R2. #0FFH	TA CONSTE	ANTS ARE IN PA	GE 3 ***********************************	12F 3 12F 3 12F 7 12F 7 12F 11 12F 11
03E0 03E1 03E3 03E4 03E5 03E7 03E8 03E0 03ED 03EF 03F1 03F3	22 43F8 A3 AE BF03 EFE7 EEE5 0A 93 D39D 96F5 34DE BAFF FA	488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504	; HBIT ; ********  HBIT : 100P1 : 100P2 : 100P	SUBR.  *********  ORG  IN ORL MOVP MOV DINZ DJNZ IN RETR  XRL JNZ CALL MOV MOV	AND THE DA *********  ZEOH  A, DBB  A, #0F8H  A, 0P8  R6, A  P7, #03H  R7, L00P2  R6, L00P1  A, P2  A, #0DH  XCR  CR  R2, #0FFH  A, R2	TA CONSTE ************* : CHECK DE ; 25US PEF	ANTS ARE IN PA	GE 3 **********  **********  TRUE  F CP THI	92F4 932F5 92F7 92F8 932F8 932F0 932F0
03E0 03E1 03E3 03E4 03E5 03E7 03EB 03EC 03ED 03EF1 03F3 03F5 03F6	22 43F8 A3 AE BF03 EFE7 EEE5 0A 93 D39D 96F5 34DE BAFF FA 62	488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504	; HBIT ; ********  HBIT : 100P1 : 100P2 : 100P	SUBR. *******  ORG  IN ORL MOVP MOV DJNZ DJNZ IN RETR  XRL JNZ CALL MOV	AND THE DA *********  2E0H  A. DBB  A. #0F8H  A. 0A R6. A P7. #03H  R7. LOOP2 R6. LOOP1 A. P2  A. #0DH  XCR CR R2. #0FFH	TA CONSTE	ANTS ARE IN PA	GE 3 **********  **********  TRUE  F CP THI	92F4 932F5 92F7 92F8 932F8 932F0 932F0
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03E0 03E1 03E3 03E4 03E5 03E7 03EB 03EC 03ED 03EF1 03F3 03F5 03F6	22 43F8 A3 AE BF03 EFE7 EEE5 0A 93 D30D 96F5 34DE BAFF FA 62 93	488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508	; HBIT  CO 734 2  LOOP1 LOOP2  SPCR:  GST	SUBR. ********  ORG  IN ORL MOV MOV DJNZ DJNZ IN RETR  XRL JNZ CALL MOV MOV MOV RETR	2E0H  A, DBB A, #8F8H A, 0BB A, #8F8H A, 0BB A, #8F8H A, 0A A, 100P2 A, 100P2 A, 100P1 A, P2  A, #80H XCR CR CR CR R2, #8FFH A, R2 T, A	TA CONSTE	ANTS ARE IN PA	GE 3 ***********************************	1436 1437 1437 1438 1438 1438 1438 1438 1438 1438 1438
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02E5	69	530		ADD	A. R1				81F5 93
02E6	69	531		ADD	9, R1		. 9K	476	81F6 BC2C
92E7	69	532		ADD	A, R1				
02E8	6A	533		ADD	A. P.2	, ADD	COLUMN	INDEX TO	CHARACTER INDEX
02E9	B6F5	534	TIS LS	JF0	PAGE3	VOH	19		93 6316
02EB	E3	535		MOVP3	A. 0A	J580			91F9 4388
02EC	83	536		RET		LICHE			BR SREA
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02F8 02FA 02FC 02FD 02FF	BD06 EDFA 07 96F8 93	548 549 550 551 552 553 554 555 556 541 115 557 558 559	WAIT: CONX: UJ 939	MOV DJNZ DEC JNZ RETR  ******* RETR  ******* PACTER IS IGN E EXAMP	R5.#06H R5.CONX A MRIT TOULAND TABLE IN P ORED. DATB LE (A)	****** AGE 2. INVERT	PER CO	UNT OF AI	9725 1326 9725 2626 98 2526 98 2526 98 2526 9326 2625 93 2626 93 262 93 262 93 262 93 262 93 262 93 262 93 262 94 262 95 262 96 262 96 262 97 262 9
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02F8 02FA 02FC 02FD 02FF 0200 0200	BD06 EDFR 97 96F8 93	548 549 550 551 552 553 554 555 556 51 11 557 558 559 561 562 563 564	WAIT: CONX: UJ 939	MOV DJNZ DEC JNZ RETR ******** PACTER IS IGN E EXAMP ******* ORG DB	R5. #06H R5. CONX A MAIT ************************************	******  ******  ******  ******  ******	PER CO 1900.1 ******* ED ********	904 904 904 904 904 904 905 906 906 906 906 906 906 906 906	93E1 43F8 93E3 AS 93E3 AS 92E5 8F83 93E5 8F87 93E5 8F87 93ED 93E 93ED 93E 93EF 98F7 93EF 98F7 93EF 98F7
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02F8 02FA 02FC 02FD 02FD 0200 0201 0202 0203 0204 0205	BD06 EDFA 97 96F8 93 3U3 41 3F 62 3F 62 3F	548 549 550 551 552 553 554 555 556 558 559 561 562 562 563 564 565 566 567 568 569	WAIT: CONX: UJ 939 ; ************************************	MOV DJNZ DEC JNZ RETR RETR IS IGN EXAMP CORG DB	######################################	948US	******** ED *******	SEA	93E1 45F8 93E3 AS 93E4 AE 93E5 8F85 93E5 8F85 93E8 8A 93E8 8A 93EF 98F5 93E7 8EF5 93E7 8E
02F8 02FA 02FC 02FD 02FF 0200 0201 0202 0203 0204	BD06 EDFA 97 96F8 93 3U3 41 3F 62 3F 62 3F	548 549 550 551 552 553 554 555 556 559 561 562 563 564 565 565 566 567 568 569 578	WAIT: CONX: 1,****** 1, CHAR 1, MSB 1, SEE 2,******	MOV DJNZ DEC JNZ RETR RETR IS IGN EXAMP  *************************  ORG  DB  DB  DB  DB  DB  DB  DB  DB	######################################	9 48US	******** ED *******	904 904 904 904 904 905 906 906 906 906 906 906 906 906	93E1 45F8 93E3 AS 93E4 AE 93E5 8F85 93E5 8F85 93E8 8A 93E8 8A 93EB 98F5 93EF 98F5
02F8 02FA 02FC 02FD 02FD 0200 0201 0202 0203 0204 0205	BD06 EDFA 07 96F8 93 3U3 41 3F 62 3F 43	548 549 550 551 552 553 554 555 556 558 559 561 562 562 563 564 565 566 567 568 569	WAIT: CONX: ;****** ; CHAR ; MSB ; SEE ;******	MOV DJNZ DEC JNZ RETR RETR IS IGN EXAMP CORG DB	######################################	948US	******* ED *******	SEA	93E1 45F8 93E3 AS 93E4 AE 93E5 8F85 93E5 8F85 93E8 8A 93E8 8A 93EF 98F5 93E7 8EF5 93E7 8E

AFF4-00875A

		ES PRINTER	A								INTER CONTI			
OC OB.	J	SEQ.	33900	SOURCE	STATEMENT			LOC	OBJ	THEFTEN	SEQ ALCO	SOURCE S	TATEME	NT 180 1
209 58		574		DB	es 5BH	j	**-	0239	7F	HIP	629 90	DB 488	7FH	, H- 83
20A 3F	¥.	575		DB	8 3FH	j	78 *RESE	023A	77		630	DB 399	77H	
20B 5B		576	80	DB	5BH	j	**-	923B	7F		631 80	DB 383	7FH	
20C 6F		577		DB	⇔6FH	i	07-3*	923C	77		632 80	DB 789	77H	30 36
200 70		578		DE	5470H	j	***	023D		184	633 90	DB 888	7FH	
		579					629E 7D	023E			634 80	DB 289	99H	
20E 3E		580	41.10	DB	3EH	; B	829F 78	DEDE	00	Hith	635	698	COIT	
20F 41		581		DB	41H		59 8858	023F	75		636	DB 193	7FH	; I
210 3E		582		DB	3EH			9240		H99	637 90	DB Sea	3EH	89.6
211 77		583		DB	77H			0241		HES	638 90	DB 283	7FH	
212 3E		584	100	DB	3EH					378	639 80		00H	
213 77		585		DB	77H			0242		HET				
214 49		586		0.5	49H		dr. SASS	0243			648		7FH	
214 43		587		VO				0244			641 80	DB 969	3EH	
045 44				DD	/52	.0		0245	14		642	DB	7FH	37.75
215 41	W.	588		DB DB	41H	; C	35 9838			Hab	643 80	869		35.3
216 3E		539			∌93EH		19 7829 B1	9246			644	DB 659	7DH	, J
217 7F		590		DB	7FH			9247	7E	HIP	645	DB	7EH	25 2
218 3E		591			3EH		30, 6428	0248	7F	Has	646	DB 16	7FH	
219 7F		592			727FH			0249	7E		647	DB S	7EH	
21A 3E		593	90	DB	3EH			024A	7F		648	DB	7FH	
218 50		594	80	DB	e-5DH			924B	7E		649	DB	7EH	
		595	90				89 3858	024C	01		650	DB	01H	QE 3
210 3E		H 596		DB	T93EH	)D	GE GRS6			HSP	651			0.42
210 41		4,597		DB	341H			924D	00		652	DB	99H	, K
21E 3E		598		DB	3EH			024E	7F	H59	653 80	DB 383	7FH	E 88
21F 7F		599		DB	127FH		R2 3858	024F		HRS	654	DB 295	6FH	
220 3E		600			3EH			9250			655	DB BIT	77H	
221 7F		601			7FH			0251			656 80	DB 11	5BH	1 7F
222 41		682			41H			0252			657 80	DB SIT	7DH	
		683						0253			658 80	DB ERS	3EH	
223 00		604			90H	E	92 MSS0	0203	25		659 93	714	JEII	4 4E
224 7F		605		0.0	7FH		9285 35	9254	00		660	715 BQ	00H	
225 36		606		DB	36H			0255			661 80	DB 917	7FH	S 49
226 7F		607		0.0	7FH		35 3908 3E	0256			662 80			, <u>e</u> c a
227 36	5			0.0	36H		8287 7B	The state of the s		HAY.	663 90		7EH 7FH	32.2
228 7F	2	609			7FH			0257		Has		DB CAN		
229 3E		610			= 3EH			0258					7EH	9.75
22. 32		611	90.4				8289 77 2000 OF	0259		HT's	665	DB 037	7FH	
22A 00		612		0.0	90H	F	828R 2E	025A	/E		666 80	DB 127	7EH	65.8
22B 7F						21					667 80			
220 37		613		08	7FH			025B			668	DB S	49H	·M
		614			e537H			0250			669	DB +27	3FH	
22D 7F		615		nn.	087FH		8280 89	025D			679 80	DB GZ	5FH	
22E 37		616		0.0	1937H		9288 75	025E	-	HEE	671	DB S	67H	
22F 7F		617			7FH			025F		1994	672	DB	5FH	
230 3F		618			883FH		8208 (F	0260	3F		673 80	DB 82	3FH	9 3F
074		613			784			9261	40	H32	674 80	DB 827	40H	
231 41		620			-841H	: G					675			
232 3E		621			383EH			9262	20		676	DB	20H	
233 7F		622		DB	787FH			9263	SF ·	H18	677 30	DB ST	5FH	; NO E
234 3E		623			3EH		82C4 3F	0264	6F		678 80	DB 25	6FH	
235 78		624			9.7BH		92.05.56	0265	77	MER	679 90	DB S	77H	
236 3E		625			3EH		49 9008 GF	9266	7B	HBT	688	DB ON	7BH	37 g
237 59		626		DB	59H			0267		H-JZ.	681 80	DB 300	7DH	77. 7
		627	130				8208 78	0268			682 90	DB 222	02H	37.8
238 00		628		0.0	99H		07 8358			HIG				18 6

.00	0BJ	тизизти	5	EQUALITIES	50	URCE	STATEME	NT 180		LOC	OBJ		THE SEQ		SOURCE	STATEMENT			
0269	41			684	D	B esa	41H	; 0					739	90					
326A	3E			685	D	B 953	3EH			029A	97		749		DB	07H	, 4		
326B	7F			686	D	B	7FH			929B	7B		741	80	DB	7BH		80	
3260	3E	457		687	D		3EH			029C	70		742		DB	7DH			
126D	7F			688	D	В	7FH			0290	7E		743		DB	7EH			
326E	3E			689	D	В	3EH			029E	70		744		DB	7DH			
326F	41			690		B 223	41H			029F	7B		745		DB	7BH			
		HEY		691						02A0			746		DB	97H			
3270	00			692	D	B 150	00H						747			382			
3271		HHS		693		B 853	7FH	i P		9281	91		748		DB	01H			
3272				694		Besa	37H			92A2	1000		749		DB	7EH			
3273						BRAG	7FH			92A3			750		OB	7DH			
0274							37H			92A4			751		DB	73H			
0275					D	B	7FH						752		DB				
0275 0276				697 698			4FH			02A5				90		7DH	. 11		
0210	45				υ	B	450			92A6					DB	7EH	; H		
2777	44	H02		699		644	4411			0287	61		754		DB	01H			
3277				700 80		Baya	41H		7450	2000			755						
3278				701 80		B 313	3EH		8248	02A8			756		DB	3EH	: X		
3279				702 80	_	B 549	7FH			02A9			757		DB	5DH			Al
327A				703 90		B 819	3FH			02AA			758		DB	6BH			
327B		HGV		704 83		B 619	7AH			02AB			759		DB	77H			
0270				705		B 000	3DH		3438	92AC			760		DB	6BH			
027D	42			796	D	B 159	42H			92RD			13761		DB	50H			
				707 gg						92AE	3E		762		DB	3EH		14	
927E				708 80		B	98H	iR.					763						
927F	7F			709 80	D	B	7FH			02AF	3F		764		DB	3FH	:Y		
0280	37			710	D	B 289	37H	. 22	8838	0280	5F		765		DB	5FH			
0281	. 7F			711 90	D	B	7FH			0281	6F		766		DB:	6FH			
3282	33	HUT		712 80	D	B	33H	0.0		82B2	70		11767		DB	70H			
9283	70			713 90	D	B 828	7DH		8253	02B3	6F		768		DB	6FH			
0284	4E			714	D	B 023	4EH			92B4	5F		769		DB	5FH			
		1466		715						02B5	3F		779		DB	3FH			
9285	4D	HAZ		716	D	В	4DH						18771						
9286	36			717		B 539	36H			02B6	3E		772		DB	3EH			
0287	7F			718		В	7FH			9287	70		773	98	DB	807DH	:2		
0288				719		B 143	36H			02B8			11774		DB	3AH	-		
9289		799		720 95		8	7FH			8289			H3775		DB	77H			
028A				721 93		8	36H			02BA			776		DB	2EH			
028B				722	D		59H			02BB			777		DB	5FH			
		15576		723 🐖			03.1			92BC			1778		DB	3EH			
9280	3E	H64		724	D	6 233	3FH			0200	7,6		779	- 89	VD	418 418			
928D				725		8	7FH			92BD	90		780	90	DB	аан	r		
928E														80		200	,[		
028F				726 gg 727 gg		8 179	3FH 40H	T		92BE 92BF			781 782	30	DB	7FH			
0290						8 279			8258					96	DB	3EH			
9291		HAE		728 90		B 229			8909	9209			783		DB	7FH			
				729 80		B +73	7FH		1988	9201			784		DE	3EH			
3292	12			730	D	B 338	3FH			0202		g.	785	0.0	DB	7FH			
2005				731 80		878	0411		2920	0203	11		786	90	DB	2FH			
3293				732 80		B 229	01H				25		787	80		223			
3294		H39		733 89		B 829	7EH			0204			789		DE	3FH	17		
3295				734 80		B 649	7FH		\$958	9205			789		DB	5FH			
3296				735 80		B 888	7EH	32	9556	0206			790	80	DB	6FH			
0297		FDH.		736 80		B 189	7FH		7958	9207			791	90	DB	77H			
9298				737 80		B 589	7EH		8928	0208	7B		792		DB	7BH			
3299	191			738	D	B 283	01H			0209	7D		793		DE	7DH			

15-11 MCS 2 7040 SE	RIES PR	-41 MI INTER	CONTR	SSEMBL OLLER	ER, V2.0 SOURCE CODE	932 0407 DRJ			/UPI-41 MACE S PRINTER CO			
OC OBJ		SEQ	2011	SOUR	CE STATEMENT	tao 30J	LOC	0BJ	SEQ.	SOURCE	STATEME	NT <sub>OO</sub> J
02CA 7E		794		DB	<sub>рэр</sub> 7ЕН		0311	7F <sub>LORG</sub>	849	BO DB	7FH	FASA
		795					0312	0F	850	DE	0FH	
32CB 7F		796	80	DB	7FH	The lateral la	0313	7F	851	DB	7FH	
9200 7F		707		DB	SELL		0314		852	OB DB	7FH	2458
	H3S						9314	HE'S			111159	
92CD 3E		798		D3	256 3EH		2745	199	80853	998	45	6345
02CE 7F		799		DB	7FH	19 9718 41	0315		854	686 DB	6BH	3 #
02CF 3E		800		DB	3EH		0316	7First	855	B to DB	7FH	
32D0 7F	N-75	801		DB	7FH	6377 7F	0317	00	856	DB	00H	
02D1 00	H36	000		DB	00H		0318	7F	857	CL DB	7FH	
		002					0319	99	858	DB	99H	
92D2 77	HT	201	80	DB	838 639 77H	8379 7F	931A		859	DB	7FH	
	H94	OOF			argent t	837N 98	031B		860	DD		
92D3 6F	Har			DB	876 9ŁH	8378 7F	6219	OD		STEDB	6BH	<b>9348</b>
32D4 5F		806		08	TOP 5FH			H22	861	916		SHEE
92D5 20				DB	STO 20H	8370 7F	031C		862	DB	4DH	;\$
32D6 5F		808		DB	SFH SFH		931D	36	863	DB	36H	
2D7 6F		809	30	DB	6FH	32 3256	031E	7F <sub>HRS</sub>	864	P NO DB	7FH	
2D8 77		810	93	DB	250 77H	8277 38	931F	00	865	ese DB	90H	28.00
		811					0320	7E	866	DD)	7FK	
92D9 7E		212		DB			0321	100.00	867	80 922 BU 922	36H	
32D8 7F					ment t	1-12 1858	0322				59H	
		813		DB	STE 7FH		6255	33/14	ag 868	DB	Jan	
02DB 7E		814		DB	ese 7EH			778	869	ASE_	- 22	1519
32DC 7F				DB	886 LEH		9323		870	SSO DB	0EH	1%
9200 7E		816		DB	188 7EH		9324	7D	871	age DB	7DH	
2DE 7F		817		DB	SSE 7FH		0325	0B	872	DB	0BH	
2DF 7E		818		DB	280 7EH		0326	77	873	eco DB	77H	
		819			186		9327	68	874	DB	68H	
		820					0328		875	D8	5FH	
		821					0329		876	DD	38H	
			80	destrot strates to the	386	93.89.2F	0323	39/11/	077	TEE DB	2011	
		822				*****	0200	HAY	ag 877	5322	4011	ACTE
					BLE ON PAGE		032A		878	DB	49H	j &
		824	; MS	B IS I	GNORED, DATA	INVERTED	932B		80 879	DB DB	36H	
		825	AND SE	E EXAM	PLE (A) IN P	AGE 2 OF ROM	032C	7F	880	DB	7FH	9850
		826	<i>;</i> ****	*****	*******	*********	032D	37	881	ace DB	37H	
		827					032E	5A	882	DB	5AH	
1300		828		ORG		93 9858 SF	032F	70	883	DD.	7DH	
		829			994	0390 20	0330		884	DD.	72H	
300 7F		830		08			0230	71.15	885	620		
						BLANK	0224	70		896	7511	1920
301 7F		831	90	30	age 7FH		0331		886	DB DB	7FI;	11
1302 7F		832		DB	SEE 7FH		0332		887	DB DB	7FH	
303 7F				ÐΒ	SEG SEH		0333	7F	888	See DB	7FH	
1304 7F		834		DB	eee 7FH		9334	0F	889	DB	0FH	
305 7F		835	80	08	8891 7FH	75 8658	0335	7F	890	(sp	7FH	
306 7F		***	80		1881 /FH	9396 76	0336		891	DB	7FH	
					2001			7F	892	DB	7FH	
307 7F				NO.		9397 3F	6331			OB DB		
					7FH	3 59 8888 GE	0220	75	893	846 00	701	
308 7F					MREE 7FH	12 6658	0338		894	DB DB	7FH	
309 7F		840			7FH		0339		ag 895	DB	63H	2328
30A 02		841		DB	3901 02H		033A	5D	896	DB		
30B 7F		842		DB	1991 7FII		033B	3E	897	CHO DB		8928
30C 7F		843			8801 7FH		033C	7F	898	DB DB	7FH	
300 7F		844			9881 7FH		933D		000	DB	7EH	
		845			1918		033E	370	999	DB	7FH	0358
30E 7F		846					9230		994	DB	11110	30:00
30F 7F					1191 7FH	939F 76";	9775	7E	901	ND.	7511	836F
NIE /F		847		DB	S191 7FH		033F	7F	902 903	DB	7FH	;)
310 OF		848			0FH					See DB	7FH	

OC OBJ	SEQ	SOURCE	STATEMENT	LOC	0BJ	TIGNETT SEQ		SOUR	CE S	TATEMENT		
9341 7F	904	30	7FH	0371		959		DB		7FH		
9342 3E	905	DB		0372		960		DB		3AH		
0343 5D	906	DB	5DH	0373	77	961		DB		77H		
9344 63	907	DB	63H	0374	2E	962	30	DB		2EH		
9345 7F	908	DB	7FH	9375	7F	963	D/3	DB		7FH		
	909		9315 68	9376	41	964		DB		41H		
9346 77	910	DB	77H **			965						
0347 5D	911	DB	5DH TARREST	0377	7F	966		DB		7FH	;1	
9348 6B	912	DB	6BH 8128	0378		HS9 967		DB		5EH	-88	
0349 14	80913	DB	14H	0379		968		DB		7FH		
934A 6B	914	DB	6BH	0379 0378		969		DB		99H		
blots.	80915	DB	5DH			979		DB		7FH		
034B 5D		130		037B		210						
934C 77	916	DB	77H OP 3229	0370		211		DB		7EH		
1495	917	530		037D	1	216		DB		7FH		
934D 77	918	DB	15000			213						
934E 7F	919	DB	7FH 3328	937E		974		DB		5CH	;2	
934F 77	920	DB	77H	037F	3B	975		DB		3BH		
0350 49	921	DB	49H	9389	7E	976		DB		7EH		
0351 77	922	DB	77H	0381	37	977		DB		37H		
0352 7F	923	DB	7FH 3358	0382	7E	978		DB		7EH		
9353 77	924	DB	77H	0383	37	107 979		DB		37H		
1498	925	- 878	8322 96	9384		980		DB		4EH		
9354 7F	926	DB	7FII 17			981				1211		
9355 7F	927	DB	7FH CSEA	0385	20	982		DB		3DH	; 3	
0356 7F			THE NAMES	0386		983	90	DB		7EH		
10.00	928	DB	1111									
0357 7E	929	DB	I LIT	0387		984		DB		2FH		
9358 79	930	DB	1.211	0388		985		DB		7EH		
9359 7F	931	DE	1FN	0389		986		DB		2FH		
035A 7F	932	DB	7FH			987				56H		
	933			038B		988		DB		39H		
035B 7B	934	DB	7BH ;-	931		1 AIRG (1989			824			
935C 7F	935	DB	7FH 3356	0380	7B	990		DB		7BH	; 4	
035D 7B	936	DB	7BK 2 0S29	038D	77	991		DB		77H		
935E 7F	937	DB	7FH	038E	6B	992		DB		6BH		
935F 7B	938	DB	7BI) 7558	038F	5F	993		DB		5FH		
9369 7F	939	DB	7FH T BEER	0390	20	994		DB		20H		
9361 7B	940	DE	7BH	0391	7F	995		DB.		7FH		
THE	80 941	888	42 TEEB	0392		996		DC		78H		
9362 7F	942	DB DB	7FH 7.			997		00		1511		
0362 7F	942	DB	7FH 7.	0393	an	998		DB		ØDH	,5	
			ttu	0394		999						
0364 7F	944	DB	(FII		-			DB		7EH		
9365 7E	945	DB	( EII	0395		2000		DB		2FH		
9366 7F	946	DB	7FK	0396		1991		DB		7EH		
0367 7F	947	DB	7FH	0397		1902		DB		3FH		
3368 7F	948	DB	7FH	0398		1903		DB		6EH		
	949			0399	31	1994		DB		31H		
9369 7E	950	DB	7EH 37			1005						
036A 7D	951	DB		039A	79	1906		DB		79H	,6	
936B 7B	952	DB	7BH	039B		1997		DB		76H		
936C 77	953	SES DB	77K 3ES8	0390		1008		DB		6FH		DSIE
936D 6F	954	DB	6FH GEER	039D		1009		DB		56H		
936E 5F	955		5FH 3229	039E		1010		DB		3FH		
		100	OLU.	039E		HRV 1011		DB				
336F 3F	956 957	DB	3FH	033P		1912						
								DB				

IS-II MCS-48/U C 7040 SERIES I					PAGE		LRC 78	40 SE	RIES PR	INTER CO	Maria Strategia (Maria Salahan	SOURCE CODE	
100 B867		CHECKS		9840 TEMENT	6668	620	9318 9338	919		832		1909 306	
LOCA OBJ	SEQ		DURCE STA		9630	W00	LOC			SEQ		E STATEMENT	6 513
FOUND 9159	8789	3917		3084	8974		And the Contract of the Contra			0030			
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03A2 7F 5J				FH	5328		03D2	7F		1070		7FH	
03A3 38 AS19	1016	340 [	)B 3	SH S	F0.16		93D3	7F	3110	1071	DB	7FH	
03A4 77	1017	8884 [	)B 7	7H	9128		03D4	3E	E300	1072	DB	3EH 3EI	
03A5 2F	1018	TBEBRI	)B 2	FH			03D5			1073	DB	5DH	
03A6 5F 00033	1019	\$100 E	OB 5	FH	91.46		03D6		9029	1074	DB	6BH	
03A7 3F J022	1020	1882 [	DB 3	FH			0307		8810		DB	277H 378	
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03AB 36	1025	[	DB 3	6H			03DB	3F		1080	DB	3FH	
03AC 7F	1026	[	DB 7	FH			03DC	7A		1081	DB	7AH	
03AD 36	1027	[	DB 3	6H			0300			1082	DB	37H	
03AE 49	1028	[	DB 4	9H			03DE			1083	DB	4FH	
	1029						93DF			1084	DB	7FH	
03AF 4F	1030	I	DB 4	FH	;9		0301	11		1085	VU	1111	
0380 37	1031			7H							THE		
03B1 7F	1032			FH						1086	END		
03B2 36	1033			6H			844						
03B3 7D	1034			DH									
03B4 3B	1035			BH BH									
0385 47	1036	[	DB 4	7H									
	1037												
03B6 7F	1038	[	DB 7	FH									
03B7 7F	1039	[	DB 7	FH	1:								
03B8 7F	1040			FH									
03B9 6B	1041			BH									
03BA 7F	1042			FH									
03BB 7F	1043			FII									
03BC 7F	1043												
03DC 1F			70 (	FH									
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03BD 7F	1046			FH	11								
03BE 7F	1047			FH			1						
03BF 7E	1048	I	)B 7	EH									
0300 69	1049	[	DB 6	9H			11.0						
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03CF 6B	1066			BH									
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	1068		)B 6	BH									

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TS .	99A5 DATA	9159	DECO 0016	DECR 9162	DMAIN	9074	DWDE	01EA	FIRE	997B	FOUND	0160
SPA	02F4 HBIT	03E0	HOME 906A	INBUF 0077	INIT	9999	INPUT	0114	110	00E9	IT1	00EA
1	0004 LARS		LF 018A	LOAD 00CE	LOOP1	03E5	L00P2	03E7	LSTCOL		LZ	00B6
1LF	0181 NHOM		NODECR 0110	NOTS 003F	NRST	016F	ONHSE	0024	ONE	00A7	P128	0193
12B	019C P12C		P30 00E3	P3F 00F6	P6A	0128	P6AA	0145	P6BB	0136	P7C	0158
PAGE	0038 PAGE		PARA 0008	PEON 02ED	PF	00DF	PRINT	001E	RESET	01BE	RJ	01F9
RJ2	0064 RJP	004D	R01 0188	R02 0188	RTAB	0146	SDMA	0109	SEND	0155	SERROR	
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STAB	0177 T1	0172		T3 0172	TAB	0132	TERROR		TOF	0184	W14	00BE
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Refer to the updated application note AP-97A "5-Volt Only Dynamia RAM interface for 8036 Systems", January 1982, for the latest product information.

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## WHY DYNAMIC MEMORIES?

Dynamic RAM offers a four-to-one size advantage over their static RAM counterparts in medium to large size memory systems. In a typical 8086 system with 128K bytes of memory, you would need over 256 IC's and 300 square inches of PC board for a static memory array. The same memory array could be implemented with 68 IC's and 80 square inches of PC board if dynamic RAMs are used.

Besides this obvious size advantage, dynamic RAM designs offer a substantial power dissipation advantage. For example, the 2142 static RAM requires 0.1 mW/bit operating power, while the 2118 dynamic RAM requires only 0.01 mW/bit.

In the following sections we will show how to construct a complete dynamic memory interface for your 8086, 8088, and 8089 systems, using the 8202 dynamic RAM Controller and the 2118 5-volt only dynamic RAMs.

## TYPES OF DYNAMIC MEMORY SYSTEMS

Dynamic memory systems can be divided into two categories: 1) those that use distributed (or asynchronous) refresh and 2) those that use hidden (or synchronous) refresh. Each type has advantages over the other type; your choice will depend on your system requirements.

In a distributed refresh system the memory controller periodically requests a refresh cycle, typically every 10–16 microseconds. Since the refresh request is asynchronous to the CPU's request for the memory, the memory controller must have logic to arbitrate the requests. Once a cycle starts, the arbiter must let that cycle complete before starting a pending cycle. The memory controller should also have circuitry which can force the CPU to add WAIT state if a memory cycle is requested while a refresh cycle is in progress.

Hidden refresh designs use circuitry to monitor the CPU status lines, and request a refresh cycle when the CPU is not performing a bus cycle with the dynamic RAM. For example, a hidden refresh cycle can overlap an instruction fetch from ROM. If the hidden refresh cycles are performed frequently enough, the dynamic memory is always ready when the CPU requests a memory cycle, and no WAIT states are required due to arbitration.

Some memory systems use a combination of asynchronous and hidden refresh. For example, many real time systems allow a processor to enter a HALT state (which stops program execution) while waiting for an interrupt. During this time, the hidden refresh circuitry is inactive, and the asynchronous refresh logic inserts the necessary refresh requests. The Intel 8202 Dynamic Memory Controller provides a complete memory interface for your dynamic RAM. It can be used in synchronous and asynchronous refresh systems, and provides automatic switching between these two modes.

## 8086 SYSTEM CONFIGURATION REVIEW

## Quick Review of 8086 Family Bus Timing

There are three basic 8086 family system configurations:

- 1) Minimum Mode
- 2) Maximum Mode
- 3) Alternate Configuration

The 8086 has a  $MN/\overline{MX}$  input which can be strapped high to select Min Mode, and grounded to select Max Mode. The  $MN/\overline{MX}$  input changes the function of several other 8086 pins based on how it is strapped.

In the Min Mode, the CPU generates the  $\overline{RD}$  and  $\overline{WR}$  outputs directly. The Max Mode uses an 8288 to generate the 8202  $\overline{RD}$  and  $\overline{WR}$  signals from the CPU status lines. Refer to the "8086 Family Users Manual" for more details.

The Alternate Configuration uses several TTL gates and flip-flops and the CPU status outputs to generate the 8202  $\overline{RD}$  and  $\overline{WR}$  signals. The Alternate Configuration can be used when the CPU is strapped in either the Min Mode or the Max Mode. Each of the three basic system configurations can be used with data buffers for additional drive capability.

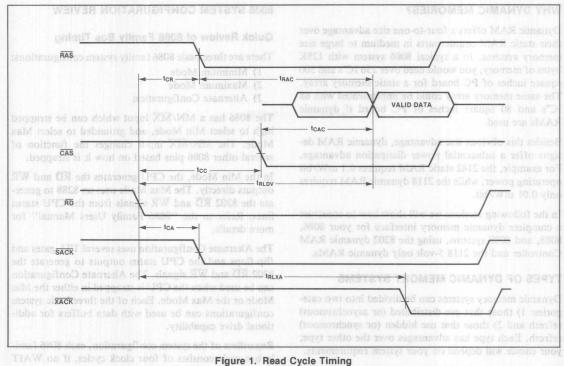
Regardless of the system configuration, each 8086 family bus cycle consists of four clock cycles, if no WAIT states are required. WAIT states can be used to extend the basic bus cycle, and thus allow the use of slower memories.

We will see in the following sections that the Min Mode will offer the lowest chip count, the Max Mode will offer better performance, while the Alternate Configuration will offer higher performance at the expense of several TTL packages.

## 8202 Read Cycle Timing

The 8202 uses its clock to sample the (asynchronous) READ requests generated by the CPU. When the RD input is sensed active, the 8202 will generate a RAS strobe and CAS strobe as shown in Figure 1. The RAM uses RAS and CAS to latch the CPU address and read the desired location onto the RAM data output pin. The 8202 also generates an XACK strobe which is used to latch the RAM data for the CPU, as shown in Figure 2. (See "READY HANDSHAKE SIGNALS" for further uses of XACK.)

We can determine the amount of time it takes to generate valid READ data by calculating the delay from  $\overline{RD}\downarrow$  to  $\overline{CAS}\downarrow$ , and add this with the RAM's CAS access time (t<sub>CAC</sub>) and the latch's propagation delay. In other words,



states are required. WAIT states can be used to extend In a distributed refresh system the memory controller

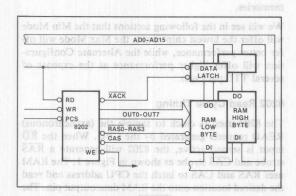


Figure 2. Basic Memory Architecture latch the RAM data for the CPU, as shown in Figure 2.

Since the t<sub>CC</sub> parameter is a function of the 8202's operating frequency, we can minimize tRI DV by running the 8202 at the highest possible frequency. We can also reduce tRLDV by choosing a RAM with a faster CAS access time. Table 1 shows the minimum tripy for the various RAMs, based on the maximum 8202 frequency for that RAM. If system constraints force you to choose a slower 8202 operating frequency, then your tRLDV will increase, which may slow down your CPU.

Table 1. 8202 System Timing

RAM TYPE	trac	tcac	tRLDV1	tca1	t <sub>RLXA</sub> 1	tcc, MIN <sup>1,2</sup>	fMAX
2118-3	100	55	280	80	445	125	25.00
2118-4	120	65	290	80	445	125	25.00
2118-7	150	80	310	81	456	126	24.24
2117-2	150	100	325	80	445	125	25,00
2117-3	200	135	361	80	449	126	24.69
2117-4	250	165	407	85	488	136	22.22
JNITS	nsec	nsec	nsec	nsec	nsec	nsec	MHz

<sup>1.</sup> ASSUMES 8202 OPERATED AT IMAX. BD SLOVE HES THEN HOS BUT IN STREET HE 1. ASSUMES GREET OF DERIVE toc. MAX.

## Read Access Time (Min Mode)

In order to operate with no WAIT states, our memory system shown in Figure 3 must guarantee valid READ time systems allow a processor to enter a limit within:

$$t_{RLDV} \le 2 t_{CLCL} (CPU) - t_{CLRL, MIN} (CPU)$$
 $-t_{DVCL, MIN} (CPU)$ 

Table 2 lists these times for various CPUs, operating at 5 MHz and 8 MHz. If your system has any additional buffers for the RD, WR, or data lines, you must subtract their propagation delay from the tRLDV values in Table 1 to derive your system access requirements.

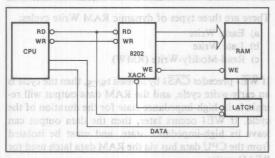


Figure 3. Unbuffered Min Mode Configuration

Now we merely have to compare our system requirements from Table 2 with the memory access times in Table 1 to see if our RAM speed selection and 8202 operating frequency will work in our system with no WAIT states. If our system requirement is too fast for our first choice memory configuration, we will have to choose either a faster RAM, or add WAIT states.

If you choose to run with WAIT states, you can multiply the CPU clock period by the number of WAIT states, and add this number to the t<sub>RLDV</sub> values in Table 2 to derive your new CPU access requirements. For example, a 5 MHz 8086 Min Mode configuration with no WAIT states requires a read access time of 205 nanoseconds, while the same configuration would need an access time of only 405 nanoseconds if we operate with one WAIT state. If we examine Table 1, we see that there is no RAM configuration which can run without WAIT states in a 5 MHz 8086 configuration; but we can use any 2118 speed selection if we operate with one WAIT state.

Table 2. Read Cycle Access Requirements

		MIN MODE			MAX	MODE	
	8086-2	8086	8088	8086-2	8086	8088	8089
fcpu	8 MHz	5 MHz	5 MHz	8 MHz	5 MHz	5 MHz	5 MHz
tRLDV	130	205	205	195	335	335	335
tRLDV,	209	345	345	209	345	345	415

# Read Access Time (Max Mode)

Figure 4 illustrates the standard unbuffered Max Mode configuration. In order to run with no WAIT states, we need to guarantee a READ access time of

$$t_{RLDV} = 2 t_{CLCL} (CPU) - t_{CLML, MAX} (8288)$$
  
-  $t_{DVCL, MIN} (CPU)$ 

These times are listed in Table 2 for the various CPUs, operating at 5 MHz and 8 MHz. If your system has buffers on the RD, WR, or data lines, you must subtract their propagation delay from the t<sub>RLDV</sub> values in Table 2.

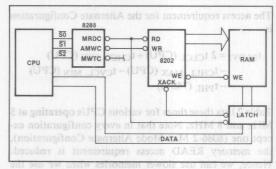


Figure 4. Unbuffered Max Mode Configuration

If we compare the Max Mode  $t_{RLDV}$  requirements in Table 2 with the Min Mode requirements, we notice that the Max Mode can run with a memory configuration that is 130 nsec slower than the memory required for an equivalent Min Mode configuration! In fact, all 5 MHz Max Mode CPU configurations can operate with no WAIT states in any of the 2118 memory configurations. Even the 8 MHz 8086-2 configuration can operate with all but one RAM configuration (2117-4) with only one WAIT state. This illustrates the advantage of using the Max Mode and the 8288 to generate the  $\overline{\rm RD}$  signal for the 8202 when compared with the lower chip count Min Mode.

# **READ Access Time (Alternate Configuration)**

We can reduce our memory speed requirement even further by using the Alternate Configuration shown in Figure 5. This circuit uses the CPU status information to generate 8202  $\overline{RD}$  and  $\overline{WR}$  commands which start earlier in the memory cycle than either the Min Mode or the Max Mode. As previously stated, the Alternate Configuration can be used when the CPU is strapped in either the Min Mode or the Max Mode.

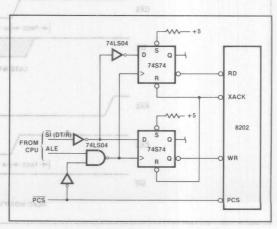


Figure 5. Alternate Configuration

The access requirement for the Alternate Configuration

 $t_{RLDV1} = 2 t_{CLCL} (CPU) + t_{CHCL, MIN} (CPU)$ -t<sub>CHLL</sub>, MAX (CPU) -t<sub>CVCL</sub>, MIN (CPU) - tphi (74S74)

Table 2 lists these times for various CPUs operating at 5 MHz and 8 MHz. Note that in every configuration except one (8086-2 Max Mode Alternate Configuration), the memory READ access requirement is reduced. Hence, we can use slower memories when we use the Alternate Configuration in all but this one configuration. In general, the Alternate Configuration offers a significant advantage over the standard Min Mode, but little advantage over the standard Max Mode for READ cycles. The women a drive air men should sald sald

# 8202 Write Cycle Timing Theo about and instavingo

8202 WRITE cycles have timing similar to READ cycles, except the WE line is pulsed for the WRITE cycle; all other signal times are the same as a READ cycle.

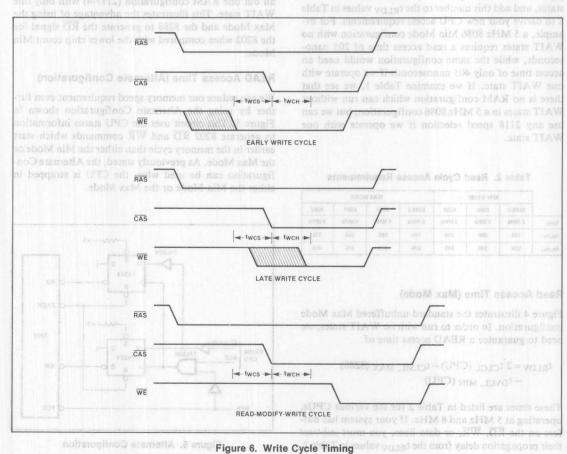
There are three types of dynamic RAM Write cycles:

- a) Early Write
- b) Late Write
- c) Read-Modify-Write (RMW)

If WE↓ precedes CAS↓ by at least twcs, then the cycle is an early-write cycle, and the RAM data output will remain in its high-impedance state for the duration of the cycle. If WE↓ occurs later, then the data output can leave its high-impedance state, and must be isolated from the CPU data bus via the RAM data latch used for READ cycles.

The dynamic RAM uses the WE and CAS signals to strobe the WRITE data into the RAM. If WE↓ precedes CAS, as shown in Figure 6, then the data setup and hold times are measured relative to CAS, and the cycle is called an "early-WRITE" cycle. If the CPU starts a WRITE cycle by driving WR active, and does not let WR go inactive until CAS1, then the 8202 will always perform an early-WRITE cycle.

The following three sections will illustrate 8202 WRITE cycles for Min Mode, Max Mode, and Alternate Con-



figurations. In most cases, we will use the 8202 early-WRITE configuration. However, in some cases, we will use a late-WRITE or READ-modify-WRITE 8202 configuration to prevent the RAM from storing the wrong information from the CPU's multiplexed address/data bus. In each case, we will examine the early-WRITE configuration first to see if the WRITE cycle will have adequate data setup and hold time for the RAM.

The twldv data setup times for the various CPU configurations are listed in Table 3. In order to use the early-WRITE configuration of the 8202, we must guarantee:

$$t_{WLDV, MIN}$$
 (CPU) +  $t_{CC, MIN}$  (8202) =  $t_{DS, MIN}$  (RAM) (Equation 1)

If this condition is not met by our system, we will have to either

- 1) Delay the 8202 WR signal, which will cause CAS ↓ to occur later in the bus cycle; or
- 2) Disconnect the 8202 WE signal from the RAM, and generate a delayed WE, that goes active after the WRITE data becomes valid, but not so late in the cycle that the RAM's t<sub>CWL</sub> parameter is violated.

The first alternative can be accomplished using the circuits shown in Figure 7. Both of these circuits will increase the  $t_{WLDV}$ , MIN values listed in Table 3 by an amount of time based on the CPU clock.

Figure 8 illustrates a method of generating a delayed WE for the RAM using the 8288 MWTC signal, while starting the WRITE cycle with the 8288 AMWC signal. This circuit has the advantage of allowing the 8202 to respond with SACK\$\(\psi\$ early enough to prevent any WAIT states in certain configurations. For this reason, the second alternative (Figure 8) is more favorable over the first configuration.

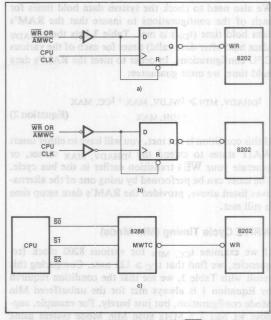


Figure 7. Generating a Delayed WR for 8202

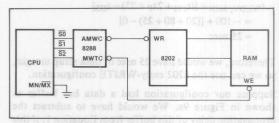


Figure 8. Using AMWC and MWTC for WRITE Cycles

Table 3. Data Setup and Hold Times for Write Cycles

	MAX	MODE <sup>1</sup>	MIN	36-2 MODE MHz	ALT.	B6-2 CONF. MHz	80 MAX N 5 N		80 MIN N 5 M	MODE	ALT.	086 CONF. MHz
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
twLDV	-50 <sup>1</sup>	25 <sup>1</sup>	-50	60	-45	60	-100 <sup>1</sup>	25 <sup>1</sup>	-100	100	-70	85
tohadv	265	Altern	265	Janon	265		420	14	420		420	

8202	80 MAX N 5 N	MODE1	80 MIN N 5 M	MODE	ALT.	88 CONF. MHz	80 MAX N 5 N		8089 ALT. CONF. 5 MHz		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
twidy	-100 <sup>1</sup>	20 <sup>1</sup>	-100	100	-70	85	-100 <sup>1</sup>	25 <sup>1</sup>	-70	85	
tDHADV	420	Ty W	420	nan e	420		420		420		

1 ASSUMES AMWC USED. ADD tolol IF MWTC USED.

We also need to check the system data hold times for each of the configurations to insure that the RAM's data hold time ( $t_{DH}$ ) is met. Table 3 lists the  $t_{DHADV}$  (data hold after data valid) times for each of the various CPU configurations. In order to meet the RAM's data hold time, we must guarantee:

$$t_{DHADV, MIN} \ge t_{WLDV, MAX} + t_{CC, MAX} + t_{DH, MAX}$$
 (Equation 2)

If this condition is not met, you will have to either insert WAIT states to extend the t<sub>DHADV</sub>, <sub>MAX</sub> values, or generate your WE \( \psi\) transition earlier in the bus cycle. The latter can be performed by using one of the alternatives listed above, provided the RAM's data setup time is still met.

## WRITE Cycle Timing (Min Mode)

If we examine  $t_{\rm CC}$ ,  $_{\rm MIN}$  for various 8202 clock frequencies, we find that  $t_{\rm CC} \geqslant 125$  nsec. Comparing this result with Table 3, we see that the condition required by Equation 1 is always met for the unbuffered Min Mode configuration, but just barely. For example, suppose we had a 5 MHz 8086 Min Mode system using 2118-3's ( $t_{\rm DS} = 0$  nsec) with a 25 MHz 8202; Equation 1 becomes:

$$t_{WLDV, MIN} + [(t_{PH} + 2t_P + 25) - t_{DS}]$$
  
= -100 + [(20 + 80 + 25) - 0]  
= 25 nsec

Therefore, we would have 25 nsec of data setup margin, so we can use the 8202 early-WRITE configuration.

Suppose our configuration had a data bus buffer as shown in Figure 9a. We would have to subtract the propagation delay of this buffer from Equation 1; if this delay is greater than 25 nanoseconds, then we cannot use the 8202 early-WRITE configuration.

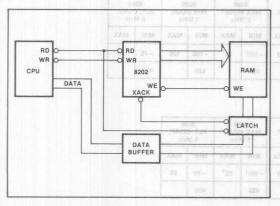


Figure 9a. Buffered Min Mode Configuration

Next, we need to examine our system to insure the RAM's data hold time is met. For the same system configuration, we can solve Equation 2:

$$t_{DHADV, MIN} \ge t_{WLDV, MAX} + t_{CC, MAX} + t_{DH}$$
  
= 100 + (t<sub>PH</sub> + 3 t<sub>P</sub> + 85) + 25  
= 350 nsec

Examining Table 3, we see that Equation 2 is satisfied with 70 nsec of margin. If we added any data buffers to our system, this margin would *increase*; if we buffer the  $8202 \overline{WR}$  input, this margin will decrease.

## Write Cycle Timing (Max Mode)

Let's see if we can get an 8 MHz 8086-2 Max Mode system to operate with 2118-4's in a 25 MHz 8202 early-WRITE configuration as shown in Figure 9b. Solving equation 1, we find:

$$t_{\text{WLDV}} + [(t_{\text{PH}} + 2t_{\text{P}} + 25) - t_{\text{DS}}] - t_{\text{IVOV}} (8286)$$

$$= -50 + [(20 + 80 + 25) - 0] - 35$$

$$= 40 \text{ nsec}$$

so we see we can use the early-WRITE configuration. Had we chosen a 5 MHz 8086 Max Mode configuration, we see from Table 3 that t<sub>WLDV</sub> would decrease by 50 nanoseconds, which means we would not have adequate data set-up time.

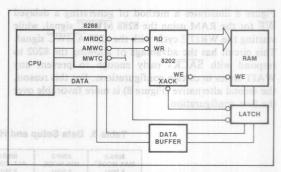


Figure 9b. Buffered Max Mode Configuration

## Write Cycle Timing (Alternate Configuration)

In general, the Alternate Configuration offers little advantage over the standard Min Mode or Max Mode, except in the earlier generation of the READY acknowledge signals, SACK and XACK. In some cases, using the Alternate Configuration will force you to generate a delayed WE signal, since the 8202 WR signal goes active earlier in the bus cycle for the Alternate Configuration than it does for either the Min Mode or the Max Mode. So, unless you need to speed up your READY signal to reduce unnecessary WAIT states for WRITE cycles, the Alternate Configuration for WRITE cycles may not offer any performance advantage for your system.

## Handling 8-Bit Write Cycles in 16-Bit Systems

Systems which perform 8-bit WRITE cycles in a 16-bit memory array require a slight modification of the WE control described previously. The memory must be broken into two 8-bit arrays with separate WE control, as shown in Figure 10.

CPU signals A0 and BHEN determine the type of bus cycle to be performed. If A0=0, then the even byte is transferred on AD0-7; if BHEN is active, then the odd byte is transferred on AD8-AD15. A word transfer is performed when A0 = 0 and  $\overline{BHEN}$  is active.

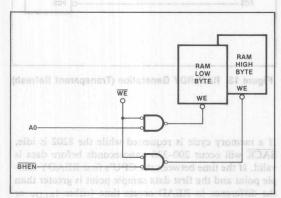


Figure 10. 8/16-Bit Write Cycle Control

# be used to generate the CPU's REA

Multibus Byte Swap ADAC to mot beyelsb s ,ear To permit compatibility with existing 8-bit CPU boards, the Multibus specification requires all byte transfers to occur on the 8 least significant data lines (DATO-DAT7). Figure 11 illustrates how to handle 8-bit and 16-bit bus cycles in a Multibus environment.

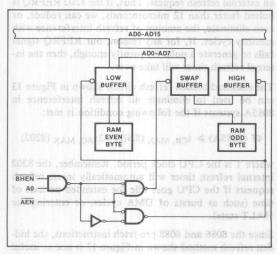


Figure 11. Multibus Byte Swap

Although Multibus uses the signals BHEN and A0, their meaning is slightly different than the CPU pin definitions. If BHEN is inactive, then the bus cycle is always 8 bits, and always uses DAT0-DAT7; if BHEN is active, then the cycle is always 16-bits, and A0 = 0.

The High Byte Buffer and the Low Byte Buffer are enabled for all word transfers, and for all byte transfers to an even address. The Swap Byte Buffer is enabled only for byte transfers to an odd address.

This control logic will allow a 16-bit memory board to be compatible with both 8-bit CPU boards and 16-bit CPU boards.

## **PCS** Generation

In order to start a memory cycle, the 8202 requires its PCS input, as well as RD or WR, to be active. Once a memory cycle is started, the 8202 will complete it, even if PCS goes inactive. This feature can be used for battery-backup RAM designs. If you have a battery backed up design, RD, WR and PCS should be pulled up to the battery supply.

Normal decoding of the processor address bus can be used to generate PCS. Since combinational logic (or even a bipolar PROM) is typically used to generate PCS; you must examine your system timing to make sure PCS is stable before RD or WR goes active. If your decoding time is greater than the address set-up to command time, then two things can happen:

- 1) Your memory cycle will not start until PCS goes active.
- 2) You may cause the 8202 to start an unwanted cycle due to a decoder glitch.

Remember, your decoding time is the amount of time it takes to ensure that only one device is selected, and that all other devices are deselected. Your decoder outputs may change after an address transition, and will only be stable after the decoding time has expired.

# Ready Handshake Signals (SACK and XACK)

If our dynamic memory system was always available when the CPU requested a memory cycle, then we could generate our RAMRDY signal as shown in Figure 13; if our RAM required no WAIT states, we could tie the READY line high, assuming the I/O and the rest of the memory (e.g., PROM) did not need any WAIT states.

In systems which use asynchronous refresh, we cannot use these methods of READY generation, since extra WAIT states are needed when a memory cycle is requested while refresh is in progress. This CPU holdoff can be performed using the 8202 XACK and SACK signals. the time they sample data, XACE

XACK is a Multibus compatible acknowledge handshake signal, since it only goes active after READ data is valid, and after WRITE data has been latched. XACK

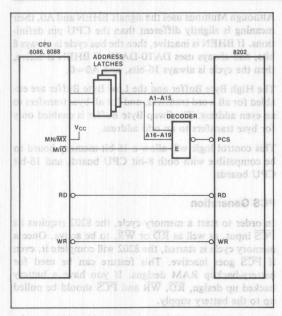


Figure 12a. 8202 PCS Generation — Minimum Mode

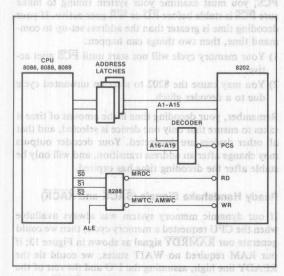


Figure 12b. 8202 PCS Generation - Maximum Mode

can be connected to the CPU's Ready input through an inverter.

Since most CPUs sample READY 1-2 clocks ahead of the time they sample data, XACK may cause more WAIT states than you really need; if your system has sufficient time between the READY sample and the data sample, SACK can be used.

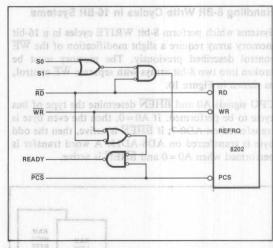


Figure 13. RAM RDY Generation (Transparent Refresh)

If a memory cycle is requested while the 8202 is idle, \$\overline{SACK}\$ will occur 200-320 nanoseconds before data is valid. If the time between the CPU's first READY sample point and the first data sample point is greater than the difference in READ access time (either t\_{RLDV}) or t\_{RLDV1}, depending on your configuration) and the t\_{CA}, \$\overline{MAX}\$ time for your 8202 configuration, then \$\overline{SACK}\$ can be used to generate the CPU's READY signal. Otherwise, a delayed form of \$\overline{SACK}\$ (or \$\overline{XACK}\$) should be used to generate the READY signal.

## Refresh Considerations lines that I will no make

The 8202 has an internal timer which generates refresh requests every 12–16 microseconds, unless it is reset by an external refresh request. Thus, if the 8202 REFRQ is pulsed faster than 12 microseconds, we can reduce, or even eliminate, the amount of refresh interference with memory cycles. If, for any reason, our REFRQ signal fails to generate a pulse frequently enough, then the internal refresh timer will take over.

The standard hidden refresh circuit shown in Figure 13 can be used to eliminate all refresh interference in 8085A systems if the following condition is met:

$$4T (8085A) \ge t_{CR, MAX} (8202) + 2t_{RC, MAX} (8202)$$

where T is the CPU clock period. Remember, the 8202 internal refresh timer will automatically insert refresh requests if the CPU goes idle for extended periods of time (such as bursts of DMA cycles, or entering the HALT state).

Since the 8086 and 8088 pre-fetch instructions, the hidden refresh method shown in Figure 13 is not as useful as it is for 8085A systems. The 8086 Family CPUs will

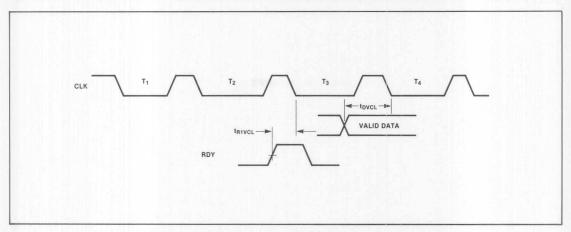


Figure 14. 8086 Family Data and READY Sample Points

have to use the 8202 internal refresh, and suffer the 3-7% performance degradation due to refresh interference. In reality, the performance degradation will be even less, since the instruction queue is normally full, and there is less chance of refresh interference than in an 8085A system.

## References

Intel Component Data Catalog Intel Peripheral Design Handbook Intel 8202 Data Sheet Intel Memory Design Handbook Intel 8086 Family User's Manual

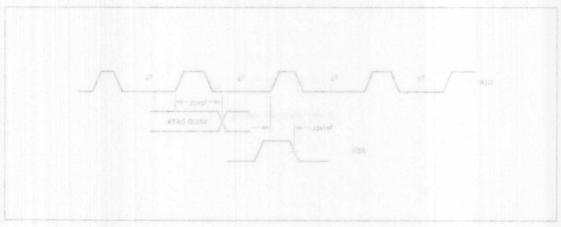


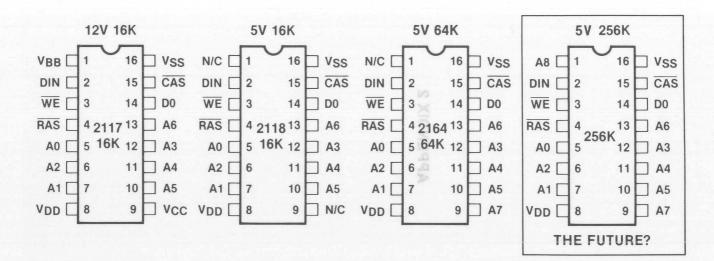
Figure 14. 6086 Family Date and READY Sample Points

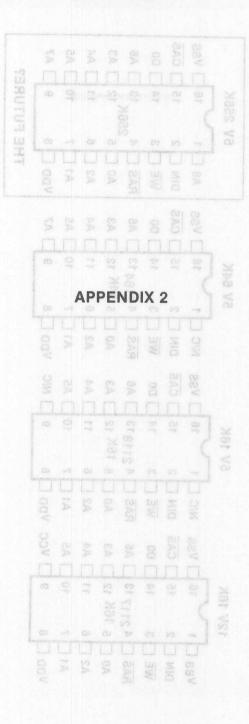
Intel Memory Design Handbook

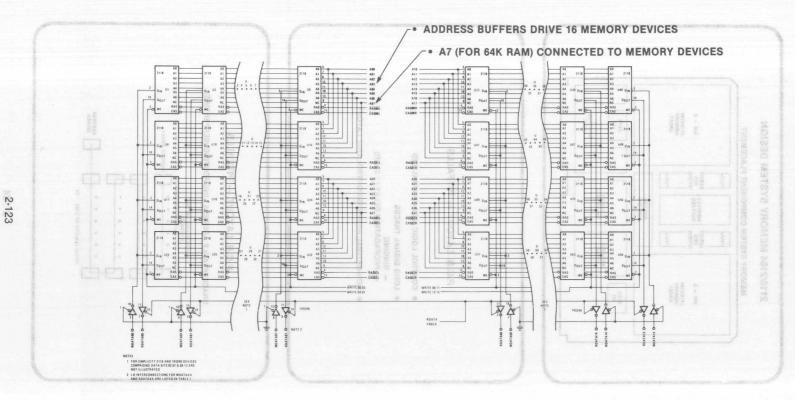
3-7% performance degradation due to refresh in 3-7% performance degradation due to refresh in page 200 p 8085 A system.

# AFN 01458A

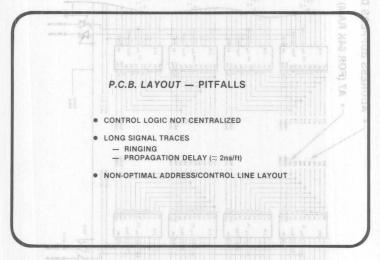
# PIN FUNCTION EVOLUTION

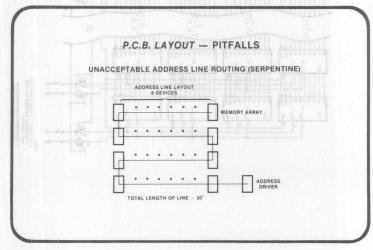




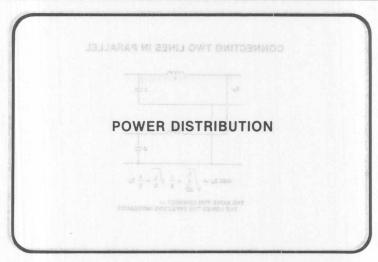


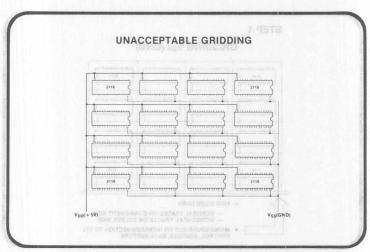
# 2118/2164 MEMORY SYSTEM DESIGN MEMORY SYSTEM COMPONENT PLACEMENT BAK × 8 SERIES RESISTORS 2118/2164 MEMORY ARRAY RASICAS BUFFERS DATA IO ADDRESS CONTROL LOGIC CONTROL LOGIC

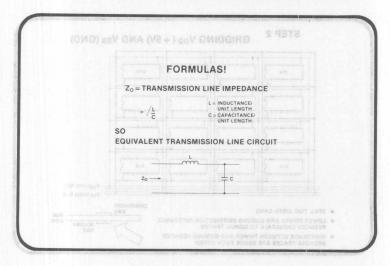




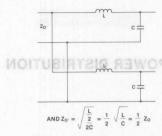
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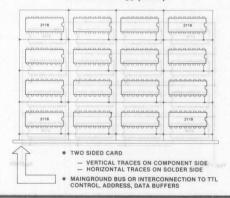
### CONNECTING TWO LINES IN PARALLEL



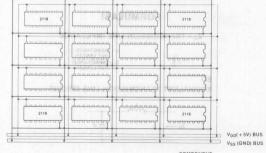
THE MORE YOU CONNECT —
THE LOWER THE EFFECTIVE IMPEDANCE

### STEP 1

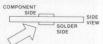
GRIDDING Vss (GND)

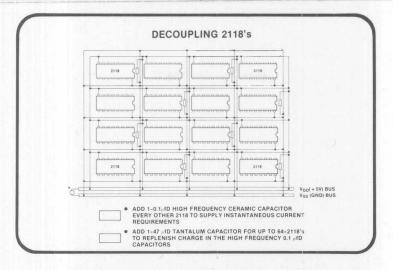


## STEP 2 GRIDDING V<sub>DD</sub> (+5V) AND V<sub>SS</sub> (GND)



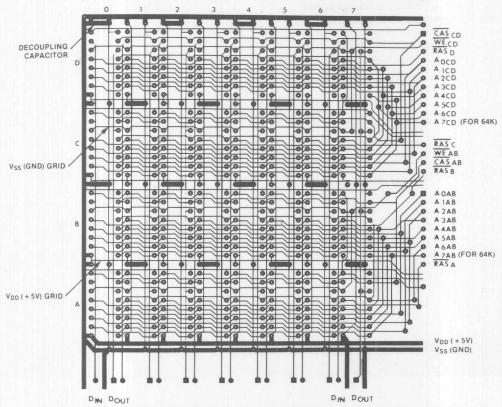
- . STILL TWO SIDED CARD
- LOWER POWER AND GROUND DISTRIBUTION IMPEDANCE REDUCES CROSSTALK TO SIGNAL TRACES.
- IMPEDANCE BETWEEN POWER AND GROUND REDUCED BECAUSE TRACES ARE ABOVE EACH OTHER



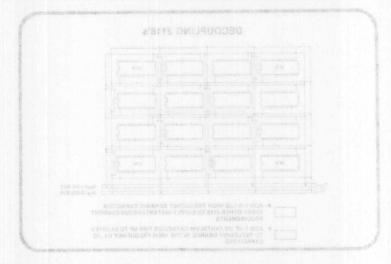


# 2118/2164 MEMORY ARRAY P.C.B. LAYOUT

POWER/GROUND GRID & DECOUPLING



NOTE: MEMORY DEVICE SPACING IS 0.4" ONE TO ONE



# 2118/2164 MEMORY ARRAY EXIDNAMA OUT



NOTE: MEMORY DEVICE SPACING IS 0.4" ONE TO ONE

**POWER CONSIDERATIONS** AND DECOUPLING

### **DETERMINING 2118 POWER** REQUIREMENTS

- NORMAL OPERATING CURRENT
- STANDBY CURRENT AND STANDS
- REFRESH CURRENT
   SACTOR

 OPERATING CURRENT 2118 SYSTEM  $I_{DD_0} = (I_{DD_2} \times K) + I_{DDLO}$ 

- K = NUMBER OF ACTIVE (RECEIVING BOTH RAS & CAS) DEVICES IN THE SYSTEM
- IDD2 = VDD SUPPLY CURRENT, OPERATING
- - 2118-2 = 29 mA (MAX) 2118-3 = 25 mA (MAX) 2118-4 = 22 mA (MAX) 2118-7 = 22 mA (MAX)
- I<sub>ODLO</sub> = 2118 OUTPUT LOAD CURRENT
  Σ LEAKAGE CURRENTS + TTL LOAD INPUT CURRENT
  2118 OUTPUT LEAKAGE [I,O] = 10 μA
  745240 INPUT CURRENT I<sub>II.E</sub> = 400 μA

STANDBY CURRENT 2118 SYSTEM

### $I_{DDS} = I_{DD_1} \times M$ WHERE

- POWER CONSIDERATION M = NUMBER ON INACTIVE (RECEIVING CAS ONLY) DEVICES IN THE SYSTEM
- I<sub>DD1</sub> = V<sub>DD</sub> SUPPLY CURRENT, STANDBY. 2118 = 3 mA (MAX)

### REFRESH CURRENT 2118 SYSTEM DETERMININ

 $I_{DD_R} = (I_{DD_3} \times N) \left( \frac{t_{RAS}}{t_{REF}} \right) (128)$ 

- N = TOTAL NUMBER OF DEVICES IN THE SYSTEM
  N=M+K
- 1<sub>D03</sub> = V<sub>DD</sub> SUPPLY CURRENT, RAS-ONLY CYCLE 2118-2 = 24 mA 2118-3 = 20 mA 2118-4 = 15 mA 2118-7 = 16 mA
- $t_{RAS} = \overline{RAS}$  pulse width in nanoseconds during the refresh cycle
- tref= TIME BETWEEN REFRESH IN MILLISECONDS

### TOTAL VDD SUPPLY CURRENT 2118 SYSTEM IDDT = IDDO + IDDS + IDDR

 TOTAL VDD POWER  $P_{DDT} = V_{DD} \times I_{DDT}$ 

### WHERE

V<sub>DD</sub> = 5.5V TO GET ABSOLUTE MAXIMUM SYSTEM POWER

ACTUAL POWER CALCULATION FOR A 64K × 16 BIT
2118-4 MEMORY ARRAY:

N = NUMBER OF 2118-4 IN THE SYSTEM = 64
M = NUMBER OF STANDBY 2118-4 IN THE SYSTEM = 48
K = NUMBER OF ACTIVE 2118-4 IN THE SYSTEM = 16
IRAS = 140 ns
IREF = 2 ms

| IDDs = (22 mA) (16) + (4) (10 µA) + 400 µA = 352 mA + 0.440 mA = 352.4 mA | IDDs = (3 mA) (48) = 144 mA | IDDn = (18 mA) (64) (140 ns) (128) = 10.3 mA | IDD = 352.4 mA + 144 mA + 10.3 mA

Data Recording Techniques

THE 8272 FLEXIBLE DISKETTE CONTROLLER 2-139

Poppy Disk Commands
Interface Registers
Command/Result Phases
Execution Phase
Multi-sector and Multi-frack Transfers
Orive Status Polling
Command Details

THE DATA SEPARATOR

Single Density
Double Density
Phase-Locked Loop Design
Initialization
Floppy Disk Data
Startup
PLL Synchronization

AN INTELLIGENT DISKETTE DATA BASE SYSTEM 2-156

Processor and Memory Serial I/O DMA Disk Drive Interface

SPECIAL CONSIDERATIONS 2-161

Schematics

# An Intelligent **Data Base System** Using the 8272

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### INTRODUCTION The Floppy Disk The Floppy Disk Drive

### 2-133

### SUBSYSTEM OVERVIEW

Controller Electronics Drive Electronics Controller/Drive Interface Processor/Memory Interface

### 2-135

### DISK FORMAT

2-136

Data Recording Techniques Sectors Tracks Sector Interleaving

### THE 8272 FLEXIBLE DISKETTE CONTROLLER

2-139

Floppy Disk Commands Interface Registers Command/Result Phases Execution Phase Multi-sector and Multi-track Transfers **Drive Status Polling** Command Details

### THE DATA SEPARATOR

2-154

Single Density Double Density Phase-Locked Loop Design Initialization Floppy Disk Data Startup PLL Synchronization

### AN INTELLIGENT DISKETTE DATA BASE SYSTEM 2-158

Processor and Memory Serial I/O DMA Disk Drive Interface

### SPECIAL CONSIDERATIONS

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### **APPENDIX**

2-163

Schematics **Power Distribution** 

### Finally, the drive provides NOITOUDONTNI 11

Most microcomputer systems in use today require lowcost, high-density removable magnetic media for information storage. In the area of removable media, a designer's choice is limited to magnetic tapes and floppy disks (flexible diskettes), both of which offer non-volatile data storage. The choice between these two technologies is relatively straight-forward for a given application. Since disk drives are designed to permit random access to stored information, they are significantly faster than tape units. For example, locating information on a disk requires less than a second, while tape movement (even at the fastest rewind or fast-forward speed) often requires several minutes. This random access ability permits the use of floppy disks in on-line storage applications (where information must be located, read, and modified/updated in real-time under program or operator control). Tapes, on the other hand, are ideally suited to archival or back-up storage due to their large storage capacities (more than 10 million bytes of data can be archived on a cartridge tape).

A sophisticated controller is required to capitalize on the abilities of the disk storage unit. In the past, disk controller designs have required upwards of 150 ICs. Today, the single-chip 8272 Floppy Disk Controller (FDC) plus approximately 30 support devices can handle up to four million bytes of on-line data storage on four floppy disk drives.

### The Floppy Disk

A floppy disk is a circular piece of thin plastic material covered with a magnetic coating and enclosed in a protective jacket (Figure 1). The circular piece of plastic revolves at a fixed speed (approximately 360 rpm) within its jacket in much the same manner that a record revolves at a fixed speed on a stereo turntable. Disks are manufactured in a variety of configurations for various storage capacities. Two standard physical disk sizes are commonly used. The 8-inch disk (8 inches square) is the larger of the two sizes; the smaller size (5-1/4 inches square) is often referred to as a mini-floppy. Singlesided disks can record information on only one side of the disk, while double-sided disks increase the storage capacity by recording on both sides. In addition, disks are classified as single-density or double-density. Doubledensity disks use a modified recording method to store twice as much information in the same disk area as can be stored on a single-density disk. Table 1 lists storage capacities for standard floppy disk media.

A magnetic head assembly (in contact with the disk) writes information onto the disk surface and subsequently reads the data back. This head assembly can move from the outside edge of the disk toward the center in fixed increments. Once the head assembly is

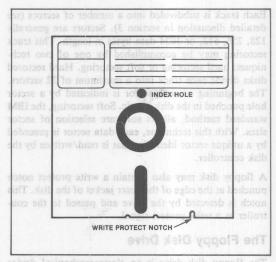


Figure 1. A Floppy Diskette

positioned at one of these fixed positions, the head can read or write information in a circular path as the disk revolves beneath the head assembly. This method divides the surface into a fixed number of cylinders (as shown in Figure 2). There are normally 77 cylinders on a standard disk. Once the head assembly is positioned at a given cylinder, data may be read or written on either side of the disk. The appropriate side of the disk is selected by the read/write head address (zero or one). Of course, a single-sided disk can only use head zero. The combination of cylinder address and head address uniquely specifies a single circular track on the disk. The physical beginning of a track is located by means of a small hole (physical index mark) punched through the plastic near the center of the disk. This hole is optically sensed by the drive on every revolution of the disk.

Table 1. Formatted Disk Capacities

Single-Density Format	same interl a immer c			
	0 9/1 128			-
Sectors/Track	9192 11926	vino 15	dans a8	evisto e4
Tracks/Disk	ideo ad77	o siam 77	ouno 77	, bete77
Bytes/Disk	256,256	295,680	315,392	315,392
Double-Density Format				
Bytes/Sector	128	256	512	1024
Sectors/Track	52	30	16	8
Tracks/Disk	77	77	77	77
Bytes/Disk	512,512	591,360	630,784	630,784

Each track is subdivided into a number of sectors (see detailed discussion in section 3). Sectors are generally 128, 256, 512, or 1024 data bytes in length. This track sectoring may be accomplished by one of two techniques: hard sectoring or soft sectoring. Hard sectored disks divide each track into a maximum of 32 sectors. The beginning of each sector is indicated by a sector hole punched in the disk plastic. Soft sectoring, the IBM standard method, allows software selection of sector sizes. With this technique, each data sector is preceded by a unique sector identifier that is read/written by the disk controller.

A floppy disk may also contain a write protect notch punched at the edge of the outer jacket of the disk. This notch is detected by the drive and passed to the controller as a write protect signal.

### The Floppy Disk Drive

The floppy disk drive is an electromechanical device that records data on, or reads data from, the surface of a floppy disk. The disk drive contains head control electronics that move the head assembly one increment (step) forward (toward the center of the disk) or backward (toward the edge of the disk). Since the recording head must be in contact with the disk material in order to read or write information, the disk drive also contains head-load electronics. Normally the read/write head is unloaded until it is necessary to read or write information on the floppy disk. Once the head assembly has been positioned over the correct track on the disk, the head is loaded (brought into contact with the disk). This sequence prevents excessive disk wear. A small time penalty is paid when the head is loaded. Approximately thirty to fifty milliseconds are needed before data may be reliably read from, or written to, the disk. This time is known as the head load time. If desired, the head may be moved from cylinder to cylinder while loaded. In this manner, only a small time interval (head settling time) is required before data may be read from the new cylinder. The head settling time is often shorter than the head load time. Typically, disk drives also contain drive select logic that allows more than one physical drive to be connected to the same interface cable (from the controller). By means of a jumper on the drive, the drive number may be selected by the OEM or end user. The drive is enabled only when selected; when not selected, all control signals on the cable are ignored.

315,392	315,392	295,680		
				Double-Density Format
1024 8 77	512 16 77	256 30 77	128 52 77	Bytes/Sector Sectors/Track Tracks/Disk
630,784	630,784			Bytes/Disk

Finally, the drive provides additional signals to the system controller regarding the status of the drive and disk. These signals include:

Drive Ready — Signals the system that the drive door as is closed and that a floppy disk is inserted into the drive.

Track Zero — Indicates that the head assembly is located over the outermost track of the disk.

This signal may be used for calibration of the disk drive at system initialization and after an error condition.

Write Protect — Indicates that the floppy disk loaded into the drive is write protected.

Dual Sided — Indicates that the floppy disk in the drive is dual-sided.

Write Fault — Indicates that an error occurred during a recording operation.

Index — Informs the system that the physical index mark of the floppy disk (signifying the start of a data track) has been sensed.

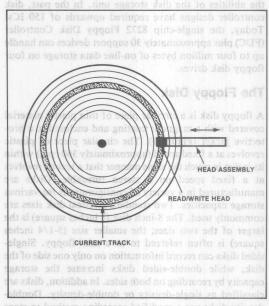


Figure 2. Concentric Cylinders on a Floppy Diskette

A magnetic head assembly (in contact with the disk) writes information onto the disk surface and subsequently reads the data back. This head assembly can nove from the outside edge of the disk toward the beater in fixed increments. Once the head assembly is

### 4. OUDOTOTEN UVERVIEW 32500A VIOLEN

A disk subsystem consists of the following functional electronic units:

- 1. Disk Controller Electronics (188 desuper a sellottino)
- 2. Disk Drive Electronics
- Controller/Disk Interface (cables, drivers, terminators)
- 4. Controller/Microprocessor System Interface

The operation of these functional units is discussed in the following paragraphs.

### Controller Electronics begins been of relient

The disk controller is responsible for converting highlevel disk commands (normally issued by software executing on the system processor) into disk drive commands. This function includes:

- 1. Disk Drive Selection Disk controllers typically manage the operations of multiple floppy disk drives. This controller function permits the system processor to specify which drive is to be used in a particular operation.
- Track Selection The controller issues a timed sequence of step pulses to move the head from its current location to the proper disk cylinder from which data is to be read or to which data is to be written. The controller stores the current cylinder number and computes the stepping distance from the current cylinder to the specified cylinder. The controller also manages the head select signal to select the correct side of the floppy disk.
- 3. Sector Selection The controller monitors the data on a track until the requested sector is sensed.
- 4. Head Loading The disk controller determines the times at which the head assembly is to be brought in contact with the disk surface in order to read or write data. The controller is also responsible for waiting until the head has settled before reading or writing information. Often the controller maintains the head loaded condition for up to 16 disk revolutions (approximately 2 seconds) after a read or write operation has been completed. This feature eliminates the head load time during periods of heavy disk I/O activity.
- 5. Data Separation The actual signal recorded on a floppy disk is a combination of timing information (clock) and data. The serial READ DATA input (from the disk drive) must be converted into two signal streams: clock and data. (The READ DATA input operates at 250K bits/second for single-density disks and 500K bits/second for double-density

- disks.) The serial data must also be assembled into 8-bit bytes for transfer to system memory. A byte must be assembled and transferred every 32 microseconds for single-density disks and every 16 microseconds for double-density.
- 6. Error Checking Information recorded on a floppy disk is subject to both hard and soft errors. Hard (permanent) errors are caused by media defects. Soft errors, on the other hand, are temporary errors caused by electromagnetic noise or mechanical interference. Disk controllers use a standard error checking technique known as a Cyclic Redundancy Check (CRC). As data is written to a disk, a 16-bit CRC Character is computed and also stored on the disk. When the data is subsequently read, the CRC character allows the controller to detect data errors. Typically, when CRC errors are detected, the controlling software retries the failed operation (attempting to recover from a soft error). If data cannot reliably be read or written after a number of retries, the system software normally reports the error to the operator. Multiple CRC errors normally indicate unrecoverable media error on the current disk track. Subsequent recovery attempts must be defined by the system designers and tailored to meet system interfacing requirements.

Today, single-chip digital LSI floppy disk controllers such as the 8272 perform all the above functions with the exception of data separation. A data separation circuit (a combination of digital and analog electronics) synchronizes itself to the actual data rate of the disk drive. This data rate varies from drive to drive (due to mechanical factors such as motor tolerances) and varies from disk to disk (due to temperature effects). In order to operate reliably with both single- and double-density storage, the data separation circuit must be based on phase-locked loop (PLL) technology. The phase-locked loop data separation logic is described in section 5. The separation logic, after synchronizing with the data stream, supplies a data window to the LSI disk controller. This window differentiates data information from clock information within the serial stream. The controller uses this window to reconstruct the data previously recorded on the floppy disk.

# Drive Electronics (Section 2) and stable about 1026

Each floppy disk drive contains digital electronic circuits that translate TTL-compatible command signals into electromechanical operations (such as drive selection and head movement/loading) and that sense and report disk or drive status to the controller (e.g., drive ready, write fault, and write protect). In addition, the drive electronics contain analog components to sense, amplify, and shape data pulses read from, or written to, the floppy disk surface by the read/write head.

### Controller/Drive Interface

The controller/drive interface consists of high-current line drivers, Schmitt triggered input gates, and flat or twisted pair cable(s) to connect the disk drive electronics to the controller electronics. Each interface signal line is resistively terminated at the end of the cable farthest from the line drivers. Eight-inch drives may be directly interfaced by means of 50-conductor flat cable. Generally, cable lengths should be less than ten feet in order to maintain noise immunity.

Normally, provisions are made for up to four disk drives to share the same interface cable. The controller may operate as many cable assemblies as practical. LSI floppy disk controllers typically operate one to four drives on a single cable.

### Processor/Memory Interface interface interface

The disk controller must interface to the system processor and memory for two distinct purposes. First, the processor must specify disk control and command parameters to the controller. These parameters include the selection of the recording density and specification of disk formatting information (discussed in section 3). In addition to disk parameter specification, the processor must also send commands (e.g., read, write, seek, and scan) to the controller. These commands require the specification of the command code, drive number, cylinder address, sector address, and head address. Most LSI controllers receive commands and parameters by means of processor I/O instructions.

In addition to this I/O interface, the controller must also be designed for high-speed data transfer between memory and the disk drive. Two implementation methods may be used to coordinate this data transfer. The lowest-cost method requires direct processor intervention in the transfer. With this method, the controller issues an interrupt to the processor for each data transfer. (An equivalent method allows the processor to poll an interrupt flag in the controller status word.) In the case of a disk write operation, the processor writes a data byte (to be encoded into the serial output stream) to the disk controller following the receipt of each controller interrupt. During a disk read operation, the processor reads a data byte (previously assembled from the input data stream) from the controller after each interrupt. The processor must transfer a data byte from the controller to memory or transfer a data byte from memory to the disk controller within 16 or 32 microseconds after each interrupt (double-density and single-density response times, respectively).

If the system processor must service a variety of other interrupt sources, this interrupt method may not be practical, especially in double-density systems. In this case, the disk controller may be interfaced to a Direct Memory Access (DMA) controller. When the disk controller requires the transfer of a data byte, it simply activates the DMA request line. The DMA controller interfaces to the processor and, in response to the disk controller's request, gains control of the memory interface for a short period of time—long enough to transfer the requested data byte to/from memory. See section 6 for a detailed DMA interface description.

### 3. DISK FORMAT TORRODO TO THE TORRODO A

New floppy disks must be written with a fixed format by the controller before these disks may be used to store data. Formatting is a method of taking raw media and adding the necessary information to permit the controller to read and write data without error. All formatting is performed by the disk controller on a track-bytrack basis under the direction of the system processor. Generally, a track may be formatted at any time. However, since formatting "initializes" a complete disk track, all previously written data is lost (after a format operation). A format operation is normally used only when initializing new floppy disks. Since soft-sectoring in such a predominant formatting technique (due to IBM's influence), the following discussion will limit itself to soft-sectored formats.

# Data Recording Techniques

Two standard data recording techniques are used to combine clock and data information for storage on a floppy disk. The single-density technique is referred to as FM encoding. In FM encoding (see Figure 3), a double frequency encoding technique is used that inserts a data bit between two adjacent clock bits. (The presence of a data bit represents a binary "one" while the absence of a data bit represents a binary "zero.") The two adjacent clock bits are referred to as a bit cell, and except for unique field identifiers, all clock bits written on the disk are binary "ones." In FM encoding, each data bit is written at the center of the bit cell and the clock bits are written at the leading edge of the bit cell.

The encoding used for double-density recording is termed MFM encoding (for "Modified FM"). In MFM encoding (Figure 3) the data bits are again written at the center of the bit cell. However, a clock bit is written at the leading edge of the bit cell only if no data bit was written in the previous bit cell and no data bit will be written in the present bit cell.

# Sectors in minut to notispidmon a 21 Asib vogoli

Soft-sectored floppy disks divide each track into a number of data sectors. Typically, sector sizes of 128, 256, 512, or 1024 data bytes are permitted. The sector size is specified when the track is initially formatted by the controller. Table 1 lists the single- and double-

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density data storage capacities for each of the four sector sizes. Each sector within a track is composed of the following four fields (illustrated in Figure 4):

- 1. Sector ID Field This field, consisting of seven bytes, is written only when the track is formatted. The ID field provides the sector identification that is used by the controller when a sector must be read or written. The first byte of the field is the ID address mark, a unique coding that specifies the beginning of the ID field. The second, third, and fourth bytes are the cylinder, head, and sector addresses, respectively, and the fifth byte is the sector length code. The last two bytes are the 16-bit CRC character for the ID field. During formatting, the controller supplies the address mark. The cylinder, head, and sector addresses and the sector length code are supplied to the controller by the processor software. The CRC character is derived by the controller from the data in the first five bytes.
- 2. Post ID Field Gap The post ID field gap (gap 2) is written initially when the track is formatted. During subsequent write operations, the drive's write circuitry is enabled within the gap and the trailing bytes of the gap are rewritten each time the sector is updated (written). During subsequent read operations, the trailing bytes of the gap are used to synchronize the data separator logic with the upcoming data field.
- Data Field The length (number of data bytes) of the data field is determined by software when the track is formatted. The first byte of the data field is the data address mark, a unique coding that specifies

- the beginning of the data field. When a sector is to be deleted, (e.g., a hard error on the disk), a deleted data address mark is written in place of the data address mark. The last two bytes of the data field comprise the CRC character.
- 4. Post Data Field Gap The post data field gap (gap 3) is written when the track is formatted and separates the preceding data field from the next physical ID field on the track. Note that a post data field gap is not written following the last physical sector on a track. The gap itself contains a programselectable number of bytes. Following a sector update (write) operation, the drive's write logic is disabled during the gap. The actual size of gap 3 is determined by the maximum number of data bits that can be recorded on a track, the number of sectors per track and the total sector size (data plus overhead information). The gap size must be adjusted so that it is large enough to contain the discontinuity generated on the floppy disk when the write current is turned on or off (at the start or completion of a disk write operation) and to contain a synchronization field for the upcoming ID field (of the next sector). On the other hand, the gaps must be small enough so that the total number of data bits required on the track (sectors plus gaps) is less than the maximum number of data bits that can be recorded on the track. The gap size must be specified for all read, write, and format operations. The gap size used during disk reads and writes must be smaller than the size used to format the disk to avoid the splice points between contiguous physical sectors. Suggested gap sizes are listed in Table 9.

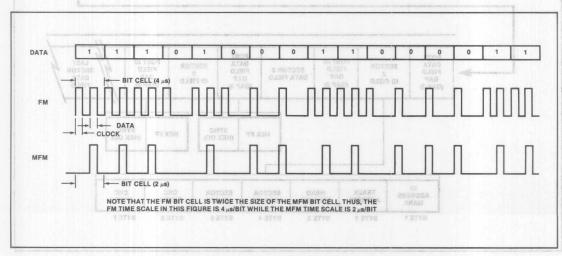


Figure 4. Standard Igniboard MFM Encoding Sac 204 Manuall

### Tracks stock a mod W , blait stab and to guinariged add

The overall format for a track is illustrated in Figure 4. Each track consists of the following fields:

- 1. Pre-Index Gap The pre-index gap (gap 5) is written only when the track is formatted.
- Index Address Mark The index address mark consists of a unique code that indicates the beginning of a data track. One index mark is written on each track when the track is formatted.
- Post Index Gap The post index gap (gap 1) is used during disk read and write operations to syn-

- chronize the data separator logic with the data to be read from the ID field (of the first sector). The post index gap is written only when the disk is formatted.
- 4. Sectors The sector information (discussed above) is repeated once for each sector on the track.
- 5. Final Gap The final gap (gap 4) is written when the track is formatted and extends from the last physical data field on the track to the physical index mark. The length of this gap is dependent on the number of bytes per sector specified, the lengths of the program-selectable gaps specified, and the drive speed.

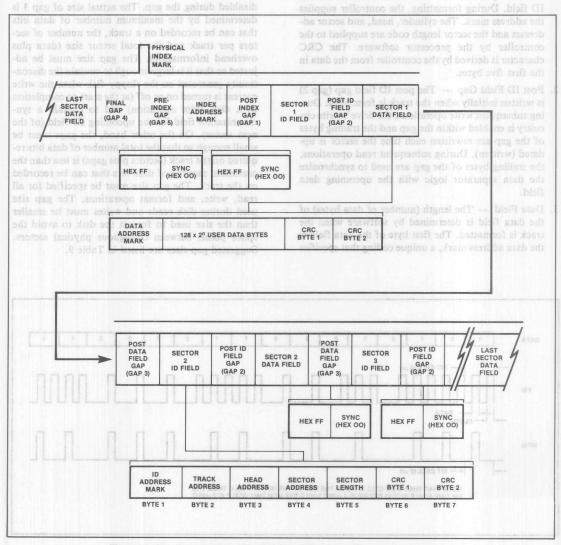


Figure 4. Standard Floppy Diskette Track Format (From SBC 204 Manual)

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### Sector Interleaving AT ARZAHS MOTTUDEXE

The initial formatting of a floppy disk determines where sectors are located within a track. It is not necessary to allocate sectors sequentially around the track (i.e., 1,2,3,...,26). In fact, is is often advantageous to place the sectors on the track in a non-sequential order. Sequential sector ordering optimizes sector access times during multi-sector transfers (e.g., when a program is loaded) by permitting the number of sectors specified (up to an entire track) to be transferred within a single revolution of the disk. A technique known as sector interleaving optimizes access times when, although sectors are accessed sequentially, a small amount of processing must be performed between sector reads/writes. For example, an editing program performing a text search reads sectors sequentially, and after each sector is read, performs a software search. If a match is not found, the software issues a read request for the next sector. Since the floppy disk continues to rotate during the time that the software executes, the next physical sector is already passing under the read/write head when the read request is issued, and the processor must wait for another complete revolution of the disk (approximately 166 milliseconds) before the data may actually be input. With interleaving, the sectors are not stored sequentially on a track; rather, each sector is physically removed from the previous sector by some number (known as the interleave factor) of physical sectors as shown in Figure 5. This method of sector allocation provides the processor additional execution time between sectors on the disk. For example, with a 26 sector/track format, an interleave factor of 2 provides 6.4 milliseconds of processing time between sequential 128 byte sector accesses.

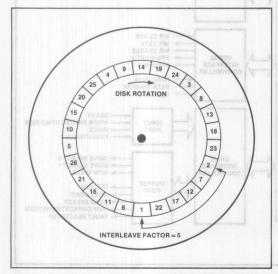


Figure 5. Interleaved Sector Allocation Within a Track Read Deleted Data

To calculate the correct interleave factor, the maximum processor time between sector operations must be divided by the time required for a complete sector to pass under the disk read/write head. After determining the interleave factor, the correct sector numbers are passed to the disk controller (in the exact order that they are to physically appear on the track) during the execution of a format operation.

# 4. THE 8272 FLEXIBLE DISKETTE CONTROLLER

The 8272 is a single-chip LSI Floppy Disk Controller (FDC) that contains the circuitry necessary to implement both single-and double-density floppy disk storage subsystems (with up to four dual-sided disk drives per FDC). The 8272 supports the IBM 3740 single-density recording format (FM) and the IBM System 34 doubledensity recording format (MFM). With the 8272, less than 30 ICs are needed to implement a complete disk subsystem. The 8272 accepts and executes high-level disk commands such as format track, seek, read sector, write sector, and read track. All data synchronization and error checking is automatically performed by the FDC to ensure reliable data storage and subsequent retrieval. External logic is required only for the generation of the FDC master clock and write clock (see Section 6) and for data separation (Section 5). The FDC provides signals that control the startup and base frequency selection of the data separator. These signals greatly ease the design of a phase-locked loop data separator.

In addition to the data separator interface signals, the 8272 also provides the necessary signals to interface to microprocessor systems with or without Direct Memory Access (DMA) capabilities. In order to interface to a large number of commercially available floppy disk drives, the FDC permits software specification of the track stepping rate, the head load time, and the head unload time.

The pin configuration and internal block diagram of the 8272 is shown in Figure 6. Table 2 contains a description for each FDC interface pin.

### Floppy Disk Commands

The 8272 executes fifteen high-level disk interface commands:

Specify Write Data
Sense Drive Status Write Deleted Data
Sense Interrupt Status Read Track
Seek Read ID
Recalibrate Scan Equal
Format Track Scan High or Equal
Read Data Scan Low or Equal

Each command is initiated by a multi-byte transfer from the processor to the FDC (the transferred bytes contain command and parameter information). After complete command specification, the FDC automatically executes the command. The command result data (after execution of the command) may require a multi-byte transfer of status information back to the processor. It is convenient to consider each FDC command as consisting of the following three phases:

### COMMAND PHASE:

The executing program transfers to the FDC all the information required to perform a particular disk operation. The 8272 automatically enters the command phase after RESET and following the completion of the result phase (if any) of a previous command.

EXECUTION PHASE: The FDC performs the operation as instructed. The execution phase is entered immediately after the last command parameter is written to the FDC in the preceding command phase. The execution phase normally ends when the last data byte is transferred to/from the disk (signalled by the TC input to the FDC) or when an error occurs.

### RESULT PHASE:

After completion of the disk operation, status and other been all nomes done notes housekeeping information ent band ton a datam are made available to the sonie rosses been sel to processor. After the procand said self annual size essor reads this information. wheels at a conhappen been off needw be mand phase and is ready to mos redions tol riew accept another command.

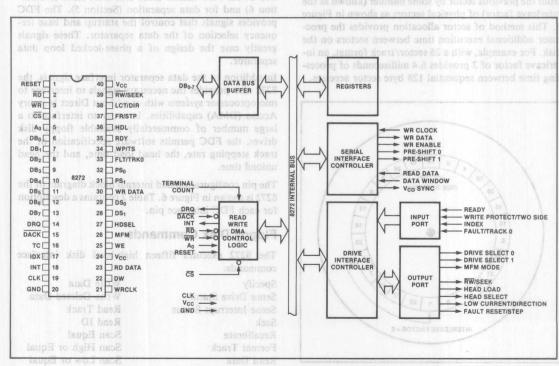


Figure 6. 8272 Pin Configuration and Internal Block Diagram of sea bevious and annual Figure 6. 8272 Pin Configuration and Internal Block Diagram of sea bevious first and annual Figure 6.

Table 2. 8272 FDC Pin Description

Number	Pin Symbol	1/0	To/From	Description loans rectang
1 <sup>stinW</sup>	RST III III	cordini sek mod t write n	sk d <b>qu</b> faul tion in the S mees the dis	Reset. Active-high signal that places the FDC in the "idle" state and all disk drive output signals are forced inactive (low). This input must be held active during power on reset while the RD and WR inputs are active.
	RD II II	The second second	ual-squd me ready status	Read. Active-low control signal that enables data transfer from the FDC to the data bus.
n3 bebsie	WR dr	bad*sic	w\ba <b>uP</b> svirib	Write. Active-low control signal that enables data transfer from the data bus into the FDC.
4 svom	odw (CS) yello			Chip Select. Active-low control signal that selects the FDC. No reading of writing will occur unless the FDC is selected.
5 -noithead	A <sub>0</sub>	ni ( <b>T</b> *bni mibross	o and per or	Address. Selects the Data Register or Main Status Register for input/out- put in conjunction with the RD and WR inputs. (See Table 3.)
6-13	DB <sub>0</sub> -DB <sub>7</sub>	I/O*	uP	Data Bus. Bidirectional three-state 8-bit data bus.
14	DRQ	o O dri	DMA	DMA Request. Active-high output that indicates an FDC request for DMA services.
15	DACK	no je. 1 toward	DMA	DMA Acknowledge. Active-low control signal indicating that the requested DMA transfer is in progress.
16	TC	indie (st	DMA	Terminal Count. Active-high signal that causes the termination of a com-
00e; a	cts the Seek m	16761 3618	ctor. A high fite mode.	mand. Normally, the terminal count input is directly connected to the TC/EOP output from the DMA controller, signalling that the DMA transfer has been completed. In a non-DMA environment, the processor must count data transfers and supply a TC signal to the FDC.
17	IDX	I	Drive	Index. Indicates detection of the physical index mark (the beginning of a track) on the selected disk drive.
18	INT	0	uP	Interrupt Request. Active-high signal indicating an 8272 interrupt service request.
19	CLK	I		Clock. Signal phase 8 MHz clock (50% duty cycle).
20	GND			Ground. DC power return.
21	WR CLK	I		Write Clock. 500 kHz (FM) or 1 MHz (MFM) write clock with a constant pulse width of 250 ns (for both FM and MFM recording). The write clock must be present at all times.
9022 XTY		Strus atus re	to LLP dais additional s	Data Window. Data sample signal from the phase-locked loop indicating that the FDC should sample input data from the disk drive.
23	RD DATA	9 P 87	Drive	Read Data. FDC input data from the selected disk drive.
24	VCO	oms	PLL	VCO Sync. Active-high output that enables the phase-locked loop to synchronize with the input data from the disk drive.
25	WE	0	Drive	Write Enable. Active-high output that enables the disk drive write gate.
26	MFM	0	PLL	MFM Mode. Active-high output used by external logic to enable the MFM double-density recording mode. When the MFM output is low,
Register	unaid maivi be	N C	Die	single-density FM recording is indicated.
27	HDSEL	0	Drive	Head Select. Selects head 0 or head 1 on a dual-sided disk.
30 30 30 30 30 30 30 30 30 30 30 30 30 3	DS <sub>1</sub> ,DS <sub>0</sub> WR DATA	0	Drive Drive	Drive Select. Selects one of four disk drives.  Write Data. Serial data stream (combination of clock and data bits) to be written on the disk.
31,32	PS <sub>1</sub> ,PS <sub>0</sub>	0	Drive	Precompensation (pre-shift) Control. Write precompensation output control during MFM mode. Specifies early, late, and normal timing signals. See the discussion in Section 5.

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Table 2. 8272 FDC Pin Description (continued)

Number	Pin Symbol	1/0	To/From	Description Over 19 19 19 19 19 19 19 19 19 19 19 19 19
33 lie bne	FLT/TRKO		Drive t places the forced inact	Fault/Track 0. Senses the disk drive fault condition in the Read/Write mode and the Track 0 condition in the Seek mode.
3405 578		es (II) as	Drive en	Write Protect/Two-Sided. Senses the disk write protect status in the Read/Write mode and the dual-sided media status in the Seek mode.
35	RDY	I	Drive	Ready. Senses the disk drive ready status.
36 b oris	mon HDL ment	erolata	Bn Drivelan	Head Load. Loads the disk drive read/write head. (The head is placed in contact with the disk.)
	FR/STP	ed.	PDC is select	Fault Reset/Step. Resets the fault flip-flop in the disk drive when operating in the Read/Write mode. Provides head step pulses (to move the head from one cylinder to another cylinder) in the Seek mode.
38	LCT/DIR	npO <sub>(S)</sub> (		Low Current/Direction. Signals that the recording head has been position ed over the inner cylinders (44-77) of the floppy disk in the Read/Write mode. (The write current must be lowered when recording on the phys-
for	и РОС годися	dicates e	utput that in	tual head position and require that the FDC supply this signal.) Deter-
-91	icating that the		Progress.	mines the head step direction in the Seek mode. In the Seek mode, a high level on this pin steps the read/write head toward the spindle (step-in); a low level steps the head away from the spindle (step-out).
f a come o the	RW/SEEK	COLLO ST	ndia mass n	Read, Write/Seek Mode Selector. A high level selects the Seek mode; a low level selects the Read/Write mode.
	q adVccamino			+ 5V DC Power 1 75 3 3 3 3

Organd, DC power return.

must be present at all times.

\*Disabled when CS is high. Index. Indicates detection of the physical index mark (the beginning of a

Interface Registers of MRM and Mrd for 1250 as (for both FM and MRM or 250 as (for both FM and MRM)

To support information transfer between the FDC and In addition to the Main Status Register, the FDC conthe system processor, the 8272 contains two 8-bit tains four additional status registers (ST0, ST1, ST2, registers: the Main Status Register and the Data and ST3). These registers are only available during the FDC status information and may be accessed at any time. The Main Status Pegisters (Table 1) time. The Main Status Register (Table 4) provides the system processor with the status of each disk drive, the A sldsnd sin W status of the FDC, and the status of the processor interface. The Data Register (read/write) stores data, commands, parameters, and disk drive status information. The Data Register is used to program the FDC during the command phase and to obtain result information after completion of FDC operations. Data is read from, or written to, the FDC registers by the combination of the A0, RD, WR, and CS signals, as described in the Table 3. Control, Write precompensation output con-

laterrupt Request. Active-high signal indicating an 8272 interrupt service

Write Clock. 300 kHz (FM) or 1 MHz (MFM) write clock with a constant

trol during MFM mode. Specifies sarly, late, and normal timing signals

Clock. Signal phase 8 MHz clock (50% duty cycle).

Table 3. FDC Read/Write Interface

CS	A <sub>0</sub>	RD	WR	Function
0 -0	0	0	1	Read Main Status Register
0	0	1	0	Illegal THEORY
0	0	0	0	Illegal
080	th 1	Orino	0	Illegal DS1,DS0 lagglII
0	1	0	1	Read from Data Register
0	1	1	0	Write into Data Register
1	X	X	X	Data Bus is three-stated

Table 5, 8272 Command Set

Table 4. Main Status Register Bit Definitions

Bit Number	Symbol	Description
0 noisemola	D <sub>0</sub> B	Disk Drive 0 Busy. Disk Drive 0 is in the Seek mode.
1	D <sub>1</sub> B	Disk Drive 1 Busy. Disk Drive 1 is in the Seek mode.
	D <sub>2</sub> B	Disk Drive 2 Busy. Disk Drive 2 is in the Seek mode.
3 erit.	D <sub>3</sub> B	Disk Drive 3 Busy. Disk Drive 3 is in the Seek mode.
4 × 30	CD	FDC Busy. A read or write command is in process.
	NDM	Non-DMA Mode. The FDC is in the non-DMA mode when this bit is high. This bit is set only during the execution phase of commands in the non-DMA mode. Transition to a low level indicates that the execution phase has ended.
	Orders of control of the control of	Data Input/Output. Indicates the direction of a data transfer between the FDC and the Data Register. When DIO is high, data is read from the Data Register by the processor; when DIO is low, data is written from the processor to the Data Register.
	RQM	Request for Master. Indicates that the Data Register is ready to send data to, or receive data from, the processor.

### Command/Result Phases

Table 5 lists the 8272 command set. For each of the fifteen commands, command and result phase data transfers are listed. A list of abbreviations used in the table is given in Table 6, and the contents of the result status registers (ST0-ST3) are illustrated in Table 7.

The bytes of data which are sent to the 8272 during the command phase, and are read out of the 8272 in the result phase, must occur in the order shown in Table 5. That is, the command code must be sent first and the other bytes sent in the prescribed sequence. All bytes of the command and result phases must be read/written as described. After the last byte of data in the command phase is sent to the 8272 the execution phase automatically starts. In a similar fashion, when the last byte of data is read from the 8272 in the result phase,

the command is automatically ended and the 8272 is ready for a new command. A command may be aborted by simply raising the terminal count signal (pin 16). This is a convenient means of ensuring that the processor may always gain control of the 8272 (even if the disk system hangs up in an abnormal manner).

It is important to note that during the result phase all bytes shown in Table 5 must be read. The Read Data command, for example, has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data command. The 8272 will not accept a new command until all seven bytes have been read. The number of command and result bytes varies from command-to-command.

In order to read data from, or write data to, the Data Register during the command and result phases, the system processor must examine the Main Status Register to determine if the Data Register is available. The DIO (bit 6) and RQM (bit 7) flags in the Main Status Register must be low and high, respectively, before each byte of the command word may be written into the 8272. Many of the commands require multiple bytes, and as a result, the Main Status Register must be read prior to each byte transfer to the 8272. To read status bytes during the result phase, DIO and ROM in the Main Status Register must both be high. Note, checking the Main Status Register in this manner before each byte transfer to/from the 8272 is required only in the command and result phases, and is NOT required during the execution phase.

### **Execution Phase**

All data transfers to (or from) the floppy drive occur during the execution phase. The 8272 has two primary modes of operation for data transfers (selected by the specify command):

- 1. DMA mode
- 2. non-DMA mode

In the DMA mode, DRQ (DMA Request) is activated for each transfer request. The DMA controller responds to DRQ with DACK (DMA Acknowledge) and RD (for read commands) or WR (for write commands). DRQ is reset by the FDC during the transfer. INT is activated after the last data transfer, indicating the completion of the execution phase, and the beginning of the result phase. In the DMA mode, the terminal count (TC/EOP) output of the DMA controller should be connected to the 8272 TC input to properly terminate disk data transfer commands.

Table 5. 8272 Command Set

BLACE 18	DAY	Dana Debat DATA BUS Amortus at	Lac command	BULL 5.5	Desi	DATA BUS	DEMARKS
PHASE	R/W	D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	REMARKS	PHASE	R/W	D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	REMARKS
		THE READ DATA	by simply raising			READ A TRACK	uniber
Command	W	MT MFM SK 0 0 1 1 0	Command Codes	Command	W	0 MFM SK 0 0 0 1 0	Command Codes
Alaria as	W	0 0 0 0 0 HDS DS1 DS0	on soousle upon	28	W	0 0 0 0 0 HDS DS1 DS0	god 1 8
Nam ou	W	19va) 7179 auc 10 1041100 Hi	Sector ID information		W	in the Seek 2 ode	Sector ID information
	W	R R	prior to Command execution	10.3	W	H	prior to Command execution
	W	N		1 8	W	N	
His sand		251 501 801 EOT 801 5501 01	mstrogmi at H		W	GPL GPL	
arsG b	W	GPL DTL	bytes shown in		W	GPL DTL	2 D-B
Execution	alab	example, has seven bytes of	Data transfer	- 0		The many of course and the second	Data transfer
Execution		Il seven bytes must be read	between the FDD	Execution		in the Seek mode.	between the FDD
200 1000		and the second s	and the main-system		8 3	Disk Drive 3 Busy, Disk Driv	and the main-system. FDC reads the
Result	R	mplete the orad Data com	Status information	1.1.	74 18	in the Seek mode.	complete track
novez l	R	ST 1	after Command			-1300211 31000 3111 111	contents from the
	R	ST 2	execution		-100	HDC Busy. A read or write S	physical index mark to EOT
	R	Н	Sector ID information	0	R	sto it is based	Status information
	R	R NOS-03-DAL R NOS IGOTI 331	after command execution	Result	R	ST 1	after Command
STREET IS	-		execution		R	ST 2	execution
med a	123 670	READ DELETED DATA	STOTE OF REPORTS	81:	R	Transit Pom P 4G-non sdr	Sector ID information
Command	W	MT MFM SK 0 1 1 0 0	Command Codes	90	R	Linear, Total R is set only due	after Command
	W	0 0 0 0 0 HDS DS1 DS0	system process		R	N	execution
	W	the Data Red cer is availab	Sector ID information prior to Command			READ ID	
	W	R	execution	Command	w	0 MFM 0 0 1 0 1 0	Command Codes
	W	N		Command	W	0 0 0 0 0 HDS DS1 DS0	Command Codes
	W	EC 1	as wolloc tentri			curion thase has ended.	
	W	SILL CATE BOLD DTL SO VENT DTO	the command v	Execution	edi :	Deta Input/Output, Indicates	The first correct ID
Execution	e 200 l	ds require multiple bytes, and	Data transfer				information on the track is stored in
		Register must be read prior	between the FDD	1 110	swis.	direction of a data transfer	Data Register
			and the main-system		- 133	the FDC and the Data Regis	
Result	R	8272. To rore status bytes	Status information	Result	R	ST 0 ST 1	Status information after Command
	R	ST 1 ST 2	after Command execution	-04	R	ST2 507 3001	execution
	R	and hardon C and Maid	must both her		R	C	
	R	is manner harme each by	Sector ID information		R	outstand and Russia restrict	Sector ID information during Execution
	R	N.	after Command execution		R	N	Phase
BBS BR	BETTE	WRITE DATA	Est shit mortivor			FORMAT A TRACK	
Command	w	MT MFM 0 0 0 1 0 1	Command Codes	Command	W	0 MFM 0 0 1 1 0 1	Command Codes
Command	W	0 0 0 0 0 HDS DS1 DS0	Command Codes	Command	W	0 0 0 0 0 HDS DS1 DS0	Communa Codeo
	w	C	Sector ID information		W	N	Bytes/Sector
	W	Н	prior to Command		W	SC	Sectors/Track
	W	R	execution	- Incident	W	GPL 1022300101	Gap 3 Filter Byte
	W	EOT	The state of the s				Titter byte
	W	GPL	All date trensf	Execution			FDC formats an
	W	VILLUIT DEL 11 310 01 318					entire track
Execution		umon phase, fire \$272 has o	Data transfer	Result	R	ST 0	Status information
ed by		stion for deta transfers (	between the main- system and the FDD		R	ST 1ST 2	after Command execution
Result	R	STO STO	Status information	-317	R	TO COMMINST OF FOR SHOP	ble 5 lists the b
riesuit	R	ST 1	after Command	data	R	Н	In this case, the ID
	R	ST 2	execution	The second second	R	R N	information has no meaning
	R	C	Sector ID information	- Elac	III'B	THE REPORT OF THE PARTY OF THE PARTY OF	meaning
129	R	R 9501	after Command	thrae	9 50	SCAN EQUAL	f ei navig zi ale
	R	N	execution	Command	W	MT MFM SK 1 0 0 0 1	Command Codes
		WRITE DELETED DATA	In the DMA m		W	0 0 0 0 0 HDS DS1 DS0	
Command	W	MT MFM 0 0 1 0 0 1	Command Codes	entr i	W	which are send to the 8272 d	Sector ID information prior to Command
	W	0 0 0 0 0 HDS DS1 DS0	T dien Chart en	the	W	CS add to the 8 bees are bees	execution
101) (I	W	C MINISTRACTION	Sector ID information		W	N	Charles and the control of
SEQ 18	W	or W.E. (tot H. ate command	prior to Command	, Z a	W	GPL EOT	suft phase, mus
botavit	W	Couring the "ransfer, LIVE"	execution	the	W	RETIT THOS DO STP T SDOO DOED	int is, the comm
to nois	W	EOT	after the last da	30 2		the prescribed sequence. All	ier bytes sentil
TOSTAL	W	GPL DTL		Execution			Data compared between the FDD
			tootusaxa ada	n as		result phases must be read/w	and the main-system
Execution		DMA mode, the term	Data transfer between the FDD	Danill	min c	he last byte of data in the c	TOTAL DEGINER
ed blu		out of the DMA controller	and the main-system	Result	R	ST 0 ST 1	Status information after Command
Result	R	STO STO	Status information	186	R	ST.2	execution
	R	ST 1	after Command		R	C C	tere francisco
	R	ST 2 19	execution	1250	R	R	Sector ID information after Command
	R	C	Sector ID information		R	N	execution
	R	R	after Command				
	R	N	execution				

Note: 1.  $A_0 = 1$  for all operations.

Table 5. Command Set (Continued)

					DAT	A BL	IS				HOUSEVENE AND THE	HS184 H	Dear	10047	HRU	1100	DAT	A BUS	S			
PHASE	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	Da	D <sub>3</sub>	1	02	D <sub>1</sub>	D <sub>0</sub>	REMARKS	PHASE	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	REMARKS
				SC	AN L	.OW	OR	EQI	JAL		100						REC	ALIB	RATE		V 10	
Command	W			1 SK		1 0		0 DS	0 DS1	1 DS0	Command Codes	Command	W	0	0	0	0	0	1 0	1 DS1	1 DS0	Command Codes
	W	0575	ed	20	hui	H	1			ylls	Sector ID information prior Command	Execution	di .(i	blait			sub.		ily w			Head retracted to Track 0
	W	e ini	e line		nd in	R _ N _			10	900	execution	6.8	a G h	BSI		-		72-723	UPT S		75	o \ bear
bi bi	W W			10131 1411					TE.	m ee	addre durin	Command Result	W R						0			Command Codes Status information at the end of each seek
Execution											between the FDD	besid	der i	W 30					bsb			operation about the FDC
	inter										and the main-system						S	PECI	FY			
Result	R R R	olds.	coer	1118	-19	ST 1	nii	80	100	en s ok a llise	Status information after Command execution	Command	W W W								1 ND	
	R		3.1			H _					Sector ID information			-		SEN	NSE I	DRIVE	ESTA	TUS	7	20
DG' basa	R	6.10	ite.	1783	anta anta	R _ N _	10	10	218	Sign Sign	after Command execution	Command	W	-	-				n 10		1010	Command Codes
				SC	AN H	IIGH	OR	EQ	UAL			Result	W	0	0	0		T 3	HDS	DS1	DS0	Status information
Command	W	МТ	MFN	1 SK	no t	and	14	1di	0	sMi.	Command Codes	nesuit 21	iz ,(d	eid)	set	mid'			she	Mc	AM	
	W	0	0	0	0	0	Н	DS	DS1	DS0	Sector ID information	the	are in	1900	03			SEE	Krad			dag in
	W W W	2 00 100 1 150 1	10) 10) 11)	is i	odi odi	H _ R _ N _ OT	7 (d	G I	(B.II 07,3 1,70	TISE TISE	prior Command execution	Command	w	0	0	0	0	0 C	HDS	DS1	DS0	Head is positioned
Execution											Data compared	017	dan	E 10								over proper Cylinder on Diskette
	isqo									Secr	between the FDD and the main-system	.2	nsfer	611			oati	NVAL	ID		TO E	วธรา อดี
Result 100	R R R R R			ebt		ST 0		10	dit	this non	Status information after Command execution  Sector ID information after Command	Command	W	ecifi	eriti Sp	or or ack	L S	TO E		ctor Sec	ez se terro terro	State) ST 0 = 80 (16)
	R	_				N _					execution											the Fo

Table 6. Command/Result Parameter Abbreviations

Symbol	Description enotitated referee	Symbol	Description
С	Cylinder Address. The currently selected cylinder address (0 to 76) on the disk.	ЕОТ	End of Track. The final sector number of the current track.
D DS0,DS1	Data Pattern. The pattern to be written in each sector data field during formatting.  Disk Drive Select.	GPL	Gap Length. The gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field as defined in section 3.)
Dris	DS1 DS0 0 0 Drive 0 0 1 Drive 1	.10115 1110	Head Address. Selected head: 0 or 1 (disk side 0 or 1, respectively) as encoded in the sector ID field.
	1 0 Drive 2 1 1 Drive 3 on bluco banango bases	HLT	Head Load Time. Defines the time interval that the FDC waits after loading the head
DTL	Special Sector Size. During the execution of disk read/write commands, this parameter is used to temporarily alter the effective disk sec-	ination. Dr	before initiating a read or write operation.  Programmable from 2 to 254 milliseconds (in increments of 2 ms).
drive	tor size. By setting N to zero, DTL may be used to specify a sector size from 1 to 256 bytes in length. If the actual sector (on the diskette) is larger than DTL specifies, the re-	sit TUH OV ror. This fit I fails to be	Head Unload Time. Defines the time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Programmable from 16 to 240 milliseconds (in
SI DAR	mainder of the actual sector is not passed to the system during read commands; during write a sector is not passed to the system during read commands;	MEM	increments of 16 ms).  MFM/FM Mode Selector, Selects MFM
	is written with all-zeroes bytes. DTL should be set to FF hexadecimal when N is not zero.	MFM	double-density recording mode when high, FM single-density mode when low.

Table 6. Command/Result Parameter Abbreviations (continued)

Symbol	Description of the States	Symbol	Description of to MAR 384
MT	Multi-Track Selector. When set, this flag selects the multi-track operating mode. In this	SK	Skip Flag. When this flag is set, sectors containing deleted data address marks will auto-
of below	mode (used only with dual-sided disks), the FDC treats a complete cylinder (under both read/write head 0 and read/write head 1) as a	noisemotal Or Brisinand no	matically be skipped during the execution of multi-sector Read Data or Scan commands. In the same manner, a sector containing a data
d Codes	single track. The FDC operates as if this		address mark will automatically be skipped
about the	expanded track started at the first sector under head 0 and ended at the last sector under head	besagme	during the execution of a multi-sector Read  Deleted Data command.
	With this flag set (high), a multi-sector read     opeation will automatically continue to the	SRT	Step Rate Interval. Defines the time interval
d Codes tings	first sector under head 1 when the FDC finishes operating on the last sector under head	n formand immand on	between step pulses issued by the FDC (track- to-track access time). Programmable from 1 to 16 milliseconds (in increments of 1 ms).
	O. SEMBE DRIVE STATUS	ST0	Status Register 0-3. Registers within the FDC
Nation to	Sector Size. The number of data bytes within a sector. (See Table 9.)	ST1 ST2	that store status information after a command has been executed. This status information is
ND	Non-DMA Mode Flag. When set (high), this flag indicates that the FDC is to operate in the	ST3	available to the processor during the Result  Phase after command execution. These
0 Copes pariented	non-DMA mode. In this mode, the processor is interrupted for each data transfer. When low, the FDC interfaces to a DMA controller by means of the DRQ and DACK signals.	nottemote: Cr bramou no	registers may only be read after a command has been executed (in the exact order shown in Table 5 for each command). These registers should not be confused with the Main Status
R	Sector Address. Specifies the sector number to	beregme	Register.
DERMINICO	be read or written. In multi-sector transfers, this parameter specifies the sector number of	STP	Scan Sector Increment. During Scan operations, this parameter is added to the current
\$tandby.	the first sector to be read or written.	home	sector number in order to determine the next
SC	Number of Sectors per Track. Specifies the number of sectors per track to be initialized by the Format Track command.	nodemolni Q primarid eo	notose O sette

### Table 7. Status Register Definitions

		Table 1. Status	Register Definitions	
Bit Number	Symbol	HOT End of Track. The English track.	Cylinder Address. The currently selected cylinder address (0 to 76) on th noisiproced	0
Status Regi	ister 0	GPL Gap Length. The gap	Data Pattern. The pattern to be written in	Q
7,6 E no	defineOIn sect	Interrupt Code.		1200.0
	ed head: 0 or l	Talac reginnin nears   Ex	ommand. The specified command was properly executed	and
	fines the time	successfully completed.	command. Command execution was started but could n	ot be
	ter leading the		equested command could not be executed.	
	d or write open t to 254 millise	changed state.	During command execution, the disk drive ready signal	
5 Isvania	SE spines the time		when the FDC has completed the Seek command and the true the correct cylinder.	he
basa a lo) babaolau	i basa sar lita		lag is set (high) if a fault signal is received from the disk become active after 77 step pulses (Recalibrate command)	
3	NR		et if a read or write command is issued and either the driffies side 1 (head 1) of a single-sided disk.	ive is
2	Н	Head Address. The head address		
1,0	DS1,DS0	Drive Select. The number of th	e drive selected at the time of the interrupt.	

Table 7. Status Register Definitions (continued)

Bit Number	Symbol	Description	Description	Symbol	
Status Regi	ster 1			Ister 3	wivs Reg
7 skib bess 6	disk MB c. from the sele	End of Track Error. This flag is set sector of the track.  Not used. This bit is always low.			final
5	d dis ad ive.	Data Error. Set when the FDC dete			ield of a
4 <sub>svirb</sub>	OR OR	Overrun Error. Set (during data tracice within the specified time interval			sor serv-
3	the currently s	Not used. This bit is always low.			
2 750 908V	ND	a) The FDC cannot locate the sector command. b) The FDC cannot locate the start c) The FDC cannot read the ID field.	or specified in the Read Data, Reading sector specified in the Read T	ad Deleted Data, of	
	A co.WN ller	Write Protect Error. This flag is set drive during the execution of a Writ			
	Of AMile ing data trail controller). The current the	<ul> <li>Missing Address Mark Error. This is</li> <li>a) The FDC cannot detect the ID a of the physical index mark).</li> <li>b) The FDC cannot detect the data specified track. (See also the MD</li> </ul>	ddress mark on the specified trac	k (after two occur	rences
Status Regi	ster 2	disk (after reception of the TC	the INT output to indicate	: 8272 activates t	sfer, the
disk <b>7</b> riu	ers; during a	Not used. This bit is always low.	phase. In the non-DMA	ng of the result	beginni
all 6 stw be	CM CM	Control Mark. This flag is set when a) A deleted data address mark during the	ing the execution of a Read Data	or Scan command	
the system ne and ini	sumber by o	Data Error. Set (high) when the FD not set when a CRC error is detected		data field. This f	lag is
ilsk sector A multi-trael	WC a ni eisrequ	Cylinder Address Error. Set when the from the current cylinder address man		sector ID field is	
bog does	SH	Scan Hit. Set during the execution of	of the Scan command if the scan		
increften	odi sasit	Scan Not Satisfied. Set during executor on the specified cylinder that sat		FDC cannot local	te a sec-
natitive re		Bad Track Error. Set when the cylin and this cylinder address is different FDC. This all "ones" cylinder number cording to the IBM soft-sectored for	from the current cylinder addres	s maintained with	in the
0	MD	Missing Data Address Mark Error. S deleted data address mark on the spo	Set if the FDC cannot detect a da	ita address mark o	r(lamito

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Register 0) to "01" (bit 7 low, bit 6 high).

(and between step pulses in the Seek command). In this

Table 7. Status Register Definitions (continued)

Bit Number	Symbol	Description	Description	Symbol .	Bit Number
Status Regi	ster 3			ter I	intus Regis
7 janii	di baFTed 10	Fault. This flag indicates the status	s of the fault signal from the sel	ected disk drive.	7
6	WP	Write Protected. This flag indicate drive.	s the status of the write protect		ected disk
n5 <sub>10</sub> bloi	STE RDY	Ready. This flag indicates the statu	as of the ready signal from the s	elected disk drive.	
4	ТО	Track 0. This flag indicates the sta	tus of the track 0 signal from th	ne selected disk driv	e.
-V398 TOSS	TS AM	Two-Sided. This flag indicates the	status of the two-sided signal fr	om the selected dis	k drive.
2	Н	Head Address. This flag indicates disk drive.	the status of the side select signa		selected
1,0	DS1,DS0	Drive Select. Indicates the currentl	y selected disk drive number.	ND Sec	

In the non-DMA mode, transfer requests are indicated by activation of both the INT output signal and the ROM flag (bit 7) in the Main Status Register, INT can be used for interrupt-driven systems and ROM can be used for polled systems. The system processor must respond to the transfer request by reading data from (activating RD), or writing data to (activating WR), the FDC. This response removes the transfer request (INT and ROM are set inactive). After completing the last transfer, the 8272 activates the INT output to indicate the beginning of the result phase. In the non-DMA mode, the processor must activate the TC signal to the FDC (normally by means of an I/O port) after the transfer request for the last data byte has been received (by the processor) and before the appropriate data byte has been read from (or written to) the FDC.

In either mode of operation (DMA or non-DMA), the execution phase ends when a terminal count signal is sensed or when the last sector on a track (the EOT parameter—Table 5) has been read or written. In addition, if the disk drive is in a "not ready" state at the beginning of the execution phase, the "not ready" flag (bit 3 in Status Register 0) is set (high) and the command is terminated.

If a fault signal is received from the disk drive at the end of a write operation (Write Data, Write Deleted Data, or Format), the FDC sets the "equipment check" flag (bit 4 in Status Register 0), and terminates the command after setting the interrupt code (bits 7 and 6 of Status Register 0) to "01" (bit 7 low, bit 6 high).

### Multi-sector and Multi-track Transfers

During disk read/write transfers (Read Data, Write Data, Read Deleted Data, and Write Deleted Data), the FDC will continue to transfer data from sequential sectors until the TC input is sensed. In the DMA mode, the

TC input is normally connected to the TC/EOP (terminal count) output of the DMA controller. In the non-DMA mode, the processor directly controls the FDC TC input as previously described. Once the TC input is received, the FDC stops requesting data transfers (from the system processor or DMA controller). The FDC, however, continues to read data from, or write data to, the floppy disk until the end of the current disk sector. During a disk read operation, the data read from the disk (after reception of the TC input) is discarded, but the data CRC is checked for errors; during a disk write operation, the remainder of the sector is filled with all-zero bytes.

If the TC signal is not received before the last byte of the current sector has been transferred to/from the system, the FDC increments the sector number by one and initiates a read or write command for this new disk sector.

The FDC is also designed to operate in a multi-track mode for dual-sided disks. In the multi-track mode (specified by means of the MT flag in the command byte—Table 5) the FDC will automatically increment the head address (from 0 to 1) when the last sector (on the track under head 0) has been read or written. Reading or writing is then continued on the first sector (sector 1) of head 1.

### **Drive Status Polling**

After the power-on reset, the 8272 automatically enters a drive status polling mode. If a change in drive status is detected (all drives are assumed to be "not ready" at power-on), an interrupt is generated. The 8272 continues this status polling between command executions (and between step pulses in the Seek command). In this manner, the 8272 automatically notifies the system processor when a floppy disk is inserted, removed, or changed by the operator.

# **Command Details**

During the command phase, the Main Status Register must be polled by the CPU before each byte is written into the Data Register. The DIO (bit 6) and RQM (bit 7) flags in the Main Status Register must be low and high, respectively, before each byte of the command may be written into the 8272. The beginning of the execution phase for any of these commands will cause DIO to be set high and RQM to be set low.

The following paragraphs describe the fifteen FDC commands in detail.

# Specify

The Specify command is used prior to performing any commands for multiple dri disk operations (including the formatting of a new disk) to define drive/FDC operating characteristics. The Specify command parameters set the values for three internal timers:

- 1. Head Load Time (HLT) This seven-bit value defines the time interval that the FDC waits after loading the head before initiating a read or write operation. This timer is programmable from 2 to 254 milliseconds in increments of 2 ms. o sides a ground
- 2. Head Unload Time (HUT) This four-bit value defines the time from the end of the execution phase (of a read or write command) until the head is unloaded. This timer is programmable from 16 to 240 milliseconds in increments of 16 ms. If the processor issues another command before the head unloads, the head will remain loaded and the head load wait will be eliminated.
- 3. Step Rate Time (SRT) This four-bit value defines the time interval between step pulses issued by the FDC (track-to-track access time). This timer is programmable from 1 to 16 milliseconds in increments

The time intervals mentioned above are a direct function of the FDC clock (CLK on pin 19). Times indicated

The Specify command also indicates the choice of DMA or ion-DMA operation (by means of the ND bit). When waishit is high the non-DMA mode is selected; when ND is , the DMA mode is selected. Sse Drive Status

Tommand may be used by the processor whenever ihes to obtain the status of the disk drives. Status Jer 3 (returned during the result phase) contains ive status information as described in Table 7.

# Sense Interrupt Status

An interrupt signal is generated by the FDC when one or more of the following events occurs: 1. The FDC enters the result phase for:

- a. Read Data command and three a

  - b. Read Track command
- c. Read ID command
- d. Read Deleted Data command
- e. Write Data command
- f. Format Track command
- g. Write Deleted Data command h. Scan commands
- 2. The ready signal from one of the disk drives changes
- 3. A Seek or Recalibrate command completes opera-
- 4. The FDC requires a data transfer during the execution phase of a command in the non-DMA mode.

Interrupts caused by reasons (1) and (4) above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons (2) and (3) above are uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the interrupt signal and by means of bits 5, 6, and 7 of Status Register 0 (returned during the result phase) identifies the cause of the interrupt (see Table 8). each step pulse is issued, the desired cylinder acc the step rate time (SET) in the Spe

Seek End	Interrup	. Inter	rupt Codes
0	Bit 6	Bit 7	Cause
	0.2 adi	0	Ready Line changed state, either polarity Normal Termination of Seek or Recalibrate Command

operating in the seek mode. When a drive has completed Neither the Seek nor the Recalibrate command has a result phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of

When an interrupt is received by the processor, the FDC busy flag (bit 4) and the non-DMA flag (bit 5) may be used to distinguish the above interrupt causes:

- 0 Asynchronous event-(2) or (3) above
- 0 1 Result phase-(1) above
- 1 Data transfer required-(4) above

A single interrupt request to the processor may, in fact, be caused by more than one of the above events. The processor should continue to issue Sense Interrupt Status commands (and service the resulting conditions) until an invalid command code is received. In this manner, all "hidden" interrupts are serviced.

### Seek

The Seek command causes the drive's read/write head to be positioned over the specified cylinder. The FDC determines the difference between the current cylinder address and the desired (specified) address, and issues the appropriate number of step pulses. If the desired cylinder address is larger than the current address, the direction signal (LCT/DIR, pin 38) is set high (step-in); the direction signal is set low (step-out) if the desired cylinder address is less than the current address. No head movement occurs (no step pulses are issued) if the desired cylinder is the same as the current cylinder.

The rate at which step pulses are issued is controlled by the step rate time (SRT) in the Specify command. After each step pulse is issued, the desired cylinder address is compared against the current cylinder address. When the cylinder addresses are equal, the "seek end" flag (bit 5 in Status Register 0) is set (high) and the command is terminated. If the disk drive becomes "not ready" during the seek operation, the "not ready" flag (in Status Register 0) is set (high) and the command is terminated.

During the command phase of the Seek operation the FDC is in the FDC busy state, but during the execution phase it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued. In this manner parallel seek operations may be in operation on up to four floppy disk drives at once. The Main Status Register contains a flag for each drive (Table 4) that indicates whether the associated drive is currently operating in the seek mode. When a drive has completed a seek operation, the FDC generates an interrupt. In response to this interrupt, the system software must issue a Sense Interrupt Status command. During the result phase of this command, Status Register 0 (containing the drive number in bits 0 and 1) is read by the processor.

### Recalibrate

This command causes the read/write head of the disk drive to retract to the track 0 position. The FDC clears the contents of its internal cylinder counter, and checks the status of the track 0 signal from the disk drive. As long as the track 0 signal is low, the direction signal remains high and step pulses are issued. When the track 0 signal goes high, the seek end flag (in Status Register 0) is set (high) and the command is terminated. If the track 0 signal is still low after 77 step pulses have been issued, the seek end and equipment check flags (in Status Register 0) are both set and the Recalibrate command is terminated.

Recalibrate commands for multiple drives can be overlapped in the same manner that Seek commands are overlapped.

### Format Track ved tes set the same many of the State of th

The Format Track command formats or "initializes" a track on a floopy disk by writing the ID field, gaps, and address marks for each sector. Before issuing the Format command, the Seek command must be used to position the read/write head over the correct cylinder. In addition, a table of ID field values (cylinder, head, and sector addresses and sector length code) must be prepared before the command is executed. During command execution, the FDC accesses the table and, using the values supplied, writes each sector on the track. The ID field address mark originates from the FDC and is written automatically as the first byte of each sector's ID field. The cylinder, head, and sector addresses are taken, in order, from the table. The ID field CRC character (derived from the data written in the first five bytes) is written as the last two bytes of the ID field. Gaps are written automatically by the FDC, with the length of the variable gap determined by one of the Format command parameters.

The data field address mark is generated by the FDC and is written automatically as the first byte of the data field. The data pattern specified in the command phase is written into each data byte of each sector. A CRC character is derived from the data address mark and the data written in the sector's data field. The two CRC bytes are appended to the last data byte.

The formatting of a track begins at the physical index mark. As previously mentioned, the order of sector assignment is taken directly from the formatting table. Four entries are required for each sector: a cylinder address, a head address, a sector address, and a sector length code. The cylinder address in the ID field should be equal to the cylinder address of the track currently being formatted.

The sector addresses must be unique (no two equal). The order of the sector entries in the table is the sequence in which sector numbers appear on the track when it is formatted. The number of entry sets (cylinder, head, and sector address and sector length code) must equal the number of sectors allocated to the track (specified in the command phase).

Since the sector address is supplied, in order, for each sector, tracks can be formatted sequentially (the first sector following the index mark is assigned sector address 1, the adjacent sector is assigned sector address 2, and so on) or sector numbers can be interleaved (see section 3) on a track.

Table 9 lists recommended gap sizes and sectors/track for various sector sizes.

### Read Data

Nine (9) bytes are required to complete the command phase specification for the Read Data command. During the execution phase, the FDC loads the head (if it is in the unloaded state), waits the specified head load time (defined in the Specify command), and begins reading ID address marks and ID fields. When the requested sector address compares with the sector address read from the disk, the FDC outputs data (from the data field) byte-by-byte to the system. The Read Data command automatically operates in the multi-sector mode described earlier. In addition, multi-track operation may be specified by means of the MT command flag (Table 5). The amount of data that can be transferred with a single command to the FDC depends on the multi-track flag, the recording density flag, and the number of bytes per sector.

During the execution of read and write commands, the special sector size parameter (DTL) is used to temporarily alter the effective disk sector size. By setting the sector size code (N) to zero, DTL may be used to specify a sector size from 1 to 256 bytes in length. If the actual sector (on the disk) is larger than DTL specifies, only the number of bytes specified by the DTL parameter are

passed to the system; the remainder of the actual disk sector is not transferred (although the data is checked for CRC errors). Multi-sector read operations are performed in the same manner as they are when the sector size code is non-zero. (The N and DTL parameters are always present in the command sequence. DTL should be set to FF hexadecimal when N is not zero.)

If the FDC detects the physical index mark twice without finding the requested sector, the FDC sets the "sector not found error" flag (bit 2 in Status Register 1) and terminates the Read Data command. The interrupt code (bits 7 and 6 of Status Register 0) is set to "01." Note that the FDC searches for each sector in a multisector operation. Therefore, a "sector not found" error may occur after successful transfer of one or more preceding sectors. This error could occur if a particular sector number was not included when the track was first formatted or if a hard error on the disk has invalidated a sector ID field.

After reading the ID field and data field in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in the ID field), the FDC sets the "data error" flag in Status Register 1; if a CRC error occurs in the data field, the FDC sets the "data error" flag in Status Register 2. In either error condition, the FDC terminates the Read Data command. The interrupt code (bits 7 and 6 in Status Register 0) is set to "01."

If the FDC reads a deleted data address mark from the disk, and the skip flag (specified during the command phase) is not set, the FDC sets the "control mark" flag (bit 6 in Status Register 2) and terminates the Read Data command (after reading all the data in the sector). If the skip flag is set, the FDC skips the sector with the deleted data address mark and reads the next sector. Thus, the skip flag may be used to cause the FDC to ignore deleted data sectors during a multi-sector read operation.

During disk data transfers between the FDC and the system, the FDC must be serviced by the system (processor or DMA controller) every 27  $\mu$ s in the FM mode, and every 13  $\mu$ s in the MFM mode. If the FDC is not

1.100 on the at (0 restate Table 9. Sector Size Relationships

Format	Sector Size	N Sector Size Code	SC Sectors/ Track	GPL <sup>1</sup> Gap 3 Length	GPL <sup>2</sup> Gap 3 Length	Remarks  IBM Diskette 1 IBM Diskette 2	
FM Mode	128 bytes/Sector 256 512	00 01 02	1A <sub>(16)</sub> 0F <sub>(16)</sub> 08	07 <sub>(16)</sub> 0E <sub>(16)</sub> 1B <sub>(16)</sub>	1B <sub>(16)</sub> 2A <sub>(16)</sub> 3A <sub>(16)</sub>		
MFM Mode	256 (d) 152 at gall 1 35 512 dr no bauot a 1024 dr no oda	01 asott 02 on 11 asott 02 on 11 asott 03 bruso	1A <sub>(16)</sub> 0F <sub>(16)</sub> 08	0E <sub>(16)</sub> 1B <sub>(16)</sub> 35 <sub>(16)</sub>	36 <sub>(16)</sub> 54 <sub>(16)</sub> 74 <sub>(16)</sub>	IBM Diskette 2D  IBM Diskette 2D	

Notes: 1. Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sectors.

2. Suggested values of GPL in Format command. Animost and the strain and the stra

serviced within this interval, the "overrun error" flag (bit 4 in Status Register 1) is set and the Read Data command is terminated.

If the processor terminates a read (or write) operation in the FDC, the ID information in the result phase is dependent upon the state of the multi-track flag and end of track byte. Table 11 shows the values for C, H, R, and N, when the processor terminates the command.

### Write Data and place of the Data and Data of the State of the Write Data

Nine (9) bytes are required to complete the command phase specification for the Write Data command. During the execution phase the FDC loads the head (if it is in the unloaded state), waits the specified head load time (defined by the Specify command), and begins reading sector ID fields. When the requested sector address compares with the sector address read from the disk, the FDC reads data from the processor one byte at a time via the data bus and outputs the data to the data field of that sector. The CRC is computed on this data and two CRC bytes are written at the end of the data field.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID fields, it sets the "data error" flag (bit 5 in Status Register 1) and terminates the Write Data command. The interrupt code (bits 7 and 6 in Status Register 0) is set to "01."

The Write Data command operates in much the same manner as the Read Data command. The following items are the same; refer to the Read Data command for details:

- Multi-sector and Multi-track operation
- Data transfer capacity
- "End of track error" flag
- "Sector not found error" flag
- · "Data error" flag and analyzant stab stab gained
- Head unload time interval
- ID information when the processor terminates the command (see Table 11)
- Definition of DTL when N=0 and when  $N\neq 0$

During the Write Data execution phase, data transfers between the processor and FDC must occur every  $31 \mu s$  in the FM mode, and every  $15 \mu s$  in the MFM mode. If the time interval between data transfers is longer than this, the FDC sets the "overrun error" flag (bit 4 in Status Register 1) and terminates the Write Data command.

### Read Deleted Data

This command operates in almost the same manner as the Read Data command operates. The only difference involves the treatment of the data address mark and the skip flag. When the FDC detects a data address mark at the beginning of a data field (and the skip flag is not set), the FDC reads all the data in the sector, sets the "control mark" flag (bit 6 in Status Register 2), and terminates the command. If the skip flag is set, the FDC skips the sector with the data address mark and continues reading at the next sector. Thus, the skip flag may be used to cause the FDC to read only deleted data sectors during a multi-sector read operation.

# Write Deleted Data

This command operates in the same manner as the Write Data command operates except that a deleted data address mark is written at the beginning of the data field instead of the normal data address mark. This command is used to mark a bad sector (containing a hard error) on the floppy disk.

### **Read Track**

The Read Track command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the physical index mark, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID field or data field CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the values specified during the command phase. If the specified ID field information is not found on the track, the "sector not found error" flag (in Status Register 1) is set. Multitrack and skip operations are not allowed with this command.

This command terminates when the last sector on the track has been read. (The number of sectors on the track is specified by the end of track parameter byte during the command phase.) If the FDC does not find an ID address mark on the disk after it encounters the physical index mark for the second time, it sets the "missing address mark error" flag (bit 0 in Status Register 1) and terminates the command. The interrupt code (bits 7 and 6 of Status Register 0) is set to "01."

### Read ID

The Read ID command transfers (reads) the first correct ID field from the current disk track (following the physical index mark) to the processor. If no correct ID address mark is found on the track, the "missing address mark error" flag is set (bit 0 in Status Register 1). If no data mark is found on the track, the "sector not found error" flag is also set (bit 2 in Status Register 1). Either error condition causes the command to be terminated.

### Scan Commands TARAGES ATAC EHT .a

The Scan commands allow the data being read from the disk to be compared against data supplied by the system (by the processor in non-DMA mode, and by the DMA controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and searches for a sector of data that meets the conditions of "disk data equal to system data", "disk data less than or equal to system data", or "disk data greater than or equal to system data". Simple binary (ones complement) arithmetic is used for comparison (FF = largest number, 00 = smallest number). If, after a complete sector of data is compared, the conditions are not met, the sector number is incremented by the scan sector increment (specified in the command phase), and the scan operation is continued. The scan operation continues until one of the following conditions occurs; the conditions for scan are met (equal, low, or high), the last sector on the track is reached, or the terminal count signal is received.

If the conditions for scan are met, the FDC sets the "scan hit" flag (bit 3 in Status Register 2) and terminates the Scan command. If the conditions for scan are not met between the starting sector and the last sector on the track (specified in the command phase), the FDC sets the "scan not satisfied" flag (bit 2 in Status Register 2) and terminates the Scan command. The receipt of a terminal count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and to terminate the command. Table 10 shows the status of the "scan hit" and "scan

Table 10. Scan Status Codes

Command	Status R	egister 2	Comments		
haeramaa	Bit 2 = SN	Bit 3 = SH	or ant on		
Scan Equal	or e0 10	propiriy.	$\begin{array}{c} D_{FDD} = D_{Processor} \\ D_{FDD} \neq D_{Processor} \end{array}$		
Scan Low or Equal	i, and the self, 20, and tor. 17 will	is sel to 2 sec0ors The n0xt se	D <sub>FDD</sub> = D <sub>Processor</sub> D <sub>FDD</sub> ≤ D <sub>Processor</sub> D <sub>FDD</sub> ≰ D <sub>Processor</sub>		
Scan High or Equal	abnoonal rather formula in maliner f		D <sub>FDD</sub> = D <sub>Processor</sub> D <sub>FDD</sub> > D <sub>Processor</sub> D <sub>FDD</sub> ≱ D <sub>Processor</sub>		

Table 11. ID Information When Processor Terminates Command

or analog one TM		b Final Sector Transferred		rq adi yd ID Information at Result Phase at grinu			
		Processor		C	for opinipar	BIOTIRO AMO TONIO	NON TO NOOR
ced to 2 µs (i pacity), Cloc	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	Sill Sill Sill Sill Sill Sill Sill Sill	NC	a available in	R+1	NC
if data bits at	a sire A1 only rent a70 pre			C+1	1	R=01	
resent) still or as. First, onl	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	,DI	ON ent to the FI	NC zi basmmoo	abnammo R+1 (badefino) l	O bilsyn NC ilsyni as 1
	aidt 1A tid si	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1		ition 1+2 6	ring this cont	R=01 di (MON bas	NC
shorter bit ce ge a playbac	or F/A1Thas olerat 70 s late are) w 80 out		0 1	NC		t+A the	
able, the FD ream so the	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	S 1:		LSB um basmusos	R=01	
tely controlle PM recording ities an early	olomia i noi	A STATE OF THE PROPERTY OF THE	.br	valid Or ma	ni na NC or ba	nex 1+8 mass of the last of th	NC NC no nem
ig informatione clock. Earl 0 ns before c	the FAO wri		-111	C+1 po sint seu ot	LSB	R = 01	NC NC

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.

2. LSB (Least Significant Bit): The least significant bit of H is complemented.

not satisfied" flags under various scan termination conditions.

If the FDC encounters a deleted data address mark in one of the sectors and the skip flag is low, it regards the sector as the last sector on the cylinder, sets the "control mark" flag (bit 6 in Status Register 2) and terminates the command. If the skip flag is high, the FDC skips the sector with the deleted address mark, and reads the next sector. In this case, the FDC also sets the "control mark" flag (bit 6 in Status Register 2) in order to show that a deleted sector had been encountered.

NOTE: During scan command execution, the last sector on the track must be read for the command to terminate properly. For example, if the scan sector increment is set to 2, the end of track parameter is set to 26, and the scan begins at sector 21, sectors 21, 23, and 25 will be scanned. The next sector, 27 will not be found on the track and an abnormal command termination will occur. The command would be completed in a normal manner if either a) the scan had started at sector 20 or b) the end of track parameter had been set to 25.

During the Scan command, data is supplied by the processor or DMA controller for comparison against the data read from the disk. In order to avoid having the "overrun error" flag set (bit 4 in Status Register 1), it is necessary to have the data available in less than 27  $\mu$ s (FM Mode) or 13  $\mu$ s (MFM Mode). If an overrun error occurs, the FDC terminates the command.

### **Invalid Commands**

If an invalid (undefined) command is sent to the FDC, the FDC will terminate the command. No interrupt is generated by the 8272 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both set indicating to the processor that the 8272 is in the result phase and the contents of Status Register 0 must be read. When the processor reads Status Register 0 it will find an 80H code indicating that an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command. Also, when the last "hidden" interrupt has been serviced, further Sense Interrupt Status commands will result in invalid command codes.

In some applications the user may wish to use this command as a No-Op command to place the FDC in a stand-by or no operation state.

### 5. THE DATA SEPARATOR

As briefly discussed in section 2, LSI disk controllers such as the 8272 require external circuitry to generate a data window signal. This signal is used within the FDC to isolate the data bits contained within the READ DATA input signal from the disk drive. (The disk READ DATA signal is a composite signal constructed from both clock and data information.) After isolating the data bits from this input signal, the FDC assembles the data bits into 8-bit bytes for transfer to the system processor or memory.

### Single Density and too ere anoitibno ed being

In single-density (FM) recording (Figure 3), the bit cell is 4 microseconds wide. Each bit cell contains a clock bit at the leading edge of the cell. The data bit (if present) is always located at the center of the cell. The job of data separation is relatively straightforward for single-density; simply generate a data window  $2 \mu s$  wide starting  $1 \mu s$  after each clock bit. Since every cell has a clock bit, a fixed window reference is available for every data bit and because the window is  $2 \mu s$  wide, a slightly shifted data bit will still remain within the data window.

A single-density data separator with these specifications may be easily generated using a digital or analog oneshot triggered by the clock bit.

### **Double-Density**

Double-density (MFM) bit cells are reduced to 2  $\mu$ s (in order to double the disk data storage capacity). Clock bits are inserted into the data stream only if data bits are not present in both the current and preceding bit cells (Figure 3). The data bit (if present) still occurs at the center of the bit cell and the clock bit (if present) still occurs at the leading edge of the bit cell.

MFM data separation has two problems. First, only some bit cells contain a clock bit. In this manner, MFM encoding loses the fixed bit cell reference pulse present in FM encoding. Second, the bit cell for MFM is one-half the size of the bit cell for FM. This shorter bit cell means that MFM cannot tolerate as large a playback data-shift (as FM can tolerate) without errors.

Since most playback data-shift is predictable, the FDC can precompensate the write data stream so that data/clock pulses will be correctly positioned for subsequent playback. This function is completely controlled by the FDC and is only required for MFM recording. During write operations, the FDC specifies an early, normal, or late bit positioning. This timing information is specified with respect to the FDC write clock. Early and late timing is typically 125 ns to 250 ns before or after the write clock transition (depending on disk drive requirements).

The data separator circuitry for double-density recording must continuously analyze the total READ DATA stream, synchronizing its operation (window generation) with the actual clock/data bits of the data stream. The data separation circuit must track the disk input data frequency very closely—unpredictable bit shifts leave less than 50 ns margin to the window edges.

### Phase-Locked Loop

Only an analog phase-locked loop (PLL) can provide the reliability required for a double-density data separation circuit. (A phase-locked loop is an electronic circuit that constantly analyzes the frequency of an input signal and locks another oscillator to that frequency.) Using analog PLL techniques, a data separator can be designed with ±1 ns resolution (this would require a 100 MHz clock in a digital phase-locked loop). The analog PLL determines the clock and data bit positions by sampling each bit in the serial data stream. The phase relationship between a data bit and the PLL generated data window is constantly fed back to adjust the position of the data window, enabling the PLL to track input data frequency changes, and thereby reliably read previously recorded data from a floppy disk.

### PLL Design

A block diagram of the phase-locked loop described in this application note is shown in Figure 7. Basically, the phase-locked loop operates by comparing the frequency of the input data (from the disk drive) against the frequency of a local oscillator. The difference of these frequencies is used to increase or decrease the frequency of the local oscillator in order to bring its frequency closer to that of the input. The PLL synchronizes the local oscillator to the frequency of the input during the all "zeroes" synchronization field on the floppy disk (immediately preceding both the ID field and the data field).

The PLL consists of nine ICs and is located on page 3 of the schematics in the Appendix. The 8272 VCO output essentially turns the PLL circuitry on and off. When the PLL is off, it "idles" at its center frequency. The VCO output turns the PLL on only when valid data is being received from the disk drive. The VCO turns the PLL on after the read/write head has been loaded and the head load time has elapsed. The PLL is turned off in the gap between the ID field and the data field and in the gap after the data field (before the next sector ID field). The GPL parameter in the FDC read and write commands specifies the elapsed time (number of data bytes) that the PLL is turned off in order to blank out discontinuities that appear in the gaps when the write current is turned on and off. The PLL operates with either MFM or FM input data. The MFM output from the FDC controls the PLL operation frequency.

The PLL consists of six functional blocks as follows:

- Pulse Shaping A 96LS02 senses a READ DATA pulse and provides a clean output signal to the FDC and to the PLL Phase Comparator and Frequency Discriminator circuitry.
- 2. Phase Comparator The phase difference between the PLL oscillator and the READ DATA input is compared. Pump up (PU) and pump down (PD) error signals are derived from this phase difference and output to the filter. If there is no phase difference between the PLL oscillator and the READ DATA input, the PU and PD pulse widths are equal. If the READ DATA pulse occurs early, the PU duration is shorter than the PD duration. If the data pulse occurs late, the PU duration is longer than the PD duration.
- Filter This analog circuit filters the PU and PD pulses into an error voltage. This error voltage is buffered by an LM358 operational amplifier.

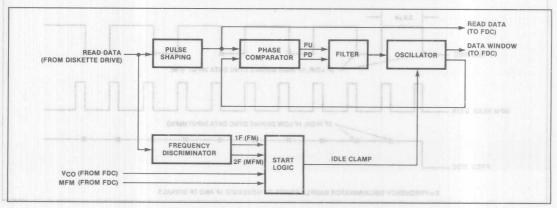


Figure 7. Phase-Locked Loop Data Separator

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- 74LS393, 74LS74, and 96LS02. The oscillator frequency is controlled by the error voltage output by the filter. This oscillator also generates the data window signal to the FDC.
- Frequency Discriminator This logic tracks the READ DATA input from the disk drive and discriminates between the synchronization gap for FM recording (250 KHz) and the gap for MFM recording (500 KHz). Synchronization gaps immediately precede address marks.
- 6. Start Logic The function of this logic is to clamp the PLL oscillator to its center frequency (2 MHz) until the FDC VCO signal is enabled and a valid data pattern is sensed by the frequency discriminator. The start logic (consisting of a 74LS393 and 74LS74) ensures that the PLL oscillator is started with zero phase error.

# PLL Adjustments

The PLL must be initially adjusted to operate at its center frequency with the VCO output off and the adjustment jumper removed. The 5K trimpot should be adjusted until the frequency at the test point (Q output of the 96LS02) is 2 MHz. The jumper should then be replaced for normal operation.

### PLL Design Details bas U9 and Jugan ATAG

The following paragraphs describe the operational and design details of the phase-locked loop data separator il-

in the appendix. Note that the analog section is operated from a separately filtered +5V supply.

### Initialization o said sisb \\ doctor lauros ord risiw (nois

As long as the 8272 maintains a low VCO signal, the data separator logic is "turned off". In this state, the PLL oscillator (96LS02) is not oscillating and therefore the 2XBR signal is constantly low. In addition, the pump up (PU) and pump down (PD) signals are inactive (PU low and PD high), the CNT8 signal is inactive (low), and the filter input voltage is held at 2.5 volts by two 1Mohm resistors between ground and +5 volts.

### Floppy Disk Data or rotallisso rantons about birs

The data separator frequency discriminator, the input pulse shaping circuitry, and the start logic are always enabled and respond to rising edges of the READ DATA signal. The rising edge of every data bit from the disk drive triggers two pulse shaping one-shots. The first pulse shaper generates a stable and well-defined 200 ns read data pulse for input to the 8272 and other portions of the data separator logic. The second one-shot generates a 2.5  $\mu$ s data pulse that is used for input data frequency discrimination.

The frequency discriminator operates as illustrated in Figure 8. The 2F output signal is active (high) during reception of valid MFM (double-density) sync fields on the disk while the 1F signal is active (high) during reception of valid FM (single-density) sync fields. A multiplexer (controlled by the 8272 MFM signal) selects the appropriate 1F or 2F signal depending on the programmed mode.

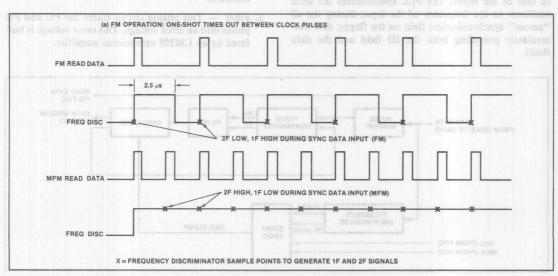


Figure 8. Input Data Frequency Discrimination

### Startup

The data separator is designed to require reception of eight valid sync bits (one sync byte) before enabling the PLL oscillator and attempting to synchronize with the input data stream (see Figure 9). This delay ensures that the PLL will not erroneously synchronize outside a valid sync field in the data stream if the VCO signal is enabled slightly early. The sync bit counter is asynchronously reset by the CNTEN signal when valid sync data is not being received by the drive.

Processor and Memory

Once the VCO signal is active and eight sync bits have been counted, the CNT8 signal is enabled. This signal turns on the PLL oscillator. Note that this oscillator starts synchronously with the rising edge of the disk input data (because CNT8 is synchronous with the data rising edge) and the oscillator also starts at its center frequency of 2 MHz (because the LM348 filter input is held at its center voltage of approximately 2.5 volts). This frequency is divided by two and four to generate the 2XBR signal (1 MHz for MFM and 500 KHz for FM).

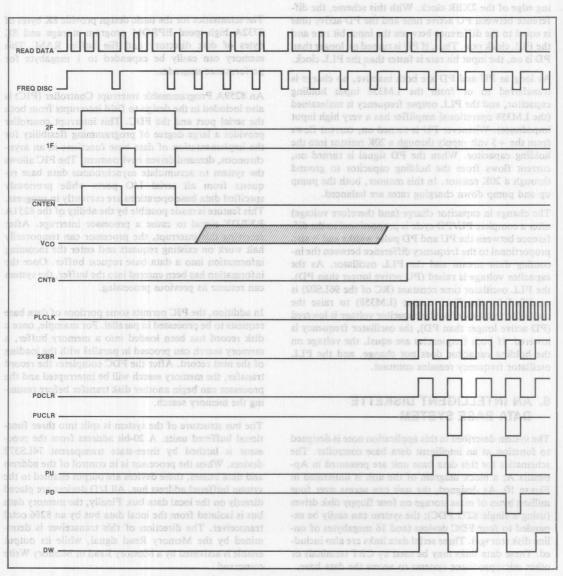


Figure 9. Typical Data Separator Startup Timing Diagram

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### PLL Synchronization al langia OOV and sonO

At this point, the PLL is enabled and begins to synchronize with the input data stream. This synchronization is accomplished very simply in the following manner. The pump up (PU) signal is enabled on the rising edge of the READ DATA from the disk drive. (When the PLL is synchronized with the data stream, this point will occur at the same time as the falling edge of the 2XBR signal as shown in Figure 9). The PU signal is turned off and the PD signal is activated on the next rising edge of the 2XBR clock. With this scheme, the difference between PU active time and the PD active time is equal to the difference between the input bit rate and the PLL clock rate. Thus, if PU is turned on longer than PD is on, the input bit rate is faster than the PLL clock.

As long as PU and PD are both inactive, no charge is transferred to or from the LM358 input holding capacitor, and the PLL output frequency is maintained (the LM358 operational amplifier has a very high input impedance). Whenever PU is turned on, current flows from the +5 volt supply through a 20K resistor into the holding capacitor. When the PD signal is turned on, current flows from the holding capacitor to ground through a 20K resistor. In this manner, both the pump up and pump down charging rates are balanced.

The change in capacitor charge (and therefore voltage) after a complete PU/PD cycle is proportional to the difference between the PU and PD pulse widths and is also proportional to the frequency difference between the incoming data stream and the PLL oscillator. As the capacitor voltage is raised (PU active longer than PD), the PLL oscillator time constant (RC of the 96LS02) is modified by the filter output (LM358) to raise the oscillator frequency. As the capacitor voltage is lowered (PD active longer than PD), the oscillator frequency is lowered. If both frequencies are equal, the voltage on the holding capacitor does not change, and the PLL oscillator frequency remains constant.

# 6. AN INTELLIGENT DISKETTE DATA BASE SYSTEM

The system described in this application note is designed to function as an intelligent data base controller. The schematics for this data base unit are presented in Appendix A; a block diagram of the unit is illustrated in Figure 10. As designed, the unit can access over four million bytes of mass storage on four floppy disk drives (using a single 8272 FDC); the system can easily be expanded to four FDC devices (and 16 megabytes of online disk storage). Three serial data links are also included. These data links may be used by CRT terminals or other microprocessor systems to access the data base.

### **Processor and Memory**

A high-performance 8088 eight-bit microprocessor (operating at 5 MHz with no wait states) controls system operation. The 8088 was selected because of its memory addressing capabilities and its sophisticated string handling instructions. These features improve the speed of data base search operations. In addition, these capabilities allow the system to be easily upgraded with additional memory, disk drives, and if required, a bubble memory or winchester disk unit.

The schematics for the basic design provide 8K bytes of 2732A high-speed EPROM program storage and 8K bytes of disk directory and file buffer RAM. This memory can easily be expanded to 1 megabyte for performance upgrades.

An 8259A Programmable Interrupt Controller (PIC) is also included in the design to field interrupts from both the serial port and the FDC. This interrupt controller provides a large degree of programming flexibility for the implementation of data base functions in an asynchronous, demand driven environment. The PIC allows the system to accumulate asynchronous data base requests from all serial I/O ports while previously specified data base operations are currently in progress. This feature is made possible by the ability of the 8251A RXRDY signal to cause a processor interrupt. After receiving this interrupt, the processor can temporarily halt work on existing requests and enter the incoming information into a data base request buffer. Once the information has been entered into the buffer, the system can resume its previous processing.

In addition, the PIC permits some portions of data base requests to be processed in parallel. For example, once a disk record has been loaded into a memory buffer, a memory search can proceed in parallel with the loading of the next record. After the FDC completes the record transfer, the memory search will be interrupted and the processor can begin another disk transfer before resuming the memory search.

The bus structure of the system is split into three functional buffered units. A 20-bit address from the processor is latched by three-state transparent 74LS373 devices. When the processor is in control of the address and data busses, these devices are output enabled to the system buffered address bus. All I/O devices are placed directly on the local data bus. Finally, the memory data bus is isolated from the local data bus by an 8286 octal transceiver. The direction of this transceiver is determined by the Memory Read signal, while its output enable is activated by a Memory Read or Memory Write command.

Floure 9. Typical Data Separator Startup Timing Diagram

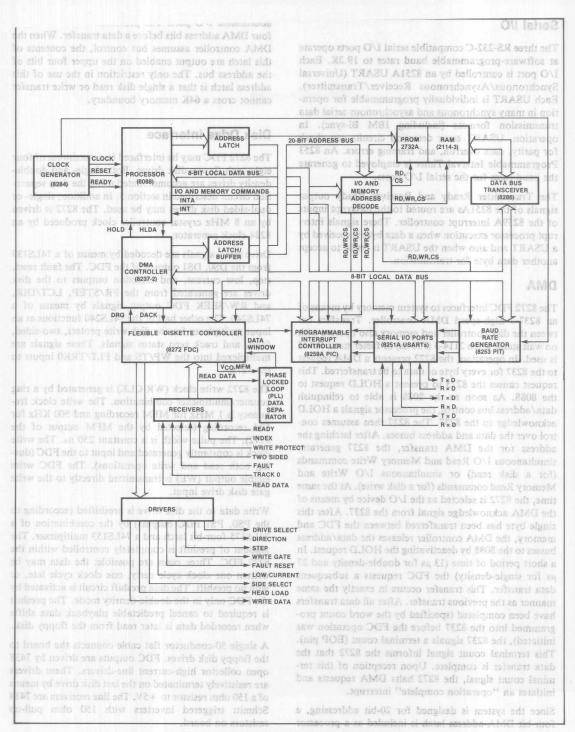


Figure 10. Intelligent Data Base Block Diagram

The three RS-232-C compatible serial I/O ports operate at software-programmable baud rates to 19.2K. Each I/O port is controlled by an 8251A USART (Universal Synchronous/Asynchronous Receiver/Transmitter). Each USART is individually programmable for operation in many synchronous and asynchronous serial data transmission formats (including IBM Bi-sync). In operation, USART error detection circuits can check for parity, data overrun, and framing errors. An 8253 Programmable Interval Timer is employed to generate the baud rates for the serial I/O ports.

The Transmitter Ready and Receiver Ready output signals of the 8251As are routed to the interrupt inputs of the 8259A interrupt controller. These signals interrupt processor execution when a data byte is received by a USART and also when the USART is ready to accept another data byte for transmission.

### DMA

The 8272 FDC interfaces to system memory by means of an 8237-2 high-speed DMA controller. Transfers between the disk controller and memory also operate with no wait states when 2114-3 (150 ns) or faster static RAM is used. In operation, the 8272 presents a DMA request to the 8237 for every byte of data to be transferred. This request causes the 8273 to present a HOLD request to the 8088. As soon as the 8088 is able to relinquish data/address bus control, the processor signals a HOLD acknowledge to the 8237. The 8237 then assumes control over the data and address busses. After latching the address for the DMA transfer, the 8237 generates simultaneous I/O Read and Memory Write commands (for a disk read) or simultaneous I/O Write and Memory Read commands (for a disk write). At the same time, the 8272 is selected as the I/O device by means of the DMA acknowledge signal from the 8237. After this single byte has been transferred between the FDC and memory, the DMA controller releases the data/address busses to the 8088 by deactivating the HOLD request. In a short period of time (13 µs for double-density and 27 us for single-density) the FDC requests a subsequent data transfer. This transfer occurs in exactly the same manner as the previous transfer. After all data transfers have been completed (specified by the word count programmed into the 8237 before the FDC operation was initiated), the 8237 signals a terminal count (EOP pin). This terminal count signal informs the 8272 that the data transfer is complete. Upon reception of this terminal count signal, the 8272 halts DMA requests and initiates an "operation complete" interrupt.

Since the system is designed for 20-bit addressing, a four-bit DMA-address latch is included as a processor

four DMA address bits before a data transfer. When the DMA controller assumes bus control, the contents of this latch are output enabled on the upper four bits of the address bus. The only restriction in the use of this address latch is that a single disk read or write transfer cannot cross a 64K memory boundary.

### **Disk Drive Interface**

The 8272 FDC may be interfaced to a maximum of four eight-inch floppy disk drives. Both single- and double-density drives are accommodated using the data separation circuit described in section 5. In addition, single- or dual-sided disk drives may be used. The 8272 is driven by an 8 MHz crystal controller clock produced by an 8224 clock generator.

Drive select signals are decoded by means of a 74LS139 from the DS0, DS1 outputs of the FDC. The fault reset, step, low current, and direction outputs to the disk drives are generated from the FR/STEP, LCT/DIR, and RW/SEEK FDC output signals by means of a 74LS240. The other half of the 74LS240 functions as an input multiplexer for the disk write protect, two-sided, fault, and track zero status signals. These signals are multiplexed into the WP/TS and FLT/TRK0 inputs to the 8272.

The 8272 write clock (WR CLK) is generated by a ring counter/multiplexer combination. The write clock frequency is 1 MHz for MFM recording and 500 KHz for FM recording (selected by the MFM output of the 8272). The pulse width is a constant 250 ns. The write clock is constantly generated and input to the FDC (during both read and write operations). The FDC write enable output (WE) is transmitted directly to the write gate disk drive input.

Write data to the disk drive is preshifted (according to the PS0, PS1 FDC outputs) by the combination of a 74LS175 four-bit latch and a 74LS153 multiplexer. The amount of preshift is completely controlled within the 8272 FDC. Three cases are possible: the data may be written one clock cycle early, one clock cycle late, or with no preshift. The data preshift circuit is activated by the FDC only in the double-density mode. The preshift is required to cancel predictable playback data shifts when recorded data is later read from the floppy disk.

A single 50-conductor flat cable connects the board to the floppy disk drives. FDC outputs are driven by 7438 open collector high-current line-drivers. These drivers are resistively terminated on the last disk drive by means of a 150 ohm resistor to +5V. The line receivers are 7414 Schmitt triggered inverters with 150 ohm pull-up resistors on board.

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### 7. SPECIAL CONSIDERATIONS

This section contains a quick review of key features and issues, most of which have been mentioned in other sections of this application note. Before designing with the 8272 FDC, it is advisable that the information in this section be completely understood. bad track operation, assume that a

### 1. Multi-Sector Transfers 1 bns 12 Joseph land comm

The 8272 always operates in a multi-sector transfer mode. The 8272 continues to transfer data until the TC input is activated. In a DMA configuration, the TC input of the 8272 must always be connected to the EOP/TC output of the DMA controller. When multiple DMA channels are used on a single DMA controller, EOP must be gated with the select signal for the proper FDC. If the TC signal is not gated, a terminal count on another channel will abort FDC operation.

In a processor driven configuration with no DMA controller, the system must count the transfers and supply a TC signal to the FDC. In a DMA environment, ORing a programmable TC with the TC from the DMA controller is a convenient means of ensuring that the processor may always gain control of the FDC (even if the diskette system hangs up in an abnormal manner).

#### 2. Processor Command/Result Phase Interface

In the command phase, the processor must write the exact number of parameters in the exact order shown in Table 5. During the result phase, the processor must read the complete result status. For example, the Format Track command requires six command bytes and presents seven result bytes. The 8272 will not accept a new command until all result bytes are read. Note that the number of command and result bytes varies from command-to-command. Command and result phases cannot be shortened. (16 viernam , de bas 0 noowing

During both the command and result phases, the Main Status Register must be read by the processor before each byte of information is read from, or written to, the FDC Data Register. Before each command byte is written, DIO (bit 6) must be low (indicating a data transfer from the processor) and RQM (bit 7) must be high (indicating that the FDC is ready for data). During the result phase, DIO must be high (indicating a data transfer to the processor) and ROM must also be high (indicating that data is ready for the processor).

NOTE: After the 8272 receives a command byte, the RQM flag may remain set for 12 microseconds (with an 8 MHz clock). Software should not attempt to read the Main Status Register before this time interval has elapsed; otherwise, the software will erroneously assume that the FDC is ready to accept the next byte.

### 3. Sector Sizes

The 8272 does not support 128 byte sectors in the MFM (double-density) mode. semmoo send T abnammoo masa

### 4. Write Clock

The FDC Write Clock input (WR CLK) must be present at all times.

the FDC may be reporting one of two distinteen s. The FDC Reset input (RST) must be held active during power-on reset while the RD and WR inputs are active. If the reset input becomes inactive while RD and WR are still active, the 8272 enters the test mode. Once activated, the test mode can only be deactivated by a power-down condition. Dissum as to additation at

### 6. Drive Status vo distinguished by subsection of the state of the sta

The 8272 constantly polls (starting after the power-on reset) all drives for changes in the drive ready status. At power-on, the FDC assumes that all drives are not ready. If a drive application requires that the ready line be strapped active, the FDC will generate an interrupt immediately after power is applied.

## 7. Gap Length was to sunitate to the processor and

Only the gap 3 size is software programmable. All other gap sizes are fixed. In addition, different gap 3 sizes must be specified in format, read, write, and scan commands. Refer to Section 3 and Table 9 for gap size recommendations.

### 8. Seek Command

The drive busy flag in the Main Status Register remains set after a Seek command is issued until the Sense Interrupt Status command is issued (following reception of the seek complete interrupt).

The FDC does not perform implied seeks. Before issuing data read or write commands, the read/write head must be positioned over the correct cylinder. If the head is not positioned correctly, a cylinder address error is data in the sector) when a deleted data addr.

After issuing a step pulse, the 8272 resumes drive status polling. For correct stepper operation in this mode, the stepper motor must be constantly enabled. (Most drives provide a jumper to permit the stepper motor to be constantly enabled.) b tady more noiteurs enzogo and taus

### 9. Step Rate Alam worlds stab a penW independent

The 8272 can emit a step pulse that is one millisecond faster than the rate programmed by the SRT parameter in the Specify command. This action may cause subsequent sector not found errors. The step rate time should be programmed to be 1 ms longer than the step rate time required by the drive.

#### 10. Cable Length

A cable length of less than 10 feet is recommended for drive interfacing.

### 11. Scan Commands

The current 8272 has several problems when using the scan commands. These commands should not be used at this time.

### 12. Interrupts

When the processor receives an interrupt from the FDC, the FDC may be reporting one of two distinct events:

- a) The beginning of the result phase of a previously requested read, write, or scan command.
- b) An asynchronous event such as a seek/recalibrate completion, an attention, an abnormal command termination, or an invalid command.

These two cases are distinguished by the FDC busy flag (bit 4) in the Main Status Register. If the FDC busy flag is high, the interrupt is of type (a). If the FDC busy flag is low, the interrupt was caused by an asynchronous event (b).

A single interrupt from the FDC may signal more than one of the above events. After receiving an interrupt, the processor must continue to issue Sense Interrupt Status commands (and service the resulting conditions) until an invalid command code is received. In this manner, all "hidden" interrupts are ferreted out and serviced.

### 13. Skip Flag (SK)

The skip flag is used during the execution of Read Data, Read Deleted Data, Read Track, and various Scan commands. This flag permits the FDC to skip unwanted sectors on a disk track.

When performing a Read Data, Read Track, or Scan command, a high SK flag indicates that the FDC is to skip over (not transfer) any sector containing a deleted data address mark. A low SK flag indicates that the FDC is to terminate the command (after reading all the data in the sector) when a deleted data address mark is encountered.

When performing a Read Deleted Data command, a high SK flag indicates that sectors containing normal data address marks are to be skipped. Note that this is just the opposite situation from that described in the last paragraph. When a data address mark is encountered during a Read Deleted Data command (and the SK flag

be programmed to be I ms longer than the step rate time

is low), the FDC terminates the command after reading all the data in the sector.

## 14. Bad Track Maintenance

The 8272 does not internally maintain bad track information. The maintenance of this information must be performed by system software. As an example of typical bad track operation, assume that a media test determines that track 31 and track 66 of a given floppy disk are bad. When the disk is formatted for use, the system software formats physical track 0 as logical cylinder 0 (C=0 in the command phase parameters), physical track 1 as logical track 1 (C=1), and so on, until physical track 30 is formatted as logical cylinder 30 (C=30). Physical track 31 is bad and should be formatted as logical cylinder FF (indicating a bad track). Next, physical track 32 is formatted as logical cylinder 31, and so on, until physical track 67 is formatted as logical cylinder 64. Next, bad physical track 66 is formatted as logical cylinder FF (another bad track marker), and physical track 67 is formatted as logical cylinder 65. This formatting continues until the last physical track (77) is formatted as logical cylinder 75. Normally, after this formatting is complete, the bad track information is stored in a prespecified area on the floppy disk (typically in a sector on track 0) so that the system will be able to recreate the bad track information when the disk is removed from the drive and reinserted at some later time.

To illustrate how the system software performs a transfer operation disk with bad tracks, assume that the disk drive head is positioned at track 0 and the disk described above is loaded into the drive. If a command to read track 36 is issued by an application program, the system software translates this read command into a seek to physical track 37 (since there is one bad track between 0 and 36, namely 31) followed by a read of logical cylinder 36. Thus, the cylinder parameter C is set to 37 for the Seek command and 36 for the Read Sector command.

### 15. Head Load versus Head Settle Times

The 8272 does not permit separate specification of the head load time and the head settle time. When the Specify command is issued for a given disk drive, the proper value for the HLT parameter is the maximum of the head load time and the head settle time.

Power Distribution

-12	+12	GND		Ref Decig	Part
		1,20		A2	
		8			224
		20	33	A6	237-2
		4		A9,89,C9	
			24		253-5
		14			259A
				010	272
			81	I A I	284
		10		B6,F4	
				F1,F2,G1,G2,H1,H2,I1,I2	
			24	D1,D2	732A
		7			41,500
		7	14		41,504
		7	14	H2,H5	
			14		41.532
				A4,05,H6	41.374
					41.3138
		8	35		
		8		2	41.5153
			16	66	
		7	14		4LS164
		8			4LS173
		8		64	
		10		010	4LS240
		8	APF	PENDIX	4LS257
				C3,E9	
				B4,C4,D4,C6	41.8373
			14	15,97	
		7	14		4508
				D6,E3	
		7	14		
			14	H8,H9,H10	438
		7		H3	
		7	- 14		
		8	- 16	to l	561,502
				G6	202.190
	8			th i	

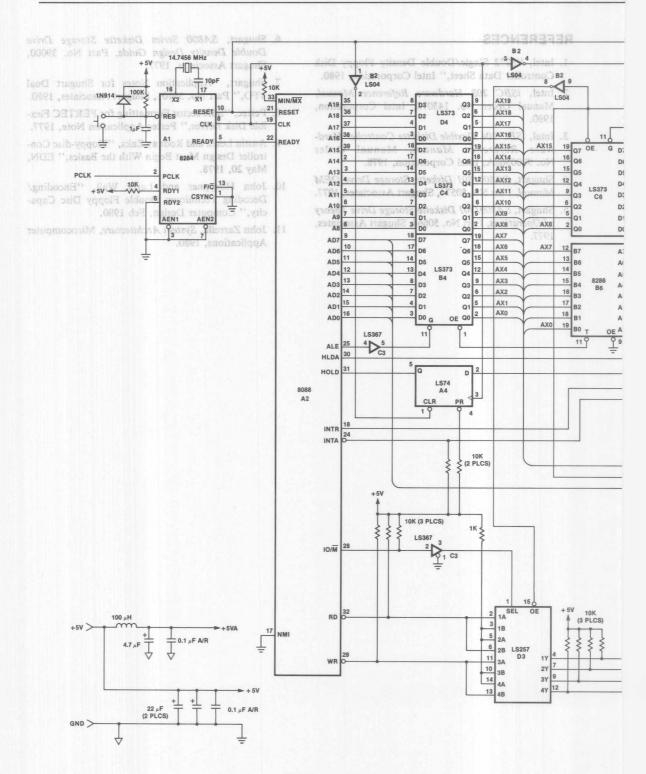
### **Power Distribution**

Part	Ref Desig	+5	GND	+12	-12
8088	A2	40	1,20		
8224	16	9,16	8		
8237-2	A6	31	20		1 111
8251A	A9,B9,C9	26	4		
8253-5	A10	24	12		
8259A	B10	28	14		
8272	D10	40	20		
8284	A1	18	9		1 1 1 1 1
8286	B6,F4	20	10		
2114	F1,F2,G1,G2,H1,H2,I	1,12 18	9		
2732A	D1,D2	24	12		
74LS00	E1	14	7		
74LS04	B2,E6,E8,F8	14	7		
74LS27	E2,E5	14	7		
74LS32	B1	14	7		100
74LS74	A4,G5,H6	14	7		
74LS138	F3	16	8		1 200
74LS139	E10	16	8	1 1 1 1 1 1 1	
74LS153	13	16	8	1000	
74LS157	F6	16	8		
74LS164	F5	14	7		
74LS173	G3	16	8		
74LS175	G4	16	8		1 1 1 1 1 1
74LS240	G10	20	10		1 1 1 1 1 1
74LS257	D3 X1	QM349A16	8		
74LS367	C3,E9	16	8		1 7 1
74LS373	B4,C4,D4,C6	20	10		
74LS393	I5,F7	14	7		
74S08	E4	14	7		
74S138	D6,E3	16	8		83.79
7414	H7	14	7		1 1
7438	H8,H9,H10	14	7		
1488	H3		7	14	1
1489	H4	14	7		
96LS02	G7	16	8	1.	
96LS02	G6			16	8
LM358	H5		La La La Taraca	8	4

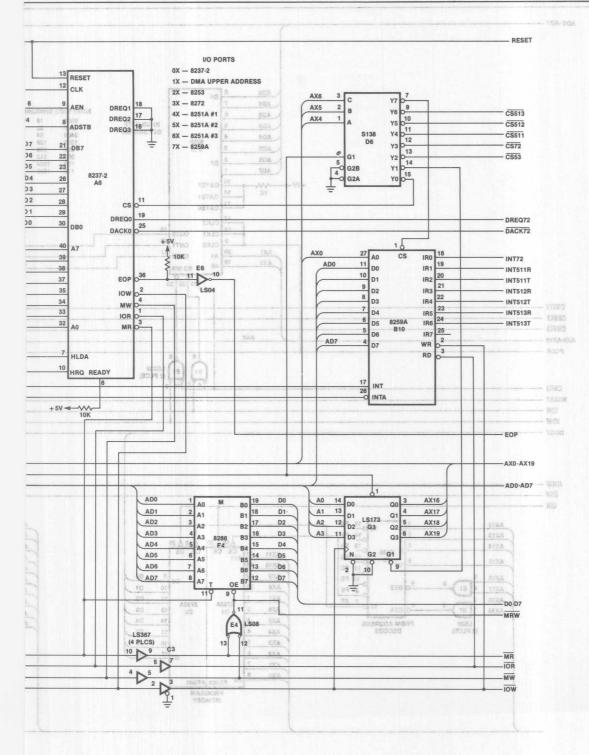
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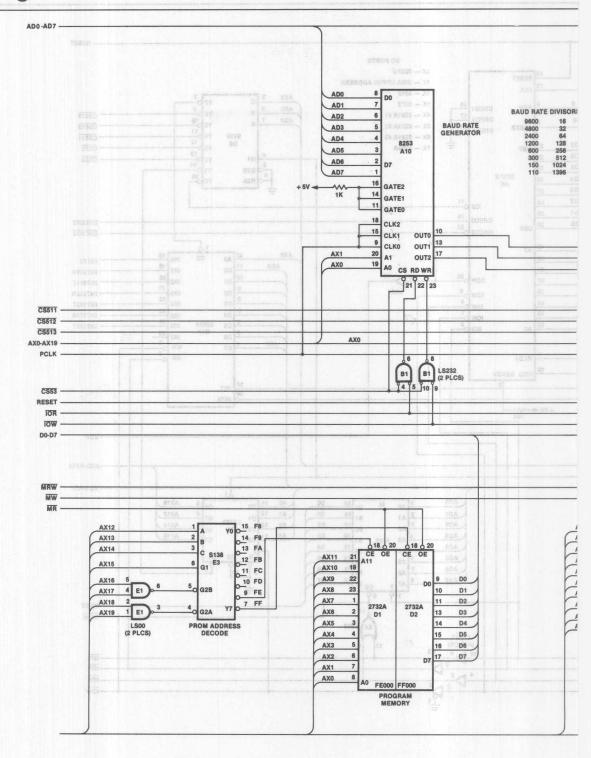
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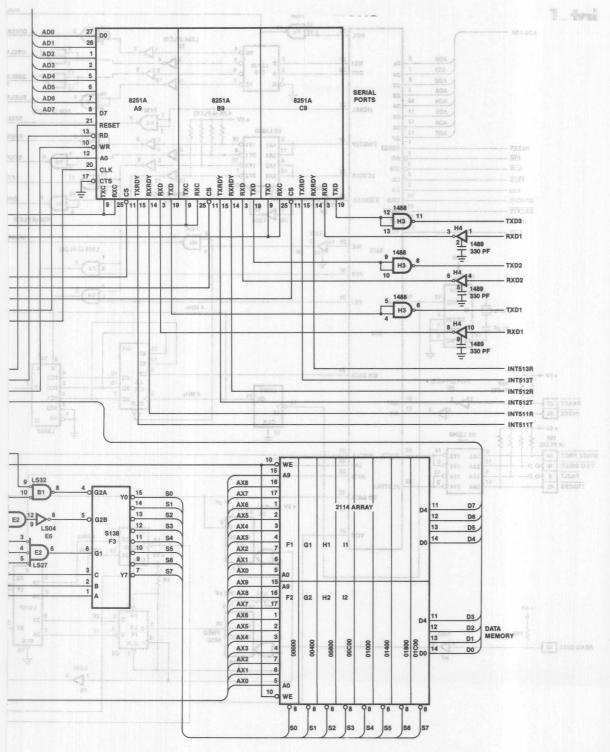


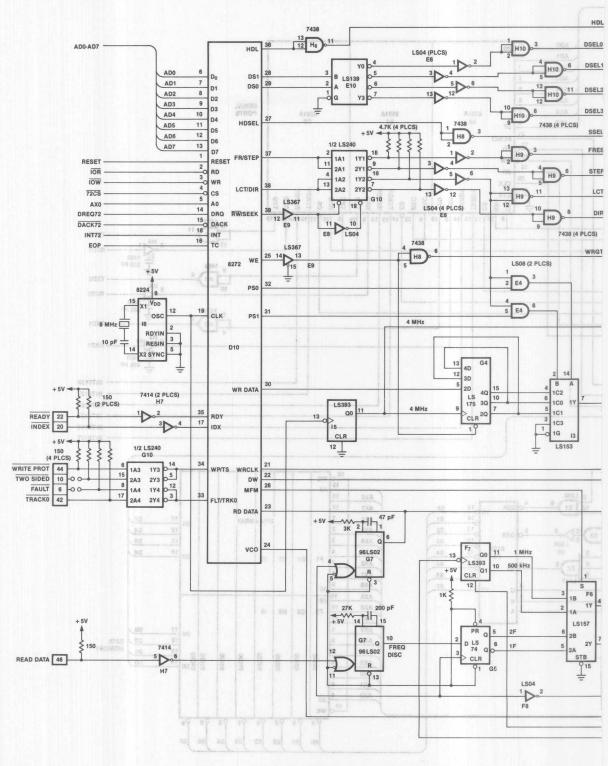


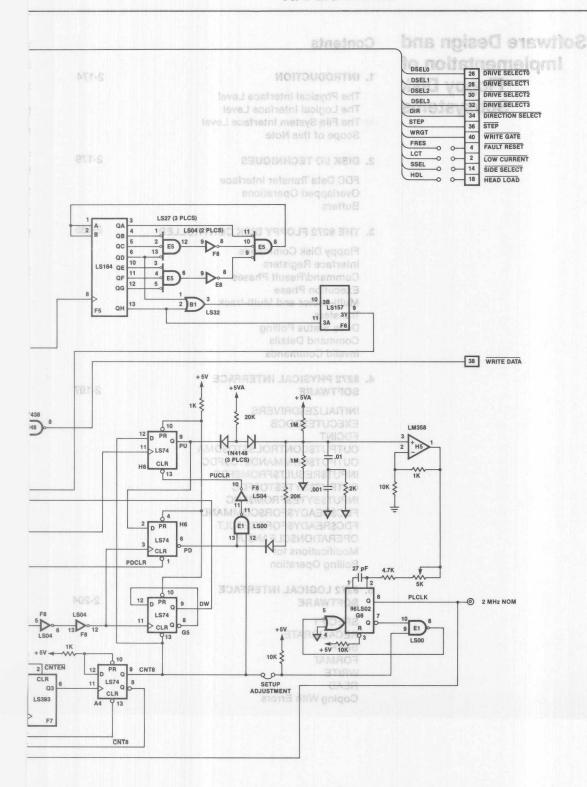












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les.	mand termination) to the requesting modul	
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	idal Interface Level	
sylce. This software incompati-	and application software modules often ap e not directly compatible with the PDC de is typically caused by one of the followi	that are
	1. The change from an existing FDC to design. Replacing a TTL based con an example of a change that may re bilities.	
is-sided, single-density sys-	2. The upgrade of an existing FDC sub- design, An expension from a single tem to a dual-sided, double-densit storage capacity is an example of	

sector) are fixed for a floppy disk (after formatting). In

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## 1. Introduction

Disk interface software is a major contributor to the efficient and reliable operation of a floppy disk subsystem. This software must be a well-designed compromise between the needs of the application software modules and the capabilities of the floppy disk controller (FDC). In an effort to meet these requirements, the implementation of disk interface software is often divided into several levels of abstraction. The purpose of this application note is to define these software interface levels and describe the design and implementation of a modular and flexible software driver for the 8272 FDC. This note is a companion to AP-116, "An Intelligent Data Base System Using the 8272."

APPENDIX A-8272 FOC

## The Physical Interface Level

The software interface level closest to the FDC hardware is referred to as the physical interface level. At this level, interface modules (often called disk drivers or disk handlers) communicate directly with the FDC device. Disk drivers accept floppy disk commands from other software modules, control and monitor the FDC execution of the commands, and finally return operational status information (at command termination) to the requesting modules.

In order to perform these functions, the drivers must support the bit/byte level FDC interface for status and data transfers. In addition, the drivers must field, classify, and service a variety of FDC interrupts.

### The Logical Interface Level

System and application software modules often specify disk operation parameters that are not directly compatible with the FDC device. This software incompatibility is typically caused by one of the following:

- The change from an existing FDC to a functionally equivalent design. Replacing a TTL based controller with an LSI device is an example of a change that may result in software incompatibilities.
- 2. The upgrade of an existing FDC subsystem to a higher capability design. An expansion from a single-sided, single-density system to a dual-sided, double-density system to increase data storage capacity is an example of such a system change.
- 3. The abstraction of the disk software interface to avoid redundancy. Many FDC parameters (in particular the density, gap size, number of sectors per track and number of bytes per sector) are fixed for a floppy disk (after formatting). In fact, in many systems these parameters are never changed during the life of the system.

- 4. The requirement to support a software interface that is independent of the type of disk attached to the system. In this case, a system generated ("logical") disk address (drive, head, cylinder, and sector numbers) must be mapped into a physical floppy disk address. For example, to switch between single-and dual-sided disks, it may be easier and more cost-effective for the software to treat the dual-sided disk as containing twice as many sectors per track (52) rather than as having two sides. With this technique, accesses to sectors 1 through 26 are mapped onto head 0 while accesses to sectors 27 through 52 are mapped onto head 1.
- 5. The necessity of supporting a bad track map. Since bad tracks depend on the disk media, the bad track mapping varies from disk to disk. In general, the system and application software should not be concerned with calculating bad track parameters. Instead, these software modules should refer to cylinders logically (0 through 76). The logical interface level procedures must map these cylinders into physical cylinder positions in order to avoid the bad tracks.

The key to logical interface software design is the mapping of the "logical disk interface" (as seen by the application software) into the "physical disk interface" (as implemented by the floppy disk drivers). This logical to physical mapping is tightly coupled to system software design and the mapping serves to isolate both applications and system software from the peculiarities of the FDC device. Typical logical interface procedures are described in Table 1.

### The File System Interface Level

The file system typically comprises the highest level of disk interface software used by application programs. The file system is designed to treat the disk as a collection of named data areas (known as files). These files are cataloged in the disk directory. File system interface software permits the creation of new files and the deletion of existing files under software control. When a file is created, its name and disk address are entered into the directory; when a file is deleted, its name is removed from the directory. Application software requests the use of a file by executing an OPEN function. Once opened, a file is normally reserved for use by the requesting program or task and the file cannot be reopened by other tasks. When a task no longer needs to use an open file, the task closes the file, releasing it for use by other tasks.

Most file systems also support a set of file attributes that can be specified for each file. File attributes may be used to protect files (e.g., the WRITE PROTECT attribute ensures that an existing file cannot accidentally be overwritten) and to supply system configuration information (e.g., a FORMAT attribute may specify that a file should automatically be created on a new disk when the disk is formatted).

At the file system interface level, application programs need not be explicitly aware of disk storage allocation techniques, block sizes, or file coding strategies. Only a "file name" must be presented in order to open, read or write, and subsequently close a file. Typical file system functions are listed in Table 2.

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Table 1: Examples of Logical Interface Procedures

Name Language	cylinder, and sector numbers) must be mapped into a principle floopy disk address noitqirosed to switch between
FORMAT DISK	
RECALIBRATE	
SEEK STEWNICS REPORT NAME OF STEWNICS AND ST	Moves the disk read/write head to a specified logical cylinder. The logical and physical cylinder numbers may be different if bad track mapping is used.
READ STATUS	Indicates the status of the floppy disk drive and media. One important use of this procedure is to determine whether a floppy disk is dual-sided.
READ SECTOR SECTOR	Reads one or more complete sectors starting at a specified disk address (drive, head, cylinder, and sector).
WRITE SECTOR	Writes one or more complete sectors starting at a specified disk address (drive, head, cylinder, and sector).

The file system typically comprises the highest level of disk interface software used by application programs. The file system is designed to treat the disk as a collection of named data areas (known as files). These files are cataloged in the disk directory. File system interface software permits the creation of new files and the deletion of existing files under software control. When a file is created, its name and disk address are entered into the directory; when a file is deleted, its name is removed from the directory. Application software requests the use of a file by executing an OPHM function. Once opened, a file is normally reserved for use by the requesting program or task and the file cannot be received by other tasks. When a task no longer needs to use an open file, the task closes the file, releasing it for use by other tasks.

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## Table 2: Disk File System Functions

	evels. A complete 8272 driver (including interrupt service software)
lame	isted in Appendix A. In addition, noifqirosed recalibrate, seek, form
OPEN -ixali	Prepare a file for processing. If the file is to be opened for input and the file name is not found in the directory, an error is generated. If the file is opened for output and the file name is not found in the directory, the file is automatically created.
CLOSE	Terminate processing of an open file.
READ	Transfer data from an open file to memory. The READ function is often designed to buffer one or more sectors of data from the disl drive and supply this data to the requesting program, as required.
VRITE	Transfer data from memory to an open file. The WRITE function is often designed to buffer data from the application program until enough data is available to fill a disk sector.
CREATE	Initialize a file and enter its name and attributes into the file directory.
DELETE	Remove a file from the directory and release its storage space.
RENAME	Change the name of a file in the directory.
ATTRIBUTE	Change the attributes of a file.
OAD	Read a file of executable code into memory.
NITDISK	Initialize a disk by formatting the media and establishing the directory file, the bit map file, and other system files.

Table 2: Disk File System Functions

### Scope of this Note

This application note directly addresses the logical and physical in	nterface
levels. A complete 8272 driver (including interrupt service softwalisted in Appendix A. In addition, examples of recalibrate, seek,	format,
read, and write logical interface level procedures are included as the exerciser program found in Appendix B. Wherever possible, spec hardware configuration dependencies are parametized to provide maximility without requiring major software changes.	ific Mago
Terminate processing of an open file.	
Transfer data from no open file to memory. The READ function is often designed to buffer one or more sectors of data from the disk drive and supply this data to the requesting program, as required.	
Transfer data from memory to an open file. The WRITE function is often designed to buffer data from the application program until enough data is available to fill a disk sector.	WRITE
Initialize a file and enter its name and attributes into the file directory.	
	araued
Change the name of a file in the directory.	
Change the attributes of a file.	ATTRIBUTS
Read a file of executable code into memory.	CAOL
Initialize a disk by formatting the media and establishing the directory file, the bit map file, and other system files.	IMITDISK

### permand of me 2. Disk I/O Techniques

One of the most important software aspects of disk interfacing is the fixed sector size. (Sector sizes are fixed when the disk is formatted.) Individual bytes of disk storage cannot be read/written; instead, complete sectors must be transferred between the floppy disk and system memory.

Selection of the appropriate sector size involves a tradeoff between memory size, disk storage efficiency, and disk transfer efficiency. Basically, the following factors must be weighed:

- 1. Memory size. The larger the sector size, the larger the memory area that must be reserved for use during disk I/O transfers. For example, a lK byte disk sector size requires that at least one lK memory block be reserved for disk I/O.
- 2. Disk Storage efficiency. Both very large and very small sectors can waste disk storage space as follows. In disk file systems, space must be allocated somewhere on the disk to link the sectors of each file together. If most files are composed of many small sectors, a large amount of linkage overhead information is required. At the other extreme, when most files are smaller than a single disk sector, a large amount of space is wasted at the end of each sector.
- Disk transfer efficiency. A file composed of a few large sectors can be transferred to/from memory more efficiently (faster and with less overhead) than a file composed of many small sectors.

Balancing these considerations requires knowledge of the intended system applications. Typically, for general purpose systems, sector sizes from 128 bytes to 1K bytes are used. For compatibility between single-density and double-density recording with the 8272 floppy disk controller, 256 byte sectors or 512 byte sectors are most useful.

# FDC Data Transfer Interface bed smeleys east at .loog relied a more bedacolls

Three distinct software interface techniques may be used to interface system memory to the FDC device during sector data transfers:

- DMA In a DMA implementation, the software is only required to set up the DMA controller memory address and transfer count, and to initiate the data transfer. The DMA controller hardware handshakes with the processor/system bus in order to perform each data transfer.
- 2. Interrupt Driven The FDC generates an interrupt when a data byte is ready to be transferred to memory, or when a data byte is needed from memory. It is the software's responsibility to perform appropriate memory reads/writes in order to transfer data from/to the FDC upon receipt of the interrupt.
- 3. Polling Software responsibilities in the polling mode are identical to the responsibilities in the interrupt driven mode. The polling mode, however, is used when interrupt service overhead (context switching) is too large to support the disk data

rate. In this mode, the software determines when to transfer data by continually polling a data request status flag in the notes be FDC status register. I wait to stoogs elevates transfer and add to end to

The DMA mode has the advantage of permitting the processor to continue executing instructions while a disk transfer is in progress. (This capability is especially useful in multiprogramming environments when the operating system is designed to permit other tasks to execute while a program is waiting for I/O.) Modes 2 and 3 are often combined and described as non-DMA operating modes. Non-DMA modes have the advantage of significantly lower system cost, but are often performance limited for double-density systems (where data bytes must be transferred to/from the FDC every 16 microseconds).

For example, a 1% byte disk sector size requires that at least

### Overlapped Operations

Some FDC devices support simultaneous disk operations on more than one disk drive. Normally seek and recalibrate operations can be overlapped in this manner. Since seek operations on most floppy drives are extremely slow, this mode of operation can often be used by the system software to reduce overall disk access times.

#### Buffers

The buffer concept is an extremely important element in advanced disk I/O strategies. A buffer is nothing more than a memory area containing the same amount of data as a disk sector contains. Generally, when an application program requests data from a disk, the system software allocates a buffer (memory area) and transfers the data from the appropriate disk sector into the buffer. The address of the buffer is then returned to the application software. In the same manner, after the application program has filled a buffer for output, the buffer address is passed to the system software, which writes data from the buffer into a disk sector. In multitasking systems, multiple buffers may be allocated from a buffer pool. In these systems, the disk controller is often requested to read ahead and fill additional data buffers while the application software is processing a previous buffer. Using this technique, system software attempts to fill buffers before they are needed by the application programs, thereby eliminating program waits during I/O transfers. Figure 1 illustrates the use of multiple buffers in a ring configuration.

to set up the DMA controller memory address and transfer count, and to initiate the data transfer. The DMA controller hardware handshakes with the processor/system bus in order to perform each data transfer.

Interrupt Driven - The FDC generates an interrupt when a data byte is ready to be transferred to memory, or when a data byte is needed from memory. It is the software's responsibility to perform appropriate memory reads/writes in order to transfer data from/to the FDC upon receipt of the interrupt.

Polling - Software responsibilities in the polling mode are identical to the responsibilities in the interrupt driven mode. The polling mode, however, is used when interrupt service overhead (context switching) is too large to support the disk data

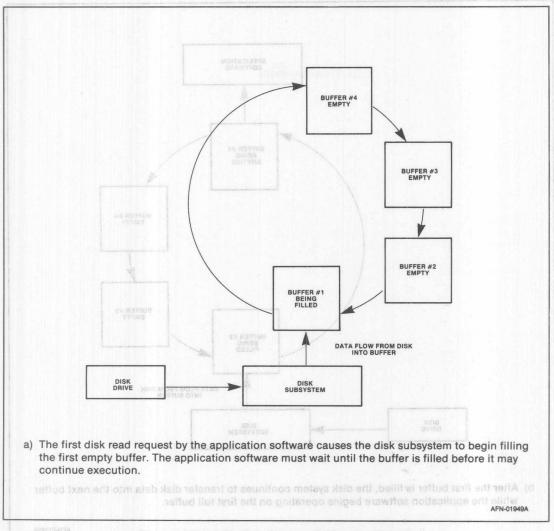


Figure 1. Using Multiple Memory Buffers for Disk I/O

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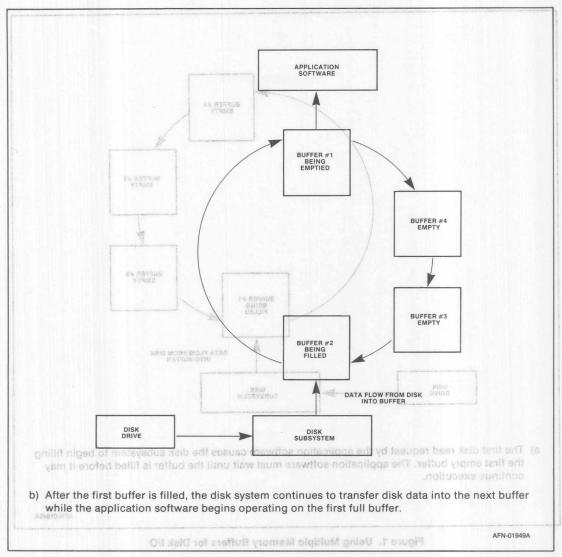
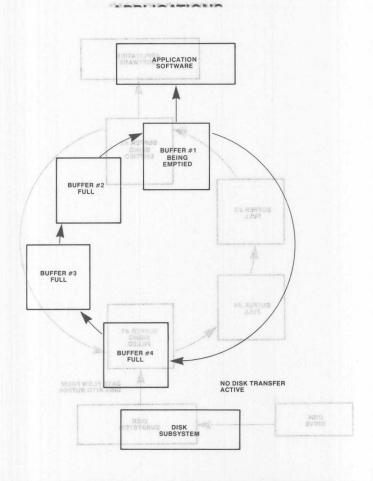


Figure 1. Using Multiple Memory Buffers for Disk I/O (Continued)



c) When all empty buffers have been filled, disk activity is stopped until the application software sector read to reflet the buffer. This strategy attempt, each to minimize data transfer delays. If maintaining a sufficient number of full data buffers in order to minimize data transfer delays. If ARM-1014 at a life of the application software requests it, no disk transfer delays.

Figure 1. Using Multiple Memory Buffers for Disk I/O (Continued)

Figure 1. Using Multiple Memory Buffers for Disk I/O (Continued)

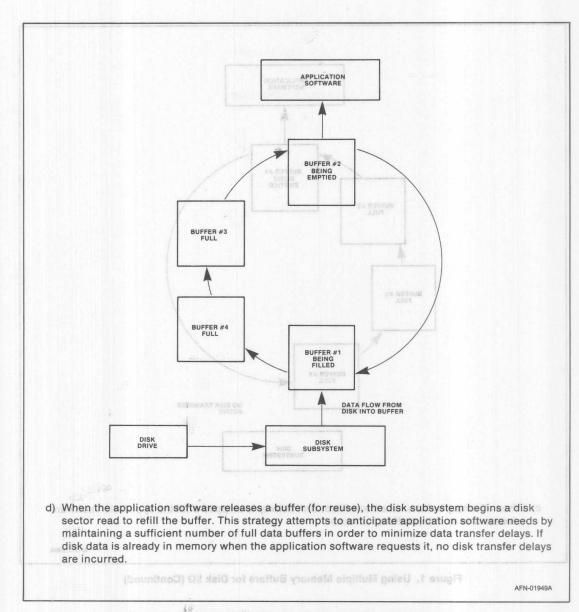


Figure 1. Using Multiple Memory Buffers for Disk I/O (Continued)

Interface Registers

### 3. THE 8272 FLOPPY DISK CONTROLLER

The 8272 is a single-chip LSI Floppy Disk Controller (FDC) that implements both single- and double-density floppy disk storage subsystems (with up to four dual-sided disk drives per FDC). The 8272 supports the IBM 3740 single-density recording format (FM) and the IBM System 34 double-density recording format (MFM). The 8272 accepts and executes high-level disk commands such as format track, seek, read sector, and write sector. All data synchronization and error checking is automatically performed by the FDC to ensure reliable data storage and subsequent retrieval. The 8272 interfaces to microprocessor systems with or without Direct Memory Access (DMA) capabilities and also interfaces to a large number of commercially available floppy disk drives.

## status registera (STO, STI, ST2, and ST3). These registers are only available fluring the result phase of a command

The 8272 executes fifteen high-level disk interface commands:

	STATE OF THE PARTY
Specify	Write Data
Sense Drive Status	Write Deleted Data goo cycs ont stall A e
Sense Interrupt Status	
Seek regult status regis ses	
Recalibrate	Scan Equal elder ni berstraulli ers (ETR-
Format Track	Scan High or Equal
Read Data - nation avoid and	Scan Low or Equal and do idw atab to setted
Read Deleted Data	se, and are read out of the 8272 in the resu

In addition to the Main Status Register, the FDC contains four additional

Each command is initiated by a multi-byte transfer from the driver software to the FDC (the transferred bytes contain command and parameter information).

After complete command specification, the FDC automatically executes the command. The command result data (after execution of the command) may require a multi-byte transfer of status information back to the driver. It is convenient to consider each FDC command as consisting of the following three phases:

Command Phase:	The driver transfers to the FDC all the information
	required to perform a particular disk operation. The
sfully complete	0070
until all seven	DECEMBER and Callering the second of the second
	phase (if any) of a previous command.

Execution Phase: The FDC performs the operation as instructed. The execution phase is entered immediately after the last command parameter is written to the FDC in the preceding command phase. The execution phase normally ends when the last data byte is transferred to/from the disk or when an error occurs.

Result Phase: After completion of the disk operation, status and other housekeeping information are made available to the driver software. After this information is read, the FDC reenters the command phase and is ready to accept another command.

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## 

To support information transfer between the FDC and the system software, the 8272 contains two 8-bit registers: the Main Status Register and the Data Register. The Main Status Register (read only) contains FDC status information and may be accessed at any time. The Main Status Register (Table 3) provides the system processor with the status of each disk drive, the status of the FDC, and the status of the processor interface. The Data Register (read/write) stores data, commands, parameters, and disk drive status information. The Data Register is used to program the FDC during the command phase and to obtain result information after completion of FDC operations.

In addition to the Main Status Register, the FDC contains four additional status registers (ST0, ST1, ST2, and ST3). These registers are only available during the result phase of a command.

### Command/Result Phases

Table 4 lists the 8272 command set. For each of the fifteen commands, command and result phase data transfers are listed. A list of abbreviations used in the table is given in Table 5, and the contents of the result status registers (STO-ST3) are illustrated in Table 6.

The bytes of data which are sent to the 8272 by the drivers during the command phase, and are read out of the 8272 in the result phase, must occur in the order shown in Table 4. That is, the command code must be sent first and the other bytes sent in the prescribed sequence. All bytes of the command and result phases must be read/written as described. After the last byte of data in the command phase is sent to the 8272 the execution phase automatically starts. In a similar fashion, when the last byte of data is read from the 8272 in the result phase, the result phase is automatically ended and the 8272 reenters the command phase.

It is important to note that during the result phase all bytes shown in Table 4 must be read. The Read Data command, for example, has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data command. The 8272 will not accept a new command until all seven bytes have been read. The number of command and result bytes varies from command-to-command.

In order to read data from, or write data to, the Data Register during the command and result phases, the software driver must examine the Main Status Register to determine if the Data Register is available. The DIO (bit 6) and RQM (bit 7) flags in the Main Status Register must be low and high, respectively, before each byte of the command word may be written into the 8272. Many of the commands require multiple bytes, and as a result, the Main Status Register must be read prior to each byte transfer to the 8272. To read status bytes during the result phase, DIO and RQM in the Main Status Register must both be high. Note, checking the Main Status Register in this manner before each byte transfer to/from the 8272 is required only in the command and result phases, and is NOT required during the execution phase.

Table 3: Main Status Register Bit Definitions

		ans arad 2 299 arad 1	
BIT	SYMBOL	MOARIA GASA	
NUMBER	1 0 Commit	N ACT MEN SK 0 0 1 1 G Command Codes Command W 0 MEN SK 0 0 0 0	Command
Distriction Comments	D <sub>0</sub> B	Disk Drive O Busy. Disk Drive O is seeking.	
1	D <sub>1</sub> B	Disk Drive 1 Busy. Disk Drive 1 is seeking.	
nater 2 o the FDD moin-system.	D <sub>2</sub> B	Disk Drive 2 Busy. Disk Drive 2 is seeking.	
3 onl abd	D <sub>3</sub> B	Disk Drive 3 Busy. Disk Drive 3 is seeking.	
4 TO3		FDC Busy. A read or write command is in progress.	
5 no		Non-DMA Mode. The FDC is in the non-DMA mode when this fla set (1). This flag is set only during the execution phase commands in the non-DMA mode. Transition of this flag to a zero (0) indicates that the execution phase has ended.	of
Of takenos to	majai	Data Input/Output. Indicates the direction of a data trans between the FDC and the Data Register. When DIO is set (1) is read from the Data Register by the processor; when DIO reset (0), data is written from the processor to the Data R	, data is
	Section ROM	Request for Master. When set (1), this flag indicates that the Data Register is ready to send data to, or receive data from, the processor.	

| March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | March | Marc

## Table 4: 8272 Command Set

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS	PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0 REMARKS
THE C		READ DATA	(10)	1117100	114	READ A TRACK
Command	w	MT MFM SK 0 0 1 1 0	Command Codes	Command	w	0 MFM SK 0 0 0 1 0 Command Codes
Communic	W	0 0 0 0 0 HDS DS1 DS0			W	0 0 0 0 0 HDS DS1 DS0
	w	C nations	Sector ID information	Vaid	W	Sector ID informatio
	W	H	prior to Command	D. CO. A. A.	W	H prior to Command
	W	R	execution		W	R execution
	W	EOT BOT STATES	Drive I is	Disk	W	1 D B DI TOS CIVE LEG
	W	GPL			W	GPL
	W	DTL			W	DTL
Execution		seeking.	Data transfer	laid.	ya!	Data transfer S
			between the FDD	Execution		between the FDD and the main-system
			and the main-system	5.00		EDC reads the
Result	R	seeking. ors	Status information	Disk	Yat	complete track
	R	ST 1	after Command	100		contents from the
	R	ST 2	execution -	or wri	bes	physical index mark to EOT
	R	Н	Sector ID information			
	R	R	after command	Result	R	ST 0 Status information
1.5	R	- Bidd godN - show ANG-	execution	DOT !	R	ST 1 after Command execution
		READ DELETED DATA	bruh vido to	a al p	R	o fultil C 4 co
Command	W	MT MFM SK 0 1 1 0 0	Command Codes		H	
	w	0 0 0 0 0 HDS DS1 DS0	EDELL . BOOM	AMCI-m	R	R after Command execution
	w	n phase has ended.	Sector ID information	3553	2033	401b01 (0) 0368
	W	Н	prior to Command			READ ID
	W	R NIO	execution	Command	W	0 MFM 0 0 1 0 1 0 Command Codes
	W	EC 1	cates the di	Indi.	W	0 0 0 0 0 HDS DS1 DS0
	W	JBB BL GPL DADW	Data Registe	ed the		between the FDC
	W	e processell, when b	dister by th	Execution		The first correct ID information on the
Execution	Re	processor to the Data	Data transfer			
	2771 1	processor to the nati	between the FDD	dinw a	EL E	Data Register
			and the main-system			
Result	R	STO STI	Status information	Result	R	ST 0 Status information after Command
	R	ST 1 ST 2	after Command execution		R	ST 2 execution
	R	C	execution	is rea	R	- er fau bapec and
	R	H	Sector ID information	. 30	R	H Sector ID information
	R		after Command execution		R	R during Execution Phase
	n	NN	execution		- 1.5	FORMAT A TRACK
		WRITE DATA				
Command	W	MT MFM 0 0 0 1 0 1	Command Codes	Command	W	0 MFM 0 0 1 1 0 1 Command Codes
	W	0 0 0 0 0 HDS DS1 DS0			W	0 0 0 0 HDS DS1 DS0
	W	C	Sector ID information prior to Command		W	N Bytes/Sector Sectors/Track
	W	R	execution		W	GPL Gap 3
	W	N			W	D Filter Byte
	W	EOT		Execution		FDC formats an
	w	DTL		Excodition		entire track
Execution			Data transfer			
Execution			between the main-	Result	R	ST 0 Status information after Command
			system and the FDD		R	ST 1 after Command execution
Result	R	ST 0	Status information		R	C
	R	ST 1ST 2	after Command		R	H In this case, the ID
	R	ST 2	execution		R	R information has no meaning
	R	C	Sector ID information			
	R	R	after Command			SCAN EQUAL
	R	N	execution	Command	W	MT MFM SK 1 0 0 0 1 Command Codes
		WRITE DELETED DATA			W	0 0 0 0 0 HDS DS1 DS0
Command	W	MT MFM 0 0 1 0 0 1	Command Codes		W	C Sector ID information
	w	0 0 0 0 0 HDS DS1 DS0	oonmand oodoo		W	H prior to Command execution
2-1	w	C	Sector ID information		W	R execution
THE PERSON	W	н	prior to Command		W	EOT
	W	R	execution		W	GPL
Dark Tolk	W	N EOT			VV	STP
	W	GPL		Execution		Data compared
Execution	W	DTL	Data transfer			between the FDD and the main-system
	His		between the FDD	Result	R	ST 0 Status information
	100		and the main-system		R	ST1   after Command
Result	R	ST 0	Status information	1018	R	ST 2 execution
	R	ST 1	after Command		R	C Sector ID information
	R	ST 2	execution		R	R after Command
		C	Sector ID information		R	N execution
	R					
	RRR	R	after Command execution			

Note: 1.  $A_0 = 1$  for all operations.

PHASE		DATA BUS	an assishbab		12.23	DATA BUS	
	R/W	D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	REMARKS	PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0 REMARK	(S
		SCAN LOW OR EQUAL				RECALIBRATE	
Command	W	MT MFM SK 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Command Codes	Command	w	0 0 0 0 0 1 1 1 1 Commar	d Codes
no	W	OJ 0) 885 HOS TODALLY	Sector ID information prior Command	Execution	65		racted to
	W	R	execution			SENSE INTERRUPT STATUS	
	W	EOT		Command	w	0 0 0 0 1 0 0 0 Commar	d Codes
inzing	W	GPL STP DOB dose	written in	Result	R	ST0 Status in	formation a
Execution			Data compared between the FDD and the main-system			SPECIFY Operation	about the
Result	R R	ST 0 ST 1	Status information after Command	Command	W	0 0 0 0 0 0 1 1 Comman	d Codes
	R	ST 2	execution		W	SPT HUT Timer Se	ttings
	R	Н	Sector ID information		-	SENSE DRIVE STATUS	
	R	R	after Command execution	Command	w		10.1
	n		execution	Command	W	0 0 0 0 0 1 0 0 Comman	d Codes
Command	W	SCAN HIGH OR EQUAL  MT MFM SK 1 1 1 0 1	Command Codes	Result	R	Status in	formation
	W	0 0 0 0 0 HDS DS1 DS0				SEEK about the	e FUU
, abe	W	OD STIWACC CO	Sector ID information prior Command	Command	W	0 0 0 0 1 1 1 1 Comman	d Codes
20	W	the effec Rive disk s	execution	tempo	w	0 0 0 0 0 HDS DS1 DS0	
98	W	EOT	may be use	ro, or	92	size. By setting N to	
	W	alb and outp rodoca (a	of the actu	Execution	o Le	Head is p	ositioned per Cylinder
Execution		of the actual sector	Data compared	des. t	110	on Diske	
197	9 4	Suring write commands	between the FDD	set on	i vei		
- 27		ith all-veroes bytes.	and the main-system	Command	W	Invalid Codes Invalid C	ommand
Result	R R R	ST0 ST1 ST2 C	Status information after Command execution	f smitog	B R	Codes (N	oOp — FDC Standby
	R R	NOSXIHILOSYUD SI	Sector ID information after Command execution	sector			(16)
		side 0 or 1, respect	deib) I to 0	:bse			
		that the FDC walts at	Isvisini en	ID fie		Head Address. Selects as ancoded in the sect Head Load Time. Defin	
		r write operation, Peats of 2 ms);	ne interval ing a read o s (in increm	ID fie the th pitiat second		as ancoded in the sect Head Load Time. Defin loading the head befor mable from 2 to 254 mi	
		r write operation. Pents of 2 ms].  I from the and of the ntil the head is unlo	me interval ing a read o a (in increm time interva e command) u	ID fie the the chicate		as andoded in the sect Head Load Time. Defin	
		r write operation. Pents of 2 ms].  1 from the and of the ntil the head is unlo n increments of 16 ms ensity recording mode	ne interval ing a read o s (in increm time interva e command) u liseconds (i MEN double-d en low.	ID fie the the chicac chicac specond on the chicac	tor test test (LLL) (LLL) sal co sal co sal co	as ancoded in the sect Head Load Time. Defin loading the head befor mable from 2 to 254 mi Head Unload Time. Defi oution phase (of a real programmable from 15 to high, FM Mode Selector.	
		r write operation. Pents of 2 ms).  1 from the end of the ntil the head is unlo n increments of 15 ms ensity recording mode the dual-sided disks).  For operates as if the under head 0 and ender the first sector to the first se	ne interval ing a read o s (in increm time interva liseconds (i liseconds (i en low. this flag der (under b der (under b irst sector this flag this flag int sector ly continue	ID file the thi column second in writ in writ the mil rede wh rede wh rede wh rede wh rede wh rede wh the	tor the state of t	es encoded in the sect  Head Load Time. Defin  loading the head befor  mable from 2 to 254 mi  Bead Unload Time. Defin  oution phase (of a real  programmable from 16 to  high, FM Mode Selector.  high, FM single-densit  operating mode. In the  the FDC treats a compl  read/write head 1) as  expanded track started  last sector under head  read coverting will as	
		r write operation. Pents of 2 ms).  1 from the end of the ntil the head is unlo n increments of 15 ms ensity recording mode the dual-sided disks).  For operates as if the under head 0 and ende to the first sector under the first sector under head sector to the first sector under the sector under the first sector under t	ne interval ing a read o s (in increm time interva liseconds (i liseconds (i min double—d en low. this flag der (under b irst sector this flag this flag s this flag s irst sector ly continue scating on t	ID fie the the case of the cas	toring the same of	as ancoded in the section dead Load Time. Defin loading the bead before mable from 2 to 254 md oution phase (of a read union phase (of a read programmable from 15 to high, FM Mode Selector.  Multi-Track Selector.  Auglti-Track Selector.	

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Table 5: Command/Result Parameter Abbreviations

SYMBOL	DESCRIPTION W bosonness season breaming / 6 0 / 1 XE MHM TM W bosonness
C Of helpsyer b	Cylinder Address. The currently selected cylinder address (0 to 76) on the disk.
sets O brand	
us information d	Data Pattern. The pattern to be written in each sector data field during
ation shoul line	offormatting. Designed stand Office and Designed Office and Design
DS0,DS1	Disk Drive Select.  W mammod mountmantar Disk Disk Drive Select.
er Settlings	M DS1 DS0 W GGINGONG STR
	0 JAN 0 JAN 0 Prive 0
mand Codes	command with the control of the cont
	080 1 0 0 Drive 2 W
tus Information out the FOD	to 1 1 Drive 3 Blood Engineer 1 0 F r M2 M464 TM W Disministra
Transport Control of C	Special Sector Size. During the execution of disk read/write commands, this parameter is used to temporarily alter the effective disk sector size. By setting N to zero, DTL may be used to specify a sector size from 1 to 256 bytes in length. If the actual sector (on the disk) is larger than DTL specifies, the remainder of the actual sector is not passed to the system during read commands; during write commands, the remainder of the actual sector is written with all-zeroes bytes. DTL should be set to FF hexadecimal when N is not zero.
EOT	End of Track. The final sector number of the current track.
GPL	Gap Length. The gap 3 size. (Gap 3 is the space between sectors.)
н	Head Address. Selected head: 0 or 1 (disk side 0 or 1, respectively) as encoded in the sector ID field.
HLT	Head Load Time. Defines the time interval that the FDC waits after loading the head before initiating a read or write operation. Programmable from 2 to 254 milliseconds (in increments of 2 ms).
нит	Head Unload Time. Defines the time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Programmable from 16 to 240 milliseconds (in increments of 16 ms).
MFM	MFM/FM Mode Selector. Selects MFM double-density recording mode when high, FM single-density mode when low.
MT	Multi-Track Selector. When set, this flag selects the multi-track operating mode. In this mode (used only with dual-sided disks), the FDC treats a complete cylinder (under both read/write head 0 and read/write head 1) as a single track. The FDC operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set (high), a multi-sector read operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.

ND	Non-DMA Mode Flag. When set (1), this flag indicates that the FDC
IND	is to operate in the non-DMA mode. In this mode, the processor
	participates in each data transfer (by means of an interrupt or by
	polling the RQM flag in the Main Status Register). When reset (0),
	the FDC interfaces to a DMA controller. 30
	REM
R	Sector Address. Specifies the sector number to be read or written. In
	multi-sector transfers, this parameter specifies the sector number of
	the first sector to be read or written.
agy br	00 - Wormen termination of command. The specified comman
SC	Number of Sectors per Track. Specifies the number of sectors per track
	to be initialized by the Format Track command.
0.60	01 - Abnormal termination of command. Command execution
SK	Skip Flag. When this flag is set, sectors containing deleted data
	address marks will automatically be skipped during the execution of
e execut	· Andrew Committee Committ
	containing a data address mark will automatically be skipped during
e disk	the execution of a multi-sector Read Deleted Data command.
	drive ready signal changed state.
SRT	Step Rate Interval. Defines the time interval between step pulses
ed the	issued by the FDC (track-to-track access time). Programmable from
end	1 to 16 milliseconds (in increments of 1 ms).
	correct cylinder.
STO	Status Register 0-3. Registers within the FDC that store status infor-
STL	mation after a command has been executed. This status information is
ST2	available to the processor during the Result Phase after command exe-
ST3	cution. These registers may only be read after a command has been
	executed (in the exact order shown in Table 4 for each command).
	These registers should not be confused with the Main Status Register.
i herem	NR Not Ready Error, This flag is set if a read or write or
	Scan Sector Increment. During Scan operations, this parameter is
Prenada	added to the current sector number in order to determine the next
	sector to be scanned.

Status Recister 1

TIE NESKU	SYMBOL	DESCRIPTION
		End of Track Error. This flag is set if the FDC attempts to access a sector beyond the final sector of the track.
		Undefined
		Data Error. Set when the FDC detects a CRC error in either the the ID field or the data field of a sector.
b		Overrum Error. Set (during data transfers) if the FDC does not receive DMA or processor service within the specified time interval.

DSI,DSO Drive Select. The number of the drive selected at the time of

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the interrupt.

Table 6: Status Register Definitions

BIT NUMBER	SYMBOL	DESCRIPTION OF AMOR OF RESCRIPTION OF AMOR OF RESCRIPTION OF AMOR OF RESCRIPTION OF AMORE OF AMO
7,6	IC 101	Interrupt Code. 200000184 8165 839186833 303398-13100
	tec siotoe	00 - Normal termination of command. The specified command was properly executed and completed without error.
		01 - Abnormal termination of command. Command execution was started but could not be successfully completed.
	anner, a se	10 - Invalid command. The requested command could not be executed
	1	11 - Abnormal termination. During command execution, the disk drive ready signal changed state.
5	SE Identification	Seek End. This flag is set (1) when the FDC has completed the Seek command and the read/write head is positioned over the correct cylinder.
4 21	rol EC nothi	Equipment Check Error. This flag is set (1) if a fault signal
	r command e nd has been command). ntus Registe	is received from the disk drive or if the track 0 signal is not received from the disk drive after 77 step pulses (Recalibrate command).
3	NR si issensi sensi sensi	Not Ready Error. This flag is set if a read or write command is issued and either the drive is not ready or the command specifies side 1 (head 1) of a single-sided disk.
2	н	Head Address. The head address at the time of the interrupt.
1,0	DS1,DS0	Drive Select. The number of the drive selected at the time of the interrupt.
Statu	ıs Register	1
BIT NUMBER	SYMBOL	DESCRIPTION
7	EN	End of Track Error. This flag is set if the FDC attempts to access a sector beyond the final sector of the track.
6		Undefined
5	DE	Data Error. Set when the FDC detects a CRC error in either the the ID field or the data field of a sector.
4	OR	Overrun Error. Set (during data transfers) if the FDC does not receive DMA or processor service within the specified time interval.

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3 disk	s from the	1 BC Had Track Error, Set when the cyl benifebnUca
		sector ID field is FF hexadecimal and this cyl
	ND	
ad track	cates a b	ing conditions. Typ "agno" [[s shir . Dur ed]
sectored	IBM soft-	(one containing hard errors) according to the
		a) The FDC cannot locate the sector specified in the Read Data, Read Deleted Data, or Scan command.
doctor	DC cannot	b) The FDC cannot locate the starting sector specified in
		the Read Track command.
1779018	DHO HO AL	c) The FDC cannot read the ID field without error during
		a Read ID command.
1	NW	Write Protect Error. This flag is set if the FDC detects a write protect signal from the disk drive during the execution of a Write Data, Write Deleted Data, or Format Track command.
0	MA	Missing Address Mark Error. This flag is set by either of the
mal from	fault sign	
		the selected disk drive.
		a) The FDC cannot detect the ID address mark on the specified
write	us of the	track (after two rotations of the disk).
		b) The FDC cannot detect the data address mark or deleted data
		address mark on the specified track. (See also the MD bit
mora fam	ready sig	edd of Status Register 2.); paid aidt .voseA - ycg
		arish with hatrafan old

BIT	SYMBOL	from the selected disk drive. DESCRIPTION		
NUMBER	the two-sid	Two-Sided. This flag indicates the status of		
7		signal from the selected disk drive.  Denifebru		
select	of the side	Control Mark. This flag is set when the FDC enco	ounters of	ne of
	d disk driv	a) A deleted data address mark during the executi Data or Scan command.	on of a l	Read
		b) A data address mark during the execution of a Data command.	Read Dele	eted
5	DD	Data Error. Set (1) when the FDC detects a CRC e sector data field. This flag is not set when a C detected in the ID field.		
4	WC	Cylinder Address Error. Set when the cylinder address from the disk sector ID field is different from the current cylinder address maintained within the FDC.		
3	SH	Scan Hit. Set during the execution of the Scan command if the scan condition is satisfied.		
2	SN	Scan Not Satisfied. Set during execution of the if the FDC cannot locate a sector on the specifie that satisfies the scan condition.		

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1	BC	Bad Track Error. Set when the cylinder address from the disk
ollow-	any of the f	sector ID field is FF hexadecimal and this cylinder address is
		the FDC. This all "ones" cylinder number indicates a bad trac
	in the Rest	(one containing hard errors) according to the IBM soft-sectors format specifications.
0	L bmplipega	Missing Data Address Mark Error. Set if the FDC cannot detect
·	crox during	a data address mark or deleted data address mark on the speci- fied track.
Statu	ıs Register	WW Write Protect Error. This flag is set if the
BIT	SYMBOL	of a Write Data, Writnortanacata, or Porma
NUMBER		
7	FT	Fault. This flag indicates the status of the fault signal from
	on the spec	the selected disk drive.
6	WP	Write Protected. This flag indicates the status of the write
adab l	k or deleted	protect signal from the selected disk drive.
	RDY	
5	RDI	Ready. This flag indicates the status of the ready signal from the selected disk drive.
		the selected disk drive.
4	TO	
4	т0	the selected disk drive.  Track 0. This flag indicates the status of the track 0 signal from the selected disk drive.
		the selected disk drive.  Track 0. This flag indicates the status of the track 0 signal from the selected disk drive.  Two-Sided. This flag indicates the status of the two-sided signal from the selected disk drive.
4	TO TS	Track 0. This flag indicates the status of the track 0 signal from the selected disk drive.  Two-Sided. This flag indicates the status of the two-sided signal from the selected disk drive.  Head Address. This flag indicates the status of the side selected disk drive.
3	TO TS H Bredneone	Track 0. This flag indicates the status of the track 0 signal from the selected disk drive.  Two-Sided. This flag indicates the status of the two-sided signal from the selected disk drive.  Head Address. This flag indicates the status of the side selected for the currently selected disk drive.
3 2 1,0 5,592	TS  H  DS1,DS0	Track 0. This flag indicates the status of the track 0 signal from the selected disk drive.  Two-Sided. This flag indicates the status of the two-sided signal from the selected disk drive.  Head Address. This flag indicates the status of the side selected for the currently selected disk drive.  Drive Select. Indicates the currently selected disk drive number.
3 2 1,0 5,000	TS  H  DS1,DS0	Track 0. This flag indicates the status of the track 0 signal from the selected disk drive.  Two-Sided. This flag indicates the status of the two-sided signal from the selected disk drive.  Head Address. This flag indicates the status of the side selected for the currently selected disk drive.  Drive Select. Indicates the currently selected disk drive number.
4 3 2 1,0 5,0 5,0 5,0 5,0 5,0 5,0 5,0 5,0 5,0 5	TS  H encounters  OSI,ISG cution of a	Track 0. This flag indicates the status of the track 0 signal from the selected disk drive.  Two-Sided. This flag indicates the status of the two-sided signal from the selected disk drive.  Head Address. This flag indicates the status of the side selected for the currently selected disk drive.  Drive Select. Indicates the currently selected disk drive number.

Scan Hit. Set during the execution of the Scan command

if the FDC cannot locate a sector on the specified cylinder

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## Execution Phase isub tol abom word-littlem a ni aistage of banglash cala al DOW and

All data transfers to (or from) the floppy drive occur during the execution phase. The 8272 has two primary modes of operation for data transfers (selected by the specify command):

- 1) DMA mode
- 2) non-DMA mode

In the DMA mode, execution phase data transfers are handled by the DMA controller hardware (invisible to the driver software). The driver software, however, must set all appropriate DMA controller registers prior to the beginning of the disk operation. An interrupt is generated by the 8272 after the last data transfer, indicating the completion of the execution phase, and the beginning of the result phase.

In the non-DMA mode, transfer requests are indicated by generation of an interrupt and by activation of the RQM flag (bit 7 in the Main Status Register). The interrupt signal can be used for interrupt-driven systems and RQM can be used for polled systems. The driver software must respond to the transfer request by reading data from, or writing data to, the FDC. After completing the last transfer, the 8272 generates an interrupt to indicate the beginning of the result phase. In the non-DMA mode, the processor must activate the "terminal count" (TC) signal to the FDC (normally by means of an I/O port) after the transfer request for the last data byte has been received (by the driver) and before the appropriate data byte has been read from (or written to) the FDC.

In either mode of operation (DMA or non-DMA), the execution phase ends when a "terminal count" signal is sensed by the FDC, when the last sector on a track (the EOT parameter - Table 4) has been read or written, or when an error of bileval occurs.

If an invalid (undefined) command is sent to the FDC, the FDC will terminate the command. No interrupt is generated by the 8272 during this condition.

#### Multi-sector and Multi-track Transfers also and al (MOA bas Old) V 31d bas 3 118

During disk read/write transfers (Read Data, Write Data, Read Deleted Data, and Write Deleted Data), the FDC will continue to transfer data from sequential sectors until the TC input is sensed. In the DMA mode, the TC input is normally set by the DMA controller. In the non-DMA mode, the processor directly controls the FDC TC input as previously described. Once the TC input is received, the FDC stops requesting data transfers (from the system software or DMA controller). The FDC, however, continues to read data from, or write data to, the floppy disk until the end of the current disk sector. During a disk read operation, the data read from the disk (after reception of the TC input) is discarded, but the data CRC is checked for errors; during a disk write operation, the remainder of the sector is filled with all-zero bytes.

If the TC signal is not received before the last byte of the current sector has been transferred to/from the system, the FDC increments the sector number by one and initiates a read or write command for this new disk sector.

The FDC is also designed to operate in a multi-track mode for dual-sided disks. In the multi-track mode (specified by means of the MT flag in the command byte - Table 4) the FDC will automatically increment the head address of IfA (from 0 to 1) when the last sector (on the track under head 0) has been read or written. Reading or writing is then continued on the first sector (sector 1) of head 1.

### Drive Status Polling

After the power-on reset, the 8272 automatically enters a drive status of AMO and polling mode. If a change in drive status is detected (all drives are assumed to be "not ready" at power-on), an interrupt is generated. The 8272 continues this status polling between command executions (and between step pulses in the Seek command). In this manner, the 8272 automatically notifies the system software whenever a floppy disk is inserted, removed, or changed by the operator.

#### In the non-DMA mode, transfer requests are indicated by generation and in

During the command phase, the Main Status Register must be polled by the driver software before each byte is written into the Data Register. The DIO (bit 6) and or RQM (bit 7) flags in the Main Status Register must be low and high, respectively, before each byte of the command may be written into the 8272. The beginning of the execution phase for any of these commands will cause DIO to be set high and RQM to be set low.

Operation of the FDC commands is described in detail in Application Note AP-116, and "An Intelligent Data Base System Using the 8272."

### Invalid Commands a whole to written, or when a Table 4) has been read or written, or when a Table 4)

If an invalid (undefined) command is sent to the FDC, the FDC will terminate the command. No interrupt is generated by the 8272 during this condition.

Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both set indicating to the processor that the 8272 is in the result phase and the contents of Status Register 0 must be read. When the processor reads Status Register 0 it will find an 80H code indicating that an invalid command was received.

The driver software in Appendix B checks each requested command and will not assume an invalid command to the 8272.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate per a command interrupt; otherwise the FDC will consider the next command to be an invalid command. Also, when the last "hidden" interrupt has been serviced, further a sense Interrupt Status commands will result in invalid command codes.

been transferred to/from the system, the FDC increments the sector number by one

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## 4. 8272 Physical Interface Software

PL/M software driver listings for the 8272 FDC are contained in Appendix A. These drivers have been designed to operate in a DMA environment (as described in Application Note AP-116, "An Intelligent Data Base System Using the 8272"). In the following paragraphs, each driver procedure is described. (A description of the driver data base variables is given in Table 7.) In addition, the modifications necessary to reconfigure the drivers for operation in a polled environment are discussed.

#### INITIALIZE\$DRIVERS dalog to years Isnaedal na

This initialization procedure must be called before any FDC operations are attempted. This module initializes the DRIVE\$READY, DRIVE\$STATUS\$CHANGE, OPERATION\$IN\$PROGRESS, and OPERATION\$COMPLETE arrays as well as the GINESON COMPLETE arrays as well as the GINESON COMPLETE ARRAY OF C

## EXECUTE\$DOCB TO and yd beau yaxra lannedni nA

This procedure contains the main 8272 driver control software and handles the execution of a complete FDC command. EXECUTE\$DOCB is called with two parameters: a) a pointer to a disk operation control block and b) a pointer to a result status byte. The format of the disk operation control block is illustrated in Figure 2 and the result status codes are described in Table 8.

Before starting the command phase for the specified disk operation, the command is checked for validity and to determine whether the FDC is busy. (For an overlapped operation, if the FDC BUSY flag is set — in the Main Status Register — the command cannot be started; non-overlapped operations cannot be started if the FDC BUSY flag is set, if any drive is in the process of seeking/recalibrating, or if an operation is currently in progress on the specified drive.)

After these checks are made, interrupts are disabled in order to set the OPERATION\$IN\$PROGRESS flag, reset the OPERATION\$COMPLETE flag, load a pointer to the current operation control block into the OPERATION\$DOCB\$PTR array and set GLOBAL\$DRIVE\$NO (if a non-overlapped operation is to be started).

At this point, parameters from the operation control block are output to the DMA controller and the FDC command phase is initiated. After completion of the command phase, a test is made to determine the type of result phase required for the current operation. If no result phase is needed, control is immediately returned to the calling program. If an immediate result phase is required, the result bytes are input from the FDC. Otherwise, the CPU waits until the OPERATION\$COMPLETE flag is set (by the interrupt service procedure).

Finally, if an error is detected in the result status code (from the FDC), an FDC operation error is reported to the calling program.

A constant flag acray that indicates if an

## Table 7: Driver Data Base

ntained in Appendix BMAN	PE/M software driver list MOITGINDSED 8272 FDC are co
described. (A description	seas a A public array containing the current "ready" at a wistatus of each drive.quaperag galwollor end at a local to the current product of the current product
DRIVE\$STATUS\$CHANGE	A public array containing a flag for each drive. The appropriate flag is set whenever the ready status of a drive changes.
OPERATION\$DOCB\$PTR	An internal array of pointers to the state operation control block currently in
	This initialization property does not exercise a attempted. This module initializes the DRIVESARADY,
	An internal array used by the driver pro- cedures to determine if a disk operation is in progress on a given drive.
OPERATION\$COMPLETE	An internal array used by the driver pro- cedures to determine when the execution phase of a disk operation is complete.
called with two parame-	execution of a complete FDC command. EXECUTASDOCB is
control block is illus-	A data byte that records the current drive number for non-overlapped disk operations.
VALIDSCOMMAND	A constant flag array that indicates
isk operation, the command FDC is busy. (For an over-	b fell whether a specified FDC command code is ended ed t valid. education of the valid education of the valid education of the value o
ons cannot be s HTDNII COMMMOD	A constant byte array specifying the number of command/parameter bytes to be trans-
ETE flag, load a pointer	Delda A constant flag array that indicates whether in the constant flag array that indicates whether in the command array and into an FDC command.
OVERLAP\$OPERATION 1838 ed of	A constant flag array that indicates whether an FDC command can be overlapped with other
block are output to the	At this point, parameters from the opt. zbriammoontrol
f result phase requirTUE3R\$ON  ded, control is immediate- result phase is required,	A constant flag array that is used to deter- mine when an FDC operation does not have a presult phase. The provided of beauty
IMMED\$RESULT (embedong ed)	A constant flag array that indicates that an FDC operation has a result phase beginning
code (from the PDC), an	immediately after the command phase is vilenty complete. If of belonger at noise nothing Dog
POSSIBLE\$ERROR	A constant flag array that indicates if an FDC operation should be checked for an error status indication during the result phase.

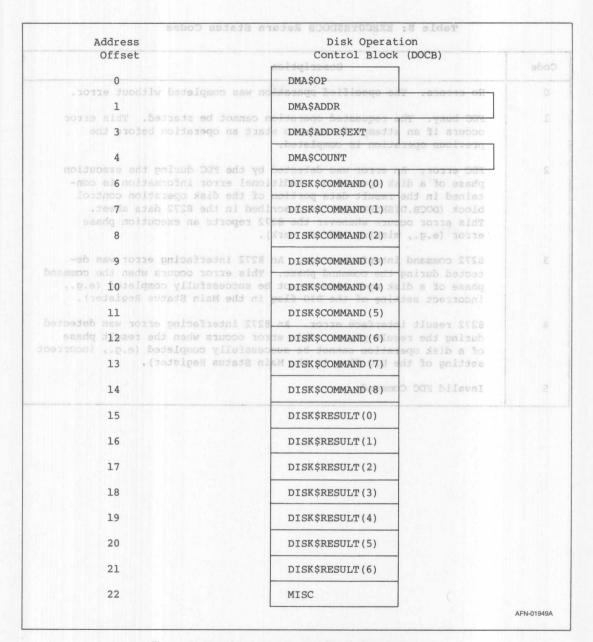


Figure 2. Disk Operation Control Block (DOCB) Format

Table 8: EXECUTE\$DOCB Return Status Codes

Code	(82	OGN NOOTE TOTANOO	aaelbA JealaO	
Code		Description		
0	No errors	. The specified operation was o	completed without error.	
1	occurs if	The requested operation cannot an attempt is made to start an operation is completed.		
2	phase of tained in block (DOC This error	An error was detected by the a disk operation. Additional er the result data portion of the CB.DISK\$RESULT) as described in coccurs whenever the 8272 reports, missing address mark).	ror information is con- disk operation control the 8272 data sheet.	
3	8272 command interface error. An 8272 interfacing error was detected during the command phase. This error occurs when the command phase of a disk operation cannot be successfully completed (e.g., incorrect setting of the DIO flag in the Main Status Register).			
4	8272 result interface error. An 8272 interfacing error was detected during the result phase. This error occurs when the result phase of a disk operation cannot be successfully completed (e.g., incorrect setting of the DIO flag in the Main Status Register).			
5	Invalid F	OC Command.		
	1	DISK\$RESULT(0)	35	
		DISKSRESULT(1)		
		DISKSRESULT(2)		

Course S. 1910th Vicensian Control Black (BOCE) Format

#### FDCINT

This procedure performs all interrupt processing for the 8272 interface drivers. Basically, two types of interrupts are generated by the 8272: (a) an interrupt that signals the end of a command execution phase and the beginning of the result phase and (b) an interrupt that signals the completion of an overlapped operation or the occurrence of an unexpected event (e.g., change in the drive "ready" status).

An interrupt of type (a) is indicated when the FDC BUSY flag is set (in the Main Status Register). When a type (a) interrupt is sensed, the result bytes a single are read from the 8272 and placed in the result portion of the disk operation control block, the appropriate OPERATION\$COMPLETE flag is set, and the OPERATION\$IN\$PROGRESS flag is reset.

When an interrupt of type (b) is indicated (FDC not busy), a sense interrupt status command is issued (to the FDC). The upper two bits of the result status usual register (Status Register Zero - STO) are used to determine the cause of the interrupt. The following four cases are possible:

- 1) Operation Complete. An overlapped operation is complete. The GOL of sham all drive number is found in the lower two bits of STO. The STO data and of sham is transferred to the active operation control block, the OPERATION\$COMPLETE flag is set, and the OPERATION\$IN\$PROGRESS flag is reset.
- 2) Abnormal Termination. A disk operation has abnormally terminated. The drive number is found in the lower two bits of STO. The STO data is transferred to the active control block, the OPERATION\$COM- and also PLETE flag is set, and the OPERATION\$IN\$PROGRESS flag is reset.
- 4) Drive Status Change. A change has occurred in the "ready" status of a disk drive. The drive number is found in the lower two bits of STO. The DRIVE\$READY flag for this disk drive is set to the new drive "ready" status and the DRIVE\$STATUS\$CHANGE flag for the drive is also set. In addition, if a command is currently in progress, the STO data is transferred to the active control block, making the OPERATION\$COMPLETE flag is set, and the OPERATION\$IN\$PROGRESS and flag is reset.

After processing a type (b) interrupt, additional sense interrupt status commands must be issued and processed until an "invalid command" result is returned from the FDC. This action guarantees that all "hidden" interrupts are serviced.

In addition to the major driver procedures described above, a number of support procedures are required. These support routines are briefly described in the equal following paragraphs.

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#### OUTPUT\$CONTROLS\$TO\$DMA

This procedure outputs the DMA mode, the DMA address, and the DMA word count to the 8237 DMA controller. In addition, the upper four bits of the 20-bit DMA address are output to the address extension latch. Finally, the disk DMA channel is started.

#### OUTPUT\$COMMAND\$TO\$FDC

This software module outputs a complete disk command to the 8272 FDC. The pass a self-number of required command/parameter bytes is found in the COMMAND\$LENGTH table. The appropriate bytes are output one at a time (by calls to OUTPUT\$BYTE\$TO\$FDC) from the command portion of the disk operation control block.

When an interrupt of type (b) is indicated (FDC not busy), a sense interrupt

4) Drive Status Change. A change has occurred in the "ready" status

## INPUT\$RESULT\$FROM\$FDC to afid own ragge edt . (DOT and of) beusal al bosomoro autain

This procedure is used to read result phase status information from the disk controller. At most, seven bytes are read. In order to read each byte, a call is made to INPUT\$BYTE\$FROM\$FDC. When the last byte has been read, a check is made to insure that the FDC is no longer busy.

#### OUTPUT\$BYTE\$TO\$FDC

This software is used to output a single command/parameter byte to the FDC. A This procedure waits until the FDC is ready for a command byte and then outputs the byte to the FDC data port.

#### 3) Invalid Command. - The execution of an invalid command invalid invalid Command.

This procedure inputs a single result byte from the FDC. The software waits until the FDC is ready to transfer a result byte and then reads the byte from the FDC data port.

## FDC\$READY\$FOR\$COMMAND a stevint dails sidt tot gell YGAGASXVIRG edt. OTS to

This procedure assures that the FDC is ready to accept a command/parameter byte by performing the following three steps. First, a small time interval (more than 20 microseconds) is inserted to assure that the RQM flag has time to become valid (after the last byte transfer). Second, the master request flag (RQM) is polled until it is activated by the FDC. Finally, the DIO flag is checked to ensure that it is properly set for FDC input (from the processor).

#### FDC\$READY\$FOR\$RESULT

The operation of this procedure is similar to the FDC\$READY\$FOR\$COMMAND with the following exception. If the FDC BUSY flag (in the Main Status Register) is not set, the result phase is complete and no more data is available from the FDC. Otherwise, the procedure waits for the RQM flag and checks the DIO flag for FDC output (to the processor).

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## OPERATION\$CLEAN\$UP

This procedure is called after the execution of a disk operation that has no result phase. OPERATION\$CLEAN\$UP resets the OPERATION\$IN\$PROGRESS flag and the good GLOBAL\$DRIVE\$NO variable if appropriate. This procedure is also called to clean up after some disk operation errors.

word 1 to be to expend the manual man

To operate in the polling mode, the following modifications should be made to the previous routines:

- 1. The OUTPUT\$CONTROLS\$TO\$DMA routine should be deleted. If add of relation and an engage
- 2. In EXECUTE\$DOCB, immediately prior to WAIT\$FOR\$OP\$COMPLETE, a polling loop should be inserted into the code. The loop should test the RQM flag (in the Main Status Register). When RQM is set, a data byte should be written to, or read from, the 8272. The buffer address may be computed from the base address contained in DOCB.DMA\$ADDR and DOCB.DMA\$ADDR\$EXT. After the correct number of bytes have been transferred, an operation complete interrupt will be issued by the FDC. During data transfer in the non-DMA mode, the NON-DMA MODE flag (bit 5 of the Main Status Register) will be set. This flag will remain set for the complete execution phase. When the transfer is finished, the NON-DMA MODE flag is reset and the result phase interrupt is issued by the FDC.

This procedure causes the floppy disk read/write head to retract to track 0. The RECALIBRATE procedure requires only one parameter — the drive number on which the recalibrate operation is to be performed. This procedure builds a disk operation control block (RECALIBRATE;DOCE) and passes the control block to the FDC driver for execution.

This procedure causes the disk read/write head (on the selected drive) to move to the desired cylinder position. The SEEK procedure is called with three perameters: drive number (DRV), head/side number (HD), and cylinder number (CFE). This software module builds a disk operation control block (SEEKSDOCB) that is executed by the FDC driver.

TAMEUT

The FORMAT procedure is designed to initialize a complete floppy disk so that sectors can subsequently be read and written by system and application programs. Three parameters must be supplied to this procedure: the drive number (DEV), the recording density (DEWS), and the interleave factor (INTLVE). The FORMAT procedure generates a data block (FMTELK) and a disk operation control block (FORMATSDOCE) for each track on the floppy disk (normally 77).

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#### 5. 8272 Logical Interface Software

Appendix B of this Application Note contains a PL/M listing of an exerciser program for the 8272 drivers. This program illustrates the design of logical interface level procedures to specify disk parameters, recalibrate a drive, seek to a cylinder, format a disk, read data, and write data.

The exerciser program is written to operate a standard single-sided 8" floppy disk drive in either the single- or double-density recording mode. Only the eight parameters listed in Table 9 must be specified. All other parameters are derived from these 8 basic variables.

Each of these logical interface procedures is described in the following paragraphs (refer to the listing in Appendix B).

 In EXECUTESDOCE, immediately prior to WAITSTORSOPSCOMPLETE, a polling loop should be inserted into the code. The loop should

#### SPECIFY

This procedure sets the FDC signal timing so that the FDC will interface correctly to the attached disk drive. The SPECIFY procedure requires four parameters, the step rate (SRT), head load time (HLT), head unload time (HUT), and the non-DMA mode flag (ND). This procedure builds a disk operation control block (SPECIFY\$DOCB) and passes the control block to the FDC driver module (EXECUTE\$DOCB) for execution. (Note carefully the computation required to transform the step rate (SRT) into the correct 8272 parameter byte.)

#### RECALIBRATE

This procedure causes the floppy disk read/write head to retract to track 0. The RECALIBRATE procedure requires only one parameter — the drive number on which the recalibrate operation is to be performed. This procedure builds a disk operation control block (RECALIBRATE\$DOCB) and passes the control block to the FDC driver for execution.

#### SEEK

This procedure causes the disk read/write head (on the selected drive) to move to the desired cylinder position. The SEEK procedure is called with three parameters: drive number (DRV), head/side number (HD), and cylinder number (CYL). This software module builds a disk operation control block (SEEK\$DOCB) that is executed by the FDC driver.

#### FORMAT

The FORMAT procedure is designed to initialize a complete floppy disk so that sectors can subsequently be read and written by system and application programs. Three parameters must be supplied to this procedure: the drive number (DRV), the recording density (DENS), and the interleave factor (INTLVE). The FORMAT procedure generates a data block (FMTBLK) and a disk operation control block (FORMAT\$DOCB) for each track on the floppy disk (normally 77).

Table 9: Basic Disk Parameters

Name (1939manag 1)	Description Laborated and the property of the
DENSITY	The recording mode (FM or MFM).
FILLER\$BYTE BUSENESS TO L	The data byte to be written in all sectors during formatting.
TRACKS\$PER\$DISK	The number of cylinders on the floppy disk.
BYTES\$PER\$SECTOR	The number of bytes in each disk sector. The exerciser accepts 128, 256, and 512 in FM mode, and 256, 512, and 1024 in MFM mode.
INTERLEAVE	The sector interleave factor for each disk track.
STEP\$RATE	The disk drive step rate (1-16 milliseconds).
HEAD\$LOAD\$TIME	The disk drive head load time (2-254 milliseconds).
HEAD\$UNLOAD\$TIME	The head unload time (16-240 milliseconds).

em operator. This error message lists the drive number, type of operation, and failure status (from the PDC). It is the operator's responsibility to take dditional action as required.

The format data block specifies the four sector ID field parameters (cylinder, head, sector, and bytes per sector) for each sector on the track. The sector numbers need not be sequential; the interleave factor (INTLVE parameter) is used to compute the logical to physical sector mapping.

After both the format data block and the operation control block are generated for a given cylinder, control is passed to the 8272 drivers for execution.

After the format operation is complete, a SEEK to the next cylinder is performed, a new format table is generated, and another track formatting operation is executed by the drivers. This track formatting continues until all tracks on the diskette are formatted.

In some systems, bad tracks must also be specified when a disk is formatted. For these systems, the existing FORMAT procedure should be modified to format bad tracks with a cylinder number of OFFH.

The sector interleave factor for each disk track

#### WRITE

The WRITE procedure transfers a complete sector of data to the disk drive. Five parameters must be supplied to this software module: the drive number (DRV), the cylinder number (CYL), the head/side number (HD), the sector number (SEC) and the recording density (DENS). This procedure generates a disk operation control block (WRITE\$DOCB) from these parameters and passes the control block to the 8272 driver for execution. When control returns to the calling program, the data has been transferred to disk.

#### READ

This procedure is identical to the WRITE procedure except the direction of data transfer is reversed. The READ procedure transfers a sector of data from the floppy disk to system memory.

#### Coping With Errors

In actual practice all logical disk interface routines would contain error processing mechanisms. (Errors have been ignored for the sake of simplicity in the exerciser programs listed in Appendix B.) A typical error recovery technique consists of a two-stage procedure. First, when an error is detected, a recalibrate operation is performed followed by a retry of the failed operation. This procedure forces the drive to seek directly to the requested cylinder (low-ering the probability of a seek error) and attempts to perform the requested operation an additional time. Soft (temporary) errors caused by mechanical or electrical interference do not normally recur during the retry operation; hard errors (caused by media or drive failures), on the other hand, will continue to occur during retry operations. If, after a number of retries (approximately 10), the operation continues to fail, an error message is displayed to the system operator. This error message lists the drive number, type of operation, and failure status (from the FDC). It is the operator's responsibility to take additional action as required.

## 6. File Systems

The file system provides the disk I/O interface level most familiar to users of interactive microcomputer and minicomputer systems. In a file system, all data is stored in named disk areas called files. The user and applications programs need not be concerned with the exact location of a file on the disk — the disk file system automatically determines the file location from the file name. Files may be created, read, written, modified, and finally deleted (destroyed) when they are no longer needed. Each floppy disk typically contains a directory that lists all the files existing on the disk. A directory entry for a file contains information such as file name, file size, and the disk address (track and sector) of the beginning of the file.

## File Allocation | ers seman slid file values of value tile names are by a period (.).

File storage is actually allocated on the disk (by the file system) in fixed size areas called blocks. Normally a block is the same size as a disk sector. Files are created by finding and reserving enough unused blocks to contain the data in the file. Two file allocation methods are currently in widespread use. The first method allocates blocks (for a file) from a sequential pool of unused blocks. Thus, a file is always contained in a set of sequential blocks on the disk. Unfortunately, as files are created, updated, and deleted, these free-block pools become fragmented (separated from one another). When this fragmentation occurs, it often becomes impossible for the file system to create a file even though there is a sufficient number of free blocks on the disk. At this point, special programs must be run to "squeeze" or compact the disk, in order to re-create a single contiguous free-block pool.

The second file allocation method uses a more flexible technique in which individual data blocks may be located anywhere on the disk (with no restrictions). With this technique, a file directory entry contains the disk address of a file pointer block rather than the disk address of the first data block of the file. This file pointer block contains pointers (disk addresses) for each data block in the file. For example, the first pointer in the file pointer block contains the track and sector address of the first data block in the file, the second pointer contains the disk address of the second data block, etc.

In practice, pointer blocks are usually the same size as data blocks. Therefore, some files will require multiple pointer blocks. To accommodate this requirement without loss of flexibility, pointer blocks are linked together, that is, each pointer block contains the disk address of the following pointer block. The last pointer block of the file is signalled by an illegal disk address (e.g., track 0, sector 0 or track OFFH, sector OFFH).

#### The Intel File System

The Intel file system (described in detail in the RMX-80 Users Guide) uses the second disk file allocation method (previously discussed). In order to lower the system overhead involved in finding free data blocks, the Intel file system incorporates a free space management data structure known as a bit map. Each disk sector is represented by a single bit in the bit map. If a bit in the bit map is set to 1, the corresponding disk sector has been allocated. A zero in the bit map indicates that the corresponding sector is free. With this technique, the process of allocating or freeing a sector is accomplished by simply altering the bit map.

File names consist of a basic file name (up to six characters) and a file extension (up to three characters). The basic file name and the file extension are separated by a period (.). Examples of valid file names are: DRIV72.OBJ, XX.TMP, and FILE.CS. In addition, four file attributes are supported (see Figure 3 for attribute definitions).

The bit map and the file directory are placed on prespecified disk tracks are sail (reserved for system use) beginning at track zero.

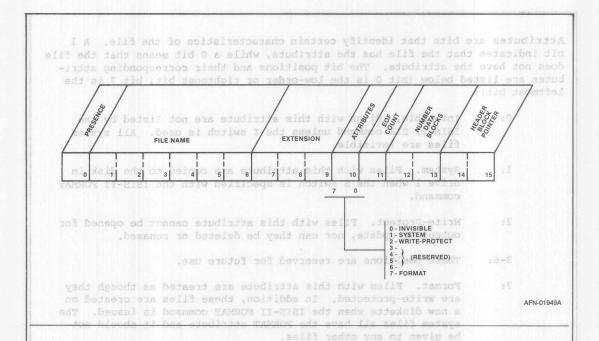
## Disk File System Functions as , bedsbon , bedsete are selfi as , yeldered , walls

Table 2 illustrates the typical functions implemented by a disk file system. As an example, the disk directory function (DIR) lists disk file information on the console display terminal. Figure 3 details the contents of a display entry in the Intel file system. The PL/M procedure outlined in Figure 4 illustrates a disk directory algorithm that displays the file name, the file attributes, and the file size (in blocks) for each file in the directory.

In practice, pointer blocks are usually the same size as data blocks. Therefore some files will require multiple pointer blocks. To accommodate this requirement without loss of flexibility, pointer blocks are linked together, that is, each pointer block contains the disk address of the following pointer block. The last pointer block of the file is signalised by an illegal disk address (e.g., track 0, sector 0 or track OFFE, sector OFTE).

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#### Directory Entry

Presence is a flag that can contain one of three values: outsy end at the life of

000H - The file associated with this entry is present on the disk.

07FH - No file is associated with this entry; the content of the rest of the entry is undefined. The first entry with its flag set to 07FH marks the current logical end of the directory and directory searches stop at this entry.

OFFH - The file named in this entry once existed on the disk but is currently deleted. The next file added to the directory will be placed in the first entry marked OFFH. This flag cannot, therefore, be used to (reliably) find a file that has been deleted. A value of OFFH should be thought of as simply marking an open directory entry.

File Name is a string of up to 6 non-blank ASCII characters specifying the name of the file associated with the directory entry. If the file name is shorter than six characters, the remaining bytes contain binary zeros. For example, the name ALPHA would be stored as: 414C50484100H.

**Extension** is a string of up to 3 non-blank ASCII characters that specifies an extension to the file name. Extensions often identify the type of data in the file such as OBJ (object module), or PLM (PL/M source module). As with the file name, unused positions in the extension field are filled with binary zeros.

Figure 3. Intel Directory Entry Format

Attributes are bits that identify certain characteristics of the file. A 1 bit indicates that the file has the attribute, while a 0 bit means that the file does not have the attribute. The bit positions and their corresponding attributes are listed below (bit 0 is the low-order or rightmost bit, bit 7 is the leftmost bit):

- O: Invisible. Files with this attribute are not listed by the ISIS-II DIR command unless the I switch is used. All system files are invisible.
- System. Files with this attribute are copied to the disk in drive 1 when the S switch is specified with the ISIS-II FORMAT command.
- Write-Protect. Files with this attribute cannot be opened for output or update, nor can they be deleted or renamed.
- 3-6: These positions are reserved for future use.
- 7: Format. Files with this attribute are treated as though they are write-protected. In addition, these files are created on a new diskette when the ISIS-II FORMAT command is issued. The system files all have the FORMAT attribute and it should not be given to any other files.

EOF Count contains the number of the last byte in the last data block of the file. If the value of this field is 080H, for example, the last byte in the file is byte number 128 in the last data block (the last block is full).

Number of Data Blocks is an address variable that indicates the number of data blocks currently used by the file. ISIS-II and the RMX/80 Disk File system both maintain a counter called LENGTH that is the current number of bytes in the file. This is calculated as:

((NUMBER OF DATA BLOCKS - 1) x 128 + EOF COUNT.

Header Block Pointer is the address of the file's header block. The high byte of the field is the sector number and the low byte is the track number. The system "finds" a disk file by searching the directory for the name and then using the header block pointer to seek to the beginning of the file.

Figure 3. Intel Directory Entry Format (Continued)

Extension is a string of up to 3 non-blank ASCII characters that specifies an extension to the file name. Extensions often identify the type of data in the file such as OBJ (object module), or PIM (FL/M source module). As with the file name, unused positions in the extension field are filled with binary zeros.

```
dir: procedure(drv,dens) no public; dio ni bendinem need eved amedi jaoMi .aepas
 oce.) herore designing 8272 software drivers, 1, styd dvisable that Vrb
          dens
                          ation in this section be thoroughly understood, , styd
          sector
                          byte,
                          byte,
          dir$ptr
                          byte,
                          based rdbptr structure (presence byte, ded AMG-MOM
          dir$entry
                          file$name(6) byte,extension(3) byte,
               to believe mattribute byte, eof$count byte, eleged said amedaya n
             Idagoo word and data$blocks address, header$ptr address),
          size (5) of tambyte, a paissened bus 2728 eds moral of scelenars at
          invisible$flag literally '1',
system$flag literally '2',
protected$flag literally '4',
                         literally '80H'; Jal essig Jimes | bnemsoo rossecong
          format$flag
  /* The disk directory starts at cylinder 1, sector 2 */
 call seek(drv,1,0); myor end telegraph of the roughly seek (drv,1,0); myor end the roughly seek (drv,1,0);
 do sector=2 to 26;
   call read(drv,1,0,sector,dens);
   do dir$ptr=0 to 112 by 4; beer era served fluser ils lidnu bearmoo ween a desco
     if dir$entry.presence=0
       then do;
  do i=0 to 5; call co(dir$entry.file$name(i)); end;
         call co(period);
do i=0 to 2; call co(dir$entry.extension(i)); end;
         do i=0 to 4; call co(space); end;
       call convert$to$decimal(@size,dir$entry.data$blocks);
      do i=0 to 4; call co(size(i)); end; and find publicable delta
     If (dir$entry.attribute and invisible$flag) <> 0 then call co('I');
         If (dir$entry.attribute and system$flag) <> 0 then call co('S');
         If (dir$entry.attribute and protected$flag) <> 0 then call co('W');
         If (dir$entry.attribure and format$flag) <> 0 then call co('F');
       end;
   end;
 end;
end dir;
                                                                   AFN-01949A
```

Figure 4. Sample PL/M Directory Procedure

The 8272 constantly polls all drives for changes in the drive ready status. This polling begins immediately following RESET. An interrupt is generated every time the FDC senses a change in the drive ready status. After reset, the FDC assumes that all drives are "not ready". If a drive is ready the FDC assumes that all drives are "not ready".

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## 7. Key 8272 Software Interfacing Considerations

This section contains a quick review of **Key** 8272 Software design features and issues. (Most items have been mentioned in other sections of this application note.) Before designing 8272 software drivers, it is advisable that the information in this section be thoroughly understood.

1. Non-DMA Data Transfers and equipment and beard

In systems that operate without a DMA controller (in the polled or interrupt driven mode), the system software is responsible for counting data transfers to/from the 8272 and generating a TC signal to the FDC when the transfer is complete.

2. Processor Command/Result Phase Interface vilgatif psiltsimnol

In the command phase, the driver software must write the exact number of parameters in the exact order shown in Table 5. During the result phase, the driver must read the complete result status. For example, the Format Track command requires six command bytes and presents seven result bytes. The 8272 will not accept a new command until all result bytes are read. Note that the number of command and result bytes varies from command-to-command. Command and result phases cannot be shortened.

During both the command and result phases, the Main Status Register must be read by the driver before each byte of information is read from, or written to, the FDC Data Register. Before each command byte is written, DIO (bit 6) must be low (indicating a data transfer from the processor) and RQM (bit 7) must be high (indicating that the FDC is ready for data). During the result phase, DIO must be high (indicating a data transfer to the processor) and RQM must also be high (indicating that data is ready for the processor).

Note: After the 8272 receives a command byte, the RQM flag may remain set for approximately 16 microseconds (with an 8 MHz clock). The driver should not attempt to read the Main Status Register before this time interval has elapsed; otherwise, the driver may erroneously assume that the FDC is ready to accept the next byte.

4. Samele PL/M Directory Proce

3. Sector Sizes

The 8272 does not support 128 byte sectors in the MFM (double-density) mode.

4. Drive Status Changes

The 8272 constantly polls all drives for changes in the drive ready status. This polling begins immediately following RESET. An interrupt is generated every time the FDC senses a change in the drive ready status. After reset, the FDC assumes that all drives are "not ready". If a drive is ready immediately after reset, the 8272 generates a drive status change interrupt.

#### 5. Seek Commands

The 8272 FDC does not perform implied seeks. Before issuing a data read or write command, the read/write head must be positioned over the correct cylinder by means of an explicit seek command. If the head is not positioned correctly, a cylinder address error is generated.

# (C=1), and so on, until physical track 30 is formatted as log prices formatted as logical 30 (C=30). Physical track 31 is bad and should be formatted as logical

When the processor receives an interrupt from the FDC, the FDC may be reporting one of two distinct events:

- a) The beginning of the result phase of a previously requested read, write, or scan command.
  - b) An asynchronous event such as a seek/recalibrate completion, an attention, an abnormal command termination, or an invalid command.

These two cases are distinguished by the FDC BUSY flag (bit 4) in the Main Status Register. If the FDC BUSY flag is high, the interrupt is of type (a). If the FDC BUSY flag is low, the interrupt was caused by an asynchronous event (b).

A single interrupt from the FDC may signal more than one of the above events.

After receiving an interrupt, the processor must continue to issue Sense
Interrupt Status commands (and service the resulting conditions) until an
invalid command code is received. In this manner, all "hidden" interrupts are
ferreted out and serviced.

#### 7. Skip Flag (SK)

The skip flag is used during the execution of Read Data, Read Deleted Data, Read Track, and various Scan commands. This flag permits the FDC to skip unwanted sectors on a disk track.

When performing a Read Data, Read Track, or Scan command, a high SK flag indicates that the FDC is to skip over (not transfer) any sector containing a deleted data address mark. A low SK flag indicates that the FDC is to terminate the command (after reading all the data in the sector) when a deleted data address mark is encountered.

When performing a Read Deleted Data command, a high SK flag indicates that sectors containing normal data address marks are to be skipped. Note that this is just the opposite situation from that described in the last paragraph. When a data address mark is encountered during a Read Deleted Data command (and the SK flag is low), the FDC terminates the command after reading all the data in the sector.

#### 8. Bad Track Maintenance

The 8272 does not internally maintain bad track information. The maintenance of this information must be performed by system software. As an example of typical bad track operation, assume that a media test determines that track 31 and track 66 of a given floppy disk are bad. When the disk is formatted for use, the system software formats physical track 0 as logical cylinder 0 (C=0 in the command phase parameters), physical track 1 as logical track 1 (C=1), and so on, until physical track 30 is formatted as logical cylinder 30 (C=30). Physcial track 31 is bad and should be formatted as logical cylinder FF (indicating a bad track). Next, physical track 32 is formatted as logical cylinder 31, and so on, until physical track 65 is formatted as logical cylinder 64. Next, bad physical track 66 is formatted as logical cylinder FF (another bad track marker), and physical track 67 is formatted as logical cylinder 65. This formatting continues until the last physical track (77) is formatted as logical cylinder 75. Normally, after this formatting is complete, the bad track information is stored in a prespecified area on the floppy disk (typically in a sector on track 0) so that the system will be able to recreate the bad track information when the disk is removed from the drive and reinserted at some later time.

To illustrate how the system software performs a transfer operation on a disk with bad tracks, assume that the disk drive head is positioned at track 0 and the disk described above is loaded into the drive. If a command to read track 36 is issued by an application program, the system software translates this read command into a seek to physical track 37 (since there is one bad track between 0 and 36, namely 31) followed by a read of logical cylinder 36.

Thus, the cylinder parameter C is set to 37 for the Seek command and 36 for the Read Sector command.

The skip flag is used during the execution of Read Data, Read Deleted Data Read Track, and various Scan commands. This flag permits the FDC to skip unwanted sectors on a disk track.

When performing a Read Data, Read Track, or Scan command, a high SK flag indicates that the FDC is to skip over (not transfer) any sector containing a deleted data address mark. A low SK flag indicates that the FDC is to terminate the command (after reading all the data in the sector) when a deleted data address mark is encountered.

When performing a Read Deleted Data command, a high SK flag indicates that sectors containing normal data address marks are to be skipped. Note that this is just the opposite situation from that described in the last paragraph. When a data address mark is encountered during a Read Deleted Data command (and the SK flag is low), the FDC terminates the command after reading all the data in the sector.

7. Skip Flag (SK)

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  8272 FDC DEVICE DRIVER SOFTWARE
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```
PL/M-86 COMPILER 8272 FLOPPY DISK CONTROLLER DEVICE DRIVERS
ISIS-II PL/M-86 V1.2 COMPILATION OF MODULE DRIVERS
                   OBJECT MODULE PLACED IN :F1:driv72.OBJ
                   COMPILER INVOKED BY: plm86 :F1:driv72.p86 DEBUG
                                                                              $title('8272 floppy disk controller device drivers')
                                                                             $nointvector
                                                                              $optimize(2)
                                                                            1
                                                                                                 2
                                          1
                                                                             declare
             * serve to sold/* floppy disk port definitions */
                         Adetermines if command car explosion and or it is also it is 
                                                                                      4
                                           1
                                            1
                                                                                    eclare
/* return status and error codes */oc revis of the 8272 fet constant and error codes */oc revis of the 8272 fet code of the status of t
                                                                                                                                                                                                                                                                        initialize@drivers: procedure public; /* initialize 8272 drivers */ declare Grysno byte;
                                                                                                                                                                            literally 'not', literally 'not', literally 'return error', lisavinbonexam of Geography
                                                                                      error$in
                                                                                      propagate$error
                                                                                                                                                                                                                                                                               /* fdc operation completed without errors */
                                                                                      statSok
                                                                                                                                                                                 literally '0',
                                                                                     stat$busy
stat$error
                                                                                                                                                                         literally 0,
literally 12,
literally 22,
literally 3,
literally 4,
literally 5;
                                                                                                                                                                                                                                                                 /* fdc is busy, operation cannot be started */
/* fdc operation error */
/* fdc not ready for command phase */
                                                                                      stat$command$error
                                                                                                                                                                                                                                                            /* fdc not ready for result phase */
/* fdc not ready for result phase */
result phase */
/* invalid fdc command */
                                                                                      stat$result$error
                                                                                      statSinvalid
                              6
                                            1
                                                                            declare
                                                                                       /* masks */
                                                                                      busy$mask
                                                                                                                                                                               literally '10H',
literally '40H',
literally '80H',
                                                                                      DIOSmask
                                                                                      ROMŚmask
                                                                                     RQMmask literally '80H', seek$mask literally '0FH', seek$mask literally '0FH', seek$ and literally '0COH', seek$ and literally '0COH', seek$ and literally '0COH', seek$ and literally '0COH', seek$ and literally '0CH', seek$ and literally
                                                                                      /* drive numbers */
                                                                                      max$no$drives
                                                                                                                                                                                 literally '3', literally '4';
                                                                                      fdcSgeneral
                                8
                                             1
                                                                             declare
                                                                                    /* miscellaneous control */
any$drive$seeking literally '((input(fdc$status$port) and seek$mask) <> 0) ',
command$code literally '((input(fdc$status$port) and DIO$mask) <> 0) ',
DIO$set$for$input literally '((input(fdc$status$port) and DIO$mask) <> 0) ',
extract$drive$no literally '((input(fdc$status$port) and DIO$mask) <> 0) ',
fdc$busy literally '((input(fdc$status$port) and busy$mask) <> 0) ',
extract$drive$no literally '((input(fdc$status$port) and busy$mask) <> 0) ',
extract$drive$no literally '(onput(fdc$status$port) and busy$mask) <> 0) ',
extract$drive$no literally 'on while ror operation$complete (drive$no); end',
extract$drive$no literally 'do while literally 'do while finput(fdc$status$port) and ROM$mask) = 0; end';
                                                                                       /* miscellaneous control */
                                                                            waitsforsRQM = MUM and literally 'do while (input(fdcsstatussport) and RQM$mask) = 0; end;';

like last parameter and an epil your and do are specific declare bear need and scend likes and to ejyd aseb dash end literal parameter.
                              9
                                            1
                                                                                      /* structures */
                                                                                    literally
                                                                             $eject
                                                                             declare
                          10 1
                                                                                     drive$status$change(4) byte public, /* when set - indicates that drve status changed */
                                                                                    drive$ready(4) byte public;
                                                                                                                                                                                                                                                                              /* current status of drives */
```

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```
declare
11 1
                                                       /* internal flags for operation with multiple drives */
/* fdc execution phase completed */
/* pointers for operations in progress */
/* temporary docb for interrupt processing */
             operation$in$progress(5) byte,
             operation$complete(5) byte,
operation$docb$ptr(5) pointer,
             interrupt$docb structure docb$type,
                                                       /* drive number of non-overlapped operation
             global$drive$no byte;
                                       ( areviab solven in progress - if any */ SR
           declare
12
   1
            drive$no$present(32) byte
              possible$error(32) byte
                                                       /* determines if command can return with an error */
              data(0,0,1,0,0,1,1,1,1,1,1,0,1,1,0,1,0,1,0,0,0,0,0,0,0,0,0,1,0,0,0,1,0,0),
             /* contains number of command bytes for each command */
              valid$command(32) byte
           /**** initialization for the 8272 fdc driver software. This procedure must
                be called prior to execution of any driver software. ****/
           initialize$drivers: procedure public;
/* initialize 8272 drivers */
13
    1
14
    2
            declare drv$no byte;
            do drvsno=0 to maxsnosdrives; drivesroady/drvsnos/s-2---
15
16
             drive$ready(drv$no)=false;
              driveSstatusSchange(drvSno)=false:
18
    operation$complete(drv$no)=false;
20
    3
            operation$in$progress(fdc$general)=false;
21
    2
            operation$complete(fdc$general)=false;
23
            global$drive$no=0:
24
    2
           end initialize$drivers;
          /*** wait until the 8272 fdc is ready to receive command/parameter bytes and in the command phase. The 8272 is ready to receive command bytes when the RQM flag is high and the DIO flag is low. ****/
25
    1
           fdc$ready$for$command: procedure byte;
             /* wait for valid flag settings in status register */
26
    2
            call time(1):
             /* wait for "master request" flag */
            wait$for$RQM;
          /* check data direction flag */
if DIO$set$for$input
then return ok;
else return error;
end fdc$ready$for$command;
30
    2
32
    2
33
    2
           /**** wait until the 8272 fdc is ready to return data bytes in the result and a sew
          phase. The 8272 is ready to return a result byte when the RQM and DIO
                flags are both high. The busy flag in the main status register will remain set until the last data byte of the result phase has been read
                by the processor.
           fdc$ready$for$result: procedure byte; 2 1552826 5200 2008880 2700 2008800
34 1
            /* wait for valid settings in status register */
35 2
            call time(1);
              * result phase has ended when the 8272 busy flag is reset */
            if not fdc$busy
then return complete;
```

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```
38
                                  41
43
            2
11
            2
                              end fdc$ready$for$result;
                              /**** output a single command/parameter byte to the 8272 fdc. The "data$byte" parameter is the byte to be output to the fdc. ****/
                             output$byte$to$fdc: procedure(data$byte) byte;
declare data$byte byte;

/* check to see if fdc is ready for command */
if not fdc$ready$for$command
47
49
            2
                                  output (fdc$data$port) =data$byte; d (sfg2d.ok) srubeoord =b1 2012b(samport)ugano
50
                             return ok;
end output$byte$to$fdc; aqqy260000 auniounts nig2doo0 beind door
51
                             /**** input a single result byte from the 8272 fdc. The "data$byte$ptr"
parameter is a pointer to the memory location that is to contain the input byte. ****/
                              input$byte$from$fdc: procedure(data$byte$ptr) byte; and of honograph of declare data$byte$ptr pointer; declare
52
53
54
                                        data$byte based data$byte$ptr bvte,
                                        status byte;
                                   /* check to see if fdc is ready */
55
                                   status=fdc$ready$for$result;
56
                                   if error$in status
                                   then propagateSerror;
then propagateSerror;
the status complete */ 120000 and (noisease bases)

/* check for result phase complete */ 120000 and (noisease bases)
if status=complete
                                  if status=complete
then return complete;
58
                                  then return complete; dated (1902doob) analyzing indicate the dataSpyte=input(fdc$data$port);
60
            2
                             61
                              $eject
                              /**** output the dma mode, the dma address, and the dma word count to the
8237 dma controller. Also output the high order four bits of the
address to the address extension latch. Finally, start the disk
dma channel. The "docbSptr" parameter is a pointer to the appropriate
disk operation control block. ****/
                             output$controls$to$dma: procedure(docb$ptr);
63
                                  declare docb$ptr pointer;
declare docb based docb$ptr structure docbtype;
64
65
66
            2
                                      /* dma port definitions */
dma$upper$addr$port literally '10H',
dma$disk$addr$port literally '00H',
dma$disk$addr$port literally '01H',
dma$disk$word$count literally '01H',
dma$command$port literally '08H',
dma$mad$port literally '08H',
dma$mad$port literally '08H',
dma$mask$sr$port literally '00H',
dma$mask$sr$port literally '00H',
dma$maser$clear$f$port literally '00H',
dma$master$clear$port literally '00H',
dma$master$clear$port literally '00H',
dma$master$clear$port literally '00H',
dma$master$clear$clear$port literally '00H',
dma$mask$clear$clear$port literally '00H',
dma$mask$clear
                                        /* dma port definitions */
                                       dma$disk$chan$start literally '00H',
dma$extended$write literally 'shl(1,5)', /* extended write flag */
dma$single$transfer literally 'shl(1,6)'; /* single transfer flag */
                                                                                                                                                     /* dma mask to start disk channel */
67
                                  if docb.dma$op < 3
                                       then do;

/* set dma mode and clear first/last flip-flop */ 220 pouglation langue
output(dma$mode$port)=shl(docb.dma$op,2) or 40H;
output(dma$clear$ff$port)=0;
69
```

2-219

71	3	/* set dma address */ output(dma\$disk\$addr\$port)=low(docb.dma\$addr);	
72 73	3	output(dma\$disk\$addr\$port)=high(docb.dma\$addr); output(dma\$upper\$addr\$port)=docb.dma\$addr\$ext;	
		if DIOS metSforSouthmet	
74 75	3	<pre>/* output disk transfer word count to dma controller *//o msuser medioutput(dma\$disk\$word\$count) = low(doob.dma\$count); output(dma\$disk\$word\$count) = high(doob.dma\$count);</pre>	
13	,	end (desired vstorsteaut)	
76 77	3	<pre>/* start dma channel 0 for fdc */ output(dma\$mask\$sr\$port)=dma\$disk\$chan\$start;</pre>	
//	3	<pre>/**** output a single command/parameter byte to the 8272 fdc. The "dat; bnete" parameter is the byte to be output to the fdc. ****/</pre>	
78	2	end output\$controls\$to\$dma;	
		<pre>/**** output a high-level disk command to the 8272 fdc. The number of bytes     required for each command is contained in the "command\$length" table.     The "docb\$ptr" parameter is a pointer to the appropriate disk operation</pre>	
		control block. ****/	
79 80	1 2	output\$command\$to\$fdc: procedure(docb\$ptr) byte; dcassb=(droq2ss555551)Jugsuo declare docb\$ptr pointer;	
81	2	declare	
01	-	<pre>docb based docb\$ptr structure docb\$type, cmd\$byte\$no byte;</pre>	
82	2	/**** input a single result byte from the 8272 fdc. The "dataSbyteSorr" berameter is a pointer to the memory location that is to contait; eldesib the input byte, ****/	
		/* output all command bytes to the fdc */	
83 84	3	<pre>do cmd\$byte\$no=0 to command\$length(command\$code)-1;   if error\$in output\$byte\$to\$fdc(docb.disk\$command(cmd\$byte\$no))</pre>	
89	3	then do; enable; propagateSerror; end; end; end;	
90	2	enable;	
91 92	2	return ok; end output\$command\$to\$fdc;  ** ybss zi 700 % ye od kusdu % ye end output\$command\$to\$fdc;  ** tiluser:road?ybszczofd?biscattatatatatatatatatatatatatatatatatata	
		<pre>/**** input the result data from the 8272 fdc during the result phase (after command execution). The "docb\$ptr" parameter is a pointer to the appropriate disk operation control block. ****/</pre>	
93	1	input\$result\$from\$fdc: procedure(docb\$ptr) byte;	
94 95	2 2	declare docb\$ptr pointer; (fdcsdataSport); declare	
93	2	docb based docb\$ptr structure docb\$type, tobl@moil@dyd2iuani his result\$byte\$no byte,	
		temp byte, status byte;	
96	2	/4** output the dms mode, the dms address, and the dms word count to the	
97	2	address to the address extension latch. Finally start the december of the channel. The "docbSpir" parameter is a ref of 0=on\$styler ob	
98 99	3	if error\$in status	
104	3	then do; enable; propagate\$error; end; ) a ubacong rambaconario status=complete	
		then do; enable; return ok; end; supposts niggoods hered doch sizioss	
109	3	<pre>docb.disk\$result(result\$byte\$no)=temp; end;</pre>	
		/* cma port definitions */	
111	2	dms5upperSaddrSport literally '104', word to be address if: fdc\$busy: mean address then return error; 'NHO'	
114	2	else return ok; sammon *\	
115		dmismodeSport literally OBH /* ;obl?morl?tluear?tugni bne cms@maskSsrSport literally OCH /* mask set/reset port */ dmisclearSfSsport literally OCH /* clear First/last flip-Flop por	
		/**** cleans up after the execution of a disk operation that has no result phase. The procedure is also used after some disk operation errors.  "drv" is the drive number, and "cc" is the command code for the	
116 117	1 2	operation\$clean\$up: procedure(drv,cc); na vilatesi salaman2afuntaamb declare (drv,cc) byte;	
118	2	diashle. 3 cook.doob if	
119	2	operation(sin(sprogress(drv))=false; teal term assis but about and beat to	
		ottput(dmasolearStEsport)=sh(doob.dmasop;2) or 40H; output(dmasolearStEsport)=sh(doob.dmasop;2) or 40H;	

2-220

```
120
            2
                              if not overlap$operation(cc)
                                  then global$drive$no=0;
122
            2
                              enable:
                          end operation$clean$up; shoonEnakeno, ondewindrauknasiodnoissasso Liso
123
            2
                          Seject
                          /**** execute the disk operation control block specified by the pointer
                                      parameter "docb$ptr". The "status$ptr" parameter is a pointer to a byte variable that is to contain the status of the requested operation when it has been completed. Six status conditions are
                                      possible on return: pre transfer trongestingerstangeautate too ment
                                                     The specified operation was completed without error.
                                           0
                                                     The fdc is busy and the requested operation cannot be started.

Fdc error (further information is contained in the result storage portion of the disk operation control block - as
                                           2
                                                     described in the 8272 data sheet).
                                                     Transfer error during output of the command bytes to the fdc.
                                           3
                                                     Transfer error during input of the result bytes from the fdc.

Invalid fdc command. ****/
                          execute a disk operation control block */
124
            1
125
                                   docb based docb$ptr structure docb$type,
            2
126
                                   status based status$ptr byte,
                                   drive$no byte:
                               /* check command validity */
                               /* check command validity */
if not valid$command(command$code)
then do: status at a continuous con
127
            2
                                    then do; status=stat$invalid; return; end;
                               /* determine if command has a drive number field - if not, set the drive
                               number for a general fdc command */
if drive$no$present(command$code)
132
                                    then drive$no=extract$drive$no;
134
            2
                                    else drive$no=fdc$general;
                               /* an overlapped operation can not be performed if the fdc is busy */ End if overlapsoperation(commandscode) and fdcsbusy then do: status=statsbusy return end.
135
            2
                                    then do; status=stat$busy; return; end;
                                /* for a non-overlapped operation, check fdc busy or any drive seeking */
140
            2
                               if not overlap$operation(command$code) and (fdc$busy or any$drive$seeking)
                                   then do; status=stat$busy; return; end;
                                /st check for drive operation in progress - if none, set flag and start operation st/
                               disable;
if operation$in$progress(drive$no)
146
                                   then do; enable; status=stat$busy; return; end;
                                   else operation$in$progress(drive$no)=true;
152
            2
                              /* at this point, an fdc operation is about to begin, so:
    1. reset the operation complete flag
    2. set the docb pointer for the current operation
    3. if this is not an overlapped operation, set the global drive
    number for the subsequent result phase interrupt. */
    operation$complete(drive$no)=0;
    operation$docb$ntr(drive$no)=0;
    operation$docb$ntr(drive$no)=0;
153
                              operation$complete(drive$no)=0;
operation$docb$ptr(drive$no)=docb$ptr;
154
                              if not overlap$operation(command$code)
    then global$drive$no=drive$no+1;
enable;
call output$controls$to$dma(docb$ptr);
if error$in output$command$to$fdc(docb$ptr)
    then do;
155
            2
157
            2
 158
159
                                      call operation$clean$up(drive$no,command$code);
161
                                       status=stat$command$error;
162
 163
164
            3
                                  * return immediately if the command has no result phase or completion interrupt - specify */
165
                               if no$result(command$code)
 167
                                       call operation$clean$up(drive$no,command$code);
168
                                       status=stat$ok:
169
                                       return:
170
                                   end:
```

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```
171
                                                                          if immed$result(command$code)
                                                                                    then do;
                                                                                            if error$in input$result$from$fdc(docb$ptr)
173
                             3
                                                                                                       then do;
                                                                                                              call operation$clean$up(drive$no,command$code);quantsloanolitarago bas
175
176
                                                                                                                 status=stat$result$error;
                              4
 177
                                                                                                               return;
                                                                                  end;
end;
end;
end;
else do;
wait$for$op$complete;
if docb.misc = error
 178
 179
 180
 183
                                                                                                       then do; status=stat$result$error; return; end; naujes do sidizaco:
188
                              3
                                                                          if no$fdc$error man nolds a balledpar and bins veco a table and then status=stat$ok; "distance and laminate and the status and
 189
                              2
 191
                                                                else status=stat$error;

(dada alab XT18 add ni bedicesta
end execute$docb; and dasamon add to begin prilate torin rateman
seriest

Select
 192
                             2
                                                                 /**** copy disk command results from the interrupt control block to the
                                                                                             currently active disk operation control block if a disk operation is in progress. ****/
                                                                copy$int$result: procedure(drv);
declare drv byte;
declare
 193
  194
                                                                                    docb$ptr pointer,
                                                                                    docbsptr pointer, docb based docbsptr structure docbstype; to structure docbst
                                                                           if operation$in$progress(drv) 15mm (Anadan | Bilavnillars=sudate (ob nord
 196
                                                                                              docbsptr=operationsdocbsptr(drv);
  198
                                                                                               do i=1 to 6; docb.disk$result(i)=interrupt$docb.disk$result(i); end;
   199
                                                                                              operation in progress (drv) = false;
operation Scorn and drawn in the contract of the contract
  202
  203
                                                                                              operation$complete(drv)=true;
   204
                               3
                                                                 end; * yourd at obt and it bearsoned and our not not and perfect and it the overlaps of the copysint copysint; was the copysint copysint; the copysint copys
  205
  206
                              2
                                                                  /**** interrupt processing for 8272 fdc drivers. Basically, two types of
   interrupts are generated by the 8272; (a) when the execution phase of
   an operation has been completed, an interrupt is generated to signal
                                                                                              the beginning of the result phase (the fdc busy flag is set when this interrupt is received), and (b) when an overlapped operation
                                                                                               is completed or an unexpected interrupt is received (the fdc busy flag is not set when this interrupt is received).
                                                                                                When interrupt type (a) is received, the result bytes from the operation
                                                                                                are read from the 8272 and the operation complete flag is set.
                                                                                              When an interrupt of type (b) is received, the interrupt result code is examined to determine which of the following four actions are indicated:
                                                                                                          1. An overlapped option (recalibrate or seek) has been completed. The
                                                                                                                        result data is read from the 8272 and placed in the currently active
                                                                                                                       disk operation control block.
                                                                                                        An abnormal termination of an operation has occurred. The result
data is read and placed in the currently active disk operation
                                                                                                                       control block.
                                                                                                         3. The execution of an invalid command has been attempted. This
                                                                                                                      The ready status of a drive has changed. The "drive$ready" and "drive$ready$status" change tables are updated. If an operation
                                                                                                                        is currently in progress on the affected drive, the result data
                                                                                                                        is placed in the currently active disk operation control block.
                                                                                              After an interrupt is processed, additional sense interrupt status commands must be issued and processed until an invalid command result is returned
                                                                                                from the fdc. This action guarantees that all "hidden" interrupts
```

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```
207
                fdcint: procedure public interrupt fdc$int$level;
208
                   declare
                     invalid byte.
                                                                                                                CODE AREA SIZE
                     drive$no byte,
                      docb$ptr pointer,
                                                                                                 WARLAND AREA SIZE = 00504
                     docb based docb$ptr structure docb$type;
                                                                                                 HAXIMUM STACK SIZE = 00328
209
       2
                      /* interrupt port definitions */
                                                   literally '70H',
literally 'shl(1,5)';
                                                                                                       SHE OF PL/M-SE COMPILATION
                      ocw2
                     nseoi
210
       2
                   declare
                     /* miscellaneous flags */
                     result$code literally 'shr(interrupt$docb.disk$result(0) and result$error$mask,6)',
result$drive$ready literally '(interrupt$docb.disk$result(0) and result$ready$mask) = 0)',
extract$result$drive$no literally '(interrupt$docb.disk$result(0) and result$tready$mask)',
end$of$interrupt literally 'output(ocw2)=nseoi';
                   /* if the fdc is busy when an interrupt is received, then the result
                       phase of the previous non-overlapped operation has begun */
                   if fdc$busy
211
                      then do:
                        /* process interrupt if operation in progress */
                        if global$drive$no <> 0
213
       3
                           then do;
215
        4
                             docb$ptr=operation$docb$ptr(global$drive$no-1);
216
                             if error$in input$result$from$fdc(docb$ptr)
                                then docb.misc=error;
218
        4
                               else docb.misc=ok;
                             operation$in$progress(global$drive$no-1) = false;
operation$complete(global$drive$no-1) = true;
global$drive$no=0;
219
220
221
                          end:
                     end:
223
                   /* if the fdc is not busy, then either an overlapped operation has been
                       completed or an unexpected interrupt has occurred (e.g., drive status
                       change) */
224
                     else do;
225
                        invalid=false;
226
       3
                        do while not invalid;
                           /* perform a sense interrupt status operation - if errors are detected,
                          in the actual fdc interface, interrupt processing is discontinued */
if error$in output$byte$to$fdc(sense$int$status) then go to ignore;
227
229
                           if error$in input$result$from$fdc(@interrupt$docb) then go to ignore;
231
       4
                           do case result$code;
                             /* case 0 - operation complete */
232
       5
233
       6
                               drive$no=extract$result$drive$no;
234
                               call copy$int$result(drive$no);
235
                             end:
                             /* case 1 - abnormal termination */
236
       5
237
       6
                               drive$no=extract$result$drive$no;
238
                               call copy$int$result(drive$no):
239
       6
                             end:
                             /* case 2 - invalid command */
240
       5
                             invalid=true;
                             /* case 3 - drive ready change */
241
                            do;
242
       6
                               drive$no=extract$result$drive$no;
243
       6
                               call copy$int$result(drive$no);
244
                               drive$status$change(drive$no)=true;
if result$drive$ready
       6
245
                                  then drive$ready(drive$no) = true;
else drive$ready(drive$no) = false;
247
       6
248
                            end;
249
       5
                          end:
250
                       end;
251
                     end:
                   ignore: end$of$interrupt;
253
       2
                end fdcint;
254
      1
                end drivers;
```

2-223

```
CODE AREA SIZE
                        = 0615H
                                       1557D
     CONSTANT AREA SIZE = 0000H
                                          OD
     VARIABLE AREA SIZE = 0050H
                                          80D
     MAXIMUM STACK SIZE = 0032H
                                          50D
     564 LINES READ
     0 PROGRAM ERROR (S)
END OF PL/M-86 COMPILATION
                            /* if the fdc is busy when an interrupt is received, then the result
phase of the previous non-overlapped operation has begun */
                                                          /* case 1 - abnormal termination */
                                                          drivesnoeextractsrawltsdrivesno;
                                                            " case 3 - drive ready change */
```

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#### ADDITIONIO

```
(dmaSop byte, dma$addr word, dma$addrSext byte, dmaScount word,
                                    1000
            APPENDIX B
  /* disk ope
                                 stepSrate
                              miltitrack
```

```
PL/M-86 COMPILER 8272 FLOPPY DISK DRIVER EXERCISE PROGRAM
ISIS-II PL/M-86 V1.2 COMPILATION OF MODULE RUN72
OBJECT MODULE PLACED IN :F1:run72.OBJ
COMPILER INVOKED BY: plm86 :F1:run72.p86 DEBUG
                $title ('8272 floppy disk driver exercise program')
                Snointvector
                Soptimize (2)
                Slarge
   1
                run72: do;
   2
       1
                   declare
                                                                         /* disk operation control block */
                     docb$type
                                                 literally
                        (dma$op byte,dma$addr word,dma$addr$ext byte,dma$count word,
                         disk$command(9) byte,disk$result(7) byte,misc byte);
       1
                   declare
                     /* 8272 fdc commands */
                                                literally '0',
literally '1',
literally '0',
literally '1',
literally '7',
literally '6',
literally '5',
literally '0DH',
literally '0PH';
                     fm
                     mfm
                     dma$mode
                     non$dma$mode
                     recalibrate$command
                     specify$command
                     readScommand
                     write$command
                     format$command
                     seek$command
                   declare
   4
       1
                                                 literally '0',
literally '1',
literally '2',
literally '3';
                     dma$verify
                     dmaSread
                     dma$write
                     dma$noop
                     eclare
/* disk operation control blocks */
format$docb structure docb$type,
seek$docb structure docb$type,
   5
       1
                   declare
                     recalibrate$docb
                                                 structure docb$type,
                     specify$docb
                                                 structure docb$type,
                     read$docb
                                                 structure docb$type,
                     write$docb
                                                 structure docb$type;
       1
                  declare
                     step$rate
                                                  byte,
                     head$load$time
                                                 byte,
                     head$unload$time
                                                  byte,
                     filler$byte
                                                  byte,
                     operation$status
                                                  byte,
                     interleave
                                                  byte,
                     format$qap
                                                  byte.
                     read$write$gap
                                                  byte,
                     index
                                                  byte,
                     drive
                                                  byte,
                     density
                                                  byte,
                     multitrack
                                                  byte,
                     sector
                                                  byte,
                     cylinder
                                                  byte,
                     head
                                                  byte,
                                                                        /* disk drive head */
                     tracks$per$disk
                                                  byte,
                     sectors$per$track
                                                 byte,
                     bytes$per$sector$code
                                                 byte,
                     bytes$per$sector
                                                 word;
                                                                        /* number of bytes in a sector on the disk */
   7 1
                  declare
                     /* read and write buffers */
                     fmtblk (104)
                                                 byte public, byte public,
                     wrbuf (1024)
                     rdbuf (1024)
                                                 byte public;
   8 1
                  declare
                     /* disk format initialization tables */
                     sec$trk$table(3)
                                                 byte data(26,15,8),
                     fmt$gap$table(8)
                                                 byte data(1BH, 2AH, 3AH, 0, 0, 36H, 54H, 74H), byte data(07H, 0EH, 1BH, 0, 0, 0EH, 1BH, 35H);
                     rd$wr$gap$table(8)
```

```
9 1 declare
/* external pointer tables and interrupt vector */
                                                                wrdptr(2) word external, wrong the state of 
                            wrbptr(2)
                                                                fbptr(2) word external, refultor (xon) a dominator (xon) a dominat
                                                         execute$docb: procedure(docb$ptr,status$ptr) external;
  10
                                                             declare docb$ptr pointer, status$ptr pointer;
   11
  12
                     2
                                                         end execute$docb; 1187agtarojosa-rojosattariaydgerojosattariaydg nedt
  13
                     1
                                                         initialize$drivers: procedure external;
                                                       end initialize$drivers;
  14
                                                $eject
                                                /**** specify step rate ("srt"), head load time ("hlt"), head unload time ("hut"),
    and dma or non-dma operation ("nd"). ****/
                                                        specify: procedure(srt,hlt,hut,nd);
 15
                                                               declare (srt,hlt,hut,nd) byte;
 16
                                                                specify$docb.dma$op=dma$noop;
                                                              specify$docb.dma$op=dma$noop;
specify$docb.disk$command(0) = specify$command;
specify$docb.disk$command(1) = sh1((not srt)+1,4) or shr(hut,4);
specify$docb.disk$command(2) = (hlt and 0FEH) or (nd and 1);
call execute$docb(@specify$docb,@operation$status);
 18
  19
 20
 21
                     2
  22
                  2
                                                       end specify:
                                                 /**** recalibrate disk drive
                                                                           8272 automatically steps out until the track 0 signal is activated
                                                                          by the disk drive. ****/
districte: procedure(drv);
                                          recalibrate: procedure(drv);
                                                           declare drv byte;
  24
                                                               recalibrate$docb.dma$op=dma$noop;
                                          recalibratesacco.dmasop=amasnoop;
recalibratesacco.diskscommand(0)=recalibratesaccommand;
recalibratesaccommand(1)=drv;
call executesaccommand(1)=drv;
call executesaccommand(1)=drv;
end recalibrate;
 26
 27
 28
 29
                                                /**** seek drive "drv", head (side) "hd" to cylinder "cyl". ****/
                                                     seek: procedure(drv,cyl,hd);
declare (drv,cyl,hd) byte;
seek$docb.dma$op=dma$noop;
seek$docb.disk$command(0)=seek$command;
seek$docb.disk$command(1)=drv or shl(hd,2);
seek$docb.disk$command(2)=cyl;
call execute$docb(@seek$docb,@operation$status);
 30
 31
 32
 33
 35
 36
                    2
 37
                                                     end seek.
                                               /**** format a complete side ("head") of a single floppy disk in drive "drv". The density, (single or double) is specified by flag "dens". ****/
38
                                                        format: procedure(drv,dens,intlve);
                   1
                                                      /* format disk */
declare (drv,dens,intlve) byte;
declare physical$sector byte;
 39
 40
                                                              call recalibrate (drv); t(8,(1) 13qdbx) fda+(0) byqdbx=ybba3axb.dbcb3ba5x
                                                              do cylinder=0 to tracks$per$disk-1;
                                                      /* set sector numbers in format block to zero before computing interleave */
43
                  3
                                                                     do physical$sector=1 to sectors$per$track; fmtblk((physical$sector-1)*4+2)=0; end;
/* physical sector 1 equals logical sector 1 */
physical$sector=1;
46
                                                                        /* assign interleaved sectors */sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sectors/sector
                                                                      47
                  3
48
                   4
```

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```
/* change sector and index if sector has already been assigned */61005
  49
              4
                                                do while fmtblk(index+2) <> 0; index=index+4; physical$sector=physical$sector+1; end;
                                                  /* set cylinder, head, sector, and size code for current sector into table */
                                                fmtblk(index)=cylinder; fmtblk(index+1)=head: fentalike blow
  53
                                                fmtblk(index+1)=head; Lagrance brow
fmtblk(index+2)=sector; Lagrance brow
  55
  56
                                                fmtblk(index+3)=bytes$per$sector$code;
                                                57
58
                                                     then physical$sector=physical$sector-sectors$per$track;
  60
                                            /* seek to next cylinder */
  61
             3
                                           call seek (drv, cylinder, head);
                                           /* set up format control block */ sol beed ("are") size gets while get a set of the set 
  62
             3
                                           format$docb.dma$op=dma$write;
                                           format$docb.dma$addr=fbptr(0)+shl(fbptr(1),4);
  63
                                           format$docb.dmasaddr=IDptr(U)T$Hit(IDptr(x),7);
format$docb.dma$addr$ext=0;
format$docb.dma$count=sectors$per$track*4-1;
format$docb.disk$command(0)=format$command or shl(dens,6);
format$docb.disk$command(1)=drv or shl(head,2);
format$docb.disk$command(2)=bytes$per$sector$code;
format$docb.disk$command(3)=sectors$per$track;
format$docb.disk$command(4)=format$qap;
  64
  65
   66
  67
   69
                                           format$docb.disk$command(4)=format$gap;
format$docb.disk$command(5)=filler$byte;
call execute$docb(@format$docb,@operation$status);
   70
   71
   72
   73
                                       end.
  74
             2
                                  end format;
                             write: procedure(drv,cyl,hd,sec,dens);
declare (drv,cyl,hd,sec,dens) byte;
write$docb.dma$op=dma$write;
write$docb.dma$addr=wrbptr(0)+shl(wrbptr(1),4);
write$docb.dma$addr$ext=0;
write$docb.dma$count=bytes$per$sector-1;
write$docb.disk$command(0)=write$command or shl(dens,6) or shl(multitrack,7);
   75
   76
             2
  77
  78
79
  81
  82
             2
                                       write$docb.disk$command(1) = drv or sh1(hd,2);
                                      write$docb.disk$command(2)=cyl; od "bd" (abis) beed , "with" eving dees kees
  83
             2
                                       write$docb.disk$command(3)=hd;
  84
                                       write$docb.disk$command(4) = sec;
  85
                                       write$docb.disk$command(4) = sec;
write$docb.disk$command(5) = bytes$per$sector$code;
  86
                                      write$docb.disk$command(5) = bytes$per$sector$code;
write$docb.disk$command(6) = sectors$per$track;
write$docb.disk$command(7) = read$write$gap;
if bytes$per$sector$code = 0
then write$docb.disk$command(8) = bytes$per$sector;
else write$docb.disk$command(8) = 0FFH;
call execute$docb(@write$docb,@operation$status);
  87
  88
  89
  91
             2
  92
  93
             2
                                  end write:
     /**** read sector "sec" on drive "drv" at head "hd" and cylinder "cyl". The disk recording density is defined by the "dens" flag. Data is read into the global read buffer ("rdbuf"). ****/
  94
                                  read: procedure(drv,cyl,hd,sec,dens);
  95
                                       declare (drv,cyl,hd,sec,dens) byte;
                                      read$docb.dma$op=dma$read;
  96
                         read$docb.dma$addr=rdbptr(0)+shl(rdbptr(1),4);
read$docb.dma$addr$ext=0;
read$docb.dma$addr$ext=0;
read$docb.dma$count=bytes$per$sector-1;
  98
  99
                                       read$docb.disk$command(0)=read$command or shl(dens,6) or shl(multitrack,7);
100
                        101
102
103
                                       read$docb.disk$command(3)=hd;
                                       read$docb.disk$command(4)=sec;
                                       read$docb.disk$command(5)=bytes$per$sector$code; begas[retal aplaas *\
105
                                      read$docb.disk$command(0)=sectors$per$track; paraloles of lengths of read$docb.disk$command(7)=read$write$gap;
106
107
```

```
108
                                                                                                    if bytes$per$sector$code = 0
                                                                                                    then read$docb.disk$command(8)=bytes$per$sector; nor a back and support else read$docb.disk$command(8)=0FFH; and a back a
     110
     111
                                                                                                                                                                                                                                                                                                             outsut (dmaSmodefport) = dmaSc3Smode)
                                    2
     112
                                                                                        end read:
/* religion of the 8159A interrupt controller */
controller controller or levelSeenattive or controller 20 or Seject 10001) = singleScontroller or levelSeenattive or controller 20 or selection of the controller or selection or s
                                                                               /**** initialize system by setting up 8237 dma controller and 8259A interrupt
                                      output (cow1) =not diskSinterruptSmask; /* m/****!! i.relornoxxcopt disk */
     113
                                                                                        initialize$system: procedure; \* obt not rossey journeys a sufferint *\
     114
                                      2
                                                                                   declare

/* I/O ports */
dma$disk$addr$port literally '00H', /* current address port */
dma$disk$word$count$port literally '01H', /* word count port */
dma$disk$word$count$port literally '08H', /* command port */
dma$mask$sr$port literally '08H', /* mode port */
dma$mask$sr$port literally '08H', /* mode port */
dma$clear$ff$port literally '0CH', /* clear first/last flip-flop port */
dma$mask$port literally '0DH', /* dma master clear port */
dma$cl$addr$port literally '09H', /* parallel mask set port*/
dma$cl$word$count$port literally '03H',
dma$cl$word$count$port literally '03H',
dma$cl$word$count$port literally '04H',
dma$cl$word$count$port literally '05H',
dma$cl$word$count$port literally '05H',
dma$cl$word$count$port literally '07H',
icwl literally '71H',
ocwl literally '71H',
ocwl literally '71H',
ocwl literally '70H',
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lite
                                                                                                declare
                                                                                                                /* I/O ports */
    115 112 siles in declare | 00845 101
       declare

/* misc masks and literals */

dma$\( \) x misc masks and literally \( \) x hl(1,5) \( \), \( \) x extended write flag */

dma$\( \) dma$\( \) x ingle \( \) transfer flag \( \) dma$\( \) x ingle transfer flag \( \) dma\( \) x ingle transfer flag \( \)
                                                                                      * 00 /* misc masks and literals */
                                                                                                    116
                                     2
   117
                                      2
                                                                                                   118
                                                                                                     /* set all addresses to zero */
    119
                                     2
                                                                                                    output (dma$clear$ff$port) = 0;
                                                                                                                                                                                                                                                                                                                                             /* reset first/last flip-flop */
    120
                                                                                                    output (dma$disk$addr$port) =0;
     121
                                                                                                   output (dma$disk$addr$port) =0;
output (dma$cl$addr$port) =0; ap$head, smlrabsol$bad, slarksslaylisecs list
     122
                                                                                                  output (dma$c1$addr$port) = 0;
output (dma$c2$addr$port) = 0;
    124
                                                                                                  output(dma$c2$addr$port)=0;
output(dma$c3$addr$port)=0;
output(dma$c3$addr$port)=0;
     125
                                      2
     126
   127
                                                                                                    /* set all word counts to valid values */
   128
                                    2
                                                                                                    output (dma$clear$ff$port) =0;
                                                                                                                                                                                                                                                                                                                                                         /* reset first/last flip-flop */
   129
                                                                                                    output (dma$disk$word$count$port) =1;
   130
                                     2
                                                                                                    output (dma$disk$word$count$port) =1;
   131
                                                                                                    output (dma$cl$word$count$port) =1; (evselvetat, ydleneb, evtab) femiol [[co
   132
                                                                                                  output (dma$cl$word$count$port) =1;
                                                                                                   output (dma$c2$word$count$port) =1;
                                                                                                   output (dma$c2$word$count$port) =1;
   134
                                                                                                    output (dma$c3$word$count$port) =1;
    135
   136
                                                                                                  output (dma$c3$word$count$port) =1;
```

2-229

```
/* initialize all dma channel modes */ 0 = sbookrodosakisqkasiyd ll
output(dma$mode$port)=dma$dišk$mode;yd=(8)bnamacokish,dookbasi kadi
output(dma$mode$port)=dma$cl$mode; NY40=(8)bnamacokish,dookbasi kadi
137
          2
138
                               output (dma$mode$port) =dma$c2$mode; issiego@.doob&beex@) doob&sseese (Lso
139
          2
                               output (dma$mode$port) =dma$c3$mode;
           2
140
                               /* initialize 8259A interrupt controller */
141
           2
                               output(icwl)=single$controller or level$sensitive or control$word4$required or base$icwl;
                               output(icw2)=interrupt$base;
output(icw4)=mode$8088; doc and 1558 qu paid/* set 8088 interrupt mode */
          2
142
143
          2
                                                                                                               /* mask all interrupts except disk */
           2
                               output(ocwl) = not disk$interrupt$mask;
144
                               /* initialize interrupt vector for fdc */ varabooorg imsdayalarilari
                                                                                 clare

' 1/0 ports */

intersily '00H'.

dmasdiskseddfsport literally '0HH'.

dmasdisksbort literally '08H'.

S88' literally '08H'.
                                                                                                                                                    declare
                               intvec(40H) = intptr(0);
intvec(41H) = intptr(1);
145
          2
146
147
                           end initialize$system;
                        $eject \" Jroq shom *\
/* Joseph (head) 0. Then
                            declare drive$ready(4) byte external;
148
          1
                            /* disable until interrupt vector setup and initialization complete */
149
           1
                                                                                                       dmaSc2SwordScountSport liber
dmaSc3SaddrScort liber
                            /* set initial floppy disk parameters */
                                                                                               vilsistil /* double-density */ look
                           density=mfm;
head=0:
150
           1
151
                            head=0:
                            filler$byte=55H;
                                                                              multitrack=0;
152
153
154
                            tracks$per$disk=77;
                            bytes$per$sector=1024;
                          interleave=6; /* set track interleave factor */
step$rate=11; /* 1024 bytes in each sector */
step$rate=11; /* 10ms for SA800 plus 1 for uncertainty */
head$load$time=40; /* 40ms head load for SA800 */
head$unload$time=240; /* derived accordance of the sector */
/* derived accordance of the sector */
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/* derived accordance of the
155
           1
156
           1
157
158
159
           1
                            /* derive dependent parameters from those above */
160
                            bytes$per$sector$code=shr(bytes$per$sector,7);
                            do index=0 to 3;
161
                                if (bytes$per$sector$code and 1) <> 0 state
162
                                   then do; bytes$per$sector$code=index; go to donebc; end; 888885558 else bytes$per$sector$code=shr(bytes$per$sector$code,1); 838885588
167
                            end;
                                                                                               singleScontroller literally levelScensitive literally
168
169
           1
                            sectors$per$track=sec$trk$table(bytes$per$sector$code-density);
170
           1
                            format$gap=fmt$gap$table(shl(density,2)+bytes$per$sector$code); I #82486M
171
           1
                            read$write$gap=rd$wr$gap$table(shl(density,2)+bytes$per$sector$code);
                            /* initialize system and drivers */
                           call initialize$system; | sallrw2behredxe2smb=(droq2ehom2smb)duqduo
172
           1
                           call initialize$drivers;
                                                                                 /* set all dma registers to valid values */
                            /* reenable interrupts and give 8272 a chance to report on drive status
                                 before proceeding */
174
                            enable:
                     \ call time (10); datil deas *\
175
                            /* specify disk drive parameters */
176
           1
                            call specify(step$rate,head$load$time,head$unload$time,dma$mode);
177
           1
                                                                                                                 /* run single disk drive #0 */
                            /* wait until drive ready */
178
           1
                            do while 1:
179
           2
                               if drive$readv(drive)
                                   then go to start;
           2
181
                           start: (I=(Jioq2Jnpoo2blow2ke1b2amb) Jugluo call format(drive,density,interleave); (I=(Jioq2Jnpoo2blow2ke2b2amb) Jugluo
182
           1
                                                                                                     output (dma$cl$word$count$port) =1;
183
                           do while 1:
                               do cylinder=0 to tracks$per$disk-1;
  call seek(drive,cylinder,head);
  do sector=1 to sectors$per$track;
           2
184
185
           3
                                     /* set up write buffer */
187
           4
                                      do index=0 to bytes$per$sector-1; wrbuf(index)=index+sector+cylinder; end;
```

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```
190 4
191 4
                                     call write(drive,cylinder,head,sector,density);
call read(drive,cylinder,head,sector,density);
                                     /* check read buffer against write buffer */
if cmpw(@wrbuf,@rdbuf,shr(bytes$per$sector,1)) <> OFFFFH
  192 4
                                         then halt;
 194
  195
                               end;
  196
          2
                           end;
 197 1
                       end run72;
MODULE INFORMATION:
       CODE AREA SIZE = 0570H 1392D
CONSTANT AREA SIZE = 0000H 0D
VARIABLE AREA SIZE = 0907H 231LD
MAXIMUM STACK SIZE = 0022H 34D
412 LINES READ
0 PROGRAM PROPORTION
        0 PROGRAM ERROR(S)
END OF PL/M-86 COMPILATION
```

APPENDIX C 8272 DRIVER FLOWCHARTS 190 & call write (drive, cylinder, head, sector, density);
191 & cell read (drive, cylinder, head, sector, density);

/\* check read buffer against write buffer \*/

192 & ff cmpw (Bwrbuf, Brdbuf, shr (bytesSper\$sector, l)) <> OFFFER

194 & end;

195 2 end;

197 l end ruh72;

\*\*CODE ANSA SIZE = 0570H 1392P

\*\*COMETANT REAS SIZE = 0570H 1392P

WANTANDE REAS SIZE = 0000H 0P

\*\*COMETANT SACH BIZE = 0002H 2311P

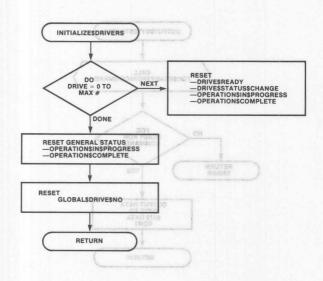
\*\*COMETANT SACH BIZE = 0002H 35P

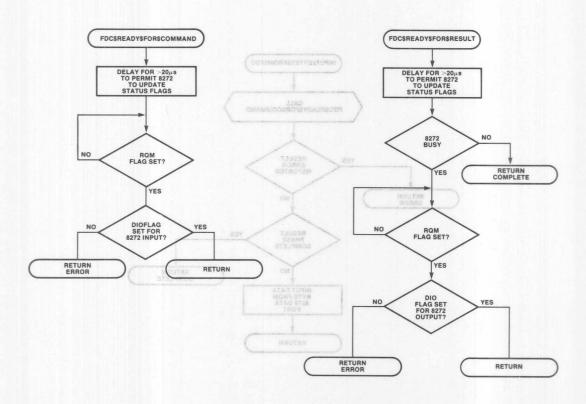
## APPENDIX C 8272 DRIVER FLOWCHARTS

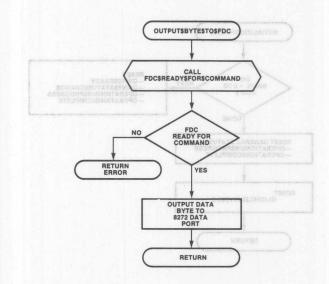
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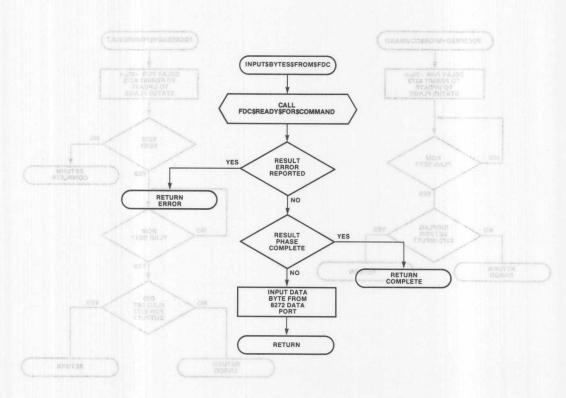
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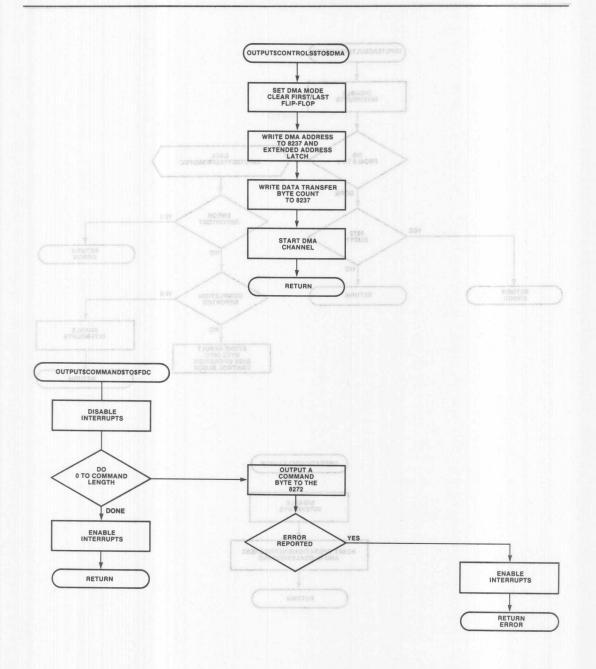


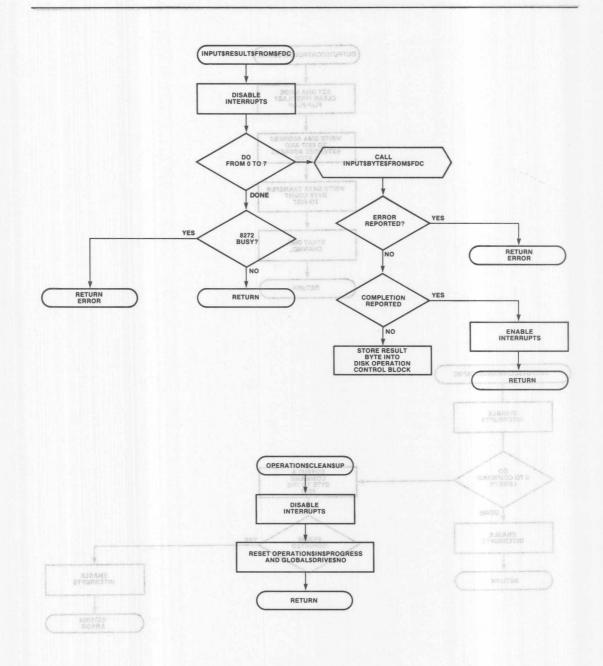


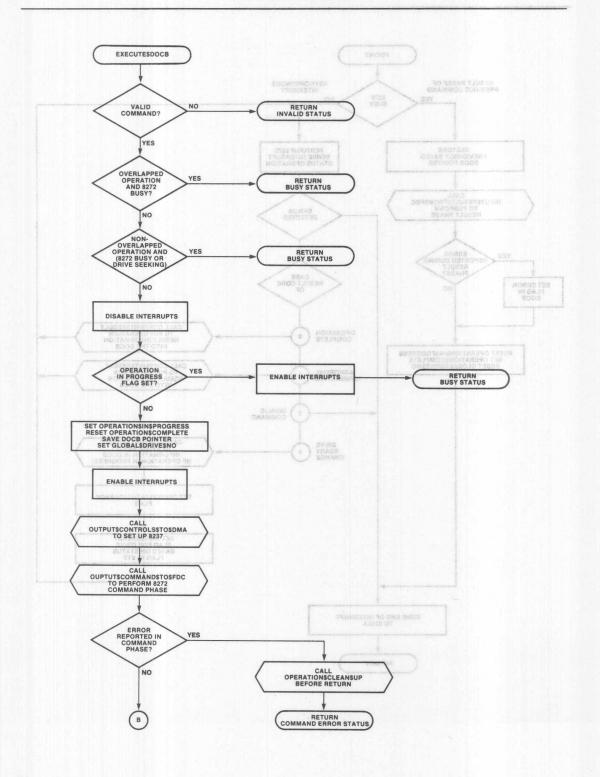


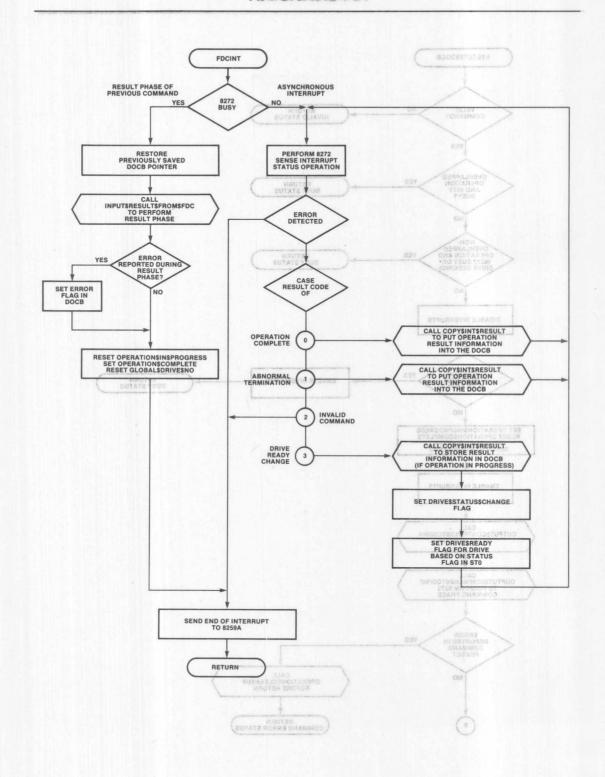


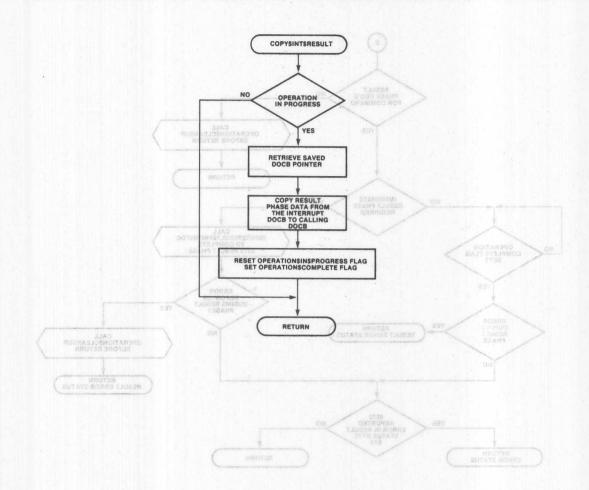
2-234

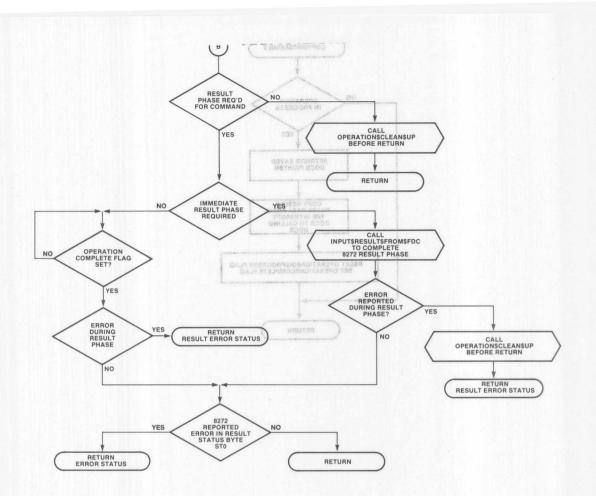












## Asynchronous Receiver/Transmitter

INTERFACE SIGNALS MODE SELECTION

PROCESSOR DATA LINK

# Using the 8251 Universal Synchronous/ Asynchronous Receiver/Transmitter

#### Contents 700 8180 INTRODUCTION 2-242 **COMMUNICATION FORMATS** 2-242 **BLOCK DIAGRAM** 2-243 Receiver Transmitter Modem Control I/O Control **INTERFACE SIGNALS** 2-245 **CPU-Related Signals Device-Related Signals MODE SELECTION** 2-248 PROCESSOR DATA LINK 2-251 CONCLUSION 2-257 **APPENDIX** 2-269 8251 Design Hints

#### INTRODUCTION

The Intel 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) which is capable of operating with a wide variety of serial communication formats. Since many peripheral devices are available with serial interfaces, the 8251 can be used to interface a microcomputer to a broad spectrum of peripherals, as well as to a serial communications channel. The 8251 is part of the MCS-80<sup>TM</sup> Microprocessor Family, and as such it is capable of interfacing to the 8080 system with a minimum of external hardware.

This application note describes the 8251 as a component and then explains its use in sample applications via several examples. A specific use of the 8251 to facilitate communication between two MCS-80 systems is discussed in detail from both the hardware and software viewpoints. The first two sections of this application note describe the 8251 first from a functional standpoint and then on a detailed level. The function of each input and output pin is fully defined. The next section describes the various operating modes and how they can be selected, and finally, a sample design is discussed using the 8251 as a data link between the MCS-80 systems.

## COMMUNICATION FORMATS

Serial communications, either on a data link or with a local peripheral, occurs in one of two basic formats; asynchronous or synchronous. These formats are similar in that they both require framing information to be added to the data to enable proper detection of the character at the receiving end. The major difference between the two formats is that the asynchronous format requires framing information to be added to each character, while the synchronous format adds framing information to blocks of data, or messages. Since the synchronous format is more efficient than the asynchronous format but requires more complex decoding, it is typically found on high-speed data links, while the asynchronous format is used on lower speed lines. The and at she harmond has no rento

The asynchronous format starts with the basic data bits to be transmitted and adds a "START" bit to the front of them and one or more "STOP" bits behind them as they are transmitted. The START bit is a logical zero, or SPACE, and is defined as the positive voltage level by RS-232-C. The STOP bit is a logical one, or MARK, and is defined as the negative voltage level by RS-232-C. In current loop applications current flow normally indicates a MARK and lack of current a SPACE. The START bit tells the receiver to start assembling a character and allows the receiver to synchronize itself with the transmitter. Since this synchronization only

has to last for the duration of the character (the next character will contain a new START bit), this method works quite well assuming a properly designed receiver. One or more STOP bits are added to the end of the character to ensure that the START bit of the next character will cause a transition on the communication line and to give the receiver time to "catch up" with the transmitter if its basic clock happens to be running slightly slower than that of the transmitter. If, on the other hand, the receiver clock happens to be running slightly faster than the transmitter clock, the receiver will perceive gaps between characters but will still correctly decode the data. Because of this tolerance to minor frequency deviations, it is not necessary that the transmitter and receiver clocks be locked to the identical frequency for successful asynchronous communication.

The synchronous format, instead of adding bits to each character, groups characters into records and adds framing characters to the record. The framing characters are generally known as SYN characters and are used by the receiver to determine where the character boundaries are in a string of bits. Since synchronization must be held over a fairly long stream of data, bit synchronization is normally either extracted from the communication channel by the modem or supplied from an external source.

An example of the synchronous and asynchronous formats is shown in Figure 1. The synchronous format shown is fairly typical in that it requires two SYN characters at the start of the message. The asynchronous format, also typical, requires a START bit preceding each character and a single STOP bit following it. In both cases, two 8-bit characters are to be transmitted. In the asynchronous mode 10\*n bits are used to transmit n characters and in the synchronous mode 8N + 16 bits are used. For the example shown the asynchronous mode is actually more efficient, using 20 bits versus 32. To transmit a thousand characters in the asynchronous mode, however, takes 10,000 bits versus 8.016 for the synchronous format mode. For long messages the synchronous format becomes much more efficient than the asynchronous format; the crossover point for the examples shown in Figure 1 is eight characters, for which both formats require 80 bits.

In addition to the differences in format between synchronous and asynchronous communication, there are differences with regards to the type of modems that can be used. Asynchronous modems typically employ FSK (Frequency Shift Keying) techniques which simply generate one audio tone for a MARK and another for a SPACE. The receiving modem detects these tones on the telephone

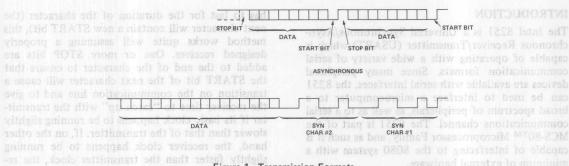


Figure 1. Transmission Formats

line, converts them to logical signals, and presents them to the receiving terminal. Since the modem itself is not concerned with the transmission speed, it can handle baud rates from zero to its maximum speed. Synchronous modems, in contrast to asynchronous modems, supply timing information to the terminal and require data to be presented to them in synchronism with this timing information. Synchronous modems, because of this extra clocking, are only capable of operating at certain preset baud rates. The receiving modem, which has an oscillator running at the same frequency as the transmitting modem, phase locks its clock to that of the transmitter and interprets changes of phase as data.

In some cases it is desirable to operate in a hybrid mode which involves transmitting data with the asynchronous format using a synchronous modem. This occurs when an increase in operating speed is required without a change in the basic protocol of the system. This hybrid technique is known as isosynchronous and involves the generation of the start and stop bits associated with the asynchronous format, while still using the modem clock for bit synchronization.

The 8251 USART has been designed to meet a broad spectrum of requirements in the synchronous, asynchronous, and isosynchronous modes. In the synchronous mode the 8251 operates with 5, 6, 7, or 8-bit characters. Even or odd parity can be optionally appended and checked. Synchronization can be achieved either externally via added hardware or internally via SYN character detection. SYN detection can be based on one or two characters which may or may not be the same. The single or double SYN characters are inserted into the data stream automatically if the software fails to supply data in time. The automatic generation of SYN characters is required to prevent the loss of synchronization. In the asynchronous mode the 8251 operates with the same data and parity structures as it does in the synchronous mode. In addition to appending a START bit to this data, the

8251 appends 1, 1½, or 2 STOP bits. Proper framing is checked by the receiver and a status flag set if an error occurs. In the asynchronous mode the USART can be programmed to accept clock rates of 16 or 64 times the required baud rate. Isosynchronous operation is a special case of asynchronous with the multiplier rate programmed as one instead of 16 or 64. Note that ×1 operation is only valid if the clocks of the receiver and transmitter are synchronized.

The 8251 USART can transmit the three formats in half or full duplex mode and is double-buffered internally (i.e., the software has a complete character time to respond to a service request). Although the 8251 supports basic data set control signals (e.g., DTR and RTS), it does not fully support the signaling described in EIA-RS-232-C. Examples of unsupported signals are Carrier Detect (CF), Ring Indicator (CE), and the secondary channel signals. In some cases an additional port will be required to implement these signals. The 8251 also does not interface to the voltage levels required by EIA-RS-232-C; drivers and receivers must be added to accomplish this interface.

#### BLOCK DIAGRAM from at tampot supportionva

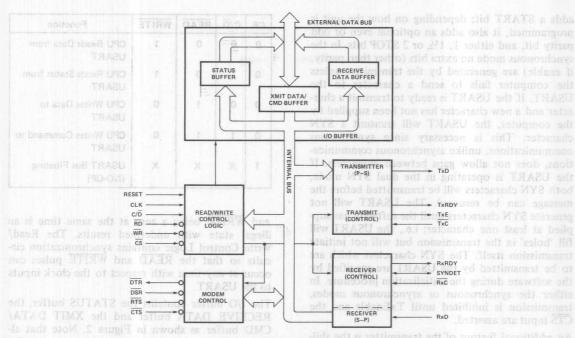
A block diagram of the 8251 is shown in Figure 2. Ås can be seen in the figure, the 8251 consists of five major sections which communicate with each other on an internal data bus. The five sections are the receiver, transmitter, modem control, read/write control, and I/O Buffer. In order to facilitate discussion, the I/O Buffer has been shown broken down into its three major subsections: the status buffer, the transmit data/command buffer, and the receive data buffer.

#### negative voltage level by RS-232-C. In our ravisos

The receiver accepts serial data on the RxD pin and converts it to parallel data according to the appropriate format. When the 8251 is in the asynchronous mode and it is ready to accept a character

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TO I Stab prote Apidw englager owl one or Figure 2. 8251 Block Diagram

(i.e., it is not in the process of receiving a character), it looks for a low level on the RxD line. When it sees the low level, it assumes that it is a START bit and enables an internal counter. At a count equivalent to one-half of a bit time, the RxD line is sampled again. If the line is still low, a valid START bit has probably been received and the 8251 proceeds to assemble the character. If the RxD line is high when it is sampled, then either a noise pulse has occurred on the line or the receiver has become enabled in the middle of the transmission of a character. In either case the receiver aborts its operation and prepares itself to accept a new character. After the successful reception of a START bit the 8251 clocks in the data, parity, and STOP bits, and then transfers the data on the internal data bus to the receive data register. When operating with less than 8 bits, the characters are right-justified. The RxRDY signal is asserted to indicate that a character is available.

In the synchronous mode the receiver simply clocks in the specified number of data bits and transfers them to the receiver buffer register, setting RxRDY. Since the receiver blindly groups data bits into characters, there must be a means of synchronizing the receiver to the transmitter so that the proper character boundaries are maintained in the serial data stream. This synchronization is achieved in the HUNT mode.

In the HUNT mode the 8251 shifts in data on the

RxD line one bit at a time. After each bit is received, the receiver register is compared to a register holding the SYN character (program loaded). If the two registers are not equal, the 8251 shifts in another bit and repeats the comparison. When the registers compare as equal, the 8251 ends the HUNT mode and raises the SYNDET line to indicate that it has achieved synchronization. If the USART has been programmed to operate with two SYN characters the process is as described above. except that two contiguous characters from the line must compare to the two stored SYN characters before synchronization is declared. Parity is not checked. If the USART has been programmed to accept external synchronization, the SYNDET pin is used as an input to synchronize the receiver. The timing necessary to do this is discussed in the SIGNALS section of this note. The USART enters the HUNT mode when it is initialized into the synchronous mode or when it is commanded to do so by the command instruction. Before the receiver is operated, it must be enabled by the RxE bit (D<sub>2</sub>) of the command instructions. If this bit is not set the receiver will not assert the RxRDY bit.

#### Transmitter and off the USART's internal and also steep

The transmitter accepts parallel data from the processor, adds the appropriate framing information, serializes it, and transmits it on the TxD pin. In the asynchronous mode the transmitter always

programmed, it also adds an optional even or odd parity bit, and either 1, 1½, or 2 STOP bits. In the synchronous mode no extra bits (other than parity, if enable) are generated by the transmitter unless the computer fails to send a character to the USART. If the USART is ready to transmit a character and a new character has not been supplied by the computer, the USART will transmit a SYN character. This is necessary since synchronous communications, unlike asynchronous communications, does not allow gaps between characters. If the USART is operating in the dual SYN mode. both SYN characters will be transmitted before the message can be resumed. The USART will not generate SYN characters until the software has supplied at least one character; i.e., the USART will fill 'holes' in the transmission but will not initiate transmission itself. The SYN characters which are to be transmitted by the USART are specified by the software during the initialization procedure. In either the synchronous or asynchronous modes, transmission is inhibited until TxEnable and the CTS input are asserted.

An additional feature of the transmitter is the ability to transmit a BREAK. A BREAK is a period of continuous SPACE on the communication line and is used in full duplex communication to interrupt the transmitting terminal. The 8251 USART will transmit a BREAK condition as long as bit 3 (SBRK) of the command register is set.

# registers compare as equal, the lortnon mabom

The modem control section provides for the generation of RTS and the reception of CTS. In addition, a general purpose output and a general purpose input are provided. The output is labeled DTR and the input is labeled DSR. DTR can be asserted by setting bit 2 of the command instruction; DSR can be sensed as bit 7 of the status register. Although the USART itself attaches no special significance to these signals, DTR (Data Terminal Ready) is normally assigned to the modem, indicating that the terminal is ready to communicate and DSR (Data Set Ready) is a signal from the modem indicating that it is ready for communications.

#### of the command instructions. If this biloration O/I

The Read/Write Control Logic decodes control signals on the 8080 control bus into signals which gate data on and off the USART's internal bus and controls the external I/O bus (DB<sub>0</sub>—DB<sub>7</sub>). The truth table for these operations is as follows:

If neither READ or WRITE is a zero, then the USART will not perform an I/O function. READ

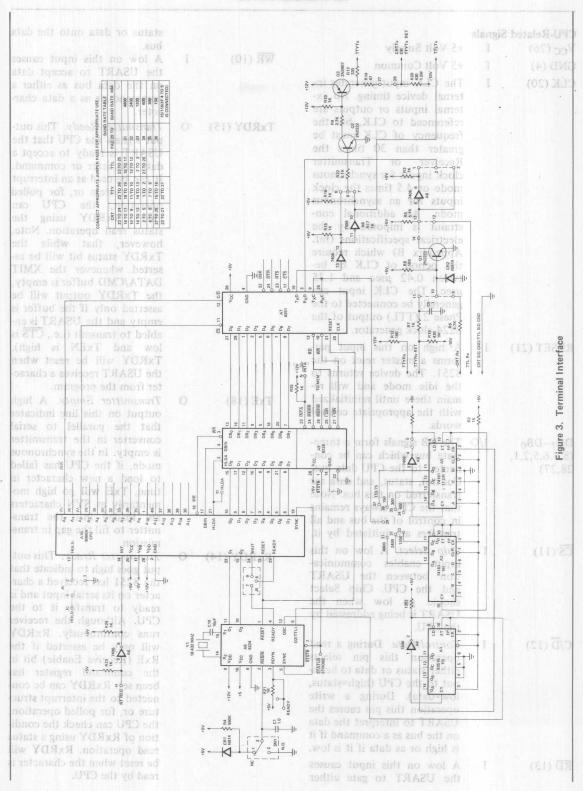
1	CE	C/D	KEAD	WRITE	Function
(	0	0	0	1	CPU Reads Data from USART
7	0	TUTA TSTR	0	1	CPU Reads Status from USART
CIRC	0	0	1	0	CPU Writes Data to USART
	0	1	1	0	CPU Writes Command to USART
	1	X	X	X	USART Bus Floating (NO-OP)

and WRITE being a zero at the same time is an illegal state with undefined results. The Read/Write Control Logic contains synchronization circuits so that the READ and WRITE pulses can occur at any time with respect to the clock inputs to the USART.

The I/O buffer contains the STATUS buffer, the RECEIVE DATA buffer and the XMIT DATA/ CMD buffer as shown in Figure 2. Note that although there are two registers which store data for transfer to the CPU (STATUS and RECEIVE DATA), there is only one register which stores data being transferred to the USART. The sharing of the input register for both transmit data and commands makes it important to ensure that the USART does not have data stored in this register before sending a command to the device. The TxRDY signal can be monitored to accomplish this. Neither data nor commands should be transferred to the USART if TxRDY is low. Failure to perform this check can result in erroneous data being transmitted.

# INTERFACE SIGNALS

The interface signals of the 8251 USART can be broken down into two groups - a CPU-related group and a device-related group. The CPU-related signals have been designed to optimize the attachment of the 8251 to a MCS-80<sup>TM</sup> system. The device-related signals are intended to interface a modem or like device. Since many peripherals (TTY, CRT, etc.) can be obtained with a modemlike interface, the USART has a broad range of applications which do not include a modem. Note that although the USART provides a logical interface to an EIA-RS-232 device, it does not provide EIA compatible drive, and this must be added via circuitry external to the 8251. As an example of a peripheral interface application and to aid in understanding the signal descriptions which follow, Figure 3 shows a system configured to interface with a TTY or CRT.



CPU-Related S					status or data onto the data
V <sub>CC</sub> (26)	I	+5 Volt Supply	WR (10)	I	bus.  A low on this input causes
GND (4) CLK (20)	I	+5 Volt Common  The CLK input generates internal device timing. No external inputs or outputs are	WK (10)		the USART to accept data on the data bus as either a command or as a data char- acter.
		referenced to CLK, but the frequency of CLK must be greater than 30 times the Receiver or Transmitter clock inputs for synchronous mode or 4.5 times the clock inputs for an asynchronous mode. An additional constraint is imposed by the electrical specifications (ref. Appendix B) which require the period of CLK be between 0.42 µsec and 1.35 µsec. The CLK input can generally be connected to the Phase 2 (TTL) output of the 8224 clock generator.	TxRDY (15)	0	Transmitter Ready. This output signals the CPU that the USART is ready to accept a data character or command. It can be used as an interrupt to the system or, for polled operation, the CPU can check TxRDY using the status read operation. Note, however, that while the TxRDY status bit will be asserted whenever the XMIT DATA/CMD buffer is empty, the TxRDY output will be asserted only if the buffer is empty and the USART is en-
RESET (21)	1 (26) 38 (36)	A high on this input performs a master reset on the 8251. The device returns to the idle mode and will remain there until reinitialized with the appropriate control words.	TxE (18)	0	abled to transmit (i.e., CTS is low and TxEN is high). TxRDY will be reset when the USART receives a character from the program.  Transmitter Empty. A high output on this line indicates that the parallel to serial
DB <sub>7</sub> -DB <sub>0</sub> (8,7,6,5,2,1, 28,27)	I/O	The DB signals form a three-state bus which can be connected to the CPU data bus. Control, status, and data are transferred on this bus. Note that the CPU always remains in control of the bus and all transfers are initiated by it.			converter in the transmitter is empty. In the synchronous mode, if the CPU has failed to load a new character in time, TxE will go high momentarily as SYN characters are loaded into the transmitter to fill the gap in transmitter.
CS (11)	. I	Chip Select. A low on this input enables communication between the USART and the CPU. Chip Select should go low when the USART is being addressed by the CPU.	RxRDY (14)	0	mission.  Transmitter Ready. This output goes high to indicate that the 8251 has received a character on its serial input and is ready to transfer it to the CPU. Although the receiver
C/D (12)	I	Control/Data. During a read operation this pin selects either status or data to be input to the CPU (high=status, low=data). During a write operation this pin causes the USART to interpret the data			runs continuously, RxRDY will only be asserted if the RxE (Receive Enable) bit in the command register has been set. RxRDY can be connected to the interrupt structure or, for polled operation,
RD (13)	I	on the bus as a command if it is high or as data if it is low.  A low on this input causes the USART to gate either			the CPU can check the condi- tion of RxRDY using a status read operation. RxRDY will be reset when the character is read by the CPU.

SYNDET (16) I/O Synch Detect. This line is used in the synchronous mode only It can be either an input or output, depending on whether the initialization program sets the USART for external or internal synchronization. SYN-DET is reset to a zero by RE-SET. When in the internal synchronization mode, the USART uses SYNDET as an output to indicate that the device has detected the required SYN character(s). A high output indicates synchronization has been achieved. If the USART is programmed to operate with double SYN characters. SYN-DET will go high in the middle of the last bit of the second SYN character. SYN-DET will be reset by a status read operation. When in the external synchronization mode a positive-going input on the SYNDET line will cause the 8251 to start assembling characters on the next falling edge of RxC. The high input should be maintained at least for one RxC cycle following (00 = od (d) about his edge. this field controls the synchronizing process. Note

Device-Related Signals DTR (24) O Data Terminal Ready. This is a notes in order value general purpose output signal of radiadw word which can be set low by pro-UTO and bloods are gramming a '1' in command instruction bit 1. This signal and notionated about allows additional device con-

appropriate SYN characte.lort, characters) must be DSR (22) I Data Set Ready. This is a genmos smas edt vd be eral purpose input signal. The status of this signal can be show and more sent tested by the CPU through a osisio MY2 owi to status read. This pin can be used to test device status and on rodman bottoper is read as bit 7 of the status register.

RTS (23) O Request to Send. This is a genanonomica et eral purpose output signal off of bourse a sequivalent to DTR. RTS is normally used to request that -small pland said mathe modem prepare itself to of Control of transmit (i.e., establish carnt myoda at noito rier). RTS can be asserted

in the command instruction CTS (17) Clear to Send. A low on this input enables the USART to transmit data. CTS is normally generated by the modem in response to a RTS.

(brought low) by setting bit 5

RxC (25) Receiver Clock. This clock controls the data rate of characters to be received by the USART. In the synchronous mode RxC is equivalent to the baud rate, and is supplied by the modem. In asynchronous mode RxC is 1, 16, or 64 times the baud rate. The clock division is preselected by the mode control instruction. Data is sampled by the USART on the rising edge of RxC.

RxD (3) Receiver Data. Characters are received serially on this pin and assembled into parallel characters. RxD is high true (i.e., High = MARK or ONE).

 $\overline{\text{TxC}}$  (9) Transmitter Clock. This clock controls the rate at which characters are transmitted by the USART. The relationship between clock rate and baud rate is the same as for RxC Data is shifted out of the USART on the falling edge of TxC

TxD (19) Transmit Data Parallel characters sent by the CPU are transmitted serially by the USART on this line. TxD is high true lorings show sall o(i.e., High = MARK or ONE).

## MODE SELECTION 2 THOU as bottsblanco ad nac

The 8251 USART is capable of operating in a number of modes (e.g., synchronous or asynchronous). In order to keep the hardware as flexible as possible (both at the chip and end product level), these operating modes are selected via a series of control outputs to the USART. These mode control outputs must occur between the time the USART is reset and the time it is utilized for data transfer. Since the USART needs this information to structure its internal logic it is essential to complete the initialization before any attempts are made at data transfer (including reading status).

A flowchart of the initialization process appears in Figure 4. The first operation which must occur following a reset is the loading of the mode control

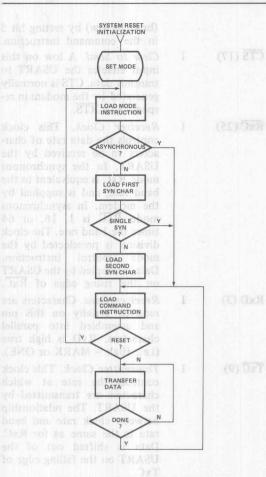


Figure 4. Initialization Flowchart

register. The mode control register is loaded by the first control output  $(C/\overline{D}=1, \overline{RD}=1, \overline{WR}=0, \overline{CS}=0)$ following a reset. The format of the mode control instruction is shown in Figure 5. The instruction can be considered as four 2-bit fields. The first 2-bit field (D<sub>1</sub> D<sub>0</sub>) determines whether the USART is to operate in the synchronous (00) or asynchronous mode. In the asynchronous mode this field also controls the clock scaling factor. As an example, if  $D_1$  and  $D_0$  are both ones, the  $\overline{RxC}$  and  $\overline{TxC}$ will be divided by 64 to establish the baud rate. The second field, D<sub>3</sub>-D<sub>2</sub>, determines the number of data bits in the character and the third, D<sub>5</sub>-D<sub>4</sub>, controls parity generation. Note that the parity bit (if enabled) is added to the data bits and is not considered as part of them when setting up the character length. As an example, standard ASCII transmission, which is seven data bits plus even parity, would be specified as:

following a resex X X 1 1 1 1 1 0 X X x see a griwoffel

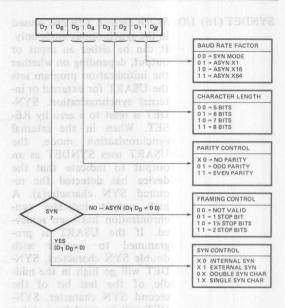


Figure 5. Mode Instruction Format

The last field, D7-D6, has two meanings, depending on whether operation is to be in the synchronous or asynchronous mode. For the asynchronous mode (i.e.,  $D_1$   $D_0 \neq 00$ ), it controls the number of STOP bits to be transmitted with the character. Since the receiver will always operate with only one STOP bit, D7 and D6 only control the transmitter. In the synchronous mode  $(D_1 D_0 = 00)$ , this field controls the synchronizing process. Note that the choice of single or double SYN characters is independent of the choice of internal or external synchronization. This is because even though the receiver may operate with external synchronization logic, the transmitter must still know whether to send one or two SYN characters should the CPU fail to supply a character in time.

Following the loading of the mode instruction the appropriate SYN character (or characters) must be loaded if synchronous mode has been specified. The SYN character(s) are loaded by the same control output instruction used to load the mode instruction. The USART determines from the mode instruction whether no, one, or two SYN characters are required and uses the control output to load SYN characters until the required number are loaded.

At completion of the load of SYN characters (or after the mode instruction in the asynchronous mode), a command character is issued to the USART. The command instruction controls the operation of the USART within the basic framework established by the mode instruction. The format of the command instruction is shown in

Figure 6. Note that if, as an example, the USART is waiting for a SYN character load and instead is issued an internal reset command, it will accept the command as a SYN character instead of resetting. This situation, which should only occur if two independent programs control the USART, can be avoided by outputting three all zero characters as commands before issuing the internal reset command. The USART indicates its state in a status register which can be read under program control. The format of the status register read is shown in Figure 7.

When operating the receiver it is important to realize that RxE (bit 2 of the command instruction) only inhibits the assertion of RxRDY; it does not inhibit the actual reception of characters. Because the receiver is constantly running, it is possible for it to contain extraneous data when it is enabled. To avoid problems this data should be read from the USART and discarded. The read should be done immediately following the setting of Receive Enable in the asynchronous mode, and following the setting of Enter Hunt in the synchronous mode. It is not necessary to wait for RxRDY before executing the dummy read.

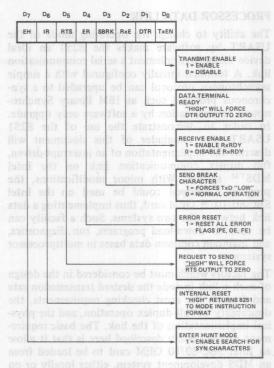
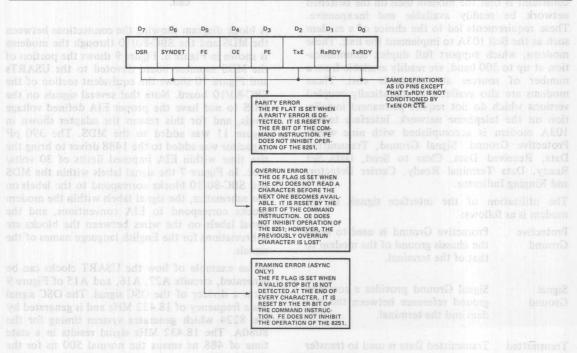


Figure 6. Command Instruction Format



applicance AUSUS ethicity don each and Figure 7. Status Register Format and another stable language.

#### PROCESSOR DATA LINK

The ability to change the operating mode of the USART by software makes the 8251 an ideal device to use to implement a serial communication link. A terminal initially configured with a simple asynchronous protocol can be upgraded to a synchronous protocol such as IBM Binary Synchronous Communication by a software only upgrade. In order to demonstrate the use of the 8251 USART, the remainder of this document will describe the implementation of an interrupt-driven, full duplex communication link on the Intel MDSTM system. With minor modifications, the program developed could be used on the Intel SBC-80/10<sup>TM</sup> OEM card, thus implementing a data link between the two systems. Such a facility can be used to down-load programs, run diagnostics, and maintain common data bases in multiprocessor systems.

The factors which must be considered in the design of such a link include the desired transmission rate and format, the error checking requirements, the desirability of full duplex operation, and the physical implementation of the link. The basic requirement of the system described here is that it allow an Intel SBC-80/10 OEM card to be loaded from an MDS development system, either locally or on the switched telephone network. An additional constraint is that the modem used on the switched network be readily available and inexpensive. These requirements led to the choice of a modem such as the Bell 103A to implement the link. These modems, which support full duplex communication at up to 300 baud, are readily available from a number of sources at reasonable cost. These modems are also available in acoustically coupled versions which do not require permanent installation on the telephone network. Interface to the 103A modem is accomplished with nine wires: Protective Ground, Signal Ground, Transmitted Data, Received Data, Clear to Send, Data Set Ready, Data Terminal Ready, Carrier Detector, and Ringing Indicator.

The utilization of the interface signals to the modem is as follows:

Protective	Protective Ground is used to bond
Ground	the chassis ground of the modem to
	that of the terminal.

Signal	Signal Ground provides a common
Ground	ground reference between the mo-
	dem and the terminal.

Transmitted	Transmitted Data is used to transfer
Data	serial data from the terminal to the
	modem.

Data teni bos	Received Data is used to transfer serial data from the modem to the terminal.
Send i bness SART, can be characters as	ready to transmit data.
Data Set Ready	Data Set Ready indicates that the modem is connected to the telephone line and is in the data mode.
Data Terminal	Data Terminal Ready is a signal from the terminal which permits the modem to enter the data mode.
Carrier Y Detector Stores	Carrier Detector is identical to Clear to Send in the 103 modem and will not be used in this interface.
	from the telephone system. This signal will not be used in the interface, since it is possible for the

A block diagram showing the connections between the MDS and the SBC-80/10 through the modems is shown in Figure 8. Figure 9 shows the portion of the MDS monitor board devoted to the USARTs and Figure 10 shows the equivalent section of the SBC-80/10 board. Note that several signals on the MDS to not have the proper EIA defined voltage levels, and for this reason the adapter shown in Figure 11 was added to the MDS. The 390 pF capacitor was added to the 1488 driver to bring the rise time within EIA imposed limits of 30 volts/ usec. In Figure 7 the signal labels within the MDS and SBC-80/10 blocks correspond to the labels on the schematics, the signal labels within the modem blocks correspond to EIA conventions, and the signal labels on the wires between the blocks are abbreviations for the English language names of the signals.

As an example of how the USART clocks can be generated, circuits A27, A16, and A15 of Figure 9 form a divider of the OSC signal. The OSC signal has a frequency of 18.432 MHz and is generated by the 8224 which generates system timing for the 8080A. The 18.432 MHz signal results in a state time of 488 ns versus the normal 500 ns for the 8080A. (This does not violate 8080A specifications.) The 18.432 MHz signal can be divided by

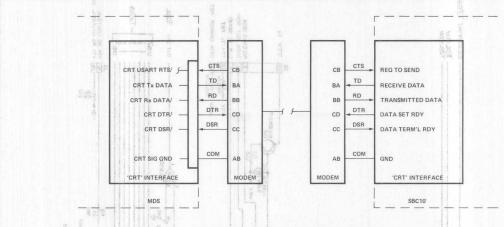
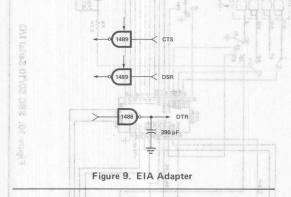


Figure 8. System Block Diagram



30 and then 64 to give a 9600 baud communication standard. The 9600 baud signal can be further divided to give 4800, 2400, 1200, 600, and 300 baud signals. The 1200 baud signal can be divided by 11 to give a 109.1 baud signal which is within 1% of the 110 baud standard signal rate. Note that because of constraints on the CLK input 9600 baud operation is not possible in the X64 mode. The divide by 64 can be accomplished by dividing by 4 with a counter and then 16 within the USART.

In order to keep the system as general purpose as possible, it was decided to transmit 8-bit data characters with an appended odd parity bit. Having a full 8-bit byte available for data enables the transmission of codes such as ASCII (which is 7-level with an additional parity bit) to be transmitted and received transparently in the system. Also, of course, it allows 8-bit bytes from the 8080A memory to be transferred in one transmission character. If error checking beyond the parity check is required, it could be added to the data record to be transmitted in the form of redundant check characters.

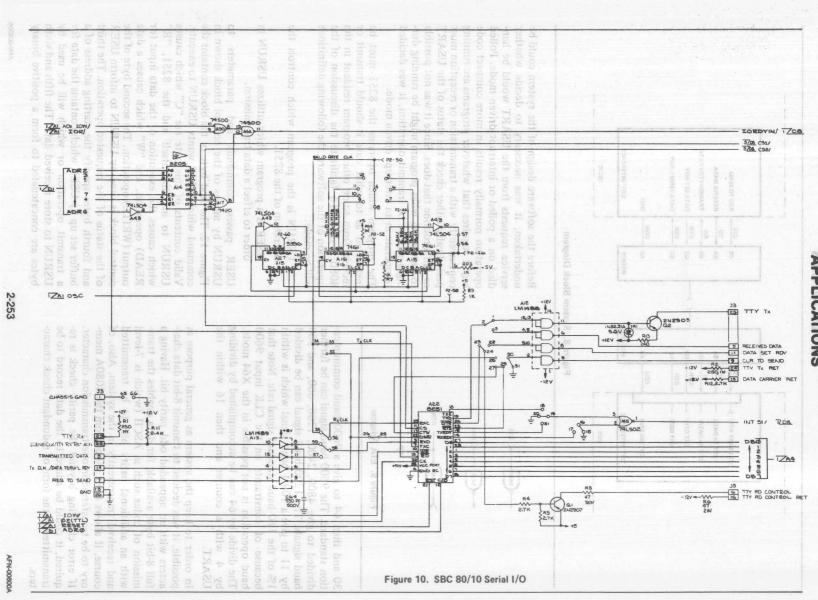
Before the software design of the system could be undertaken, it was necessary to decide whether service requests from the USART would be handled on a polled or interrupt driven mode. Polled operation normally results in more compact code but it requires that whatever programs are running concurrently with a transmission or reception must periodically either check the status of the USART or call a routine that does. Since it was not possible to determine what program might be running during a receive or transmit operation, it was decided to operate in an interrupt driven mode.

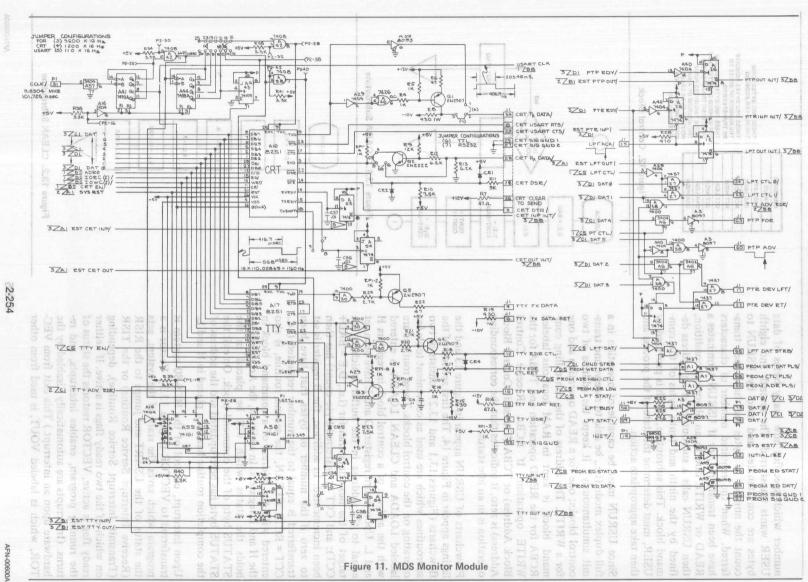
The program which operates the 8251 must be instructed as to what data it should transmit or receive from some other program resident in the 8080 system. To facilitate the discussion of the operation of the software, the following definitions will be made:

USRUN is the program which controls the operation of the 8251.

USER is a program which utilizes USRUN in order to effect a data transmission.

USER passes commands and parameters to USRUN by means of the control block shown in Figure 12. The first byte of the block contains the command which USER wants USRUN to execute. Valid contents of this byte are "C" which causes USRUN to initialize itself and the 8251, "R" which causes the execution of the data input (or READ) operation, and "W" which causes a data output (WRITE) operation. The second byte of the control block is used by USRUN to inform USER of the status of the requested operation. The third and fourth bytes specify the starting address of a buffer set up by USER which contains the data for a transmit operation or which will be used by USRUN to store received data. The fifth and sixth bytes are concatenated to form a positive binary





number which specifies how many bytes of data USER wants transferred. The seventh and eighth bytes are concatenated and used by USRUN to count the number of bytes that have been transferred. When the required number of characters have been transferred, or if USRUN terminates a READ or WRITE due to an abnormal condition, then USRUN calls a subroutine at an address defined by the ninth and tenth bytes of the command block. This subroutine, which is provided by USER, must determine the state of the process and then take appropriate action.

Since USRUN must be capable of operation in a full duplex mode (i.e., be able to receive and transmit simultaneously), it keeps the address of two control blocks; one for a READ operation and one for a WRITE. The address of the controlling command block is kept in RAM locations labeled RCBA for the READ operation and TCBA for the WRITE operation. If RCBA (Receive Control Block Address) or TCBA (Transmit Control Block Address) is zero, it indicates that the corresponding operation is in an idle status.

Flowcharts of USRUN appear in Figure 13 and the listings appear in Figure 14. The first section of the flowcharts (Figures 13.1 and 13.2) consists of two subroutines which are used as convenient tools for operating on the control blocks. These routines are labeled LOADA and CLEAN. LOADA is entered with the address of a control block in registers H and L. Upon return registers D and E have been set equal to the address in the buffer which is the target of the next data transfer (i.e., D,E = BAD+ CCT); and CCT (transferred byte count) has then been incremented. In addition, the B register is set to zero if the number of bytes that have been transferred is equal to the number requested (i.e., CCT = RCT). CLEAN, the second routine, is also entered with the address of a command block in the H and L registers. In addition, the Accumulator holds the status which will be placed in the STATUS byte of the command block. On exit the STATUS byte has been updated and the address of the completion routine has been placed in H and L.

Upon interrupt, control of the MCS-80 system is transferred to VECTOR (Figure 13.3). Vector is a program which saves the state of the system, gets the status of the USART and jumps to the RISR (Receive Interrupt Service Routine) or the TISR (Transmit Interrupt Service Routine), depending on which of the two ready flags is active. If neither ready flag is active, VECTOR restores the status of the running program, enables interrupts, and returns. (Interrupts are automatically disabled by the hardware upon an interrupt.) This exit from VEC-TOR, which is labeled VOUT, is used from other

	COMMAND	
-	STATUS	
	BAD LOW	
	BAD HIGH	
1	RCT LOW	
	RCT HIGH	
19	CCT LOW	
	CCT HIGH	13
3	CRA LOW	-
1	CRA HIGH	
-		

THESE TWO BYTES FORM THE BUFFER ADDRESS THESE TWO BYTES INDICATE THE NUMBER OF BYTES TO BE TRANSFERRED THESE TWO BYTES INDICATE THE NUMBER OF BYTES THAT HAVE BEEN TRANSFERRED THESE TWO BYTES FORM THE ADDRESS OF A SUB ROUTINE TO BE CALLED WHEN THE OPERATION IS TERMINATED

Figure 12 Control Block

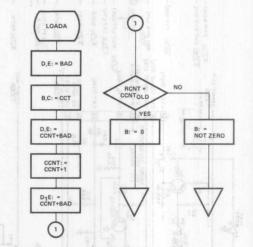
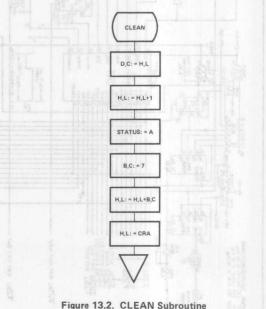


Figure 13.1. LOADA Subroutine



PUSH STATUS

PUSH STATUS

INPUT USART
STATUS

REPORT

Figure 13.3. Interrupt Entry

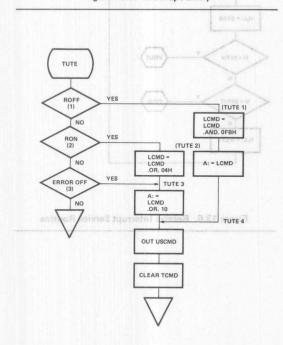


Figure 13.4. Transmit Interrupt Service Routine

portions of USRUN if return from the interrupt mode is required.

In addition to handling normal data transfers, TISR (Figure 13.4) checks a location in memory named TCMD in order to determine if the receive program wishes to send a command to the USART. Since the transmit data and command must share a buffer within the USART, any command output must occur when TxRDY is asserted. If TCMD is zero, TISR proceeds with the data transfer. If TCMD is non-zero, TISR calls TUTE (Transmit Utility, Figure 13.5) which, depending on the value

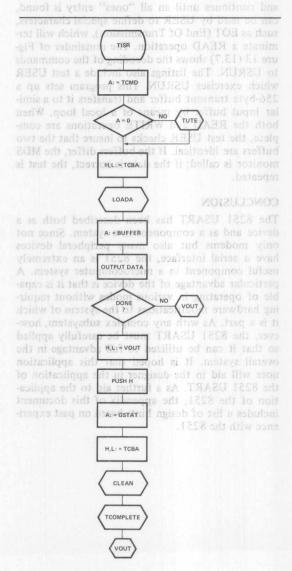


Figure 13.5. Transmit Utility Routine

first enabled. engine settermine and TCMD in order to determine

The flowchart of the RISR is shown in Figure 13.6. Note that in addition to terminating whenever the required number of characters have been received, the RISR also terminates if one of the error flags becomes set or if the received character matches a character found in a table pointed to by the label ETAB. This table, which starts at ETAB and continues until an all "ones" entry is found, can be used by USER to define special characters, such as EOT (End Of Transmission), which will terminate a READ operation. The remainder of Figure 13 (13.7) shows the decoding of the commands to USRUN. The listings also include a test USER which exercises USRUN. This program sets up a 256-byte transmit buffer and transfers it to a similar input buffer by means of a local loop. When both the READ and WRITE operations are complete, the test USER checks to insure that the two buffers are identical. If the buffers differ, the MDS monitor is called; if the data is correct, the test is repeated.

#### CONCLUSION

The 8251 USART has been described both as a device and as a component in a system. Since not only modems but also many peripheral devices have a serial interface, the 8251 is an extremely useful component in a microcomputer system. A particular advantage of the device is that it is capable of operating in various modes without requiring hardware modifications to the system of which it is a part. As with any complex subsystem, however, the 8251 USART must be carefully applied so that it can be utilized to full advantage in the overall system. It is hoped that this application note will aid in the designer in the application of the 8251 USART. As a further aid to the application of the 8251, the appendix of this document includes a list of design hints based on past experience with the 8251.

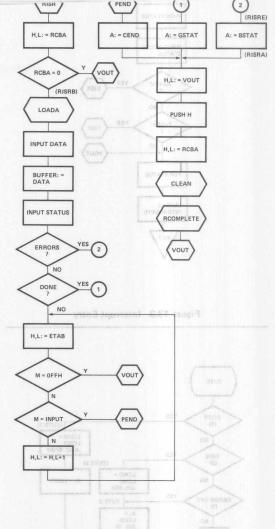


Figure 13.6. Receive Interrupt Service Routine



Figure 13.5. Transmit Utility Routin

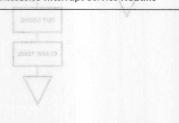


Figure 13.4. Transmit Interrupt Service Routine

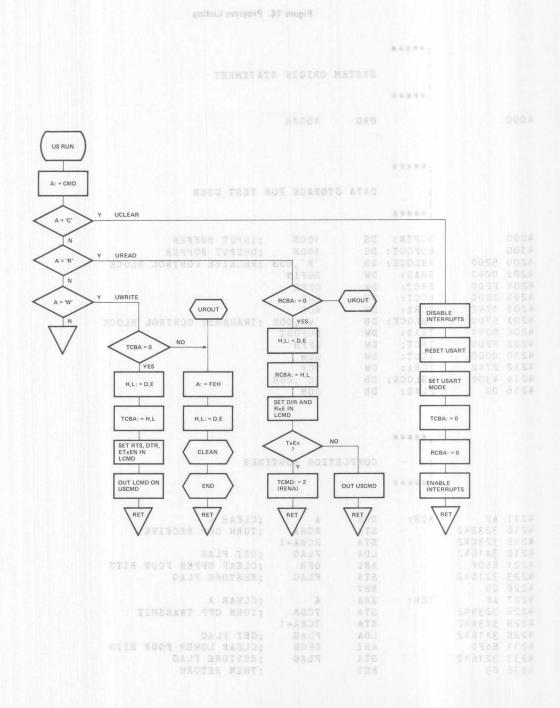


Figure 13.7. URUN Command Decode

Figure 14. Program Listing

```
. * * * *
                        SYSTEM ORIGIN STATEMENT
               ; * * * * *
4000
                        ORG
                                4000H
               : * * * * *
                       DATA STORAGE FOR TEST USER
               ; * * * * *
4000
               BUFIN: DS
                               100H ; INPUT BUFFER
4100
               BUFOUT: DS
                                100H ; OUTPUT BUFFER
4200 5200
                                'R', OOH ; RECEIVE CONTROL BLOCK
               RBLOCK: DB
4202 0040
               RBAD: DW
                                BUFIN
4204 FF00
               RRCT:
                       DW
                                OFFH
4206 0000
               RCCT:
                       DW
                                00H
4208 1742
               RCRA:
                       DW
                                RCR
420A 5700
               TBLOCK: DB
                                'W', OOH ; TRANSMIT CONTROL BLOCK
420C 0041
               TBAD: DW
                                BUFOUT
420E FF00
               TRCT:
                       DW
                                OFFH
4210 0000
               TCCT:
                       DW
                                OOH
4212 2742
               TCRA:
                       DW
                                TCR
4214 4300
                                'C',00H
               GBLOCK: DB
4216 00
               FLAG:
                       DB
                                OOH
                       COMPLETION ROUTINES
                                A THE
4217 AF
               RCR:
                       XRA
                                         ;CLEAR A
4218 323B42 V
                       STA
                                         ; TURN OFF RECEIVE
                                RCBA
421B 323C42
                       STA
                                RCBA+1
421E 3A1642
                       LDA
                                FLAG
                                        GET FLAG
4221 E60F
                                OFH
                       ANI
                                        ;CLEAR UPPER FOUR BITS
4223 321642
                       STA
                                FLAG
                                        ; RESTORE FLAG
4226 C9
                       RET
4227 AF
               TCR:
                       XRA
                                        :CLEAR A
4228 323942
                       STA
                                TCBA
                                        ; TURN OFF TRANSMIT
422B 323A42
                       STA
                                TCBA+1
422E 3A1642
                       LDA
                                FLAG
                                        ; GET FLAG
4231 E6F0
                       ANI
                                OFOH
                                         ;CLEAR LOWER FOUR BITS
4233 321642
                       STA
                                FLAG
                                        ; RESTORE FLAG
4236 C9
                       RET
                                        ; THEN RETURN
```

```
: * * * * *
                         SYSTEM EQUATES SMITHOR RESERVOR GROAT
 LOADA IS ENTERED WITH THE ADDRESS OF A CONTROL

BLOCK IN H.L. ON EXIT D.E. CONTAINS THE******; ESS
WHICH IS THE TARGET OF THE NEXT DATA TRANSFER (BAD#CCNT)
 00F5 TO ARAMUM USTAT UPBEQUET TIOF5H 2 OT; USART STATUS ADDRESS
00F5 GETWAMER USCMD TEQU GHROF5HOOD ; USART CMD ADDRESS
           USDAI JAEQUISS COF4H 239 ; USART DATA INPUT ADDRESS
              USDAO EQU OF4H ; USART DATA OUTPUT ADDRESS GSTAT EQU OOH ; GOOD STATUS BSTAT EQU OFFH ; BAD STATUS
 00F4
 0000
              BSTAT EQU OFFH ;BAD STATUS
CEND SHEQU RESIDENCE H XMI RAGAOJ

;*****
; AMOG M. Q. VOM
 OOFF
 0001
```

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```
: * * * *
                                                              LOAD ADDRESS ROUTINE SETAUDE METEYS
                                                             LOADA IS ENTERED WITH THE ADDRESS OF A CONTROL
                                                            BLOCK IN H, L. ON EXIT D, E CONTAINS THE ADDRESS
                                                            WHICH IS THE TARGET OF THE NEXT DATA TRANSFER (BAD+CCNT)
                                                          SCAND B HAS BEEN SET TO ZERO IF THE REQUESTED NUMBER OF 300
                                                              TRANSFERS HAS TBEEN ACCOMPLISHED. UCCNT IS INCREMENTED 3300
                                         ; 223 HO CAFTER THE TARGET SADDRESS HAS BEEN CALCULATED.
                                         USDAO BQU OFH ;USART DATA OUTPUT ADDRESS;
GSTAT EQU OGH ;GOOD STATUS *****;
BSTAT EQU OFFH ;BAD STATUS
 423E 23
                                         LOADA: INX
                                                                                H ; D, E GETS BUFFER ADDRESS MBO
 423F 23
                                                              INX
                                                                                 Н
 4240 5E
                                                                           E,M
                                                             MOV
 4241 23
                                                             INX
                                                                                 Н
                                                                                                                                                                    ****
                                                           MOV D,M ;DONE
INX H ;B,C GETS COMPLETED COUNT (CCNT)
 4242 56
 4243 23
 4244 23
                                                            INX H
4245 23
                                                            INX H
MOV C, M
                                                                                                                                                                       安存 等 20 0
 4246 4E
#257 00 LCMD: DB 00H ; CURRENTIXALCOMMAND TO BE SENT 34 8454 4258 00 TCMD: DB 00H 30OC; NON M780 A CVOMAND TO BE SENT 34 8454 4259 0000 TCBA: DTAND+CAGO TCBA: 
 424C 03
                                                              INX B
                                                                                                        :CCNT GETS INCREMENTED
 424D 70
                                                              MOV
                                                                                    M.B
 424E 2B
                                                              DCX
                                                                                     H
 424F 71
                                                              MOV
                                                                                     M.C
                                                                                                        ; DONE
 4250 OB
                                                              DCX
                                                                                     В
                                                                                                           ; DOES OLD CCNT=RCNT?
 4251 2B
                                                            DCX
                                                                                     Н
 4252 7E
                                                            MOV
                                                                                     A, M
 4253 90
                                                              SUB
                                                                                      В
 4254 47
                                                             MOV
                                                                                    B, A
 4255 CO
                                                             RNZ
                                                                                                            ; NO-RETURN WITH B NOT ZERO
 4256 2B
                                                             DCX
                                                                                    Н
 4257 7E
                                                             MOV
                                                                                   A, M
 4258 91
                                                              SUB
                                                                                     C
4259 47
                                                             VOM
                                                                                    B, A
 425A C9
                                                              RET
                                                                                                            ; RETURN WITH B=O IF RCNT=CCNT
```

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CLEAN-UP ROUTINESSE TSUSSINI SVISOSS ; THURSCLEANVIS ENTERED WITH THE ADDRESS OF A CONTROL GHT; 9902 HBLOCKTIN H, DHAND AGNEW STATUS TO BE MA WIST THE ENTEREDZINTOTITOINNA. TONGEXIT THE ADDRESS OF THE ; CONTROL BLOCK IS IN D.E; THE STATUS OF THE BLOCK HAS BEEN UPDATED; AND THE ADDRESS OF THE COMPLETION ROUTINE IS IN H,L.

```
: * * * * *
                                                                                            4288 2A3B42 RISH: LHLD RCBA #MDS-CLEAR RECEIVE INTERUPT 428B 3E82 OUT 0F3H :MDS
                                                                                      CLEAN: MOV E,L ;SAVE THE ADRESS OF THE COMMAND BLOCK BSA COMMAND B
      425B 5D
      425C 54
     425D 23
      425E 77
     425F 010700
4262 09
     4263 7E
      4264 23
      4265 66
      4266 6F
      4267 C9
                                                                                                                                   VECTOR SAVES THE STATUS OF THE RUNNING PROGRAM ODES DASH
                                                                                                                                        THEN READS THE STATUS OF THE USART TO DETERMINE SPECIES HAS !
                                                                                            ; MOAT & SIF ATRECEIVE OR TRANSMIT INTERUPT OCCURRED.
                                                                                            ; NOOLH OVECTOR THEN CALLS THE APPROPRIATE SERVICE ROUTINE SEAS SES#
                                                                                                                                   SIFTNEITHERAINTERUPTS OCCURRED THENAVECTOR RESTORES 300 384
                                     BUITUOH W: ITBU THE STATUS OF THE RUNNING PROGAM, HTHE SERVICE 02 8454
HERE STANDERS USE THE EXIT CODE, LABLED VOUT, TO EFFECT

THEIR EXIT FROM INTERUPT MODE

HARD STAND BETT AND ASSESSED BEST OF THE STAND BETT AND ASSESSED BET
                                          H H209 %; SSUADEROUTINESTUSE THETEXIT CODE, LABLED VOUT, TO EFFECT
```

POP B
MVI A,20H; MDS-RESTORE CURRENT LEVEL
OUT OFDH; MDS
EI; ENABLE INTERUPT MI 4283 D3FD 4286 FB 4287 C9

POP D

427F D1

4280 C1 4281 3E20

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; RECEIVE INTERUPT SERVICE ROUTINE;
; RECEIVE INTERUPT
; AT THE END OF RECEIVE THE USER SUPPLIED
; COMPLETION ROUTINE IS CALLED AND THEN AN
; EXIT IS TAKEN THROUGH VOUT OF THE

VECTOR

NOUTINE IS IN H. L.

```
4288 2A3B42 RISR: LHLD RCBA
428B 3E82 MVI A,82H ;MDS-CLEAR RECEIVE INTERUPT
428D D3F3 OUT OF3H ;MDS
428F 2C INR L
4290 2D DCR L
4291 C29942 JNZ RISRB
4295 25 DCR H
4295 25 DCR H
4296 CA7E42 JZ VOUT
4299 CD3E42 RISRB: CALL LOADA ;READY-SET UP ADDRESS
4290 CDBF4 IN USDAI ;GET INPUT DATA
429E 12 STAX D ;AND PUT IN THE BUFFER
429F 4F MOV C,A ;SAVE INPUT DATA IN C
42AO DBF5 IN USTAT ;GET STATUS AGAIN
42A2 E638 ANI 38H ;MASK FOR ERROR FIELD
42A4 C2B942 JNZ RISRE ;NOT ZERO-TAKE ERROR EXIT
42A7 O4 INR B ;B WAS OO IF DONE
42A9 C2BE42 JNZ EXCHAR ;NOT DONE-EXIT
42A0 C2BE42 JNZ EXCHAR ;NOT DONE-EXIT
42A0 C2BE42 JNZ EXCHAR ;NOT DONE-EXIT
42A0 C2BE42 JNZ EXCHAR ;NOT DONE-EXIT
 42AC 3E00 MARGORI MVI A.GSTAT : A GETS GOOD STATUS
 42AE 217E42 RISRA: CLXI AZO H, VOUT Z; GET RETURN ADDRESS
 42B1 E5 GARAUPUSH UNGHUI AMB; AND PUSH IT INTO THE STACK
 42B2 2A3B42 UND BOLVELHLD BEARCHA POINT H, L AT THE CMD BLOCK
 42B5 CD5B42 TBS GCALL CLEAN CLEAN CLEAN CLEANUP ROUTINE
  4288 E9 SOLVERS SPCHL MADORS ON THE EFFECTIVELY CALLS COMPLETION ROUTINE
TOSASS OT THOU OSISAL SACO FRETURN IS TO VOUT BECAUSE OF PUSH H
```

. \* \* \* \*

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TRANSMIT INTERUPT SERVICE ROUTINE

日本等书书:

; \* \* \* \* \*

```
; ZZZZTISR PROCCESSES TRANSMITTER INTERUPTS
                                                                                                                        ; ZEMIMAX WHEN THE END OF A TRANSMISSIONEIS TO
                                                                                       MOIT; RESO GEDETECTED THE USER SUPPLIED COMPLETION
                                                                                                                                                                                   ROUTINE IS CALLED AND THEN AN EXIT IS
                                                                                                                                                                                   TAKEN THROUGH VOUT OF VECTOR
      42D7 B7
42D8 C40443
42D8 3E81
42DB 3E81
42DB 03F3
42DF 2A3942
42DF 2A3942
42DF 3A3942
42DF
     42E2 2C INRTHURELMI BLAKE SURE HAVE VALID CONTROL BLOCK BETTE BLOCK BLOCK BETTE BLOCK BLOCK BLOCK BETTE BLOCK BLOC
```

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: \* \* \* \* \*

```
USART COMMAND BLOCK INTERPRETER
                                            USRUN IS CALLED BY USER WITH THE ADDRESS
                                             OF THE COMMAND BLOCK IN H.L. USRUN EXAMINES
                                             THE BLOCK AND INTIALIZES THE REQUESTED OPERATION
                                            ROUTINE IS CALLED AND THEN AN EXIT IS TAKEN THROUGH YOUT OF VECTOR
  432F 1A USRUN: LDAX D ;GET THE CMD FROM THE BLOCK
4330 FE43 CPI 'C' ;IS IT A CLEAR COMMAND?
4332 CA4043 MJZ O JAUCLEAR ;YES GO TO CLEAR ROUTINE RASE AGEN
4335 FE52 CPI TI M'R'TAMOL;IS IT A READ COMMAND?
4337 CA5D43 JZ MMO UREADIU;YES-GO TO READ ROUTINE RASE AGEN
433A FE57 ZATURCPI TIM'W'ARD ;IS IT A WRITE COMMAND?
433C CA9D43 JZ UWRITE ;GO TO WRITE ROUTINE RESE GOST AGEN
433F C9 RET ;NOT A GOOD COMMAND-RETURN
4377 EB URDA: XCHG ;H GETS COMMAND BLOCK ADDRESS
4378 223B42 SHLD RCBA ;RCBA GETS COMMAND BLOCK ADDRESS
437B 3A3742 LDA LCMD ;GET LAST COMMAND
437E F616 ORI 16H ;SET RXE AND DTR AND RESET ERRORS
4380 323742 STA LCMD ;AND RETURN TO MEMORY
4383 OF RRC ;SET CARRY EQUAL TO TXE
```

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```
JNC URDC
MVI A,2
   4384 D28C43
    4387 3E02
   4389 323842
                                                           MURBU ZESTAREKE TCMDW WARDONS TEST A ET REEU
                                                          URDC: RLC
   438C 07
                                                                                                                           USCMD ;OUTPUT CMD
USDAI ;CLEAR USART OF LEFT OVER CHARACTERS
    438D D3F5
                                                                                            OUT
   438F DBF4
                                                                                            IN
HERE SECS SEERS MVI A DOSH SMOS-SLIADSUS NICTOR
  4391 DBF4
 43AA EB
43AB 223942 SMLD SHLD ORI
                                                             SHLD TCBA TCBA GETS COMMAND BLOCK ADDRESS
                                                          LDA LCMD ; GET LAST COMMAND BLOCK ADDRESS

ORI 023H ; SET RTS, DTR, AND TXEN

STA LCMD
OUT USCMD

MVI A, 0F6H ; MDS-ENABLE LEVEL THREE INTERUPTS
OUT OFCH ; MDS
EI ; ENABLE SYSTEM INTERUPTS
  43B3 323742
  43B6 D3F5
  43B8 3EF6
  43BA D3FC
                                                        ### 221042 STQURATINI MATERY BARMS; IS A STQUENT OF THE STATE OF THE S
  43BC FB
  43BD C9
```

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```
: ****
               USER IS A TEST PROGRAM WHICH EXERCISES USRUN SARESE PREA
    438C OT URDC: BLC
438D D3F5 OUT USCHD ; OUTPUT CHD *****
438F D8F4 IN USDAI ; CLEAR USART OF LEFT OVER CHARACTERS
4416 25
4417 2C
             INR L
4418 C21044 JNZ COMLP
441B C3BE43 JMP USER
441E C7 COMER: RST 0
                      USER ;GOOD COMPARE-REPEAT TEST
                            ; ERROR-RETURN TO MONITOR
0000
                END
```

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BSTAT	OOFF	BUFIN	4000	BUFOU	4100		CEND	0001	
CLEAN	425B	COMER	441E	COMLP	4410		EXA	42C1	
EXCHA	42BE	FLAG	4216	GBLOC	4214		GSTAT	0000	
LCMD	4237	LOADA	423E	MTAB	423D		PEND	42CF	
RBAD	4202	RBLOC	4200	RCBA	423B		RCCT	4206	
RCR	4217	RCRA	4208	RISR	4288		RISRA	42AE	
RISRB	4299	RISRE	42B9	RRCT	4204		TBAD	420C	
TBLOC	420A	TCBA	4239	TCCT	4210		TCMD	4238	
TCR	4227	TCRA	4212	TISR	42D4		TISRA	42EC	
TRCT	420E	TUTE	4304	TUTE1	4324		TUTE2	4314	
TUTE3	431C and 1	TUTE4	4321	UCLEA	4340		URDA	4377	
URDB	4376	URDC	438C	UREAD	435D	-nao le	UROUT	436B	
USCMD	00F5	USDAI	00F4	USDAO	00F4		USER	43BE	
USRUN	432F	USTAT		UWRIT	439D		VECTO	4268	
VOUT	427E								

ing a command it transmission is taking places.

Due to the internal structure of the USART, it is also possible to disturb the transmission if a command is sent while a SYN character is being generated by the cievice. (The USART generates a SYN if the software fails to respond to TARDY.) If this occurrence is possible in a system, commands should be transferred only when ten positive going edge is detacted on the TARDY.

 RxE only acts as a mask to RxRDY; it does not control the operation of the receiver.

When the reneiver is enabled, it is possible for it to already contain one or two characters. These characters should be read and discarded when the RxE bit is first set. Because of these extraneous characters the proper sequence for gaining extratreneixarium is as follows:

- 1. Disable inter upts
- 2. Issue a command to enter hunt mode, clear errors, and enable the receiver (EH,ER,RxE=
- 3. Read USART data (it is not necessary to check status)
  - 4. Enable interrupts

The first RARDY that occurs after the above sequence will indicate that the SYM character or

- Extraneous transitions can occur on TxEmpty while data (including USART generated SYNs) is transferred to the parallel-to-serial converter.

This situation can be avoided by ensuring that TxEmpty occurs during several consecutive status reads before assuming that the transmitter is truly in the empty state.

 A BREAK (i.e., long space) detected by the receiver results in a string of characters which have framing errors.

If reception is to be continued after a BEHAK, our must be taken to ensure that valid data is being received; special care must be taken with the last character perceived during a BREAK, since its value, including any framing error associated with it, is indeterminate.

# APPENDIX A 0000 TATE 8251 DESIGN HINTS

BUSE

1. Output of a command to the USART destroys the integrity of a transmission in progress if timed incorrectly.

Sending a command into the USART will over- #SE# 3. Loss of CTS or dropping TxEnable will immediate write any character which is stored in the buffer OAEA waiting for transfer to the parallel-to-serial converter in the device. This can be avoided by waiting for TxRDY to be asserted before sending a command if transmission is taking place. Due to the internal structure of the USART, it is also possible to disturb the transmission if a command is sent while a SYN character is being generated by the device. (The USART generates a SYN if the software fails to respond to TxRDY.) If this occurrence is possible in a system, commands should be transferred only when a positive-going edge is detected on the TxRDY line.

2. RxE only acts as a mask to RxRDY; it does not control the operation of the receiver.

When the receiver is enabled, it is possible for it to already contain one or two characters. These characters should be read and discarded when the RxE bit is first set. Because of these extraneous characters the proper sequence for gaining synchronization is as follows:

- 1. Disable interrupts
- 2. Issue a command to enter hunt mode, clear errors, and enable the receiver (EH,ER,RxE=
- 3. Read USART data (it is not necessary to check status)
- 4. Enable interrupts

The first RxRDY that occurs after the above sequence will indicate that the SYN character or characters have been detected and the next character has been assembled and is ready to be read.

ately clamp the serial output line.

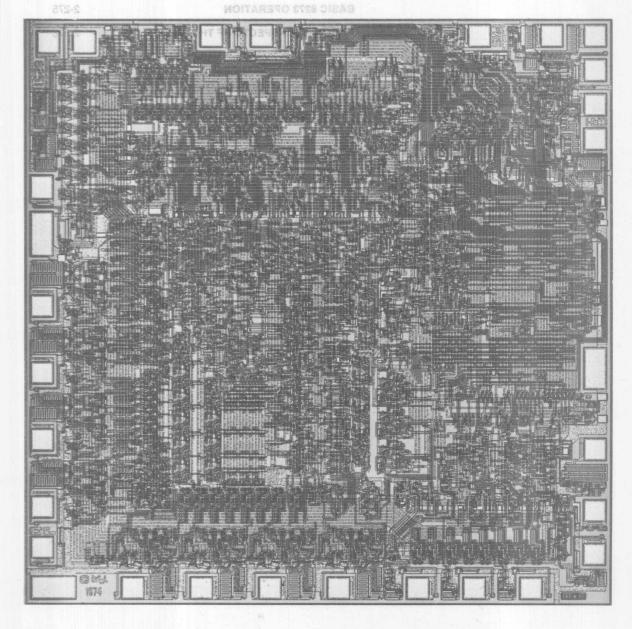
TxEnable and RTS should remain asserted until the transmission is complete. Note that this implies that not only has the USART completed the transfer of all bits of the last character, but also that they have cleared the modem. A delay of 1 msec following a proper occurrence of TxEmpty is usually sufficient (see item 4). An additional problem can occur in the synchronous mode because the loss of TxEnable clamps the data in at a SPACE instead of the normal MARK. This problem, which does not occur in the asynchronous mode, can be corrected by an external gate combining RTS and the serial output data.

- 4. Extraneous transitions can occur on TxEmpty while data (including USART generated SYNs) is transferred to the parallel-to-serial converter. This situation can be avoided by ensuring that TxEmpty occurs during several consecutive status reads before assuming that the transmitter is truly in the empty state.
- 5. A BREAK (i.e., long space) detected by the receiver results in a string of characters which have framing errors.

If reception is to be continued after a BREAK. care must be taken to ensure that valid data is being received; special care must be taken with the last character perceived during a BREAK, since its value, including any framing error associated with it, is indeterminate.

# 8251 PROGRAMMABLE COMMUNICATION INTERFACE

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# 2251 PROGRAMMABLE COMMUNICATION INTERFACE

### Using the 8273 **Contents** SDLC/HDLC INTRODUCTION 2-272 **Protocol Controller** SDLC/HDLC OVERVIEW 2-272 **BASIC 8273 OPERATION** 2-275 HARDWARE ASPECTS OF THE 8273 2-275 CPU Interface Modem Interface **SOFTWARE ASPECTS OF THE 8273** 2-281 Command Phase Software **Execution Phase Software** Result Phase Software 2-284 8273 COMMAND DESCRIPTION Initialization/Configuration Commands Operating Mode Register Serial I/O Mode Register Data Transfer Mode Register One Bit Delay Register Receive Commands General Receive Selective Receive Selective Loop Receive Receive Disable **Transmit Commands** Transmit Frame Loop Transmit Transmit Transparent Abort Commands Reset Commands Modem Control Commands **HDLC CONSIDERATIONS** 2-289 LOOP CONFIGURATION 2-290 **APPLICATION EXAMPLE** 2-294 CONCLUSION 2-299

**APPENDIX** 

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### control field, the Information field is nonocupally

The Intel 8273 is a Data Communications Protocol Controller designed for use in systems utilizing either SDLC or HDLC (Synchronous or High-Level Data Link Control) protocols. In addition to the usual features such as full duplex operation, automatic Frame Check Sequence generation and checking, automatic zero bit insertion and deletion, and TTL compatibility found on other single component SDLC controllers; the 8273 features a frame level command structure, a digital phase locked loop, SDLC loop operation, and diagnostics.

The frame level command structure is made possible by the 8273's unique internal dual processor architecture. A high-speed bit processor handles the serial data manipulations and character recognition. A byte processor implements the frame level commands. These dual processors allow the 8273 to control the necessary byte-by-byte operation of the data channel with a minimum of CPU (Central Processing Unit) intervention. For the user this means the CPU has time to take on additional tasks. The digital phase locked loop (DPLL) provides a means of clock recovery from the received data stream on-chip. This feature, along with the frame level commands, makes SDLC loop operation extremely simple and flexible. Diagnostics in the form of both data and clock loopback are available to simplify board debug and link testing. The 8273 is a dedicated function peripheral in the MCS-80/85 Microcomputer family and as such, it interfaces to the 8080/8085 system with a minimum of external hardware.

This application note explains the 8273 as a component and shows its use in a generalized loop configuration and a typical 8085 system. The 8085 system was used to verify the SDLC operation of the 8273 on an actual IBM SDLC data communications link.

The first section of this application note presents an overview of the SDLC/HDLC protocols. It is fairly tutorial in nature and may be skipped by the more knowledgeable reader. The second section describes the 8273 from a functional standpoint with explanation of the block diagram. The software aspects of the 8273, including command examples, are discussed in the third section. The fourth and fifth sections discuss a loop SDLC configuration and the 8085 system respectively.

# SDLC/HDLC OVERVIEW to sloed a bas sloed 207

SDLC is a protocol for managing the flow of information on a data communications link. In other words, SDLC can be thought of as an envelope — addressed, stamped, and containing an s.a.s.e. — in which information is transferred from location to location on a data communications link. (Please note that while SDLC is discussed specifically, all comments also apply to HDLC except where noted.) The link may be either point-to-point or multi-point, with the point-to-point configuration being either switched or nonswitched. The information flow may use either full or half duplex exchanges. With this many configurations supported, it is difficult to find a synchronous data communications application where SDLC would not be appropriate.

Aside from supporting a large number of configurations. SDLC offers the potential of a 2x increase in throughput over the presently most prevalent protocol: Bi-Sync. This performance increase is primarily due to two characteristics of SDLC: full duplex operation and the implied acknowledgement of transferred information. The performance increase due to full duplex operation is fairly obvious since, in SDLC, both stations can communicate simultaneously. Bi-Sync supports only half-duplex (twoway alternate) communication. The increase from implied acknowledgement arises from the fact that a station using SDLC may acknowledge previously received information while transmitting different information. Up to 7 messages may be outstanding before an acknowledgement is required. These messages may be acknowledged as a block rather than singly. In Bi-Sync, acknowledgements are unique messages that may not be included with messages containing information and each information message requires a separate acknowledgement. Thus the line efficiency of SDLC is superior to Bi-Sync. On a higher level, the potential of a 2x increase in performance means lower cost per unit of information transferred. Notice that the increase is not due to higher data link speeds (SDLC is actually speed independent), but simply through better line utilization.

Getting down to the more salient characteristics of SDLC; the basic unit of information on an SDLC link is that of the frame. The frame format is shown in Figure 1. Five fields comprise each frame: flag, address, control, information, and frame check sequence. The flag fields (F) form the boundary of the frame and all other fields are positionally related to one of the two flags. All frames start with an opening flag and end with a closing flag. Flags are used for frame synchronization. They also may serve as time-fill characters between frames. (There are no intraframe time-fill characters in SDLC as there are in Bi-Sync.) The opening flag serves as a reference point for the address (A) and control (C) fields. The frame check sequence (FCS) is referenced from the closing flag. All flags have the binary configuration 01111110 (7EH).

SDLC is a bit-oriented protocol, that is, the receiving station must be able to recognize a flag (or any other special character) at any time, not just on an 8-bit boundary. This, of course, implies that a frame may be N-bits in length. (The vast majority of applications tend to use frames which are multiples of 8 bits long, however.)

OPENING FLAG	ADDRESS FIELD (A)	CONTROL FIELD (C)	INFORMATION FIELD (I)	FRAME CHECK SEQUENCE (FCS)	CLOSING
01111110	8 BITS	8 BITS	ANY LENGTH 0 TO N BITS	16 BITS	0111111

Figure 1. SDLC Frame Format

received, invalidating the frame. SDLC handles this situation through a technique called zero bit insertion. This techniques specifies that within a frame a binary 0 be inserted by the transmitter after any succession of five contiguous binary 1s. Thus, no pattern of 011111110 is ever transmitted by chance. On the receiving end, after the opening flag is detected, the receiver removes any 0 following 5 consecutive 1s. The inserted and deleted 0s are not counted for error determination.

Before discussing the address field, an explanation of the roles of an SDLC station is in order. SDLC specifies two types of stations: primary and secondary. The primary is the control station for the data link and thus has responsibility of the overall network. There is only one predetermined primary station, all other stations on the link assume the secondary station role. In general, a secondary station speaks only when spoken to. In other words, the primary polls the secondaries for responses. In order to specify a specific secondary, each secondary is assigned a unique 8-bit address. It is this address that is used in the frame's address field.

When the primary transmits a frame to a specific secondary, the address field contains the secondary's address. When responding, the secondary uses its own address in the address field. The primary is never identified. This ensures that the primary knows which of many secondaries is responding since the primary may have many messages outstanding at various secondary stations. In addition to the specific secondary address, an address common to all secondaries may be used for various purposes. (An all 1s address field is usually used for this "All Parties" address.) Even though the primary may use this common address, the secondaries are expected to respond with their unique address. The address field is always the first 8 bits following the opening flag.

The 8 bits following the address field form the control field. The control field embodies the link-level control of SDLC. A detailed explanation of the commands and responses contained in this field is beyond the scope of this application note. Suffice it to say that it is in the control field that the implied acknowledgement is carried out through the use of frame sequence numbers. None of the currently available SDLC single chip controllers utilize the control field. They simply pass it to the processor for analysis. Readers wishing a more detailed explanation of the control field, or of SDLC in general, should consult the IBM documents referenced on the front page overleaf.

In some types of frames, an information field follows the control field. Frames used strictly for link management may or may not contain one. When an information field is used, it is unrestricted in both content and length. This code transparency is made possible because of the zero bit insertion mentioned earlier and the bit-oriented nature of SDLC. Even main memory core dumps may be transmitted because of this capability. This feature is unique to bit-oriented protocols. Like the

The final field is the frame check sequence (FCS). The FCS is the 16 bits immediately preceding the closing flag. This 16-bit field is used for error detection through a Cyclic Redundancy Checkword (CRC). The 16-bit transmitted CRC is the complement of the remainder obtained when the A, C, and I fields are "divided" by a generating polynomial. The receiver accumulates the A, C, and I fields and also the FCS into its internal CRC register. At the closing flag, this register contains one particular number for an error-free reception. If this number is not obtained, the frame was received in error and should be discarded. Discarding the frame causes the station to not update its frame sequence numbering. This results in a retransmission after the station sends an acknowledgement from previous frames. [Unlike all other fields, the FCS is transmitted MSB (Most Significant Bit) first. The A. C. and I fields are transmitted LSB (Least Significant Bit) first. The details of how the FCS is generated and checked is beyond the scope of this application note and since all single component SDLC controllers handle this function automatically, it is usually sufficient to know only that an error has or has not occurred. The IBM documents contain more detailed information for those readers desiring it.

The closing flag terminates the frame. When the closing flag is received, the receiver knows that the preceding 16 bits constitute the FCS and that any bits between the control field and the FCS constitute the information field.

SDLC does not support an interframe time-fill character such as the SYN character in Bi-Sync. If an unusual condition occurs while transmitting, such as data is not available in time from memory or CTS (Clear-to-Send) is lost from the modem, the transmitter aborts the frame by sending an Abort character to notify the receiver to invalidate the frame. The Abort character consists of eight contiguous 1s sent without zero bit insertion. Intraframe time-fill consists of either flags, Abort characters, or any combination of the two.

While the Abort character protects the receiver from transmitted errors, errors introduced by the transmission medium are discovered at the receiver through the FCS check and a check for invalid frames. Invalid frames are those which are not bounded by flags or are too short, that is, less than 32 bits between flags. All invalid frames are ignored by the receiver.

Although SDLC is a synchronous protocol, it provides an optional feature that allows its use on basically asynchronous data links — NRZI (Non-Return-to-Zero-Inverted) coding. NRZI coding specifies that the signal condition does not change for transmitting a binary 1, while a binary 0 causes a change of state. Figure 2 illustrates NRZI coding compared to the normal NRZ. NRZI coding guarantees that an active line will have a transition at least every 5-bit times; long strings of zeroes cause a transition every bit time, while long strings of 1s are broken up by zero bit insertion. Since asynchronous

operation requires that the receiver sampling clock be derived from the received data, NRZI encoding plus zero bit insertion make the design of clock recovery circuitry easier.

All of the previous discussion has applied to SDLC on either point-to-point or multi-point data networks, SDLC (but not HDLC) also includes specification for a loop configuration. Figure 3 compares these three configurations. IBM uses this loop configuration in its 3650 Retail Store System. It consists of a single loop controller station with one or more down-loop secondary stations. Communications on a loop rely on the secondary stations repeating a received message down loop with a delay of one bit time. The reason for the one bit delay will be evident shortly.

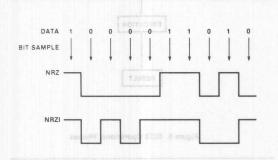
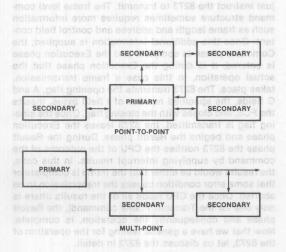


Figure 2. NRZI vs NRZ Encoding

Loop operation defines a new special character: the EOP (End-of-Poll) character which consists of a 0 followed by 7 contiguous, non-zero bit inserted, ones. After the loop controller transmits a message, it idles the line (sends all 1s). The final zero of the closing flag plus the first 7 1s of the idle form an EOP character. While repeating, the secondaries monitor their incoming line for an EOP character. When an EOP is detected, the secondary checks to see if it has a message to transmit. If it does, it changes the seventh 1 to a 0 (the one bit delay allows time for this) and repeats the modified EOP (now alias flag). After this flag is transmitted, the secondary terminates its repeater function and inserts its message (with multiple preceding flags if necessary). After the closing flag, the secondary resumes its one bit delay repeater function. Notice that the final zero of the secondary's closing flag plus the repeated 1s from the controller form an EOP for the next down-loop secondary, allowing it to insert a message if it desires.

One might wonder if the secondary missed any messages from the controller while it was inserting its own message. It does not. Loop operation is basically half-duplex. The controller waits until it receives an EOP before it transmits its next message. The controller's reception of the EOP signifies that the original message has propagated around the loop followed by any messages inserted by the secondaries. Notice that secondaries cannot communicate with one another directly, all secondary-to-secondary communication takes place by way of the controller.



SECONDARY SECONDARY LOOP

spatished dose associated a feel spatished Figure 3. Network Configurations

Loop protocol does not utilize the normal Abort character. Instead, an abort is accomplished by simply transmitting a flag character. Down loop, the receiver sees the abort as a frame which is either too short (if the abort occurred early in the frame) or one with an FCS error. Either results in a discarded frame. For more details on loop operation, please refer to the IBM documents referenced earlier.

Another protocol very similar to SDLC which the 8273 supports is HDLC (High-Level Data Link Control). There are only three basic differences between the two: HDLC offers extended address and control fields, and the HLDC Abort character is 7 contiguous 1s as opposed to SDLC's 8 contiguous 1s.

Extended addressing, beyond the 256 unique addresses possible with SDLC, is provided by using the address field's least significant bit as the extended address modifier. The receiver examines this bit to determine if the octet should be interpreted as the final address octet. As long as the bit is 0, the octet that contains it is considered an extended address. The first time the bit is a 1, the receiver interprets that octet as the final address octet. Thus the address field may be extended to any number of octets. Extended addressing is illustrated in Figure 4a.

A similar technique is used to extend the control field although the extension is limited to only one extra control octet. Figure 4b illustrates control field extension.

Those readers not yet asleep may have noticed the similarity between the SDLC loop EOP character (a 0 followed by 7 1s) and the HDLC Abort (7 1s). This possible incompatibility is neatly handled by the HDLC protocol not specifying a loop configuration.

This completes our brief discussion of the SDLC/HDLC protocols. Now let us turn to the 8273 in particular and discuss its hardware aspects through an explanation of the block diagram and generalized system schematics.

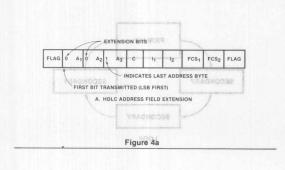
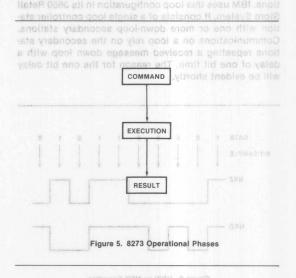




Figure 4b

### BASIC 8273 OPERATION or add tadt applicant notices

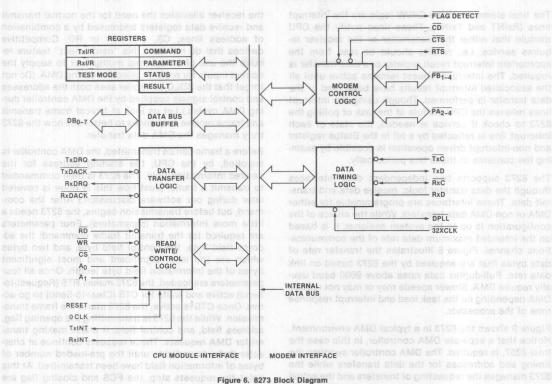
It will be helpful for the following discussions to have some idea of the basic operation of the 8273. Each operation, whether it is a frame transmission, reception or port read, etc., is comprised of three phases: the Command, Execution, and Result phases. Figure 5 shows the sequence of these phases. As an illustration of this sequence, let us look at the transmit operation.



When the CPU decides it is time to transmit a frame, the Command phase is entered by the CPU issuing a Transmit Frame command to the 8273. It is not sufficient to just instruct the 8273 to transmit. The frame level command structure sometimes requires more information such as frame length and address and control field content. Once this additional information is supplied, the Command phase is complete and the Execution phase is entered. It is during the Execution phase that the actual operation, in this case a frame transmission, takes place. The 8273 transmits the opening flag, A and C fields, the specified number of I field bytes, inserts the FCS, and closes with the closing flag. Once the closing flag is transmitted, the 8273 leaves the Execution phase and begins the Result phase. During the Result phase the 8273 notifies the CPU of the outcome of the command by supplying interrupt results. In this case, the results would be either that the frame is complete or that some error condition causes the transmission to be aborted. Once the CPU reads all of the results (there is only one for the Transmit Frame command), the Result phase and consequently the operation, is complete. Now that we have a general feeling for the operation of the 8273, let us discuss the 8273 in detail.

### HARDWARE ASPECTS OF THE 8273

The 8273 block diagram is shown in Figure 6. It consists of two major interfaces: the CPU module interface and the modem interface. Let's discuss each interface separately.



# CPU Interface bes because islant ent sette Isrii

The CPU interface consists of four major blocks: Control/Read/Write logic (C/R/W), internal registers, data transfer logic, and data bus buffers.

The CPU module utilizes the C/R/W logic to issue commands to the 8273. Once the 8273 receives a command and executes it, it returns the results (good/bad completion) of the command by way of the C/R/W logic. The C/R/W logic is supported by seven registers which are addressed via the A<sub>0</sub>, A<sub>1</sub>, RD, and WR signals, in addition to CS. The A<sub>0</sub> and A<sub>1</sub> signals are generally derived from the two low order bits of the CPU module address bus while RD and WR are the normal I/O Read and Write signals found on the system control bus. Figure 7 shows the address of each register using the C/R/W logic. The function of each register is defined as follows:

ADDRESS INPUTS		CONTROL INPUTS			
A <sub>1</sub>	A <sub>0</sub>	CS.RD	CS · WR		
0	0	STATUS	COMMAND		
0 1		RESULT	PARAMETER		
1	0	TxI/R	TEST MODE		
1	1	RxI/R	-		

Figure 7. 8273 Register Selection

Command — 8273 operations are initiated by writing the appropriate command byte into this register.

Parameter - Many commands require more information than found in the command itself. This additional information is provided by way of the parameter register. In most and teauper a fact 2728 and

Immediate Result (Result) - The completion information (results) for commands which execute immediately are provided in this register.

Transmit Interrupt Result (TxI/R) - Results of transmit operations are passed to the CPU in this register. Sylocon a lant CASS and applicant II A 258 and

Receiver Interrupt Result (RxI/R) - Receive operation results are passed to the CPU via this register.

Status — The general status of the 8273 is provided in this register. The Status register supplies the handshaking necessary during various phases of the 8273 operation. The most excellent of deline ad of

Test Mode — This register provides a software reset function for the 8273.

The commands, parameters, and bit definition of these registers are discussed in the following software section. Notice that there are not specific transmit or receive data registers. This feature is explained in the data transfer logic discussion.

The final elements of the C/R/W logic are the interrupt lines (RxINT and TxINT). These lines notify the CPU module that either the transmitter or the receiver requires service; i.e., results should be read from the appropriate interrupt result register or a data transfer is required. The interrupt request remains active until all the associated interrupt results have been read or the data transfer is performed. Though using the interrupt lines relieves the CPU module of the task of polling the 8273 to check if service is needed, the state of each interrupt line is reflected by a bit in the Status register and non-interrupt driven operation is possible by examing the contents of these bits periodically.

The 8273 supports two independent data interfaces through the data transfer logic; receive data and transmit data. These interfaces are programmable for either DMA or non-DMA data transfers. While the choice of the configuration is up to the system designer, it is based on the intended maximum data rate of the communications channel. Figure 8 illustrates the transfer rate of data bytes that are acquired by the 8273 based on link data rate. Full-duplex data rates above 9600 baud usually require DMA. Slower speeds may or may not require DMA depending on the task load and interrupt response time of the processor.

Figure 9 shows the 8273 in a typical DMA environment. Notice that a separate DMA controller, in this case the Intel 8257, is required. The DMA controller supplies the timing and addresses for the data transfers while the 8273 manages the requesting of transfers and the actual counting of the data block lengths. In this case, elements of the data transfer interface are:

TxDRQ: Transmit DMA Request — Asserted by the 8273, this line requests a DMA transfer from memory to the 8273 for transmit.

TxDACK: Transmit DMA Acknowledge — Returned by the 8257 in response to TxDRQ, this line notifies the 8273 that a request has been granted, and provides access to the transmitter data register.

RxDRQ: Receiver DMA Request — Asserted by the 8273, it requests a DMA transfer from the 8273 to memory for a receive operation.

TxDACK: Receiver DMA Acknowledge — Returned by the 8257, it notifies the 8273 that a receive DMA cycle has been granted, and provides access to the receiver data register.

RD: Read — Supplied by the 8257 to indicate data is to be read from the 8273 and placed in memory.

WR: Write — Supplied by the 8257 to indicate data is to be written to the 8273 from memory.

To request a DMA transfer the 8273 raises the appropriate DMA request line; let us assume it is a transmitter request (TxDRQ). Once the 8257 obtains control of the system bus by way of its HOLD and HLDA (hold acknowledge) lines, it notifies the 8273 that TxDRQ has been granted by returning TxDACK and WR. The TxDACK and WR signals transfer data to the 8273 for a transmit, independent of the 8273 chip select pin (CS). A similar sequence of events occurs for receiver requests. This "hard select" of data into the transmitter or out of

the receiver alleviates the need for the normal transmit and receive data registers addressed by a combination of address lines, CS, and WR or RD. Competitive devices that do not have this "hard select" feature require the use of an external multiplexer to supply the correct inputs for register selection during DMA. (Do not forget that the SDLC controller sees both the addresses and control signals supplied by the DMA controller during DMA cycles.) Let us look at typical frame transmit and frame receive sequences to better see how the 8273 truly manages the DMA data transfer.

Before a frame can be transmitted, the DMA controller is supplied, by the CPU, the starting address for the desired information field. The 8273 is then commanded to transmit a frame. (Just how this is done is covered later during our software discussion.) After the command, but before transmission begins, the 8273 needs a little more information (parameters). Four parameters are required for the transmit frame command: the address field byte, the control field byte, and two bytes which are the least significant and most significant bytes of the information field byte length. Once all four parameters are loaded, the 8273 makes RTS (Request-to-Send) active and waits for CTS (Clear-to-Send) to go active. Once CTS is active, the 8273 starts the frame transmission. While the 8273 is transmitting the opening flag, address field, and control field; it starts making transmitter DMA requests. These requests continue at character (byte) boundaries until the pre-loaded number of bytes of information field have been transmitted. At this point the requests stop, the FCS and closing flag are transmitted, and the TxINT line is raised, signaling the CPU that the frame transmission is complete. Notice that after the initial command and parameter loading. absolutely no CPU intervention was required (since DMA is used for data transfers) until the entire frame was transmitted. Now let's look at a frame reception.

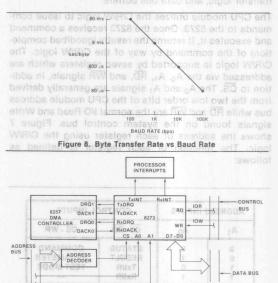


Figure 9. DMA, Interrupt-Driven System

The receiver operation is very similar. Like the initial transmit sequence, the DMA controller is loaded with a starting address for a receiver data buffer and the 8273 is commanded to receive. Unlike the transmitter, there are two different receive commands: General Receive, where all received frames are transferred to memory, and Selective Receive, where only frames having an address field matching one of two preprogrammed 8273 address fields are transferred to memory. Let's assume for now that we want to general receive. After the receive command, two parameters are required before the receiver becomes active: the least significant and most significant bytes of the receiver buffer length. Once these bytes are loaded, the receiver is active and the CPU may return to other tasks. The next frame appearing at the receiver input is transferred to memory using receiver DMA requests. When the closing flag is received, the 8273 checks the FCS and raises its RxINT line. The CPU can then read the results which indicate if the frame was error-free or not. (If the received frame had been longer than the pre-loaded buffer length, the CPU would have been notified of that occurrence earlier with a receiver error interrupt. The command description section contains a complete list of error conditions.) Like the transmit example, after the initial command, the CPU is free for other tasks until a frame is completely received. These examples have illustrated the 8273's management of both the receiver and transmitter DMA channels.

It is possible to use the DMA data transfer interface in a non-DMA interrupt-driven environment. In this case, 4 interrupt levels are used: one each for TxINT and RxINT. and one each for TxDRQ and RxDRQ. This configuration is shown in Figure 10. This configuration offers the advantages that no DMA controller is required and data requests are still separated from result (completion) reguests. The disadvantages of the configuration are that 4 interrupt levels are required and that the CPU must actually supply the data transfers. This, of course, reduces the maximum data rate compared to the configuration based strictly on DMA. This system could use an Intel 8259 8-level Priority Interrupt Controller to supply a vectored CALL (subroutine) address based on requests on its inputs. The 8273 transmitter and receiver make data requests by raising the respective DRQ line. The CPU is interrupted by the 8259 and vectored to a data transfer routine. This routine either writes (for transmit) or reads (for receive) the 8273 using the respective TxDACK or RxDACK line. As in the case above, the DACK lines serve as "hard" chip selects into and out of the 8273. (TxDACK + WR writes data into the 8273 for transmit. RxDACK + RD reads data from the 8273 for receive.) The CPU is notified of operation completion and results by way of TxINT and RxINT lines. Using the 8273, and the 8259, in this way, provides a very effective, yet simple, interrupt-driven interface.

Figure 11 illustrates a system very similar to that described above. This system utilizes the 8273 in a non-DMA data transfer mode as opposed to the two DMA approaches shown in Figures 9 and 10. In the non-DMA case, data transfer requests are made on the TxINT and RxINT lines. The DRQ lines are not used. Data transfer requests are separated from result requests by a bit in

the Status register. Thus, in response to an interrupt, the CPU reads the Status register and branches to either a result or a data transfer routine based on the status of one bit. As before, data transfers are made via using the DACK lines as chip selects to the transmitter and receiver data registers.

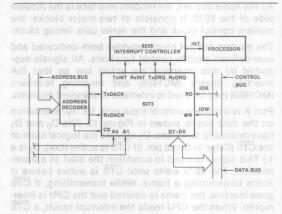


Figure 10. Interrupt-Based DMA System

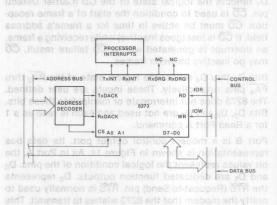


Figure 11. Non-DMA Interrupt-Driven System 10190101

Figure 12 illustrates the simplest system of all. This system utilizes polling for all data transfers and results. Since the interrupt pins are reflected in bits in the Status register, the software can read the Status register periodically looking for one of these to be set. If it finds an INT bit set, the appropriate Result Available bit is examined to determine if the "interrupt" is a data transfer or completion result. If a data transfer is called for, the DACK line is used to enter or read the data from the 8273. If the interrupt is a completion result, the appropriate result register is read to determine the good/bad completion of the operation.

The actual selection of either DMA or non-DMA modes is controlled by a command issued during initialization. This command is covered in detail during the software discussion.

The final block of the CPU module interface is the Data Bus Buffer. This block supplies the tri-state, bidirectional data bus interface to allow communication to and from the 8273.

#### Modem Interface

As the name implies, the modem interface is the modem side of the 8273. It consists of two major blocks: the modem control block and the serial data timing block.

The modem control block provides both dedicated and user-defined modem control functions. All signals supported by this interface are active low so that EIA inverting drivers (MC1488) and inverting receivers (MC1489) may be used to interface to standard modems.

Port A is a modem control input port. Its representation on the data bus is shown in Figure 13. Bits  $\mathsf{D}_0$  and  $\mathsf{D}_1$  have dedicated functions.  $\mathsf{D}_0$  reflects the logical state of the  $\overline{\text{CTS}}$  (Clear-to-Send) pin. [If  $\overline{\text{CTS}}$  is active (low),  $\mathsf{D}_0$  is a 1.] This signal is used to condition the start of a transmission. The 8273 waits until  $\overline{\text{CTS}}$  is active before it starts transmitting a frame. While transmitting, if  $\overline{\text{CTS}}$  goes inactive, the frame is aborted and the CPU is interrupted. When the CPU reads the interrupt result, a  $\overline{\text{CTS}}$  failure is indicated.

 $D_1$  reflects the logical state of the  $\overline{CD}$  (Carrier Detect) pin.  $\overline{CD}$  is used to condition the start of a frame reception.  $\overline{CD}$  must be active in time for a frame's address field. If  $\overline{CD}$  is lost (goes inactive) while receiving a frame, an interrupt is generated with a  $\overline{CD}$  failure result.  $\overline{CD}$  may go inactive between frames.

Bits  $D_2$  thru  $D_4$  reflect the logical state of the  $\overline{PA_2}$  thru  $\overline{PA_4}$  pins respectively. These inputs are user defined. The 8273 does not interrogate or manipulate these bits. Bits  $D_5$ ,  $D_6$ , and  $D_7$  are not used and each is read as a 1 for a Read Port A command.

Port B is a modern control output port. Its data bus representation is shown in Figure 14. As in Port A, the bit values represent the logical condition of the pins.  $D_0$  and  $D_5$  are dedicated function outputs.  $D_0$  represents the  $\overline{\text{RTS}}$  (Request-to-Send) pin.  $\overline{\text{RTS}}$  is normally used to notify the modern that the 8273 wishes to transmit. This function is handled automatically by the 8273. If  $\overline{\text{RTS}}$  is inactive (pin is high) when the 8273 is commanded to transmit, the 8273 makes it active and then waits for  $\overline{\text{CTS}}$  before transmitting the frame, One byte time after the end of the frame, the 8273 returns  $\overline{\text{RTS}}$  to its inactive state. However, if  $\overline{\text{RTS}}$  was active when a transmit command is issued, the 8273 leaves it active when the frame is complete.

Bit D<sub>5</sub> reflects the state of the Flag Detect pin. This pin is activated whenever an active receiver sees a flag character. This function is useful to activate a timer for line activity timeout purposes.

Bits  $D_1$  thru  $\overline{D_4}$  provide four user-defined outputs. Pins  $\overline{PB_1}$  thru  $\overline{PB_4}$  reflect the logical state of these bits. The 8273 does not interrogate or manipulate these bits.  $D_6$  and  $D_7$  are not used. In addition to being able to output to Port B, Port B may be read using a Read Port B command. All Modem control output pins are forced high on

reset. (All commands mentioned in this section are covered in detail later.).

The final block to be covered is the serial data timing block. This block contains two sections: the serial data logic and the digital phase locked loop (DPLL).

Elements of the serial data logic section are the data pins, TxD (transmit data output) and RxD (receive data input), and the respective data clocks,  $\overline{\text{TxC}}$  and  $\overline{\text{RxC}}$ . The transmit and receive data is synchronized by the  $\overline{\text{TxC}}$  and  $\overline{\text{RxC}}$  clocks. Figure 15 shows the timing for these signals. The leading edge (negative transition) of  $\overline{\text{TxC}}$  generates new transmit data and the trailing edge (positive transition) of  $\overline{\text{RxC}}$  is used to capture the receive data.

It is possible to reconfigure this section under program control to perform diagnostic functions; both data and clock loopback are available. In data loopback mode, the TxD pin is internally routed to the RxD pin. This allows simple board checkout since the CPU can send an SDLC message to itself. (Note that transmitted data will still appear on the TxD pin.)

section confeins a complete list of error condi-

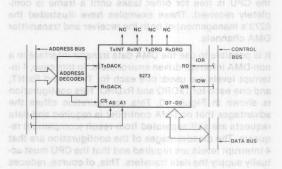


Figure 12. Polled System

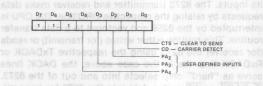


Figure 13. Port A (Input) Bit Definition

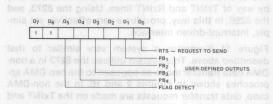


Figure 14. Port B (Output) Bit Definition

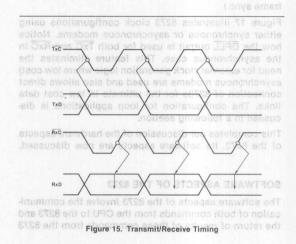
When data loopback is utilized, the receiver may be presented incorrect sample timing  $(\overline{RxC})$  by the external circuitry. Clock loopback overcomes, this problem by allowing the internal routing of  $\overline{TxC}$  and  $\overline{RxC}$ . Thus the same clock used to transmit the data is used to receive it. Examination of Figure 15 shows that this method ensures bit synchronism. The final element of the serial data logic is the Digital Phase Locked Loop.

The DPLL provides a means of clock recovery from the received data stream. This feature allows the 8273 to interface without external synchronizing logic to low cost asynchronous modems (modems which do not supply clocks). It also makes the problem of clock timing in loop configurations trivial.

To use the DPLL, a clock at 32 times the required baud rate must be supplied to the  $32 \times CLK$  pin. This clock provides the interval that the DPLL samples the received data. The DPLL uses the  $32 \times$  clock and the received data to generate a pulse at the  $\overline{DPLL}$  output pin. This  $\overline{DPLL}$  pulse is positioned at the nominal center of the received data bit cell. Thus the  $\overline{DPLL}$  output may be wired to  $\overline{RxC}$  and/or  $\overline{TxC}$  to supply the data timing. The exact position of the pulse is varied depending on the line noise and bit distortion of the received data. The adjustment of the  $\overline{DPLL}$  position is determined according to the rules outlined in Figure 16.

Adjustments to the sample phase of DPLL with respect to the received data is made in discrete increments. Referring to Figure 16, following the occurrence of DPLL pulse A, the DPLL counts 32 × CLK pulses and examines the received data for a data edge. Should no edge be detected in 32 pulses, the DPLL positions the next DPLL pulse (B) at 32 clock pulses from pulse A. Since no new phase information is contained in the data stream, the sample phase is assumed to be at nominal 1 × baud rate. Now assume a data edge occurs after

DPLL pulse B. The distance from B to the next pulse C is influenced according to which quadrant (A1, B1, B2, or A2) the data edge falls in. (Each quadrant represents 8 32 × CLK times.) For example, if the edge is detected in quadrant A<sub>1</sub>, it is apparent that pulse B was too close to the data edge and the time to the next pulse must be shortened. The adjustment for quadrant A1 is specified as -2. Thus, the next DPLL pulse, pulse C, is positioned 32-2 or 30 32 x CLK pulses following DPLL pulse B. This adjustment moves pulse C closer to the nominal bit center of the next received data cell. A data edge occurring in quadrant B2 would have caused the adjustment to be small, namely 32+1 or 33 32×CLK pulses. Using this technique, the DPLL pulse converges to the nominal bit center within 12 data transitions. worse case — 4-bit times adjusting through quadrant A<sub>1</sub> or A<sub>2</sub> and 8-bit times adjusting through B<sub>1</sub> or B<sub>2</sub>.



1 BIT TIME RyD NO TRANSITION (1 (2 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 DPLL 32 CLOCKS 30 CLOCKS C-2 33 CLOCKS C+1 32 CLOCKS CNOMINAL QUADRANT ADJUSTMENT A1 Figure 16. DPLL Phase Adjustments

When the receive data stream goes idle after 15 ones, DPLL pulses are generated at 32 pulse intervals of the 32x CLK. This feature allows the DPLL pulses to be used as both transmitter and receiver clocks.

In order to guarantee sufficient transitions of the received data to enable the  $\overline{DPLL}$  to lock, NRZI encoding of the data is recommended. This ensures that, within a frame, data transitions occur at least every five bit times — the longest sequence of 1s which may be transmitted with zero bit insertion. It is also recommended that frames following a line idle be transmitted with preframe sync characters which provide a minimum of 12 transitions. This ensures that the  $\overline{DPLL}$  is generating  $\overline{DPLL}$  pulses at the nominal bit centers in time for the opening flag. (Two 00H characters meet this requirement by supplying 16 transitions with NRZI encoding. The 8273 contains a mode which supplies such a preframe sync.)

Figure 17 illustrates 8273 clock configurations using either synchronous or asynchronous modems. Notice how the  $\overline{DPLL}$  output is used for both  $\overline{TxC}$  and  $\overline{RxC}$  in the asynchronous case. This feature eliminates the need for external clock generation logic where low cost) asynchronous modems are used and also allows direct connection of 8273s for the ultimate in low cost data links. The configuration for loop applications is discussed in a following section.

This completes our discussion of the hardware aspects of the 8273. Its software aspects are now discussed.

### **SOFTWARE ASPECTS OF THE 8273**

The software aspects of the 8273 involve the communication of both commands from the CPU to the 8273 and the return of results of those commands from the 8273

to the CPU. Due to the internal processor architecture of the 8273, this CPU-8273 communication is basically a form of interprocessor communication. Such communication usually requires a form of protocol of its own. This protocol is implemented through use of handshaking supplied in the 8273 Status register. The bit definition of this register is shown in Figure 18.

CBSY: Command Busy — CBSY indicates when the 8273 is in the command phase. CBSY is set when the CPU writes a command into the Command register, starting the Command phase. It is reset when the last parameter is deposited in the Parameter register and accepted by the 8273, completing the Command phase.

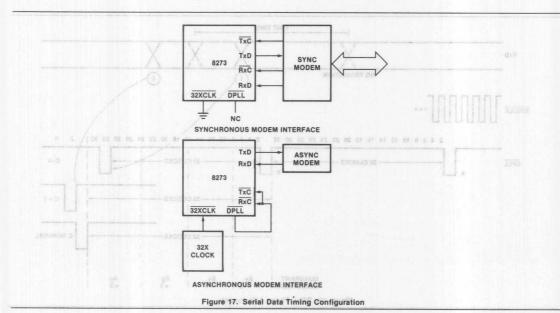
CBF: Command Buffer Full — When set, this bit indicates that a byte is present in the Command register. This bit is normally not used.

CPBF: Command Parameter Buffer Full — This bit indicates that the Parameter register contains a parameter. It is set when the CPU deposits a parameter in the Parameter register. It is reset when the 8273 accepts the parameter.

CRBF: Command Result Buffer Full — This bit is set when the 8273 places a result from an immediate type command in the Result register. It is reset when the CPU reads the result from the Result register.

RxINT: Receiver Interrupt — The state of the RxINT pin is reflected by this bit. RxINT is set by the 8273 whenever the receiver needs servicing. RxINT is reset when the CPU reads the results or performs the data transfer.

TxINT: Transmitter Interrupt — This bit is identical to RxINT except action is initiated based on transmitter interrupt sources.



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RxIRA: Receiver Interrupt Result Available - RxIRA is set when the 8273 places an interrupt result byte into the RxI/R register, RxIRA is reset when the CPU reads the RxI/R register. The standard standard standard

TxIRA: Transmitter Interrupt Result Available -TxIRA is the corresponding Result Available bit for the transmitter. It is set when the 8273 places an interrupt result byte in the TxI/R register and reset when the CPU reads the register.

The significance of each of these bits will be evident shortly. Since the software requirements of each 8273 phase are essentially independent, each phase as is covered separately. The same APIXT and

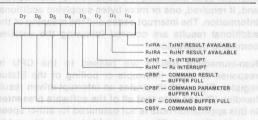


Figure 18. Status Register Format

# Command Phase Software AMD garyolome areau noit

Recalling the Command phase description in an earlier section, the CPU starts the Command phase by writing a command byte into the 8273 Command register. If further information about the command is required by the 8273, the CPU writes this information into the Parameter register. Figure 19 is a flowchart of the Command phase. Notice that the CBSY and CPBF bits of the Status register are used to handshake the command and parameter bytes. Also note that the chart shows that a command may not be issued if the Status register indicates the 8273 is busy (CBSY = 1). If a command is issued while CBSY = 1, the original command is overwritten and lost. (Remember that CBSY signifies the command phase is in progress and not the actual execution of the command.) The flowchart also includes a Parameter buffer full check. The CPU must wait until CPBF = 0 before writing a parameter to the Parameter register. If a parameter is issued while CPBF = 1, the previous parameter is overwritten and lost. An example of command output assembly language software is provided in Figure 20a. This software assumes that a command buffer exists in memory. The buffer is pointed at by the HL register. Figure 20b shows the command buffer structure.

The 8273 is a full duplex device, i.e., both the transmitter and receiver may be executing commands or passing interrupt results at any given time. (Separate Rx and Tx interrupt pins and result registers are provided for this reason.) However, there is only one Command register. Thus, the Command register must be used for only one command sequence at a time and the transmitter and receiver may never be simultaneously in a command phase. A detailed description of the commands and their parameters is presented in a following section.

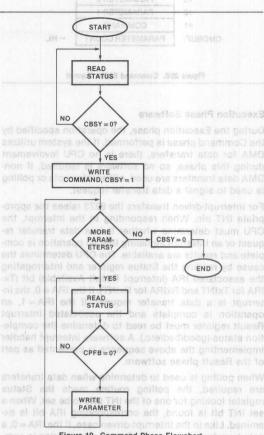


Figure 19. Command Phase Flowchart

.FUNCTION: COMMAND DISPATCHER

```
;INPUTS: HL - COMMAND BUFFER ADDRESS
;OUTPUTS: NONE
; CALLS: NONE
;DESTROYS: A,B,H,L,F/F'S;DESCRIPTION: CMDOUT ISSUES THE COMMAND + PARAMETERS
; IN THE COMMAND BUFFER POINTED AT BY HL
                  H, CMDBUF; POINT HL AT BUFFER
CMDOUT: LXI
                            ;1ST ENTRY IS PAR. COUNT 100
;POINT AT COMMAND BYTE
;READ 8273 STATUS
         MOV B,M
         INX
CMD1:
                  STAT73
         RLC
              ROTATE CBSY INTO CARRY
                   CMD1
                            ;WAIT UNTIL CBSY=0
;MOVE COMMAND BYTE TO A
         MOV
                  A.M
                           ; PUT COMMAND IN COMMAND REG
; GET PARAMETER COUNT
CMD2:
                  A,B
                            TEST IF ZERO
                  ; IF 0
         RZ
                         THEN DONE
         INX
                            NOT DONE, SO POINT AT NEXT PAR
                            DEC PARAMETER COUNT
         DCR
                  B
CMD3:
                            ;READ 8273 STATUS
;TEST CPBF BIT
;WAIT UNTIL CPBF IS 0
         IN
                  STAT73
         ANI
                   CPBF
         JNZ
                   CMD3
                            GET PARAMETER FROM BUFFER
                        3 ;OUTPUT PAR TO PARAMETER REG
;CHECK IF MORE PARAMETERS
                  PARM73
         OUT
```

Figure 20A. Command Phase Software

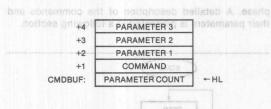


Figure 20B. Command Buffer Format

### **Execution Phase Software**

During the Execution phase, the operation specified by the Command phase is performed. If the system utilizes DMA for data transfers, there is no CPU involvement during this phase, so no software is required. If non-DMA data transfers are used, either interrupts or polling is used to signal a data transfer request.

For interrupt-driven transfers the 8273 raises the appropriate INT pin. When responding to the interrupt, the CPU must determine whether it is a data transfer request or an interrupt signaling that an operation is complete and results are available. The CPU determines the cause by reading the Status register and interrogating the associated IRA (Interrupt Result Available) bit (TX-IRA for TXINT and RXIRA for RXINT). If the IRA = 0, the interrupt is a data transfer request. If the IRA = 1, an operation is complete and the associated Interrupt Result register must be read to determine the completion status (good/bad/etc.). A software interrupt handler implementing the above sequence is presented as part of the Result phase software.

When polling is used to determine when data transfers are required, the polling routine reads the Status register looking for one of the INT bits to be set. When a set INT bit is found, the corresponding IRA bit is examined. Like in the interrupt-driven case, if the IRA = 0, a data transfer is required. If IRA = 1, an operation is complete and the Interrupt Result register needs to be read. Again, example polling software is presented in the next section.

### **Result Phase Software**

During the Result phase the 8273 notifies the CPU of the outcome of a command. The Result phase is initiated by either a successful completion of an operation or an error detected during execution. Some commands such as reading or writing the I/O ports provide immediate results, that is, there is essentially no delay from the issuing of the command and when the result is available. Other commands such as frame transmit, take time to complete so their result is not available immediately. Separate result registers are provided to distinguish these two types of commands and to avoid interrupt handling for simple results.

Immediate results are provided in the Result register. Validity of information in this register is indicated to the CPU by way of the CRBF bit in the Status register. When the CPU completes the Command phase of an immediate command, it polls the Status register waiting until CRBF = 1. When this occurs, the CPU may read the

Result register to obtain the immediate result. The Result register provides only the results from immediate commands.

Example software for handling immediate results is shown in Figure 21. The routine returns with the result in the accumulator. The CPU then uses the result as is appropriate.

All non-immediate commands deal with either the transmitter or receiver. Results from these commands are provided in the TxI/R (Transmit Interrupt Result) and RxI/R (Receive Interrupt Result) registers respectively. Results in these registers are conveyed to the CPU by the TxIRA and RxIRA bits of the Status register. Results of non-immediate commands consist of one byte result interrupt code indicating the condition for the interrupt and, if required, one or more bytes supplying additional information. The interrupt codes and the meaning of the additional results are covered following the detailed command description.

Non-immediate results are passed to the CPU in response to either interrupts or polling of the Status register. Figure 22 illustrates an interrupt-driven result handler. (Please note that all of the software presented in this application note is not optimized for either speed or code efficiency. They are provided as a guide and to illustrate concepts.) This handler provides for interruptdriven data transfers as was promised in the last section. Users employing DMA-based transfers do not need the lines where the IRA bit is tested for zero. (These lines are denoted by an asterisk in the comments column.) Note that the INT bit is used to determine when all results have been read. All results must be read. Otherwise, the INT bit (and pin) will remain high and further interrupts may be missed. These routines place the results in a result buffer pointed at by RCRBUF and

A typical result handler for systems utilizing polling is shown in Figure 23. Data transfers are also handled by this routine. This routine utilizes the routines of Figure 22 to handle the results.

At this point, the reader should have a good conceptual feel about how the 8273 operates. It is now time for the particulars of each command to be discussed.

```
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Figure 21. Immediate Result Handler

; FUNCTION: RXI - INTERRUPT DRIVEN RESULT/DATA HANDLER ; DESTROYS: B,C ; INPUTS: RCRBUF, RCVPNT : CALLS: NONE ;OUTPUTS: RCRBUF, RCVPNT ; DESTROYS: NOTHING ; DESCRIPTION: RXI IS ENTERED AT A RECEIVER INTERRUPT. ;THE INTERRUPT IS TESTED FOR DATA TRANSFER (IRA=0);OR RESULT (IRA=1). FOR DATA TRANSFER, THE DATA IS ; PLACED IN A BUFFER AT RCVPNT. RESULTS ARE PLACED IN ; A BUFFER AT RCRBUF. ; A FLAG(RXFLAG) IS SET IF THE INTERRUPT WAS A RESULT. ; (DATA TRANSFER INSTRUCTIONS ARE DENOTED BY (\*) AND ; MAYBE ELIMINATED BY USERS USING DMA. RXT: PUSH ; SAVE HL PUSH PSW SAVE PSW SAVE B PUSH STAT73 ; (\*) READ 8273 STATUS IN ANI RXIRA TEST IRA BIT ; (\*) IF 0, DATA TRANSFER NEEDED RXI2 RXI1: RCRBUF GET RESULT BUFFER POINTER LHLD TN STAT73 ; READ 8273 STATUS AGAIN TEST INT BIT ANI RXINT ; IF 0, THEN DONE RXT4 STAT73 TO STATE IN ; READ 8273 STATUS AGAIN RXIRA ANI TEST IRA AGAIN ;LOOP UNTIL RESULT IS READY ;READY, READ RXI/R 12 RXI1 RXIR73 IN STORE RESULT IN BUFFER M.A TNX BUMP RESULT POINTER RESTORE BUFFER POINTER RCRBUF SHLD JMP RXIL GO BACK TO SEE IF MORE RCVPNT RXI2: SHLD ; (\*) GET DATA BUFFER POINTER IN RCVDAT (\*) READ DATA VIA RXDACK STORE DATA IN BUFFER MOV M,A INX BUMP DATA POINTER RXI3 JMP RXI4: MVT SET RX FLAG TO SHOW COMPLETION A,01H STA RXFLAG : COMPLETION RESTORE BC RXI3: POP POP RESTORE PSW RESTORE HL POP B ; ENABLE INTERRUPTS ET ;FUNCTION: TXI - INTERRUPT DRIVEN RESULT/DATA HANDLER ()INPUTS: TAKBUF, TXPNT, TXFLAG ()UTPUTS: TXKBUF, TXPNT, TXFLAG () :DESTROYS: NOTHING ; LESCRIPTION: TXI IS ENTERED AT A TRANSMITTER INTERRUPT. ; THE INTERRUPT IS TESTED BY WAY OF THE IRA BIT TO SEE ;IF A DATA TRANSFER OR RESULT COMPLETION HAS OCCURED. ;FOR DATA TRANSFERS (IRA=0), THE DATA IS OBTAINED FROM ;A BUFFLE LOCATION POINTED AT BY TEXPIT. FOR COMPLETION, ;(IRA-1), THE RESULTS ARE READ AND PLACED AT A RESULT ;BUFFER POINTED AT BY TARBUF, AND THE TXFLAG IS SET ;TO INDICATE TO THE MAIN PROGRAM THAT A OPERATION IS COMPLETE. TX OPERATIONS HAVE ONLY ONE RESULT. ; DATA TRANSFER INSTRUCTIONS ARE DENOTED BY (\*). THESE MAYBE REMOVED BY USERS USING DMA. Dent portions PUSH :SAVE HL PUSH PSW STAT73 ; (\*) READ 8273 STATUS ; (\*) TEST TXIRA BIT IN ANI TXIRA JZ TXI2 ; (\*) IF Ø, DATA TRANSFER ;1, THEN READ TXIR ;GET RESULT BUFFER POINTER TXIR73 LHLD TXRBUF STORE RESULT IN BUFFER MOV M.A BUMP RESULT POINTER SHLD TXRBUF RESTORE RESULT POINTER ;SET TXFLAG TO SHOW COMPLETION ;SET FLAG MVI A.OlH STA TXFLAG TXI1: RESTORE PSW POP ; RESTORE HL ; ENABLE INTERRUPTS E. I

> Figure 22. Interrupt-Driven Result Handlers with Non-DMA Data Transfers

GET DATA POINTER

BUMP DATA POINTER

RESTORE POINTER

: (\*) RETURN AFTER RESTORE

GET DATA FROM BUFFER OUTPUT TO 8273 VIA TXDACK

: DONE

TXPNT

TXPNT

TXII

TXDATA

TXI2:

LHLD

MOV

OUT

SHLD

JMP

; DESCRIPTION: POLOP IS CALLED TO POLL THE 8273 FOR ;DATA TRANSFERS AND COMPLETION RESULTS. THE ;ROUTINES TXI AND RXI ARE USED FOR THE ACTUAL TRANSFERS AND BUFFER WORK. POLOP RETURNS ; SAVE PSW PUSH POLOP: MVI C.00H :CLEAR C

STAT73 ; READ 8273 STATUS POLOP1: IN ; ARE TXINT OR RXINT SET? ANI INT ; READ 8273 STATUS IN STAT73 ANI RXINT ; TEST RX INT ;YES, GO SERVICE RX ;MUST BE TX, GO SERVICE IT JNZ RXIC CALL TXI TXFLAG GET TX FLAG LDA ; WAS IT A COMPLETION? (01) ; NO, SO JUST EXIT s lant lamp CPI 01H JN2 PEXIT NAID NO EOP C :YES. UPDATE C Jessy a INK JMP POLOP1 TRY AGAIN CALL RXT

RXIC: ;GO SERVICE RX ;GET RX FLAG LDA RXFLAG ; WAS IT A COMPLETION? (01) CPI 01H ;NO, SO JUST EXIT JNZ PEXIT :YES, UPDATE C INR need JMP POLOP1 ; TRY AGAIN

> ; RESTORE PSW RET ; RETURN WITH COMP. STATUS IN C Figure 23. Polling Result Handler

### 8273 COMMAND DESCRIPTION

PEXIT: POP PSW

In this section, each command is discussed in detail. In order to shorten the notation, please refer to the command key in Table 1. The 8273 utilizes five different command types: Initialization/Configuration, Receive, Transmit, Reset, and Modem Control.

### Initialization/Configuration Commands

The Initialization/Configuration commands manipulate registers internal to the 8273 that define the various operating modes. These commands either set or reset specified bits in the registers depending on the type of command. One parameter is required. Set commands perform a logical OR operation of the parameter (mask) and the internal register. This mask contains 1s where register bits are to be set. A 0 in the mask causes no change in the corresponding register bit. Reset commands perform a logical AND operation of the parameter (mask) and the internal register, i.e., the mask is 0 to reset a register bit and a 1 to cause no change. Before presenting the commands, the register bit definitions are discussed.

## TABLE 1. COMMAND SUMMARY KEY

B<sub>0</sub>, B<sub>1</sub> - LSB AND MSB OF RECEIVE BUFFER LENGTH R<sub>0</sub>, R<sub>1</sub> — LSB AND MSB OF RECEIVED FRAME LENGTH Lo, L1 - LSB AND MSB OF TRANSMIT FRAME LENGTH A<sub>1</sub>, A<sub>2</sub> — MATCH ADDRESSES FOR SELECTIVE RECEIVE - RECEIVER INTERRUPT RESULT CODE - TRANSMITTER INTERRUPT RESULT CODE - ADDRESS FIELD OF RECEIVED FRAME - CONTROL FIELD OF RECEIVED FRAME

### Operating Mode Register (Figure 24) 3309 3903739439

- D<sub>7</sub>-D<sub>6</sub>: Not Used These bits must not be manipulated by any command; i.e., D<sub>7</sub>-D<sub>6</sub> must be 0 for the Set command and 1 for the Reset command.
- D<sub>5</sub>: HDLC Abort When this bit is set, the 8273 will interrupt when 7 1s (HDLC Abort) are received by an active receiver. When reset, an SDLC Abort (8 1s) will cause an interrupt.
- D<sub>4</sub>: EOP Interrupt Reception of an EOP character (0 followed by 7 1s) will cause the 8273 to interrupt the CPU when this bit is set. Loop controller stations use this mode as a signal that a polling frame has completed the loop. No EOP interrupt is generated when this bit is reset.
- D<sub>3</sub>: Early Tx Interrupt This bit specifies when the transmitter should generate an end of frame interrupt. If this bit is set, an interrupt is generated when the last data character has been passed to the 8273. If the user software issues another transmit command within two byte times, the final flag interrupt does not occur and the new frame is transmitted with only one flag of separation. If this restriction is not met, more than one flag will separate the frames and a frame complete interrupt is generated after the closing flag. If the bit is reset, only the frame complete interrupt occurs. This bit, when set, allows a single flag to separate consecutive frames.
- D<sub>2</sub>: Buffered Address and Control When set, the address and control fields of received frames are buffered in the 8273 and passed to the CPU as results after a received frame interrupt (they are not transferred to memory with the information field). On transmit, the A and C fields are passed to the 8273 as parameters. This mode simplifies buffer management. When this bit is reset, the A and C fields are passed to and from memory as the first two data transfers.
- D<sub>1</sub>: Preframe Sync When set, the 8273 prefaces each transmitted frame with two characters before the opening flag. These two characters provide 16 transitions to allow synchronization of the opposing receiver. To guarantee 16 transitions, the two characters are 55H-55H for non-NRZI mode (see Serial I/O Register description) or 00H-00H for NRZI mode. When reset, no preframe characters are transmitted.
- D<sub>0</sub>: Flag Stream When set, the transmitter will start sending flag characters as soon as it is idle; i.e., immediately if idle when the command is issued or after a transmission if the transmitter is active when this bit is set. When reset, the transmitter starts sending Idle characters on the next character boundary if idle already, or at the end of a transmission if active.

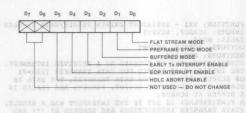


Figure 24. Operating Mode Register

### Serial I/O Mode Register (Figure 25)

- D<sub>7</sub>-D<sub>3</sub>: Not Used These bits must be 0 for the Set command and 1 for the Reset command.
- D<sub>2</sub>: Data Loopback— When set, transmitted data (TxD) is internally routed to the receive data circuitry. When reset, TxD and RxD are independent.
- D<sub>1</sub>: Clock Loopback When set, TxC is internally routed to RxC. When reset, the clocks are independent.
- D<sub>0</sub>: NRZI (Non-Return to Zero Inverted) When set, the 8273 assumes the received data is NRZI encoded, and NRZI encodes the transmitted data. When reset, the received and transmitted data are treated as a normal positive logic bit stream.

### **Data Transfer Mode Register (Figure 26)**

- D<sub>7</sub>-D<sub>1</sub>: Not Used These bits must be 0 for the Set command and 1 for the Reset command.
- D<sub>0</sub>: Interrupt Data Transfer When set, the 8273 will interrupt the CPU when data transfers are required (the corresponding IRA Status register bit will be 0 to signify a data transfer interrupt rather than a Result phase interrupt). When reset, 8273 data transfers are performed through DMA requests on the DRQ pins without interrupting the CPU.

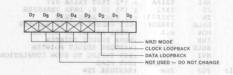


Figure 25. Serial I/O Mode Register

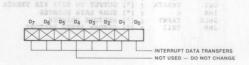


Figure 26. Data Transfer Mode Register

### One Bit Delay Register (Figure 27)

D7: One Bit Delay — When set, the 8273 retransmits the received data stream one bit delayed. This mode is entered and exited at a received character boundary. When reset, the transmitted and received data are independent. This mode is utilized for loop operation and is discussed in a later section.

D<sub>6</sub>-D<sub>0</sub>: Not Used — These bits must be 0 for the Set command and 1 for the Reset command.

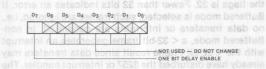


Figure 27. One Bit Delay Mode Register

Figure 28 shows the Set and Reset commands associated with the above registers. The mask which sets or resets the desired bits is treated as a single parameter. These commands do not interrupt nor provide results during the Result phase. After reset, the 8273 defaults to all of these bits reset.

REGISTER	COMMAND	HEX	PARAMETER
ONE BIT DELAY MODE	SET	A4	SET MASK
ONE BIT DELAY MODE	RESET	64	RESET MASK
DATA TRANSFER MORE	SET	97	SET MASK
DATA TRANSFER MODE	RESET	57	RESET MASK
OPERATING MODE	SET	91	SET MASK
OPERATING MODE	RESET	51	RESET MASK
SERIAL I/O MODE	SET	A0	SET MASK
SERIAL I/O MODE	RESET	60	RESET MASK

Figure 28. Initialization/Configuration Command Summary

# result for this second interrupt will be a Receive Receive Command to eausal cause of the Amammon Series and the Series of the Series S

The 8273 supports three receive commands plus a receiver disable function.

### General Receive of solvies tournatri edi il igunatri

When commanded to General Receive, the 8273 passes all frames either to memory (DMA mode) or to the CPU (non-DMA mode) regardless of the contents of the frame's address field. This command is used for primary and loop controller stations. Two parameters are required: B<sub>0</sub> and B<sub>1</sub>. These parameters are the LSB and MSB of the receiver buffer size. Giving the 8273 this extra information alleviates the CPU of the burden of checking for buffer overflow. The 8273 will interrupt the CPU if the received frame attempts to overfill the allotted buffer space.

### Selective Receive

In Selective Receive, two additional parameters besides  $B_0$  and  $B_1$  are required:  $A_1$  and  $A_2$ . These parameters are two address match bytes. When commanded to Selective Receive, the 8273 passes to memory or the CPU only those frames having an address field matching either  $A_1$  or  $A_2$ . This command is usually used for secondary stations with  $A_1$  being the secondary address and  $A_2$  is the "All Parties" address. If only one match byte is needed,  $A_1$  and  $A_2$  should be equal. As in General Receive, the 8273 counts the incoming data bytes and interrupts the CPU if  $B_0$ ,  $B_1$  is exceeded.

### Selective Loop Receive

This command is very similar in operation to Selective Receive except that One Bit Delay mode must be set and that the loop is captured by placing transmitter in Flag Stream mode automatically after an EOP character is detected following a selectively received frame. The details of using the 8273 in loop configurations is discussed in a later section so please hold questions until then

The handling of interrupt results is common among the three commands. When a frame is received without error, i.e., the FCS is correct and  $\overline{\text{CD}}$  (Carrier Detect) was active throughout the frame or no attempt was made to overfill the buffer; the 8273 interrupts the CPU following the closing flag to pass the completion results. These results, in order, are the receiver interrupt result code (RIC), and the byte length of the information field of the received frame (R<sub>0</sub>, R<sub>1</sub>). If Buffered mode is selected, the address and control fields are passed as two additional results. If Buffered mode is not selected, the address and control fields are passed as the first two data transfers and R<sub>0</sub>, R<sub>1</sub> reflect the information field length plus two.

# Receive Disable tem tolbus AMQ nolingeder email dose

The receiver may also be disabled using the Receive Disable command. This command terminates any receive operation immediately. No parameters are required and no results are returned.

The details for the Receive command are shown in Figure 29. The interrupt result code key is shown in Figure 30. Some explanation of these result codes is appropriate.

The interrupt result code is the first byte passed to the CPU in the RxI/R register during the Result phase. Bits  $D_4$ – $D_0$  define the cause of the receiver interrupt. Since each result code has specific implications, they are discussed separately below.

error conditions.) Note that the FCS, either transmitted or

BOST COMMAND TOTAL	HEX	PARAM- ETERS	RESULTS*
GENERAL RECEIVE	CO	B <sub>0</sub> , B <sub>1</sub>	RIC, R <sub>0</sub> , R <sub>1</sub> , A, C
SELECTIVE RECEIVE	C1	B <sub>0</sub> , B <sub>1</sub> , A <sub>1</sub> , A <sub>2</sub>	RIC, RO, R1, A, C
SELECTIVE LOOP RECEIVE	C2	B <sub>0</sub> , B <sub>1</sub> , A <sub>1</sub> , A <sub>2</sub>	RIC, RO, R1, A, C
DISABLE RECEIVER	C5	NONE	NONE

\*A AND C ARE PASSED AS RESULTS ONLY IN BUFFERED MODE.

Figure 29. Receiver Command Summary

RIC D7-D0	RECEIVER INTERRUPT RESULT CODE	AFTER INT
* 00000	A1 MATCH OR GENERAL RECEIVE	ACTIVE
* 00001	A2 MATCH	ACTIVE
00 00011	CRC ERROR HOW . serve floor	ACTIVE
00 00100	ABORT DETECTED	ACTIVE
00 00101		DISABLED
000 00110	EOP DETECTED	DISABLED
000 00111	FRAME < 32 BITS	ACTIVE
000 01000	DMA OVERRUN	DISABLED
000 01001	MEMORY BUFFER OVERFLOW	DISABLED
000 01010	CARRIER DETECT FAILURE	DISABLED
000 01011	RECEIVER INTERRUPT OVERRUN	DISABLED
*D7-D5	PARTIAL BYTE RECEIVED	
111	ALL 8 BITS OF LAST BYTE	
	D1-D0 oo ni ratimis viev zi	
100	TO SHOW IN SHOW IN THE PROPERTY OF THE PROPERT	
010	D2-D0	
010 110	D <sub>2</sub> -D <sub>0</sub> while different particular particu	
010 110 001	D <sub>2</sub> -D <sub>0</sub> m vslad HE and Lsd1 D <sub>3</sub> -D <sub>0</sub> D <sub>4</sub> D-0 photol vd bankasa i	
010 110	D <sub>2</sub> -D <sub>0</sub> while different particular particu	

Figure 30. Receiver Interrupt Result Codes (RIC)

The first two result codes result from the error-free reception of a frame. If the frame is received correctly after a General Receive command, the first result is returned. If either Selective Receive command was used (normal or loop), a match with A1 generates the first result code and a match with A2 generates the second. In either case, the receiver remains active after the interrupt; however, the internal buffer size counters are not reset. That is, if the receive command indicated 100 bytes were allocated to the receive buffer (B0, B1) and an 80-byte frame was received correctly, the maximum next frame size that could be received without recommanding the receiver (resetting Bo and B1) is 20 bytes. Thus, it is common practice to recommand the receiver after each frame reception. DMA and/or memory pointers are usually updated at this time. (Note that users who do not wish to take advantage of the 8273's buffer management features may simply use B<sub>0</sub>, B<sub>1</sub> = 0FFH for each receive command. Then frames of 65K bytes may be received without buffer overflow errors.)

The third result code is a CRC error. This indicates that a frame was received in the correct format (flags, etc.); however, the received FCS did not check with the internally generated FCS. The frame should be discarded. The receiver remains active. (Do not forget that even though an error condition has been detected, all frame information up until that error has either been transferred to memory or passed to the CPU. This information should be invalidated. This applies to all receiver error conditions.) Note that the FCS, either transmitted or received, is never available to the CPU.

The Abort Detect result occurs whenever the receiver sees either an SDLC (8 1s) or an HDLC (7 1s), depending on the Operating Mode register. However, the intervening Abort character between a closing flag and an Idle does not generate an interrupt. If an Abort character (seen by an active receiver within a frame) is not preceded by a flag and is followed by an Idle, an interrupt will be generated for the Abort, followed by an Idle inter-

rupt one character time later. The Idle Detect result occurs whenever 15 consecutive 1s are received. After the Abort Detect interrupt, the receiver remains active. After the Idle Detect interrupt, the receiver is disabled and must be recommanded before further frames may be received.

If the EOP Interrupt bit is set in the Operating Mode register, the EOP Detect result is returned whenever an EOP character is received. The receiver is disabled, so the Idle following the EOP does not generate an Idle Detect interrupt.

The minimum number of bits in a valid frame between the flags is 32. Fewer than 32 bits indicates an error. If Buffered mode is selected, such frames are ignored, i.e., no data transfers or interrupts are generated. In non-Buffered mode, a < 32-bit frame generates an interrupt with the < 32-bit Frame result since data transfers may already have disturbed the 8257 or interrupt handler. The receiver remains active.

The DMA Overrun result results from the  $\overline{DMA}$  controller being too slow in extracting data from the 8273, i.e., the  $\overline{RxDACK}$  signal is not returned before the next received byte is ready for transfer. The receiver is disabled if this error condition occurs.

The Memory Buffer Overflow result occurs when the number of received bytes exceeds the receiver buffer length supplied by the  $B_0$  and  $B_1$  parameters in the receive command. The receiver is disabled.

The Carrier Detect Failure result occurs when the  $\overline{CD}$  pin goes high (inactive) during reception of a frame. The  $\overline{CD}$  pin is used to qualify reception and must be active by the time the address field starts to be received. If  $\overline{CD}$  is lost during the frame, a  $\overline{CD}$  Failure interrupt is generated and the receiver is disabled. No interrupt is generated if  $\overline{CD}$  goes inactive between frames.

If a condition occurs requiring an interrupt be generated before the CPU has finished reading the previous interrupt results, the second interrupt is generated after the current Result phase is complete (the RxINT pin and status bit go low then high). However, the interrupt result for this second interrupt will be a Receive Interrupt Overrun. The actual cause of the second interrupt is lost. One case where this may occur is at the end of a received frame where the line goes idle. The 8273 generates a received frame interrupt after the closing flag and then 15-bit times later, generates an Idle Detect interrupt. If the interrupt service routine is slow in reading the first interrupt's results, the internal RxI/R register still contains result information when the Idle Detect interrupt occurs. Rather than wiping out the previous results, the 8273 adds a Receive Interrupt Overrun result as an extra result. If the system's interrupt structure is such that the second interrupt is not acknowledged (interrupts are still disabled from the first interrupt), the Receive Interrupt Overrun result is read as an extra result, after those from the first interrupt. If the second interrupt is serviced, the Receive Interrupt Overrun is returned as a single result. (Note that the INT pins supply the necessary transitions to support a Program-

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mable Interrupt Controller such as the Intel 8259. Each interrupt generates a positive-going edge on the appropriate INT pin and the high level is held until the interrupt is completely serviced.) In general, it is possible to have interrupts occurring at one character time intervals. Thus the interrupt handling software must have at least that much response and service time.

The occurrence of Receive Interrupt Overruns is an indication of marginal software design; the system's interrupt response and servicing time is not sufficient for the data rates being attempted. It is advisable to configure the interrupt handling software to simply read the interrupt results, place them into a buffer, and clear the interrupt as quickly as possible. The software can then examine the buffer for new results at its leisure, and take appropriate action. This can easily be accomplished by using a result buffer flag that indicates when new results are available. The interrupt handler sets the flag and the main program resets it once the results are retrieved.

Both SDLC and HDLC allow frames which are of arbitrary length (>32 bits). The 8273 handles this N-bit reception through the high order bits ( $D_7$ – $D_5$ ) of the result code. These bits code the number of valid received bits in the last received information field byte. This coding is shown in Figure 30. The high order bits of the received partial btye are indeterminate. [The address, control, and information fields are transmitted least significant bit ( $A_0$ ) first. The FCS is complemented and transmitted most significant bit first.]

## Transmit Commands bus session AO labigo a session

The 8273 transmitter is supported by three Transmit commands and three corresponding Abort commands.

# Transmit Frame of large to not safeulli dis as babiyong

The Transmit Frame command simply transmits a frame. Four parameters are required when Buffered mode is selected and two when it is not. In either case, the first two parameters are the least and the most significant bytes of the desired frame length ( $L_0$ ,  $L_1$ ). In Buffered mode,  $L_0$  and  $L_1$  equal the length in bytes of the desired information field, while in the non-Buffered mode,  $L_0$  and  $L_1$  must be specified as the information field length plus two. ( $L_0$  and  $L_1$  specify the number of data transfers to be performed.) In Buffered mode, the address and control fields are presented to the transmitter as the third and fourth parameters respectively. In non-Buffered mode, the A and C fields must be passed as the first two data transfers.

When the Transmit Frame command is issued, the 8273 makes RTS (Request-to-Send) active (pin low) if it was not already. It then waits until CTS (Clear-to-Send) goes active (pin low) before starting the frame. If the Preframe Sync bit in the Operting Mode register is set, the transmitter prefaces two characters (16 transitions) before the opening flag. If the Flag Stream bit is set in the Operating Mode register, the frame (including Preframe Sync if selected) is started on a flag boundary. Otherwise the frame starts on a character boundary.

At the end of the frame, the transmitter interrupts the CPU (the interrupt results are discussed shortly) and returns to either Idle or Flag Stream, depending on the Flag Stream bit of the Operating Mode register. If RTS was active before the transmit command, the 8273 does not change it. If it was inactive, the 8273 will deactivate it within one character time.

# Loop Transmit peles at about bereftuß-non it sernant

Loop Transmit is similar to Frame Transmit (the parameter definition is the same). But since it deals with loop configurations, One Bit Delay mode must be selected.

If the transmitter is not in Flag Stream mode when this command is issued, the transmitter waits until after a received EOP character has been converted to a flag (this is done automatically) before transmitting. (The one bit delay is, of course, suspended during transmit.) If the transmitter is already in Flag Stream mode as a result of a selectively received frame during a Selective Loop Receive command, transmission will begin at the next flag boundary for Buffered mode or at the third flag boundary for non-Buffered mode. This discrepancy is to allow time for enough data transfers to occur to fill up the internal transmit buffer. At the end of a Loop Transmit, the One Bit Delay mode is re-entered and the flag stream mode is reset. More detailed loop operation is covered later. note however that no Abort Complete

# Transmit Transparent Stransparent Stranspare

The Transmit Transparent command enables the 8273 to transmit a block of raw data. This data is without SDLC protocol, i.e., no zero bit insertion, flags, or FCS. Thus it is possible to construct and transmit a Bi-Sync message for front-end processor switching or to construct and transmit an SDLC message with incorrect FCS for diagnostic purposes. Only the  $L_0$  and  $L_1$  parameters are used since there are not fields in this mode. (the 8273 does not support a Receive Transparent command.)

# Abort Commands us ин вязтамавая за отвежая заа о ома а-

Each of the above transmit commands has an associated Abort command. The Abort Frame Transmit command causes the transmitter to send eight contiguous ones (no zero bit insertion) immediately and then revert to either idle or flag streaming based on the Flag Stream bit. (The 8 1s as an Abort character is compatible with both SDLC and HDLC.)

For Loop Transmit, the Abort Loop Transmit command causes the transmitter to send one flag and then revert to one bit delay. Loop protocol depends upon FCS errors to detect aborted frames.

The Abort Transmit Transparent simply causes the transmitter to revert to either idles or flags as a function of the Flag Stream mode specified.

The Abort commands require no parameters, however, they do generate an interrupt and return a result when complete.

A summary of the Transmit commands is shown in Figure 31. Figure 32 shows the various transmit interrupt result codes. As in the receiver operation, the transmitter generates interrupts based on either good

completion of an operation or an error condition to start the Result phase.

The Early Transmit Interrupt result occurs after the last data transfer to the 8273 if the Early Transmit Interrupt bit is set in the Operating Mode register. If the 8273 is commanded to transmit again within two character times, a single flag will separate the frames. (Buffered mode must be used for a single flag to separate the frames. If non-Buffered mode is selected, three flags will separate the frames.) If this time constraint is not met, another interrupt is generated and multiple flags or idles will separate the frames. The second interrupt is the normal Frame Transmit Complete interrupt. The Frame Transmit Complete result occurs at the closing flag to signify a good completion.

The DMA Underrun result is analogous to the DMA Overrun result in the receiver. Since SDLC does not support intraframe time fill, if the DMA controller or CPU does not supply the data in time, the frame must be aborted. The action taken by the transmitter on this error is automatic. It aborts the frame just as if an Abort command had been issued.

Clear-to-Send Error result is generated if  $\overline{\text{CTS}}$  goes inactive during a frame transmission. The frame is aborted as above.

The Abort Complete result is self-explanatory. Please note however that no Abort Complete interrupt is generated when an automatic abort occurs. The next command type consists of only one command.

COMMAND	HEX	PARAMETERS*	RESULTS TxI/R
TRANSMIT FRAME	C8 CC	L <sub>0</sub> , L <sub>1</sub> , A, C NONE	IS TIC
LOOP TRANSMIT ABORT	CA	L <sub>0</sub> , L <sub>1</sub> , A, C NONE	TIC
TRANSMIT TRANSPARENT ABORT	C0 CD	LO, L1 NONE	TIC

\*A AND C ARE PASSED AS PARAMETERS IN BUFFERED MODE ONLY.

Figure 31. Transmitter Command Summary

		TRANSMITTER INTERRUPT RESULT CODE	Tx STATUS AFTER INT
	000 01100	EARLY TX INTERRUPT	ACTIVE
	000 01101	FRAME TX COMPLETE O DOCA AS AS	IDLE OR FLAGS
	000 01110	DMA UNDERRUN	ABORT
	000 01111	CLEAR TO SEND ERROR	ABORT
n	000 10000	ABORT COMPLETE	IDLE OR FLAGS

Figure 32. Transmitter Interrupt Result Codes

### Reset Command In Indianate Hannat Hoda and

The Reset command provides a software reset function for the 8273. It is a special case and does not utilize the normal command interface. The reset facility is provided in the Test Mode register. The 8273 is reset by simply outputting a 01H followed by a 00H to the Test Mode register. Writing the 01 followed by the 00 mimicks the action required by the hardware reset. Since the 8273 requires time to process the reset internally, at least 10 cycles of the ØCLK clock must occur between the

writing of the 01 and the 00. The action taken is the same as if a hardware reset is performed, namely:

- 1. The modem control outputs are forced high inactive).
  - 2. The 8273 Status register is cleared.
  - 3. Any commands in progress cease.
  - The 8273 enters an idle state until the next command is issued.

#### Modem Control Commands

The modem control ports were discussed earlier in the Hardware section. The commands used to manipulate these ports are shown in Figure 33. The Read Port A and Read Port B commands are immediate. The bit definition for the returned byte is shown in Figures 13 and 14. Do not forget that the returned value represents the logical condition of the pin, i.e., pin active (low) = bit set.

PORT	COMMAND	HEX	PARAMETER	REG RESULT
A INPUT	READ	22	NONE	PORT VALUE
100-10	READ	23	NONE	PORT VALUE
B OUTPUT	SET 9	A3	SET MASK	NONE
blail no	RESET	63	RESET MASK	NONE

Figure 33. Modem Control Command Summary

The Set and Reset Port B commands are similar to the Initialization commands in that they use a mask parameter which defines the bits to be changed. Set Port B utilizes a logical OR mask and Reset Port B uses a logical AND mask. Setting a bit makes the pin active (low), Resetting the bit deactivates the pin (high).

To help clarify the numerous timing relationships that occur and their consequences, Figures 34 and 35 are provided as an illustration of several typical sequences. It is suggested that the reader go over these diagrams and re-read the appropriate part of the previous sections if necessary.

### HLDC CONSIDERATIONS lead only to selved insollingle

The 8273 supports HDLC as well as SDLC. Let's discuss how the 8273 handles the three basic HDLC/SDLC differences: extended addressing, extended control, and the 7 1s Abort character.

Recalling Figure 4A, HDLC supports an address field of indefinite length. The actual amount of extension used is determined by the least significant bit of the characters immediately following the opening flag. If the LSB is 0, more address field bytes follow. If the LSB is 1, this byte is the final address field byte. Software must be used to determine this extension.

If non-Buffered mode is used, the A, C, and I fields are in memory. The software must examine the initial characters to find the extent of the address field. If Buffered mode is used, the characters corresponding to the SDLC A and C fields are transferred to the CPU as interrupt results. Buffered mode assumes the two characters following the opening flag are to be transferred as interrupt results regardless of content or meaning. (The 8273

does not know whether it is being used in an SDLC or an HDLC environment.) In SDLC, these characters are necessarily the A and C field bytes, however in HDLC, their meaning may change depending on the amount of extension used. The software must recognize this and examine the transferred results as possible address field extensions.

Frames may still be selectively received as is needed for secondary stations. The Selective Receive command is still used. This command qualifies a frame reception on the first byte following the opening flag matching either of the  $A_1$  or  $A_2$  match byte parameters. While this does not allow qualification over the complete range of HDLC addresses, it does perform a qualification on the first address byte. The remaining address field bytes, if any, are then examined via software to completely qualify the frame.

Once the extent of the address field is found, the following bytes form the control field. The same LSB test used for the address field is applied to these bytes to determine the control field extension, up to two bytes maximum. The remaining frame bytes in memory represent the information field.

The Abort character difference is handled in the Operating Mode register. If the HDLC Abort Enable bit is set, the reception of seven contiguous ones by an active receiver will generate an Abort Detect interrupt rather than eight ones. (Note that both the HDLC Abort Enable bit and the EOP Interrupt bit must not be set simultaneously.)

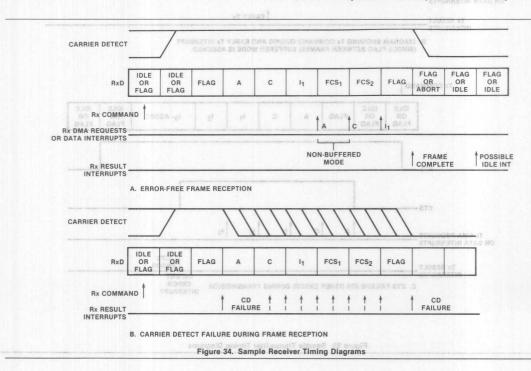
Now let's move on to the SDLC loop configuration discussion.

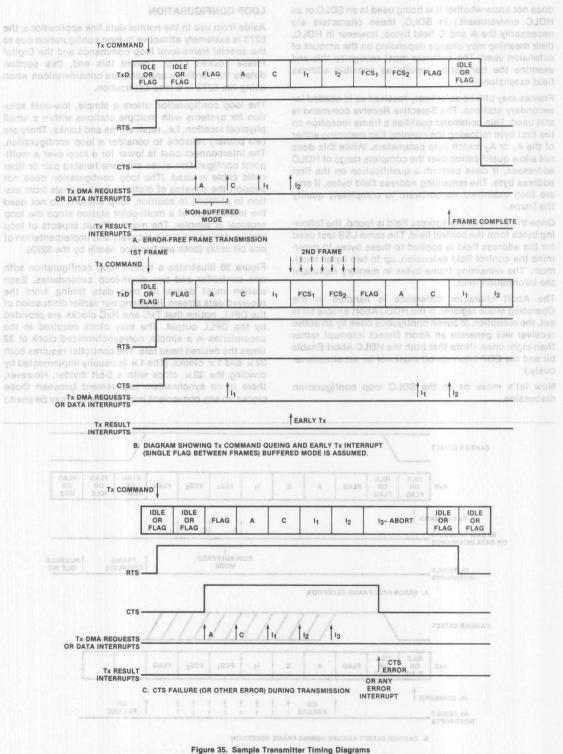
#### LOOP CONFIGURATION

Aside from use in the normal data link applications, the 8273 is extremely attractive in loop configuration due to the special frame-level loop commands and the Digital Phase Locked Loop. Toward this end, this section details the hardware and software considerations when using the 8273 in a loop application.

The loop configuration offers a simple, low-cost solution for systems with multiple stations within a small physical location, i.e., retail stores and banks. There are two primary reasons to consider a loop configuration. The interconnect cost is lower for a loop over a multipoint configuration since only one twisted pair or fiber optic cable is used. (The loop configuration does not support the passing of distinct clock signals from station to station.) In addition, loop stations do not need the intelligence of a multi-point station since the loop protocal is simpler. The most difficult aspects of loop station design are clock recovery and implementation of one bit delay (both are handled neatly by the 8273).

Figure 36 illustrates a typical loop configuration with one controller and two down-loop secondaries. Each station must derive its own data timing from the received data stream. Recalling our earlier discussion of the DPLL, notice that TxC and RxC clocks are provided by the DPLL output. The only clock required in the secondaries is a simple, non-synchronized clock at 32 times the desired baud rate. The controller requires both 32 x and 1 x clocks. (The 1 x is usually implemented by dividing the 32 x clock with a 5-bit divider. However, there is no synchronism requirement between these clocks so any convenient implementation may be used.)





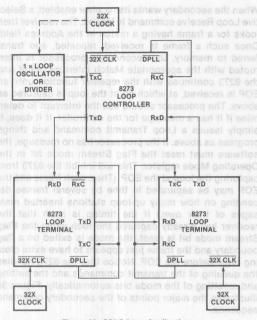


Figure 36. SDLC Loop Application

A quick review of loop protocol is appropriate. All communication on the loop is controlled by the loop controller. When the controller wishes to allow the secondaries to transmit, it sends a polling frame (the control field contains a poll code) followed by an EOP (End-Foll) character. The secondaries use the EOP character to capture the loop and insert a response frame as will be discussed shortly.

The secondaries normally operate in the repeater mode, retransmitting received data with one bit time of delay. All received frames are repeated. The secondary uses the one bit time of delay to capture the loop.

When the loop is idle (no frames), the controller transmits continuous flag characters. This keeps transitions on the loop for the sake of down-loop phase locked loops. When the controller has a non-polling frame to transmit, it simply transmits the frame and continues to send flags. The non-polling frame is then repeated around the loop and the controller receives it to signify a complete traversal of the loop. At the particular secondary addressed by the frame, the data is transferred to memory while being repeated. Other secondaries simply repeat it.

If the controller wants to poll the secondaries, it transmits a polling frame followed by all 1s (no zero bit insertion). The final zero of the closing frame plus the first seven 1s form an EOP. While repeating, the secondaries monitor their incoming line for an EOP. When an EOP is received, the secondary checks if it has any response for the controller. If not, it simply continues repeating. If the secondary has a response, it changes the seventh EOP one into a zero (the one bit time of delay allows time for this) and repeats it, forming a flag for the down-loop stations. After this flag is transmitted,

the secondary terminates its repeater function and inserts its response frame (with multiple preceding flags if necessary). After the closing flag of the response, the secondary re-enters its repeater function, repeating the up-loop controller 1s. Notice that the final zero of the response's closing flag plus the repeated 1s from the controller form a new EOP for the next down-loop secondary. This new EOP allows the next secondary to insert a response if it desires. This gives each secondary a chance to respond.

Back at the controller, after the polling frame has been transmitted and the continuous 1s started, the controller waits until it receives an EOP. Receiving an EOP signifies to the controller that the original frame has propagated around the loop followed by any responses inserted by the secondaries. At this point, the controller may either send flags to idle the loop or transmit the next frame. Let's assume that the loop is implemented completely with the 8273s and describe the command flows for a typical controller and secondary.

The loop controller is initialized with commands which specify that the NRZI, Preframe Sync, Flag Stream, and EOP Interrupt modes are set. Thus, the controller encodes and decodes all data using NRZI format. Preframe Sync mode specifies that all transmitted frames be prefaced with 16 line transitions. This ensures that the minimum of 12 transitions needed by the DPLLs to lock after an all 1s line have occurred by the time the secondary sees a frame's opening flag. Setting the Flag Stream mode starts the transmitter sending flags which idles the loop. And the EOP Interrupt mode specifies that the controller processor will be interrupted whenever the active receiver sees an EOP, indicating the completion of a poll cycle.

When the controller wishes to transmit a non-polling frame, it simply executes a Frame Transmit command. Since the Flag Stream mode is set, no EOP is formed after the closing flag. When a polling frame is to be transmitted, a General Receive command is executed first. This enables the receiver and allows reception of all incoming frames; namely, the original polling frame plus any response frames inserted by the secondaries. After the General Receive command, the frame is transmitted with a Frame Transmit command. When the frame is complete, a transmitter interrupt is generated. The loop controller processor uses this interrupt to reset Flag Stream mode. This causes the transmitter to start sending all 1s. An EOP is formed by the last flag and the first 7 1s. This completes the loop controller transmit sequence.

At any time following the start of the polling frame transmission the loop controller receiver will start receiving frames. (The exact time difference depends, of course, on the number of down-loop secondaries due to each inserting one bit time of delay.) The first received frame is simply the original polling frame. However, any additional frames are those inserted by the secondaries. The loop controller processor knows all frames have been received when it sees an EOP Interrupt. This interrupt is generated by the 8273 since the EOP Interrupt mode was set during initialization. At this point, the transmitter may be commanded either to enter Flag

Stream mode, idling the loop, or to transmit the next frame. A flowchart of the above sequence is shown in Figure 37.

The secondaries are initialized with the NRZI and One Bit Delay modes set. This puts the 8273 into the repeater mode with the transmitter repeating the received data with one bit time of delay. Since a loop station cannot transmit until it sees and EOP character, any transmit command is gueued until an EOP is received. Thus whenever the secondary wishes to transmit a response, a Loop Transmit command is issued. The 8273 then waits until it receives an EOP. At this point, the receiver changes the EOP into a flag, repeats it, resets One Bit Delay mode stopping the repeater function, and sets the transmitter into Flag Stream mode. This captures the loop. The transmitter now inserts its message. At the closing flag, Flag Stream mode is reset, and One Bit Delay mode is set, returning the 8273 to repeater function and forming an EOP for the next down-loop station. These actions happen automatically after a Loop Transmit command is issued, lini ai reflorance gool enT

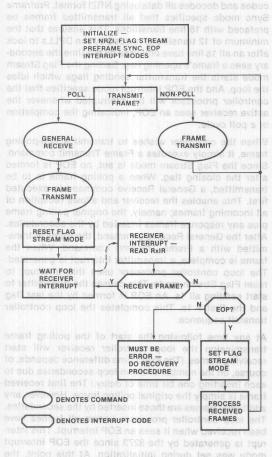
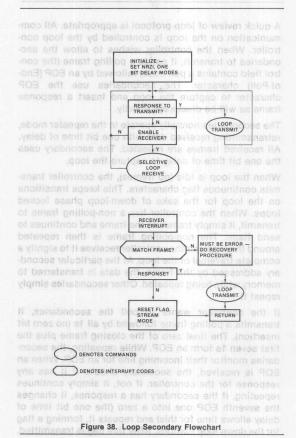


Figure 37. Loop Controller Flowchart

When the secondary wants its receiver enabled, a Selective Loop Receive command is issued. The receiver then looks for a frame having a match in the Address field. Once such a frame is received, repeated, and transferred to memory, the secondary's processor is interrupted with the appropriate Match interrupt result and the 8273 continues with the repeater function until an EOP is received, at which point the loop is captured as above. The processor should use the interrupt to determine if it has a message for the controller. If it does, it simply issues a Loop Transmit command and things progress as above. If the processor has no message, the software must reset the Flag Stream mode bit in the Operating Mode register. This will inhibit the 8273 from capturing the loop at the EOP. (The match frame and the EOP may be separated in time by several frames depending on how many up-loop stations inserted messages of their own.) If the timing is such that the receiver has already captured the loop when the Flag Stream mode bit is reset, the mode is exited on a flag boundary and the frame just appears to have extra closing flags before the EOP. Notice that the 8273 handles the queuing of the transmit commands and the setting and resetting of the mode bits automatically. Figure 38 illustrates the major points of the secondary command sequence.



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When an off-line secondary wishes to come on-line, it must do so in a manner which does not disturb data on the loop. Figure 39 shows a typical hardware interface. The line labeled Port could be one of the 8273 Port B outputs and is assumed to be high (1) initially. Thus up-loop data is simply passed down-loop with no delay; however, the receiver may still monitor data on the loop. To come on-line, the secondary is initialized with only the EOP Interrupt mode set. The up-loop data is then monitored until an EOP occurs. At this point, the secondary's CPU is interrupted with an EOP interrupt. This signals the CPU to set One Bit Delay mode in the 8273 and then to set Port low (active). These actions switch the secondary's one bit delay into the loop. Since after the EOP only 1s are traversing the loop, no loop disturbance occurs. The secondary now waits for the next EOP, captures the loop, and inserts a "new on-line" message. This signals the controller that a new secondary exists and must be acknowledged. After the secondary receives its acknowledgement, the normal command flow is used.

It is hopefully evident from the above discussion that the 8273 offers a very simple and easy to implement solution for designing loop stations whether they are controllers or down-loop secondaries.

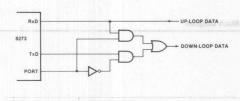


Figure 39. Loop Interface

### APPLICATION EXAMPLE

This section describes the hardware and software of the 8273/8085 system used to verify the 8273 implementation of SDLC on an actual IBM SDLC Link. This IBM link was gratefully volunteered by Raytheon Data Systems in Norwood, Mass. and I wish to thank them for their generous cooperation. The IBM system consisted of a 370 Mainframe, a 3705 Communications Processor, and a 3271 Terminal Controller. A Comlink II Modem supplied the modem interface and all communications took place at 4800 baud. In addition to observing correct responses, a Spectron D601B Datascope was used to verify the data exchanges. A block diagram of the system is shown in Figure 40. The actual verification was accomplished by the 8273 system receiving and responding to polls from the 3705. This method was ed on both point-to-point and multi-point configuras. No attempt was made to implement any higher ol software over that of the poll and poll resince such software would not affect the verithe 8273 implementation. As testimony to the

of the 8273, the system worked on the first

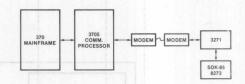


Figure 40. Raytheon Block Diagram

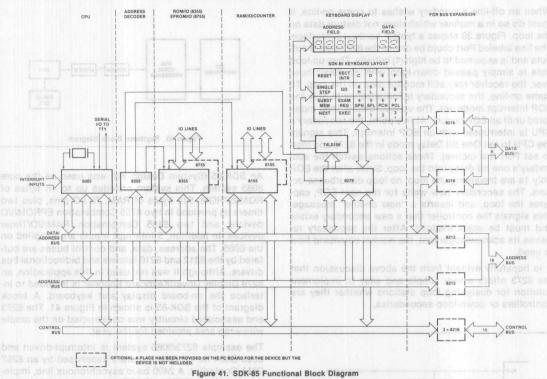
An SDK-85 (System Design Kit) was used as the core 8085 system. This system provides up to 4K bytes of ROM/EPROM, 512 bytes of RAM, 76 I/O pins, plus two timers as provided in two 8755 Combination EPROM/I/O devices and two 8155 Combination RAM/I/O/Timer devices. In addition, 5 interrupt inputs are supplied on the 8085. The address, data, and control buses are buffered by the 8212 and 8216 latches and bidirectional bus drivers. Although it was not used in this application, an 8279 Display Driver/Keyboard Encoder is included to interface the on-board display and keyboard. A block diagram of the SDK-85 is shown in Figure 41. The 8273 and associated circuitry was constructed on the ample wire-wrap area provided for the user.

The example 8273/8085 system is interrupt-driven and uses DMA for all data transfers supervised by an 8257 DMA Controller. A 2400 baud asynchronous line, implemented with an 8251A USART, provides communication between the software and the user. 8253 Programmable Interval Timer is used to supply the baud rate clocks for the 8251A and 8273. (The 8273 baud rate clocks were used only during initial system debug. In actual operation, the modem supplied these clocks via the RS-232 interface.) Two 2142 1K x 4 RAMs provided 512 bytes of transmitter and 512 bytes of receiver buffer memory. (Command and result buffers, plus miscellaneous variables are stored in the 8155s.) The RS-232 interface utilized MC1488 and MC1489 RS-232 drivers and receivers. The schematic of the system is shown in Figure 42.

One detail to note is the DMA and interrupt structure of the transmit and receive channels. In both cases, the receiver is always given the higher priority (8257 DMA channel 0 has priority over the remaining channels and the 8085 RST 7.5 interrupt input has priority over the RST 6.5 input.) Although the choice is arbitrary, this technique minimizes the chance that received data could be lost due to other processor or DMA commitments.

Also note that only one 8205 Decoder is used for both the peripherals' and the memorys' Chip Selects. This was done to eliminate separate memory and I/O decoders since it was known beforehand that neither address space would be completely filled.

The 4 MHz crystal and 8224 Clock Generator were used only to verify that the 8273 operates correctly at that maximum spec speed. In a normal system, the 3.072 MHz clock from the 8085 would be sufficient. (This fact was verified during initial checkout.)



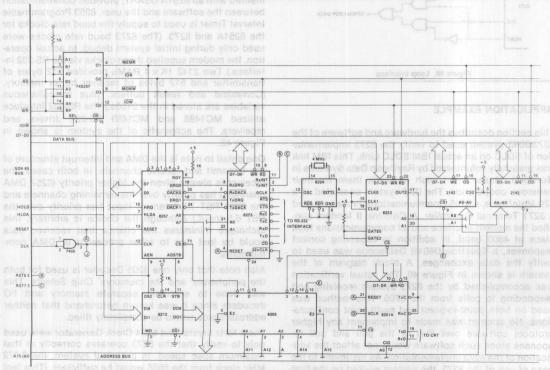


Figure 42. 8273/SDK-85 System

The software consists of the normal monitor program supplied with the SDK-85 and a program to input commands to the 8273 and to display results. The SDK-85 monitor allows the user to read and write on-board RAM, start execution at any memory location, to single-step through a program, and to examine any of the 8085's internal registers. The monitor drives either the on-board keyboard/LED display or a serial TTY interface. This monitor was modified slightly in order to use the 8251A with a 2400 baud CRT as opposed to the 110 baud normally used. The 8273 program implements monitor-like user interface. 8273 commands are entered by a twocharacter code followed by any parameters required by that command. When 8273 interrupts occur, the source of the interrupt is displayed along with any results associated with it. To gain a flavor of how the user/program interface operates, a sample output is shown in Figure 43. The 8273 program prompt character is a "-" and user inputs are underlined.

The "SO 05" implements the Set Operating Mode command with a parameter of 05H. This sets the Buffer and Flag Stream modes. "SS 01" sets the 8273 in NRZI mode using the Set Serial I/O Mode command. The next command specifies General Receiver with a receiver buffer size of 0100H bytes ( $B_0 = 00, B_1 = 01$ ). The "TF" command causes the 8273 to transmit a frame containing an address field of C2H and control field of 11H. The information field is 001122. The "TF" command has a special format. The  $L_0$  and  $L_1$  parameters are computed from the number of information field bytes entered.

After the TF command is entered, the 8273 transmits the frame (assuming that the modem protocol is observed). After the closing flag, the 8273 interrupts the 8085. The 8085 reads the interrupt results and places them in a buffer. The software examines this buffer for new results and if new results exist, the source of the interrupt is displayed along with the results.

In this example, the 0DH result indicates a Frame Complete interrupt. There is only one result for a transmitter interrupt, the interrupt's trailing zero results were included to simplify programming.

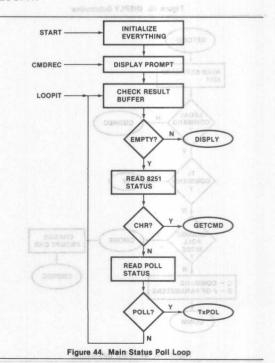
The next event is a frame reception. The interrupt results are displayed in the order read from the 8273. The E0H indicates a General Receive interrupt with the last byte of the information field received on an 8-bit boundary. The 03 00 (R<sub>0</sub>, R<sub>1</sub>) results show that there are 3H bytes of information field received. The remaining two results indicate that the received frame had a C2H address field and a 34H control field. The 3 bytes of information field are displayed on the next line.

Figure 43. Sample 8273 Monitor I/O

Figures 44 through 51 show the flowcharts used for the 8273 program development. The actual program listing is included as Appendix A. Figure 44 is the main status poll loop. After all devices are initialized and a prompt character displayed, a loop is entered at LOOPIT. This loop checks for a change of status in the result buffer of a keyboard character has been received by the 8251 or if a poll frame has been received. If any of these conditions are met, the program branches to the appropriate routine. Otherwise, the loop is traversed again.

The result buffer is implemented as a 255-byte circular buffer with two pointers: CNADR and LDADR. CNADR is the console pointer. It points to the next result to be displayed LDADR is the load pointer. It points to the next empty position in the buffer into which the interrupt handler places the next result. The same buffer is used for both transmitter and receiver results. LOOPIT examines these pointers to detect when CNADR is not equal to LDADR indicating that the buffer contains results which have not been displayed. When this occurs, the program branches to the DISPLY routine.

DISPLY determines the source of the undisplayed results by testing the first result. This first result is necessarily the interrupt result code. If this result is OCH or greater, the result is from a transmitter interrupt. Otherwise it is from a receiver source. The source of the result code is then displayed on the console along with the next four results from the buffer. If the source was a transmitter interrupt, the routine merely repoints the pointer CNADR and returns to LOOPIT. For a receiver source, the receiver data buffer is displayed in addition to the receiver interrupt results before returning to LOOPIT.



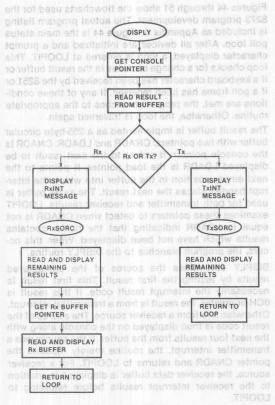


Figure 45. DISPLY Subroutine

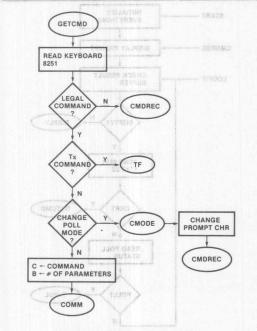


Figure 46. GETCMD Subroutine

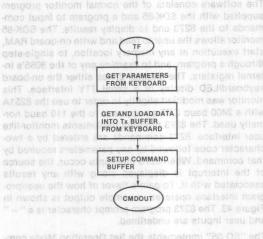


Figure 47. TF Subroutine

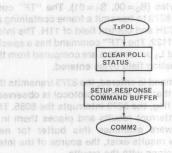


Figure 48. TxPOL Subroutine

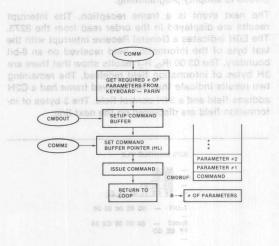
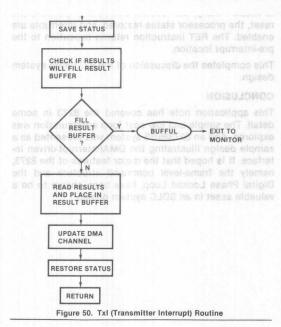


Figure 49. COMM Subroutine with Command Buffer Format



If the result buffer pointers indicate an empty buffer, the 8251A is polled for a keyboard character. If the 8251 has a character, GETCMD is called. There the character is read and checked if legal. Illegal characters simply cause a reprompt. Legal characters indicate the start of a command input. Most commands are organized as two characters signifying the command action; i.e., GR — General Receive. The software recognizes the two character command code and takes the appropriate action. For non-Transmit type commands, the hex equivalent of the command is placed in the C register and the number of parameters associated with that command is placed in the B register. The program then branches to the COMM routine.

The COMM routine builds the command buffer by reading the required number of parameters from the keyboard and placing them at the buffer pointed at by CMDBUF. The routine at COMM2 then issues this command buffer to the 8273.

If a Transmit type command is specified, the command buffer is set up similarly to the the COMM routine; however, since the information field data is entered from the keyboard, an intermediate routine, TF, is called. TF loads the transmit data buffer pointed at by TxBUF. It counts the number of data bytes entered and loads this number into the command buffer as  $L_0$ ,  $L_1$ . The command is then issued to the 8273 by jumping to CMDOUT.

One command does not directly result in a command being issued to the 8273. This command, Z, operates a software flip-flop which selects whether the software will respond automatically to received polling frames. If

memory location POLIN is made nonzero by the receiver interrupt handler. LOOPIT examines this location and if it is nonzero, causes a branch to the TxPOL routine. The TxPOL routine clears POLIN, sets a pointer to a special command buffer at CMDBUF1, and issues the command by way of the COMM2 entry in the COMM routine. The special command buffer contains the appropriate response frame for the poll frame received. These actions only occur when the Z command has changed the prompt to a '+'. If the prompt is normal '-', polling frames are displayed as normal frames and no response is transmitted. The Poll-Response mode was used during the IBM tests.

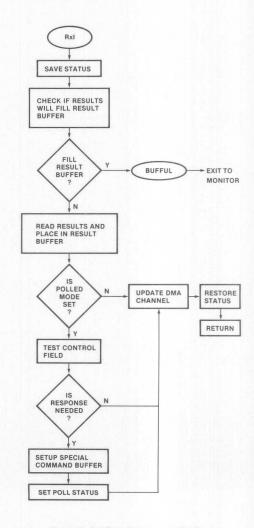


Figure 51. RxI (Recevier Interrupt) Routine

The final two software routines are the transmitter and receiver interrupt handlers. The transmit interrupt handler, TxI, simply saves the registers on the stack and checks if loading the result buffer will fill it. If the result buffer will overfill, the program is exited and control is passed to the SDK-85 monitor. If not, the results are read from the TxI/R register and placed in the result buffer at LDADR. The DMA pointers are then reset, the registers restored, and interrupts enabled. Execution then returns to the pre-interrupt location.

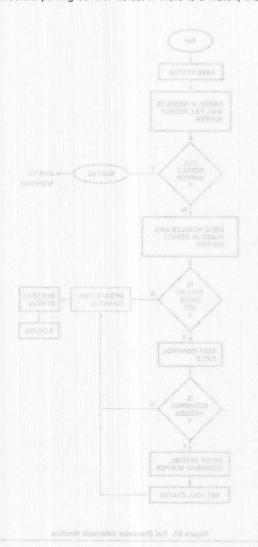
The receiver interrupt handler, RxI, is only slightly more complex. As in TxI, the registers are saved and the possibility of overfilling the result buffer is examined. If the result buffer is not full, the results are read from RxI/R and placed in the buffer. At this point the prompt character is examined to see if the Poll-Response mode is selected. If so, the control field is compared with two possible polling control fields. If there is a match, the

special command buffer is loaded and the poll indicator, POLIN, is made nonzero. If no match occurred, no action is taken. Finally, the receiver DMA buffer pointers are reset, the processor status restored, and interrupts are enabled. The RET instruction returns execution to the pre-interrupt location.

This completes the discussion of the 8273/8085 system design.

### CONCLUSION

This application note has covered the 8273 in some detail. The simple and low cost loop configuration was explored. And an 8273/8085 system was presented as a sample design illustrating the DMA/interrupt-driven interface. It is hoped that the major features of the 8273, namely the frame-level command structure and the Digital Phase Locked Loop, have been shown to be a valuable asset in an SDLC system design.



UPDATE DISA
CHARIST

RESTORE STATES

RESTORE S

If the result buffer pointers indicate an empty buffer, the 8251 has a character, difficult to a keyboard character, if the 8251 has a character, difficult is called. There the character is a character, difficult is called. There the character simply read and characters amply a command input. Most commands are organized as two characters signifying the command action; i.e., GR—deneral Receive. The command action; i.e., GR—action command code and takes the appropriate action. For non-Transmit type commands, the hex equivalent of the command is praced in the C register and the number of parameters associated with that command is placed in the program then branches to the

The COMM routine builds the command buffer by reading the required number of parameters from the keyboard and placing them at the buffer pointed at by CMDBUF. The routine at COMM2 then issues this command buffer to the 8273.

If a Transmit type command is specified, the command buffer is set up similarly to the the COMM routine; however, since the information fled data is entered from the keyboard, an intermediate routine, TF, is called, TF loads the transmit data buffer pointed at by TRBUF, it counts the number of data bytes entered and loads this number into the command buffer as Lo.

L., The command is then issued to the 8273 by jumping

One command does not directly result in a command being issued to the 8273. This command, Z, operates a rotiware flip-flop which selects whether the software will respond automatically to received polling frames. If

## APPENDIX A

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TH PRYTHEOU POLL MODE RODED				
			12	
			83	
APPEND	IX	B SUPPOR		
RO - RESET OPERATING MODE				
SO = 25T OPENITING NODE				
			ES /	
AMERY TROOPS - NA			27	
2P - SET PORT B				
SD - SET ONE BIT DELRY (PRR = 88)				
ST - 25 ECLINE F005 BECEINE				
PPOPPER TO THE COLUMN TO THE TRANSPORT OF THE ASSESSMENT OF THE COLUMN TWO				
INPLEMENT LOGICAL 'OR' PUNCTIONS				
S DEPLOYER LOSIONS (SND) FUNCTIONS				
te in etak kingila dan ang salat kapan kaka ang salat kingka kapan pag				
SOURCIED WARN SELECTIVE RECEIVE IS USED.				
The second of the second desirable				
#### (2 LTRS)* 'PRR ##* 'PRC #2' ETC				
		Desired & All		
INVO FORMAL IS: "TH" "R" "C" "BUFFER CONTENTS".				
IS NEEDED, BUFFER CONTENTS IS ENCED HITH A CR.			86	
TO RECEIVE OF CHESTERS STAND TREETS ST				
with the statement of the second department of the second				

## APPENDIX A

ASM80 :F1:RAYT73. SRC

ISIS-II	8080/8085	MACRO	ASSEMBLER	X108		MODULE	PAGE	1
LOC	np r	CEN	50	IDCE CT	OTEMENT			
LUC	003	DE@	30	ORCE 31	HICHCHI			
		- 1	\$NOPAGING	MOD85	NOCONE	,		
0000			TRUE E		00H		: 00 FOR	RAYTHEON
			;					SELF-TEST
0000			TRUE1 E	QU	99H			NORMAL RESPONSE
			;					LOOP RESPONSE
0000		6	DEM E	QU	00H			NO DEMO
		7	j				FF FOR	DEMO DEMO
		8	;					
		9	;					
		10	GENERAL	8273 MC	ONITOR 6	IITH RAYT	HEON POL	L MODE ADDED
		11						
		17						
		18				new areas		
				SUPPORT	ED ARE	The Contract of the Contract o	W 237 10	AL I/O MODE
		20						I/O MODE
		21 22					T OPERAT	ATING MODE
		23					CEIVER D	
		24					NERAL RE	
		25					LECTIVE	
		26					ANSMIT F	
		27	;			AF - AB	ORT FRAM	E
		28	;			SP - SE	T PORT B	
		29	;			RP - RE	SET PORT	В
		30	;			RB - RE	SET ONE	BIT DELAY (PAR = 7F)
		31				SB - SE	T ONE BI	T DELAY (PAR = 80)
		32						LOOP RECEIVE
		33					RANSMIT L	
		34				Z - CH	IANGE MODI	ES FLIP/FLOP
		38						
				skrakrakrakrakra	kajtajtajtajtajtaj	kajajajajajajajajaj	olololololololol	
		40		CET/ CO	MMONING	TMDL CMCN	IT LOCTOR	CODY EUROTIONS
								L 'OR' FUNCTIONS CAL 'AND' FUNCTIONS
		43		KESEI	COMMINIC	75 INFLER	ENI LUGI	CHL HND FUNCTIONS
				oleoleoleoleoleoleol	iololololololol	oleskaleskaleskale	niciololololololo	otalestestestestestestestestestestestesteste
		45						
		46	BUFFERED	MODE M	NUST BE	SELECTED	WHEN SEI	LECTIVE RECEIVE IS USED.
		47	;					
		48	; COMMAND	FORMAT	IS: 'CO	MMAND (2	LTRS)	'PAR. #1' 'PAR. #2' ETC.
		49	;					
		50	; THE TRAN	SMIT FR	RAME COM	MAND FOR	MAT IS:	'TF' 'A' 'C' 'BUFFER CONTENTS'.
		51	; N	O LENGT	TH COUNT	IS NEED	ED. BUF	FER CONTENTS IS ENDED WITH A CR.
		52						
				ojenjenjenjenjenje		olejejejejejejej	njojojojojojojo	
		54		00.5	I II IFN S	HIER WAT		
		55	FULLED M	UDE:	WHEN PO	ILLED MOD	E IS SELI	ECTED (DENOTED BY A '+' PROMPT), IF

```
A SNRM-P OR RR(0)-P IS RECEIVED, A RESPONSE FRAME OF NSA-F
              56 ;
              57;
                             OR RR(0)-F IS TRANSMITTED. OTHER COMMANDS OPERATE NORMALLY.
              62; SELECTED BOW TOUTHOUT TOUTHOUT MOUNTED TENTER 15
              63 ; actorologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologicologic
              65 ; 8273 EQUATES 138 6180 XX
              MUDE LEXA 2 STOP, NO. PERSIT; 66
              67 STAT73 EQU 90H
0090
                                         STATUS REGISTER
                             90H
                                         COMMAND REGISTER
0090
              68 COMM73 EQU
              69 PARM73 EQU
                             91H
0091
                                          PARAMETER REGISTER
                                         RESULT REGISTER
0091
              70 RESL73 EQU
                             91H
0092
              71 TXIR73 EQU
                              92H
                                          TX INTERRUPT RESULT REGISTER
          72 RXIR73 EQU 93H
0093
                                          RX INTERRUPT RESULT REGISTER
              73 TEST73 EQU 92H 0509
                                         ; TEST MODE REGISTER OF THE
0092
     74 CPBF EQU 20H
                                          ; PARAMETER BUFFER FULL BIT
9929
0004
              75 TXINT EQU 04H
                                          TX INTERRUPT BIT IN STATUS REGISTER
              76 RXINT EQU 08H
0008
                                          ; RX INTERRUPT BIT IN STATUS REGISTER
      77 TXIRA EQU 01H
0001
                                          TX INT RESULT AVAILABLE BIT
              78 RXIRA EQU
0002
                              02H
                                          FRX INT RESULT AVAILABLE BIT
              79;
              80 ; 8253 EQUATES
              81 :
              82 MODE53 EQU 98H
                                        ; 8253 MODE WORD REGISTER
AA9R
                                         COUNTER 0 REGISTER
                             9CH
009C
              83 CNT053 EQU
                           9DH
                                        COUNTER 1 REGISTER
009D
              84 CNT153 EQU
                                        ; COUNTER 2 REGISTER
009E
         85 CNT253 EQU 9EH
                             000CH
                                        ; CONSOLE BAUD RATE (2400)
000C
              86 COBR
                       EQU
                             36H
                                        ; MODE FOR COUNTER 0
0036
              87 MDCNT0 EQU
                                         ; MODE FOR COUNTER 2
              88 MDCNT2 EQU 0B6H
00B6
                                         ; 8273 BAUD RATE LSB ADR
2017
              89 LKBR1 EQU 2017H
         90 LKBR2 EQU 2018H
2018
                                         ; 8273 BAUD RATE MSB ADR
       RESULT BUFFER CONSOLE POINTER STORAGE
            92 ; BAUD RATE TABLE: BAUD RATE
                                             LKBR1 LKBR2
              93 ; 2003 2081000 9-159 stateletetetete stateletete statelete
              94 ; 3000 100000 9-(8)99 9600
                                              2E 00
                    3000 3000000 7-8201 4800
                                              5C 00 4824 221
              95;
                    3000 1087800 9-(8)88 2400
                                              B9
                                                     00
              96;
                   1200
              97 ;
                                             H21872 01 THIS COL
              98 ; 1041 401733.532 3004 1104 600
                                             HB18 E5 11 02 11 109 381
              99; 901601081 3008 0801 300
                                             HT C9 00 05 300130 521
              100 ;
              101 ;
              102 : 8257 EQUATES
              103;
                                         ; 8257 MODE PORT
00A8
              104 MODES7 EQU
00A0
              105 CHOADR EQU
                              0A0H
                                         CH0 (RX) ADR REGISTER
                                  ; CHO TERMINAL COUNT REGISTER
00A1
              106 CHOTC
                       EQU
                              OA1H
                              0A2H ; CH1 (TX) ADR REGISTER
00A2
              107 CH1ADR
                       EQU
                                  CH1 TERMINAL COUNT REGISTER
00A3
              108 CH1TC
                       FOU
                              HEAD
                              9A8H STATUS REGISTER
00A8
             109 STAT57
                       EQU
8200
             110 RXBUF
                              8200H ; RX BUFFER START ADDRESS
                              8000H ; TX BUFFER START ADDRESS
8000
             111 TXBUF
                       EQU
                              62H ; DISABLE RX DMA CHANNEL, TX STILL ON
0062
              112 DRDMA
                       EQU
41FF
              113 RXTC
                       EQU
                                        ; TERMINAL COUNT AND MODE FOR RX CHANNEL
                              63H ; ENABLE BOTH TX AND RX CHANNELS-EXT. WR. TX STOP
0063
              114 ENDMA FOU
                              61H ; DISABLE TX DMA CHANNEL, RX STILL ON
9961
              115 DTDMA
                       EQU
81FF
             116 TXTC
                       EQU
                                    ; TERMINAL COUNT AND MODE FOR TX CHANNEL
 117;
```

2-302 AFN-00811A

```
120 CNTL51 EQU
                                                                   CONTROL WORD REGISTER
                    121 STAT51 EQU 89H
                                                                  STATUS REGISTER
                      122 TXD51 EQU
                                               88H
                                                                   ; TX DATA REGISTER
0088
                      123 RXD51
                                     EQU
                                                88H
                                                                   RX DATA REGISTER
00CE
                      124 MDE51 EQU
                                               OCEH
                                                                   MODE 16X, 2 STOP, NO PARITY
                      125 CMD51 EQU 27H
                                                                ; COMMAND, ENABLE TX&RX
0027
0002
                      126 RDY
                                     EQU 02H
                                                                   RXRDY BIT
                      127 ;
                      128 ; MONITOR SUBROUTINE EQUATES
                      129 Fines T 11239 THUSSING XT
                      130 GETCH EQU 061FH
BE1F
                                                                    GET CHR FROM KEYBOARD, ASCII IN CH
05F8
                      131 ECHO EQU 05F8H
                                                                   ; ECHO CHR TO DISPLAY
075E
                      132 VALDG EQU 075EH
                                                                   ; CHECK IF VALID DIGIT, CARRY SET IF VALID
05BB
               133 CNVBN EQU 05BBH
                                                                   CONVERTS ASCII TO HEX
05EB
               134 CRLF EQU 05EBH
                                                                   DISPLAY CR, HENCE LF TOO
96C7
                       135 NMOUT EQU 06C7H
                                                                   CONVERT BYTE TO 2 ASCII CHR AND DISPLAY
                       136 A SER HAVE THESE THE NEED
                      137 ; MISC EQUATES
                      138 ;
2000
                      139 STKSRT EQU
                                               PACAH
                                                                   STACK START
                      140 CNTLC EQU 03H
0003
                                                                   ; CNTL-C EQUIVALENT
8000
                      141 MONTOR EQU 0008H
                                                                   ; MONITOR OF THE SECOND SE
2000
                      142 CMDBUF EQU 2000H
                                                                   START OF COMMAND BUFFER
                                                                   POLL MODE SPECIAL TX COMMAND BUFFER
                      143 CMDBF1 EQU 2020H
2020
0000
                      144 CR EQU ODH
                                                                   JASCII CR USB SSOC 38
AAAA
                      145 LF EQU OAH
                                                                   ASCII LE
2004
                      146 RST75 EQU 2004H
                                                                   RST7. 5 JUMP ADDRESS
20CE
                      147 RST65 EQU 20CEH
                                                                   RST6. 5 JUMP ADDRESS
                      148 LDADR EQU 2010H
2010
                                                                   RESULT BUFFER LOAD POINTER STORAGE
                      149 CNADR EQU
                                                2013H
2013
                                                                   RESULT BUFFER CONSOLE POINTER STORAGE
                      150 RESBUF EQU 2800H
                                                          RESULT BUFFER START - 255 BYTES
2800
0093
                      151 SNRMP EQU 93H
                                                           SNRM-P CONTROL CODE
                      152 RR0P EQU 11H
0011
                                                              ; RR(0)-P CONTROL CODE
                      153 NSAF
                                    EQU
                                            73H
0073
                                                              ; NSA-F CONTROL CODE
                                                              ; RR(0)-F CONTROL CODE
0011
                      154 RR0F
                                   EQU
                                             11H
2015
                      155 PRMPT EQU
                                            2015H
                                                              PRMPT STORAGE
2016
                      156 POLIN EQU 2016H
                                                              ; POLL MODE SELECTION INDICATOR
                      157 DEMODE EQU 2027H ; DEMO MODE INDICATOR
2027
                       163;
                       164 ; RAM STORAGE DEFINITIONS:
                       165 ; LOC DEF
                      166; 9377777 908 00777
                       167 ; 2000-200F COMMAND BUFFER (1997)
                       168; 2010-2011 RESULT BUFFER LOAD POINTER
                       169; 2013-2014 RESULT BUFFER CONSOLE POINTER
                                      2015 PROMPT CHARACTER STORAGE
                       171; 2016 POLL MODE INDICATOR
                       172; 2017 BAUD RATE LSB FOR SELF-TEST
              173; 2018 BAUD RATE MSB FOR SELF-TEST
           177 ; 2019 SPARE
179 ; 2020-2026 RESPONSE COMMAND BUFFER FOR POLL MODE
             180 ; 2800-28FF RESULT BUFFER HIS DOT THE
            PARENO V.181 ; SOOM ONE TRANS INCREST. HERMAN HOS STOT ARE
                      182 ; we determine the contract cont
```

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	183 ; 184 ; PR0	GRAM START		
		BRILO TEE		
				AND RESET 8273.
				RINT SIGNON MESSAGE 20093400 300
	188 ;	PROD T30:		
9800		ORG ORG		
	190	090 J T30 ;	9,090	
0800 310020	191 STAF	ET IXI	SP, STKSRT	; INITIALIZE SP 28 08 898
0803 3E36	1924 21	MVT	A. MDCNTA	; 8253 MODE SET 35
0805 DZ98	193	OUT	MODE53	; 8253 MODE PORT 8
0807 3A1720	194	100	I KRP4	GET 8273 BAUD RATE LSB
080A D39C TI TB				
				GET 8273 BUAD RATE MSB
080F D39C				COUNTER 0 Sas Sa Sa Sa
0811 CD1A0B				; INITIALIZE 8257 RX DMA CHANNEL
0814 CD300B	199	CHLL	1 AUTH	; INITIALIZE 8257 TX DMA CHANNEL ; OUTPUT 1 FOLLOWED BY A 0
0817 SE01	200	MAI	H, 01H	OUTPUT 1 FULLUMED BY H U
0819 D392		OUT	TEST73	
081B 3E00	202	MVI	H, 00H	; TO RESET THE 8273
081D D392				
081F 3E2D	204	MVI	A, '-'	NORMAL MODE PROMPT CHR
0821 321520	205	STA	PRMP1	PUT IN STURHUE
0824 3E00	206	MVI	A, 00H	; TX POLL RESPONSE INDICATOR
0826 321620	207	STA	POLIN	; 0 MEANS NO SPECIAL TX 55 888 ; CLEAR DEMO MODE 5888
0829 322720	208	STA	DEMODE	; CLEAR DEMO MODE
082C 21A30C	212	SPORLXI	H, SIGNON	; SIGNON MESSAGE ADR
082F CD920C	213	CALL		DISPLAY SIGNON S 8839 883
	214;			
	215 ; MON	ITOR USES 3	TUMPS IN RAM TO	DIRECT INTERRUPTS STAURANT TO SEE FEEL SEE SEE SEE SEE SEE SEE SEE SEE SEE
	216;			
0832 21D420			H, RST75	RST7. 5 JUMP LOCATION USED BY MONI
0835 01000C	218			
0835 01000C 0838 36C3	219	MVI	M. AC3H	; LOAD 'JMP' OPCODE 1437 809
0020 02	229		H WHOS	
// M/SIN			M, C	
983A 23 983R 71				LOIN KAI LOD
083B 71	221		u siner	- INC DOINTED THE PRICE TO
083B 71 083C 23	221	INX	H 30040	
083B 71 083C 23	221	INX	H M. B	; INC POINTER  ; LOAD RXI MSB
083B 71 083C 23 083D 70 083E 21CE20	221 30 222 223 224 140	MOV LXI	M. B H. RST65	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI
083B 71 083C 23 083D 70 083E 21CE20 0841 01CE0C	221 222 223 224 140 225	INX MOV LXI	M, B H, RST65 B, TXI	;LOAD RXI MSB ;RST6.5 JUMP LOCATION USED BY MONI ;ADDRESS OF TX INT ROUTINE
083B 71 083C 23 083D 70 083E 21CE20 0841 01CE0C	221 222 223 224 140 225	INX MOV LXI	M, B H, RST65 B, TXI	;LOAD RXI MSB ;RST6.5 JUMP LOCATION USED BY MONI ;ADDRESS OF TX INT ROUTINE
0838 71 083C 23 083D 70 083E 21CE20 0841 01CE0C 0844 36C3	221 222 223 224 MO 225 226 227	INX MOV LXI LXI MVI MVI JINX	M. B H. RST65 B. TXI M. 0C3H H	;LOAD RXI MSB ;RST6.5 JUMP LOCATION USED BY MONI ;ADDRESS OF TX INT ROUTINE ;LOAD 'JMP' OPCODE ;INC POINTER
0838 71 083C 23 083D 70 083E 21CE20 0841 01CE0C 0844 36C3	221 222 223 224 MO 225 226 227	INX MOV LXI LXI MVI MVI MVI MX	M. B H. RST65 B. TXI M. 0C3H H	;LOAD RXI MSB ;RST6.5 JUMP LOCATION USED BY MONI ;ADDRESS OF TX INT ROUTINE ;LOAD 'JMP' OPCODE ;INC POINTER
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71	221 222 223 224 140 225 226 227 228 229 140	INX MOV LXI LXI MVI INX MOV INX	M. B H. RST65 B. TXI M. 0C3H H M. C H	;LOAD RXI MSB ;RST6.5 JUMP LOCATION USED BY MONI ;ADDRESS OF TX INT ROUTINE ;LOAD 'JMP' OPCODE ;INC POINTER ;LOAD TXI LSB ;INC POINTER
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23	221 222 223 224 THO 225 226 227 228 229 SH3 230	INX MOV INX MOV INX MOV MOV	M. B H. RST65 B. TXI M. 0C3H H M. C H	;LOAD RXI MSB ;RST6.5 JUMP LOCATION USED BY MONI ;ADDRESS OF TX INT ROUTINE ;LOAD 'JMP' OPCODE ;INC POINTER ;LOAD TXI LSB ;INC POINTER ;LOAD TXI MSB
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23 9849 70 9848 3E18	221 222 223 224 140 225 226 227 228 229 230 231	XAI WOM COME IX I I I I I I I I I I I I I I I I I I	M. B H. RST65 B. TXI M. 0C3H H M. C H M. B B. 18H	;LOAD RXI MSB ;RST6.5 JUMP LOCATION USED BY MONI ;ADDRESS OF TX INT ROUTINE ;LOAD 'JMP' OPCODE ;INC POINTER ;LOAD TXI LSB ;INC POINTER ;LOAD TXI MSB ;GET SET TO RESET INTERRUPTS
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23 9849 70 9848 3E18 984C 30	221 222 223 224 225 226 227 228 229 230 231	INX MOV INX MOV INX MOV INX MOV INX MOV SIM	M. B H. RST65 B. TXI M. 9C3H H M. C H M. B R. 18H	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD 'JMP' OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23 9849 70 9848 3E18	221 222 223 224 140 225 226 227 228 229 230 231	INX MOV LXI LXI LXI MVI INX MOV INX MOV INX MOV INX INVI INVI INVI INVI INVI INVI INVI	M. B H. RST65 B. TXI M. 0C3H H M. C H M. B A. 18H	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD 'JMP' OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23 9849 70 9848 3E18 984C 30	221 222 223 224 140 225 226 227 228 229 230 231 232 233 234;	INX MOV LXI LXI MVI INX MOV INX MOV INX MOV INX	M. B H. RST65 B. TXI M. 0C3H H M. C H M. B A. 18H	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD 'JMP' OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23 9849 70 9848 3E18 984C 30	221 222 223 224 140 225 226 227 228 229 230 231 232 233 234;	INX MOV LXI LXI MVI INX MOV INX MOV INX MOV INX	M. B H. RST65 B. TXI M. 0C3H H M. C H M. B A. 18H	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD 'JMP' OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23 9849 70 9848 3E18 984C 30	221 222 223 224 140 225 226 227 228 229 230 231 232 233 234;	INX MOV LXI LXI MVI INX MOV INX MOV INX MOV INX	M. B H. RST65 B. TXI M. 0C3H H M. C H M. B A. 18H	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD 'JMP' OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23 9849 70 9848 3E18 984C 30	221 222 223 224 225 226 227 228 229 230 231 232 233 234; 235; INI 236;	INX MOV LXI LXI MVI INX MOV INX MOV SIM EI ITIALIZE BUF	M. B H. RST65 B. TXI M. 0C3H H M. C H M. B A. 18H	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD 'JMP' OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS
9838 71 983C 23 983D 70 983E 21CE20 9841 01CE0C 9844 36C3 9846 23 9847 71 9848 23 9849 70 9848 3E18 984C 30	221 222 223 224 225 226 227 228 229 230 231 232 233 234; 235; INI 236;	INX MOY LXI LXI LXI MYI INX MOY INX MOY SIM EI ITIALIZE BUF	M. B H. RST65 B. TXI M. 0C3H H M. C H M. B A. 18H	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD 'JMP' OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS
983B 71 983C 23 983D 70 983E 21CE20 984H 91CE0C 9844 36C3 9846 23 9847 71 9848 23 9848 23 9849 70 9848 3E18 9840 FB	221 222 223 224 H/O 225 226 227 228 229 H/O 231 232 233 234 ; 235 ; INI 236 ; 237 ;	INX MOV LXI LXI LXI MVI INX MOV INX MOV SIM EI  CTIALIZE BUF	M. B H. RST65 B. TXI M. 0C3H H. C H M. C H M. B A. 18H  FER POINTER	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD 'JMP' OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS ; SET RESULT BUFFER POINTERS
983B 71 983C 23 983D 70 983E 21CE20 984H 91CE0C 984H 36C3 9846 23 9847 71 9848 23 9849 70 9848 23 9849 FB	221 222 223 224 H0 225 226 227 228 229 H0 231 232 233 234; 235; INI 236; 237; 238 239	INX MOV LXI LXI MVI INX MOV INX MOV MVI SIM EI  CTIALIZE BUF	M. B H. RST65 B. TXI M. 0C3H H. C H. M. C H. M. B A. 18H  FFER POINTER  H. RESBUF CNADR	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD / JMP/ OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS ; SET RESULT BUFFER POINTERS ; RESULT CONSOLE POINTER
983B 71 983C 23 983D 70 983E 21CE20 984H 91CE0C 984H 36C3 9846 23 9847 71 9848 23 9849 70 9848 23 9849 FB	221 222 223 224 140 225 226 227 228 229 230 231 232 233 234 ; 235 ; INI 236 ; 237 ; 238 239 240	INX MOY LXI LXI MYI INX MOY INX MOY MYI SIM EI  CTIALIZE BUF LXI SHLD SHLD	M. B H. RST65 B. TXI M. 0C3H H. C H. M. C H. M. B A. 18H  FFER POINTER  H. RESBUF CNADR	; LOAD RXI MSB ; RST6. 5 JUMP LOCATION USED BY MONI ; ADDRESS OF TX INT ROUTINE ; LOAD /JMP/ OPCODE ; INC POINTER ; LOAD TXI LSB ; INC POINTER ; LOAD TXI MSB ; GET SET TO RESET INTERRUPTS ; RESET INTERRUPTS ; ENABLE INTERRUPTS ; SET RESULT BUFFER POINTERS ; RESULT CONSOLE POINTER ; RESULT LOAD POINTER

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	244 ;			
9057 CDED95		OII CDIE		
0050 704520	245 CHDREC. CI	NO DOMOT	; DISPLAY CR ; GET CURRENT PROMPT CHR ; MOVE TO C ; DISPLAY IT ; GET CONSOLE POINTER ; SAVE POINTER LSB ; GET LOAD POINTER ; SAME LSB? ; NO, RESULTS NEED DISPLAYING	
002U 7UT350	240 Li	OH CO	HOUE TO C	
953U 4F	247	UV C/H	FROME TO C	
083E CDF803	248 U	HLL EUHU	DISPLHY II	
0861 2H1320	249 LUUPII: L	HLD CNHDR	GET CONSULE PUINTER	
0864 7D	250 M	OV A, L	; SAVE POINTER LSB	
0865 2A1020	251 L	HLD LDADR	GET LOAD POINTER	
0868 BD	252 C	MP L TREATS R	SAME LSB?	
0869 C2390A	253 J	NZ DISPY	; NO, RESULTS NEED DISPLAYING	
000C DD03	200	BIO SINIOT	TEST CHECK KETDURKU	
086E E602	260 A	NI RDY	; CHR RECEIVED?	
0870 C27D08	261 J	NZ GETCMD	; CHR RECEIVED? ; MUST BE CHR SO GO GET IT	
0873 3A1620	262 L	DA POLIN	GET POLL MODE STATUS	
0876 A7	263 8	NA A CENTRAL	: IS IT 02	
9877 C24C99	264 I	NZ TYPOI	; IS IT 0? ; NO, THEN POLL OCCURRED	
9979 C76199	265	MP LOODIT	; YES, TRY AGAIN	
00111 020100	266	EDOFTI PRIGAT	TIEST INT BUILTI	
	200			
	267 )	DECONUTED DOUTING	; GET CHR ; ECHO IT ; SETUP FOR COMPARE ; R? ; GET MORE ; S? ; GET MORE	
	268 ; CUMMHND	RECOGNIZER ROUTINE		
	269 ;			
	270 ;			
087D CD1F06	271 GETCMD: C	ALL GETCH	GET CHR	
0880 CDF805	272 C	ALL ECHO	; ECHO IT 309	
0883 79	273 M	OV A.C	SETUP FOR COMPARE OSBES	826
0884 FE52	274 C	PI 'R' 300/31	7 R? 288 885 85 555	
0886 CAAF08	275 J	Z ROWN	GET MORE SES SESSES	
0889 FE53	276 C	PI 'S'	;5?*** \$1\$ 000e00	
088B CAD708	277 J	Z SDWN	GET MORE	
088E FE47	278 C	PI de 'G'	GET MORE  GR  GET MORE  TP  GET MORE  AP  GET MORE  AP  GET MORE  ZP  GE	
0890 CAFFOR	279 I	7 GOLIN	: GET MOPE	
0090 CHI 1 00	200 0	DI /T/	. T2	
9005 COGERO	200 C	700 TOUR THE	CET MODE	
0000 FF44	201	DT (O/	OCH PORE DES DOSCES	
0000 C00000	202	TI T	OFT HODE	
000h CH2209	283 A 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	Z HUMN	JUET PIURE	
0890 FESH	284 Bell 189 U	MID: 'Z' DA	129.04 155 11.11	
089F CH3109	285 SETHIOSI	Z CMODE	; YES, GO CHANGE MODE	
08R2 FE03	290	PI CNTLC	; CNTL-C?	
08A4 CA0800	291 J	Z MONTOR	; EXIT TO MONITOR 053335	
08R7 0E3F	292 ILLEG: M	VI C. '?' INT.	; PRINT ? 355 083318	
08A9 CDF805	293 0	ALL ECHO	; DISPLAY IT	
08AC C35708	294 J	MP CMDREC	; DISPLAY IT ; LOOP FOR COMMAND ; GET NEXT CHR ; ECHO IT	
	295 E IXT 0			
08AF CD1F06	296 RDWN: C	ALL GETCH	GET NEXT CHR	
0882 CDF805	297	ALL ECHO 9 M	; ECHO IT	
08R5 79	298 M	nv a.c	SETUP FOR COMPARE	
08B6 FE4F	299 C	PI '0'	; 0?	
08B8 CA5D09	300 J			
08BB FE53		PI 'S'		
08BD CA6709			; 5?	
	302 J.		A SECTION OF SECTION O	
08C0 FE44		PI 'D'	; D? : 325	
08C2 CA7109	304 J		; RD COMMAND	
08C5 FE50		PI 'P' TURESTA H		
08C7 CAD809	306 J	Z RPCMD	; RP COMMAND	
08CA FE52	307 C	PI 'R'	;R? 42 858 858 153	
08CC CA0008	308 J	Z START	START OVER	
08CF FE42	309 CI	PI - 'B'	J B? OF MIRE SAS	
08D1 CA7B09	310 J		; RB COMMAND	

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USUY CUIFUS SIS SUNN: CAEC"
                                  "GEICH" ; GEI NEXI CHK
                                   ECH0
            314 CALL
                                               ECHO IT
08DA CDF805
9800 78 315 MOV
                                   A, B
                                               SETUP FOR COMPARE
                                               ;0?
08DE FE4F 316 CPI
                                   '0'
08E0 CAA609
                317 JZ
                                   SOCMD
                                                 SO COMMAND
                318 CPI
                                   151
08E3 FE53
                                                15?
08E5 CAB009
                319 JZ
                                   SSCMD
                                                 ; SS COMMAND
                                   'R'
                                                 ; R?
08E8 FE52
                320
                           CPI
08EA CABA09
                321
                           JZ
                                   SRCMD
                                                 ; SR COMMAND
08ED FE50
                722
                           CPI
                                   /P/
                                                  ; P?
                323
                           JZ -
                                   SPCMD
                                                  ; SP COMMAND
08EF CAE209
08F2 FE42
                324
                           CPI
                                   'B'
                                                  ; B?
08F4 CA8509
                325
                           JZ
                                   SBCMD
                                                  ; SB COMMAND
                326
                           CPI
                                   1/
                                                  ;L?
08F7 FE4C
08F9 CA8F09
                327
                           JZ
                                   SLCMD
                                                  ; SL COMMAND
08FC C3A708
                328
                            IMP
                                   ILLEG
                                                  ; ILLEGAL, TRY AGAIN
                329
08FF CD1F06
                330 GDWN
                           CALL
                                   GETCH
                                                  GET NEXT CHR
                                   ECH0
                                                  ECHO IT
0902 CDF805
                331
                           CALL
0905 78
                332
                           MOV
                                   A, B
                                                  SETUP FOR COMPARE
                                   'R'
                                                  ; R?
0906 FE52
                333
                           CPI
0908 CAC409
                334
                            JZ
                                   GRCMD
                                                  GR COMMAND
                335
                            JMP
090B C3A708
                                   ILLEG
                                                  ; ILLEGAL, TRY AGAIN
                336
090E CD1F06
                337 TDWN:
                           CALL
                                   GETCH
                                                  GET NEXT CHR
                338
                           CALL
                                   ECHO
0911 CDF805
                                                  ECHO IT
0914 78
                339
                           MOY
                                   A, B
                                                  ; SETUP FOR COMPARE
                                   F'
0915 FE46
                           CPI
                                                  ; F?
                349
                                                 ; TF COMMAND
0917 CAEC09
                341
                           JZ
                                   TECMD
                                   T, 1100 19
091A FE4C
                342
                           CPI
                                                  ; L?
091C CA9909
                343
                           JZ
                                   TLCMD
                                                  TL COMMAND
091F C3A708
                344
                                   ILLEG
                                                  ; ILLEGAL, TRY AGAIN
                345
0922 CD1F06
                346 ADWN:
                           CALL
                                   GETCH
                                                  GET NEXT CHR
                                   ECHO
0925 CDF805
                347
                           CALL
                                                  ; ECHO IT
0928 78
                348
                           YOM
                                   A, B
                                                  ; SETUP FOR COMPARE
                349
                                   F' HER O
0929 FE46
                           CPI
                                                  ; F?
                350
                           JZ
                                   AFCMD
092B CACE09
                                                  ; AF COMMAND
092E C3A708
                351
                                   ILLEG
                                                  ; ILLEGAL, TRY AGAIN
                353 ; RESET POLL MODE RESPONSE - CHANGE PROMPT CHR AS INDICATOR
                354;
0931 F3
                355 CMODE:
                          DI
                                                  DISABLE INTERRUPTS
0932 3R1520
                356
                           LDA
                                   PRMPT
                                                  GET CURRENT PROMPT
                                   1_20MB.O
0935 FE2D
                357
                           CPI
                                                  ; NORMAL MODE?
                                   SW
0937 C24309
                358
                            JNZ
                                                  ; NO, CHANGE IT
                                   A, '+'
093A 3E2B
                359
                           MYI
                                                  ; NEW PROMPT
093C 321520
                360
                           STA
                                                  STORE NEW PROMPT
                365
093F FB
                            EI
                                                  ENABLE INTERRUPTS
0940 C35708
                366
                            JMP
                                   CMDREC
                                                  RETURN TO LOOP
                                   A '-'
0943 3E2D
                367 SW.
                           MYI
                                                  ; NEW PROMPT CHR
0945 321520
                368
                           STA
                                   PRMPT
                                                  STORE IT
0948 FB
                369
                           EI
                                                  ENABLE INTERRUPTS
0949 C35708
                370
                            JMP
                                   CMDREC
                                                  RETURN TO LOOP
                371;
                372;
```

```
373 ; TRANSMIT ANSWER TO POLL SETUP
               374;
               382 TXPOL: MVI
094C REDO
                                A, 00H
                                          CLEAR POLL INDICATOR
094E 321620
               384 T G STA
                                POLIN
                                          INDICATOR ADR
                                H, LOOPIT
0951 216108
               385 LXI
                                           SETUP STACK FOR COMMAND OUTPUT
                  PUSH
0954 E5
               386
                               H
                                           PUT RETURN TO CMDREC ON STACK
                                           GET # OF PARAMETERS READY
0955 0604
               387 MVI
                                B. 04H
0957 212020
               388
                  CO LXI
                                H. CMDBF1
                                           POINT TO SPECIAL BUFFER
                                COMM2
095A C3FF0A
               389 JMP
                                           JUMP TO COMMAND OUTPUTER
               390 ;
               391 jenn 92:
               392;
                                                              600D FE50
               393 COMMAND IMPLEMENTING ROUTINES
               394 ;
               396 ; RO - RESET OPERATING MODE
               397 i
095D 0601
                                B. 01H
                                           # OF PARAMETERS
               398 ROCMD: MYI
095F 0E51
               399
                         MYI
                                C, 51H
                                             COMMAND
                  THEM THE CALL
                               COMM
                                           GET PARAMETERS AND ISSUE COMMAND
0961 CDE50A
               400
               401 JMP
                                CMDREC
                                           GET NEXT COMMAND
0964 C35708
               402 ;
               403 ; RS - RESET SERIAL I/O MODE COMMAND
               494 ;
                                B, 01H
                                            # OF PARAMETERS
               405 RSCMD: MVI
0967 0601
0969 0E60
               496
                         MVI
                                C. 60H
                                             COMMAND
                                COMM
               497 ____ CALL
                                            GET PARAMETERS AND ISSUE COMMAND
096B CDE50A
               408 JMP
                                           GET NEXT COMMAND
096E C35708
                                CMDREC
               409 ;
               410 ; RD - RECEIVER DISABLE COMMAND
               411 ;
                                            # OF PARAMETERS
0971 0600
               412 RDCMD:
                         MVI
                                B, 00H
               413
0973 0EC5
                         MVI
                                C. 0C5H
                                             COMMAND
               414 CALL
415 JMP
                                COMM
                                            ; ISSUE COMMAND
0975 CDE50A
0978 C35708
                                CMDREC
                                             GET NEXT COMMAND
               416 ;
417 ; RB - RESET ONE BIT DELAY COMMAND
               418 ;
                                                               8928 78
                                B, 01H
                                            # OF PARAMETERS
097B 0601
               419 RBCMD:
                        MVI
                                C, 64H
               420
097D 0E64
                         MYI
                                             COMMAND
               421
                                            GET PARAMETER AND ISSUE COMMAND
097F CDE50A
                         CALL
                                COMM
0982 C35708
               422
                         JMP
                                CMDREC
                                             GET NEXT COMMAND
               423 ;
               424 ; SB - SET ONE BIT DELRY COMMAND
               425 ;
                                              # OF PARAMETERS
0985 0601
               426 SBCMD:
                         MYI
                                B. 01H
0987 0EA4
               427
                         MYI
                                C, 084H
                                              ; COMMAND
0989 CDE50A
               428
                         CALL
                                COMM
                                             GET PARAMETER AND ISSUE COMMAND
                                           GET NEXT COMMAND
098C C35708
               429
                                CMDREC
               430 ;
               431 ; SL - SELECTIVE LOOP RECEIVE COMMAND
               432 ;
098F 0604
               433 SLCMD:
                                B, 04H
                                              # OF PARAMETERES
               434
0991 0EC2
                         MYI
                                C. 0C2H
                                              ; COMMAND
                         CALL
0993 CDE50A
               435
                                COMM
                                              GET PARAMETERS AND ISSUE COMMAND
0996 C35708
               437 ; 100,730
               436
                                CMDREC
                                              GET NEXT COMMAND
               438 ; TL - TRANSMIT LOOP COMMAND
```

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		439 ;		H, CMDBUF			
0999	210020	440 TLCMD	: LXI	H, CMDBUF	SET COMM	AND BUFFER	POINTER
099C	0602	441	MVI	B, 02H	; LOAD PAR	AMETER COU	NTER 199
099E	36CA	442	MVI	M, OCAH	:LOAD COM	MAND INTO I	BUFFER
09A0	210220	443	LXI	H, CNDBUF+2 TFCMD1	POINT AT	ADR AND C	NTL POSITIONS
09A3	C3F609	444	JMP	TFCMD1	FINISH 0	FF COMMAND	IN TE ROUTINE
	9377						
		446 ; 50 -	SET OPE	RATING MODE COMMA	ND		
		447 ;		83.111 B, 91H H C, 91H S			
09A6	0601	448 SOCMD	: MVI	B. 01H	# OF PAR	AMETERS	
09A8	0E91	449	MYI	C, 91H	; COMMAND		
09AH	CDE50H	450	CALL	COMM	GET PARA	METER AND	ISSUE COMMAND
09AD	C35708	451	JMP	CMDREC LONGET	GET NEXT	COMMAND	
		4E2 .					
		453 ; 55 -	SET SER	IAL I/O COMMAND			
		454					
09B0	0601	455 SSCMD	MVI	B. 01H	# OF PAR	AMETERS	
99B2	0EA0	456	MVI	B, 01H C, 0A0H	COMMAND	514	
29R4	CDF588	457	CALL	COMM	GET PAPA	METER AND	TSSUE COMMAND
99B7	C35708	458	IMP	CMDREC.	GET NEXT	COMMAND	PM 22
		459 :	THE BUT	A	Sun	547	
		469 : SR -	SELECTI	CMDREC  VE RECEIVE COMMAN	0 9/9		
		461 :	CAST CAST :	TE TEOLITE OUT THE	1247	218	
agra.	9694	462 SPCMD	. MUT	В, 04Н	# OF PAP	AMETERS	
ager	BEC4 CON	467	MUT	C, 0C1H	· COMMOND	THILLIENS	
2005	CDCEGO	ACA TO	COLL	COMM	CET DODG	METERC ON	TECHE COMMOND
3964	C75708	465	TMP	CMUDEC	GET NEVT	COMMOND	1550E CONTINUE
2201	030100	A66 :	mora i ii	CHEREC	JUET HEAT	COLUMNIA	
		467 : GP -	GENERAL	COMPICATION COMPINED  B. 92H C. 9C9H COMM CMDREC	900 10		
		469	GLITERIE	RECEITE COMMIND			
904	9692	469 GPCMD	MUT	p gou	NO DODOM	ETEDE	
3004	OCO2	470	MUI	C GCGH	· COMMOND	LIEKS	
9900	CDE500	474	COLL	COMM	· TCCHE CO	MMOUD	
ane	C75700	472	TMD	CMDDEC	GET NEVT	CUMMOND	
3200	C201.00	472	JIII	CHUREC	JUE! NEA!	COMPINIO	1000 CT 1000
		474 : OF -	OPODT E	RAME COMMAND 8  B, 00H C, 0CCH			
		477 JIII	HOUR!	KINIE COMMINIO			
agre	9599	A7C DECMD	MUT	D GOU	NO DODOM	ETEDO	
3000	9000	470 NFUND	MUT	C GCCH	ODMINION IN	LIEKS	
משכנ	CDEECO	477	LIAT	COMM	COMPIND	MACAIR	
300E	CZEZGO	470	TMD	CMUDEC	ISSUE CUI	COMMOND	
בעכם	C231.00	480 ;	Jrw	CMDREC	JUET NEXT	CUMPINIO	
			DECET D	ORT COMMAND	ora no manua		
2000	0.004	482 ;	MILE	B, 01H	A OF BOD	OMETER !	
	0E63	484	MVI		; COMMAND	1 245	
		485					SSUE COMMAND
99UF	C35708	486			GET NEXT		
		487 ;					
		488 ; SP -			YSK		
		489 ;			Diff		
		490 SPCMD			# OF PAR		
				C, OR3H	; COMMAND		
	CDE50A	492					SSUE COMMAND
9E9	C35708	493			GET NEX		
		494 ;					
				T FRAME COMMAND			
		496 ;		. 100904			

09EC 210020	497 TFCMD: LXI	H, CMDBUF	; SET COMMAND BUFFER POINTER
09EF 0602	498 MVI	B, 02H	; LOAD PARAMETER COUNTER
09F1 36C8	499 MVI	M, 0C8H	; LOAD COMMAND INTO BUFFER SHOW DAYS
09F3 210220	500 LXI	H, CMDBUF+2	POINT AT ADR AND CNTL POSITIONS
09F6 78	501 TFCMD1: MOV	A, B	TEST PARAMETER COUNT MISSING MARKET
09F7 R7	502 ANA	A MARCHE	315 ET 0? 444 6837ED 5968
09F8 CA070A	503 JZ	TBUFL	: YES, LOAD TX DATA BUFFER
09FB CDADOA	504 CALL	PARIN	GET PARAMETER
09FE D00708	595 JC	TILEG	GET PARAMETER  JILLEGAL CHR RETURNED  JINC COMMAND BUFFER POINTER
0001 23	506 INX	H 1/16.5	: INC COMMAND RHEFER POINTER
0002 05	597 DCP	B 819.1	; DEC PARAMETER COUNTER
9993 77	500 MOV	M. A. IRING	; LOAD PARAMETER INTO COMMAND BUFFER
			GET NEXT PARAMETER 665223 0978
	519		
0A07 210080	511 TBUFL: LXI	H, TXBUF	LOAD TX DATA BUFFER POINTER
0A0A 010000	512 LXI	в, 0000Н	; CLEAR BC - BYTE COUNTER
0A0D C5	513 TBUFL1: PUSH	B H19.8	; SAVE BYTE COUNTER 1888 9909 ; GET DATA, ALIAS PARAMETER 1889 9909
0A0E CDADOA	514 CALL	PARIN HOSE	GET DATA, ALIAS PARAMETER
0A11 DA1B0A	515 JC	ENDCHK	; MAYBE END IF ILLEGAL MODESCO MODE
0A14 77	516 MOV	M. A. GREGO	; LOAD DATA BYTE INTO BUFFER 3 5888
9045 22	E47 THU	ti .	. THE DUFFED DOTHITED
0816 C1	518 POP	CORMON SUTSTAN	RESTORE BYTE COUNTER
9917 93	519 TNX	B	RESTORE BYTE COUNTER  INC BYTE COUNTER
0018 C30000	520 JMP	TRUE 1 1 115 G	GET NEXT DATA
0A1B FE0D	521 FNDCHK - CPT	CD HAND O	RETURNED ILLEGAL CHR CR?
			; YES, THEN TX BUFFER FULL
9929 64	522 000	D TOURTL	DECTOR D TO COUR CTOCK
9024 C20700	524 TMD	THE	; RESTORE B TO SAVE STACK
9A24 C1	505 TOUCEL - DOD	P	RESTORE BYTE COUNTER
0025 240420	525 IDUFFE. FUF	II CMDDISE*4	DOINT INTO COMMOND DUCCED
9020 74	J20 LA1	M C	; POINT INTO COMMAND BUFFER ; STORE BYTE COUNT LSB
9020 71	327 MUY	not was a	STURE BYTE COUNT LSB
0020 70	528 INX	H HEUS J	; INC POINTER ; STORE BYTE COUNT MSB ; LOAD PARAMETER COUNT INTO B
002D 0004	529 MUY	IL B MAUS	STUKE BYTE COUNT FISH THESE
002D 243C00	534 MVI	B) 04H	LUMD PHRHMETER COUNT INTO B
0A2D 21360A 0A30 C5	231 FXI	H, TFRET	GET RETURN ADR FOR THIS ROUTINE
0H30 C3	532 PUSH	B - 09/19/03 34	PUSH ONCE
0H31 E3	533 XTHL		; PUT RETURN ON STACK ; PUSH IT SO CMDOUT CAN USE IT ; ISSUE COMMAND
0H32 C5	534 PUSH	B H00 8	; PUSH IT SO CMDOUT CAN USE IT
OR33 C3FBOR	535 JMP	CMDOUT HOSE TO	; ISSUE COMMAND
0A36 C35708	536 TFRET: JMP	CMDREC	GET NEXT COMMAND ASSESSED SOME
	537 JOHN TANK	CHDREC	8905 C35786 479 FP
	538 ;		1 884
			RESULT BUFFER WHEN LOAD AND CONSOLE
	540 ; POINTERS ARE	DIFFERENT.	
	541 3 38888 9 90 0		ESSE BEEL 483 KICHD: MVI
	542 ; OSRIPSOD :		ENH 484 EASO AGES
0A39 1605	543 DISPY: MYI	D, 05H	; D IS RESULT COUNTER
0A3B 2A1320	544 LHLD	CNADR	GET CONSOLE POINTER
OA3E E5	545 PUSH		; SAVE IT
0A3F 7E	546 MOV	A.M. Australia	GET RESULT IC
0A40 É61F	547 ANI	1FH	; LIMIT TO RESULT CODE
0A42 FE0C	548 CPI		; TEST IF RX OR TX SOURCE
0844 DR6208	549 JC		; CARRY, THEN RX SOURCE
	550 TXSORC: LXI		TX INT MESSAGE
0A4A CD920C		TUNCO	
984D E1	552 DISPY2: POP	H	; DISPLRY IT ; RESTORE CONSOLE POINTER
OR4E 7E			GET RESULT
ORAF CDC706	553 DISPY1: MOV 554 CALL	NMOUT	
CIPI COCTEO	UTLL	NMOUT	; CONVERT AND DISPLAY

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```
557 INR
                            L H19 .0
                                      I'M; INC BUFFER POINTER 1991 3999
0A57 2C
                                      DEC RESULT COUNTER
0A58 15
             558 DCR
                             D HJ
                                      NOT DONE
             559 JNZ
0A59 C24E0A
                             DISPY1
             560 SHLD
                             CNADR
                                      UPDATE CONSOLE POINTER
0A5C 221320
                   JMP
                                       RETURN TO LOOP
0A5F C35708
             561
                             CMDREC
     MIADR YRT 5621, II ON
      931399089563 $40 T30 t
             564 RECEIVER SOURCE - DISPLAY
                                     RESULTS AND RECEYIE BUFFER CONTENTS
        9HD 01565 9 11 21
            566
                                      RX INT MESSAGE ADR
0A62 21B80C 567 RXSORC: LXI
                             H, RXIMSG
             568 CALL
                                       DISPLAY MESSAGE
                             TYMSG
0A65 CD920C
                             H GA
          569 POP
                                       RESTORE CONSOLE POINTER
0A68 E1
                             A.M
0A69 7E
             570 RXS1: MOV
                                       RETRIEVE RESULT FROM BUFFER
                                         CONVERT AND DISPLAY IT
0A6A CDC706 571 CALL
                             NMOUT
          572 MVI
                             C. / / 9
                                       ASCII SP
0A6D 0E20
             573 CALL
                             ECHO R
                                       DISPLAY IT
0A6F CDF805
                             L 3.8
          574 INR
                                         ; INC CONSOLE POINTER
0873 15 209 575 DCR
                                         DEC RESULT COUNTER
                             D
                             A.D
                                         GET SET TO TEST COUNTER
0A74 7A
             576
                       MOV
                       CPI
                             94H
0A75 FE04
                                         ; IS THE RESULT RO?
0A77 CAA20A
             578
                       JZ
                             ROPT
                                         ; YES, GO SAVE IT
             579 CPI
                             03H
0A7A FE03
                                         ; IS THE RESULT R1?
                                         ; YES, GO SAVE IT
             580 JZ
                             R1PT
0A7C CAA70A
                                         ; TEST RESULT COUNTER
                             A 3.8
             581 RXS2: ANA
OA7F A7
             582 JNZ
0A80 C2690A
                             RXS1
                                         ; NOT DONE YET, GET NEXT RESULT
             583 SHLD
                             CNADR
0A83 221320
                                         ; DONE, SO UPDATE CONSOLE POINTER
             584 CBLL
0A86 CDEB05
                             CRLF
                                         ; DISPLAY CR
989 219982 585 IXI
                             H. RXRIJE
                                         POINT AT RX BUFFER
0A8C C1 586 POP
                                         RETRIEVE RECEIVED COUNT
                             В
             587 RXS3: MOY
                             A, B
0A8D 78
                                         ; IS COUNT 0?
088E B1
             588 ORA
                             C
0A8F CA5708
              589
                       JZ
                             CMDREC
                                         ; YES, GO BACK TO LOOP
0A92 7E
              590
                       MOY
                             A, M
                                         ; NO, GET CHR
                             B REFER B
0A93 C5
              591
                       PUSH
                                         SAVE BC
                                         CONVERT AND DISPLAY CHR
0A94 CDC706
              592
                       CALL
                             NMOUT
                 MVI MVI
0A97 0E20
             593
                             C. / / /
                                         ; ASCII SP
0A99 CDF805
              594
                       CALL
                             ECHO
                                         ; DISPLAY IT TO SEPARATE DATA
0A9C C1
                       POP
                                         ; RESTORE BC
0A9D 0B
              596
                       DCX
                                         DEC COUNT
                             B
889F 23
              597
                       INX
                             Н
                                         ; INC POINTER
0A9F C38D0A
                                         GET NEXT CHR
             599
                             H. CHORUF
                                                        BESS 21.6628
0002 4F
             600 ROPT: MOY
                             C, M
                                         GET RO FOR RESULT BUFFER
                            B 3.5
0AA3 C5
                                       SAVE IT
             601 PUSH
                             RXS2
             602 JMP
ORA4 C37FOR
                                         RETURN
             603 0 11 211
                             B TUDGED
                                         GET RO
9887 C1 604 R1PT: POP
                             B, M
            605 MOV
0AA8 46
                                         GET R1 FOR RESULT BUFFER
                             B
                                        SAVE IT
0009 C5 606 PUSH
0AAA C37F0A 607 JMP
                             RXS2
     608 ;
       609
        610 ;
          611 ; PARAMETER INPUT - PARAMETER RETURNED IN E REGISTER
    612 ;
```

	613 ; 307 30	NO THE PER ACRESSES
OAAD C5	614 PARIN: PUSH B	SAVE BC COUNTER SET CHR COUNTER
9AAE 1601	615 MVI D. 01	H SET CHR COUNTER
0AB0 CD1F06	616 CALL GETC	H g god; GET CHR and all all all
0AB3 CDF805	616 CALL GETC 617 CALL ECHO 618 MOV A, C	end set; ECHO IT eaz
0AB6 79	618 MOV A, C	PUT CHR IN A
0AB7 FE20	619 CPI ' 1	1910 911 ; SP? 198 805250 479
0AB9 C2E00A	620 JNZ PART	N1 : NO. ILLEGAL, TRY AGAIN
0ABC CD1F06	621 PARIN3: CALL GETC	H ; GET CHR OF PARAMETER
0ABF CDF805	622 CBLL ECHO	ECHO IT
0AC2 CD5E07	623 CALL VALD	G : IS IT A VALID CHR?
0AC5 D2E00A	624 JNC PARI	G ; IS IT A VALID CHR? N1 ; N0, TRY AGAIN
OAC8 CDBB05	625 CALL CNVB	N ; CONVERT IT TO HEX
	625 CALL CNYB 626 MOV C, A	SAVE IT IN C
99CC 79	627 MOV A, D	GET CHR COUNTER
	628 ANA A	GET CHR COUNTER
OUCD UL	629 JZ PARI	; IS IT 0? N2 ; YES, DONE WITH THIS PARAMETER
0AD1 15	630 DCR D	NE OUD COUNTED
OAD2 AF	630 DCR D	DEC CHR COUNTER
	631 XRA A	DESCRIPTION OF THE PROPERTY CONTROL OF THE PROPERTY CO
0AD3 79	632 MOV A.C	RECOVER 1ST CHR
0AD4 17	633 RAL	ROTATE LEFT 4 PLACES
0AD5 17	634 RAL	95'4 78 576 NOV 6.5 2075 FEBA 577 CP3 849
0AD6 17	635 RAL	97'A 7A 576 MOV 6.0 ANTO FEBA 577 CP3 BAGA
0AD7 17	636 RAL	
0AD8 5F	637 MOV E, A	SAVE IT IN E
0AD9 C3BC0A	638 JMP PARI	N3 GET NEXT CHR
0ADC 79	639 PARIN2: MOV A, C	; 2ND CHR IN A
OADD B3	640 UKH E	COURTUE BOTH CHK2
OADE C1	641 POP B	; RESTORE BC
OADF C9	642 RET	RETURN TO CALLING PROGRAM
0AE0 79	643 PARIN1: MOV A.C	; PUT ILLEGAL CHR IN A
0AE1 37	644 STC	; SET CARRY AS ILLEGAL STATUS
0AE2 C1	645 POP B	RESTORE BC
0RE3 C9	646 RET	RETURN TO CALLING PROGRAM
onn r c	647 ;	
	640	
	650 ; CHEST	MANY THOU GOS DOLLAND FOOT
0AE4 CF	651 BUFFUL: DB OCFH	FULL HAMP ES SENSE  LONG LINE EXIT TO MONITOR SCALE FOR
	652 ; , , , , , , , , , , , , , , , , , ,	AND THE PART OF TH
	(E3 .	
	654 ; COMMAND DISPATCHER	NASC CL 595 POP B NASO 88 596 DCK 8 NASC 23 597 DMK H NASE CACOUN 588 JAP CKISS
	655 ;	
	656 ;	996 23 597 INK H 1936 (3800A 598 JAP 8855
0AE5 210020	657 COMM: LXI H, CM	DDIE CET DOTATED
	CEO DICU D	DBUF ; SET POINTER
99E9 74	658 PUSH B 659 MOV M. C	SAVE BC
0AEA 78	603 COMMA MOU O D	B LOAD COMMAND INTO BUFFER
	660 COMM1: MOV A, B	
OREB A7	661 ANA A	; IS IT 0?
OREC CAFBOA	662 JZ CMD0	
OAEF CDADOA		N GET PARAMETER
OAF2 DAA708	664 JC ILLE	
0AF5 23		; INC BUFFER POINTER
0AF6 05	666 DCR B	; DEC PARAMETER COUNTER
0AF7 77	667 MOY M, A	
OAF8 C3EAOA	668 JMP COMM	1 ; GET NEXT PARAMETER
ORFB 210020	669 CMDOUT: LXI H, CM	DBUF REPOINT POINTER
ORFE C1	670 POP B	; RESTORE PARAMETER COUNT

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ORFF DB90
            671 COMM2: IN STAT73 READ 8273 STATUS
            672
                     RLC
                                     ROTATE CBSY INTO CARRY
0B01 07
0B02 DAFF0A
            673
                     JC
                                   ; WAIT FOR OK
            674
                     MOY
                          A, M
                                     OK, MOVE COMMAND INTO A
0B05 7E
0B06 D390
            675
                     OUT
                          COMM73
                                     ; OUTPUT COMMAND
0B08 78
            676 PAR1: MOV
                         A, B GET PARAMETER COUNT
                     ANA
            677
0B09 A7
                                     ; IS IT 0?
            678 H 3472 RZ
                                  ; YES, DONE, RETURN
0B0A C8
                          H 4829
                                  ; INC COMMAND BUFFER POINTER
0B0B 23
            679 INX
            680 DCR
                          B 8
                                  HEUM; DEC PARAMETER COUNT SEEDS
0B0C 05
0B0D DB90
            681 PAR2: IN
                          STAT73
                                  READ STATUS
                                   IVII; IS CPBF BIT SET? SEES MICH
        682 ANI
                          CPBF
0B0F E620
                          PAR2
                                   TUO; WAIT TIL ITS 0 8420 8400
0B11 C20D0B
         683 JNZ
0814 7E
         684 MOV
                          A. M
                                   IN OK, GET PARAMETER FROM BUFFER
            685 OUT
                          PARM73
                                   OUTPUT PARAMETER
0B15 D391
                                   GET NEXT PARAMETER
0B17 C3080B 686 3 2 4 JMP
                          PAR1
                          RORGE
         SET LOG 780 LATER
            688 ; 3483
                           - 14
           689 ; INITIALIZE AND ENABLE RX DMA CHANNEL
                                  VOH
            6907; 1 3YA2 1 3A9
      SETMING 691 ;00 THE
                        A, DRDMA
0B1A 3E62 692 RXDMA: MVI
                                   DISABLE RX DMA CHANNEL
                                   90%; 8257 MODE PORT 85 5108
0B1C D388 693 0UT
                         MODE57
0B1E 010082 694 LXI
                          B, RXBUF
                                   RX BUFFER START ADDRESS
0B21 79 LOT 695 W MOV
                          A.C
                                   RX BUFFER LSB
            696 OUT
                          CHØADR |
                                   CHO ADR PORT
                                                  24 0136
0B22 D3A0
0B24 78 /18 / 697 / 697 MOV
                          A.B
                                   RX BUFFER MSB
0B25 D3A0 698 0UT
                          CHOADR
                                   CHO ADR PORT
0B27 01FF41 699 LXI
                          B, RXTC
                                   RX CH TEERMINAL COUNT AND SSOR
            700 MOY
                          A, C
                                   RX TERMINAL COUNT LSB
0B2A 79
       T18 701 39 T23T OUT
                          CHATC
                                   CHO TC PORT
OB2B D381
0B2D 78 9 12 1702 3 100 MOY
                          A, B
                                   RX TERMINAL COUNT MSB
                          CHOTC C
                                   #1; CHO TC PORT 9880 AS38
0B2E D3R1 703 0UT
0B30 3E63
        794 MVI
                          A. FNDMA
                                   ENABLE DMA WORD
        705 241 OUT
                          MODE57
                                   3 8257 MODE PORT
0B32 D3A8
       706 RET
                          RK11R73
                                   RETURN
0B34 C9
       A M STORE (707 FERR
                                   941
            709 ; INITIALIZE AND ENABLE TX DMA CHANNEL
        21.U2710 (N T30: SIX9
                                   316
         711 711
                                   DISABLE TX DMA CHANNEL
0835 3E61
           712 TXDMA: MYI A DTDMA
0837 D3R8 713 2 23 OUT
                          MODE57
                                   31;8257 MODE PORT 382493 BE38
0B39 010080 714 LXI
                                   TX BUFFER START ADDRESS
                          B, TXBUF
                                   TX BUFFER LSB
0B3C 79 715 900 MOV
                          A.C
         716 000 000 OUT
9B3D D382
                          CH1ADR
                                   ; CH1 ADR PORT
                                                 8042 C33980
            717 MOV
                          A, B
                                   TX BUFFER MSB
0B3F 78
0B40 D3R2 718 0UT
                                  ; CH1 ADR PORT
                          CH1 ADR
0B42 01FF81 719 TXDMR1: LXI
                          B, TXTC
                                   TX CH TERMINAL COUNT
                          A.C
       720 MOY
                                   TX TERMINAL COUNT LSB
9845 79
0846 D3A3 721 OUT
                          CHITC
                                   ; CH1 TC PORT
AR48 78
            722
                     YOM
                          A.B
                                    ; TX TERMINAL COUNT MSB
            723 OUT CHITC CHITC ; CHI TC PORT
0B49 D3A3
0848 3E63 724 NVI A, ENDMA ; ENABLE DMA WORD
            725 OUT MODE57 8257 MODE PORT
084D D3R8
            726
0B4F C9
                    RET
                                  RETURN
FORT PREFERENCES LORD FOR POLINTER
                                   785 P09
                            MA
   927 FOR 728 ; II T39 ;
                                   YON
                                                     903t 7E
```

2-312

	732 ;			624 1939	
	733 ;		COMPAS	7. 5 (LOC 3CH)  ; SAVE HL ; SAVE PSH ; SAVE BC ; SAVE DE ; DISABLE RX DMA ; 8257 MODE PORT ; RESET RST7. 5 F/F  ; D IS RESULT COUNT ; GET LOAD POINTER ; SAVE IT ; SAVE IT AGAIN ; SAVE LSB ; GET CONSOLE POINT ; BUMP LOAD POINTER ; GET SET TO TEST ; LOAD=CONSOLE? ; YES, BUFFER FULL ; DEC COUNTER ; NOT DONE, TRY AGA ; RESET COUNTER ; RESTORE LOAD POIN ; READ STATUS ; TEST RX INT BIT ; DONE, GO FINISH UE ; READ STATUS AGAIN ; IS RESULT READY? ; NO, TEST AGAIN ; YES, READ RESULT ; STORE IN BUFFER ; INC BUFFER POINTER ; DEC COUNTER ; GET MORE RESULTS ; GET SET TO TEST ; ALL RESULTS? ; YES, SO FINISH UE ; NO, LOAD 0 TIL DO ; BUMP POINTER ; DEC COUNTER ; GO AGAIN ; UPDATE LOAD POINT ; GET MODE INDICATO ; NORMAL MODE? ; YES, CLEAN UP BEF	6896 0389
	734 ; RECEIVE	R INTE	RRUPT - RST	7. 5 (LOC 3CH)	87 8688
	735 ; 11 21		ñ	627 680	
9C99 F5	736 RXI	PUSH	Н	SAVE HL	
9C91 F5	737	PLISH	PSH	SAVE PSW	
9C92 C5	770	DUCH	D	COUE DC	
9092 05	770	DUCH	D	COUE DE	
9093 D3	740	MUT	O DODMO	ATCODI E DV AMO	
0004 3562	740 1010 211	LIAI	n, DRUMM	DISHBLE KA DAH	
0000 D240	741	001	MODEST	; 8257 MUDE PURT	
0C08 3E18	142	MAI	H, 18H	RESEL KSIZ 5 FZF	
OCOH 30	743	SIM	E TARAN	100 283	THE CITY
0C0B 1604	744	MYI	D. 04H	; D IS RESULT COUNT	ER
0C0D 2R1020	745	LHLD	LDADR	GET LOAD POINTER	
0C10 E5	746	PUSH	Н	; SAVE IT	
0C11 E5	747	PUSH	KH BURNE O	SAVE IT AGAIN	
0C12 45	748	MOY	B, L	; SAVE LSB	
0C13 2A1320	749	LHLD	CNADR	GET CONSOLE POINT	TER
0C16 04	750 RXI1:	INR	Barcas	BUMP LOAD POINTER	LSB
0C17 78	751	MOY	A, B	GET SET TO TEST	
0C18 BD	752	CMP	Lasses a	LOAD=CONSOLE?	
0C19 CAE40A	753	JZ	BUFFUL	YES, BUFFER FULL	
0C1C 15	754	DCR	D occurr	DEC COUNTER	easn coas
0C1D C2160C	755	JNZ	RXI1	NOT DONE. TRY AGE	RIN STACES
9C29 1695	756	MVT	D. 05H	RESET COUNTER	apro Fega
9C22 F1	757	POP	Н	PESTOPE LOSD POTA	ITED
9C27 DR99	750 PV12	TN	STAT77	PEON CTOTIC	DE 0000
0C25 E600	750 KM12.	ONT	DVINT	TECT DV INT DIT	
9023 E000	769	17	DV17	- DONE CO EINICH I	ID av anda
0021 CH3300	764	TM	CTOT72	DEOD CTOTIC OCOTA	(a) (170)
9020 CC90	762	ONIT	DUTTO	KEND SINIUS NUMBER	7145/A 32/24
902C E002	702	LRAT	RAIRH	113 RESULT REPUT!	5,655, 145,03
BUSE CUSSOC	764	JZ	KVIS	INU, IEST HUHIN	8MS/0 7/58A
0031 0693	764	IN	KXIK/3	YES, KEHD KESULI	
0033 77	765	MUY	Mr. H	STURE IN BUFFER	
0C34 2C	766	INR	L	; INC BUFFER POINTE	:R
0C35 15	767	DCR	XD TIBER C	DEC COUNTER	
0C36 C3230C	768	JMP	RXI2	GET MORE RESULTS	
0C39 7A	769 RXI3:	YOM	A, D	GET SET TO TEST	
0C3A A7	770	ANA	Regroup.	; ALL RESULTS?	0835 3861
0C3B CA450C	771	JZ	RXI4	YES, SO FINISH UF	8827 7288
0C3E 3600	772	MVI	M- 00H	; NO, LOAD 0 TIL DO	NE BRIEF COSS
0C40 2C	773 AND XT	INR	L O.R	BUMP POINTER	
0C41 15	774	DCR	D SIGNING	; DEC COUNTER	SREO 0599
0C42 C3390C	775 XX	JMP	RXI3	; GO AGAIN	
0C45 221020	776 RXI4:	SHLD	LDADR	UPDATE LOAD POINT	ER casul toda
0C48 3R1520	777	LDA	PRMPT	GET MODE INDICATO	Recognic
AC4R FE2D	778	CPT	1-1 20	NORMAL MODE?	6042.53
0C4D CA850C	779	17	PYIG	YES, CLERN UP BEF	ODE DETIEN
00 10 01 0000	780 ;	O.L.	8.8	100 FEEE CO. 1000	ONE RETORN
acts max	W Too Mat VI				61-0450
				CONTROL BYTE	EREO CAGO
				LL SET UP SPECIAL TX CO	
			TURN WITH PU	LL INDICATOR NOT 0	SAEG GASS
2002 54	784 ; (6) (13)			726 RET	60 FM98
9C50 E1	785	POP	H	GET PREVIOUS LOAD	
0C51 7E	796	MOA	A, M	GET IC BYTE FROM	BUFFER

	1000	APPLICAL	SCHARGER JACO
0C59 2C	790 INK	L	
9C5A 56	792 MOV		GET ADR BYTE AND SAVE IT IN D
	793 INR		, GET HUR BYTE HAD SHIVE IT IN U
0C5B 2C 0C5C 7E		L	GET CNTL BYTE FROM BUFFER TO SEED
0C5D FE93	795 CPI		; WAS IT SNRM-P?
0C5F CA6C0C	796 JZ	T1	; YES, GO SET RESPONSE
0C62 FE11	797 CPI	RR0P	; WAS IT RR(0)-P?
0C64 C2890C	798 JNZ		; YES, GO SET RESPONSE, OTHERWISE RETURN
0C67 1E11	799 MVI	E, RRØF	; RR(0)-P SO SET RESPONSE TO RR(0)-F ; GO FINISH LOADING SPECIAL BUFFER
0C69 C36E0C			
0C6C 1E73	801 T1: MVI	E, NSAF	; SNRM-P SO SET RESPONSE TO NSA-F
0C6E 212020	802 TXRET: LXI	H, CMDBF1	; SPECIAL BUFFER ADR
0C71 36C8	806 MVI		; LOAD TX FRAME COMMAND
0C73 23	808 INX	Н	; INC POINTER
0074 3600	809 MVI	M, 00H	;L0=0 77 \$338
0C76 23	810 INX	Н	; INC POINTER
0077 3600	811 MVI		;L1=0
0C79 23	812 INX	Н	; INC POINTER
0C7A 72	813 MOY		; LOAD RCVD ADR BYTE
0C7B 23	814 INX		; INC POINTER
0C7C 73	815 MOV		; LOAD RESPONSE CNTL BYTE
0C7D 3E01	816 MVI		SET POLL INDICATOR NOT 0
0C7F 321620			; LOAD POLL INDICATOR
0C82 C3890C	818 JMP	RXI5	RETURN
	819		
0C85 E1			CLEAN UP STACK IF NORMAL MODE
0C86 C3890C	821 JMP	RXI5	; RETURN
2022 201220	822 M 3M2.		
0C89 CD1A0B	823 RXI5: CALL		AUPTI DINI ONNAMET
0C8C D1	824 POP	D	; RESTORE REGISTERS
0C8D C1		-	
0C8E F1	826 POP		
0C8F E1	827 POP		
0C90 FB	828 EI		; ENABLE INTERRUPTS
0C91 C9	829 RET		; RETURN SAME SCHOOL
	830 ; 11 3462		9000 ES 873 P05H
	831 ; 1 82.1 3482 1	1.8	9000 45 874 MOV
	832 ; MESSAGE TYPER -		
	833 3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		0.00 64 64 1MIT: 1ME
2000 05	834 ; 01 152 1501	9.8	A04 228 82 1376
0C92 C5	835 TYMSG: PUSH 836 TYMSG2: MOV	В	; SAVE BC
0C93 7E	836 TYMSG2: MOV	A, M	GET ASCII CHR
	837 INX	H	; INC POINTER
0C95 FEFF	838 CPI	OFFH 4384	) 310F:
	839 JZ	TYMSG1	; YES, GET SET FOR EXIT
0C9A 4F		C. A EXSENS	A DE LOI LOI DAN DILL
0C98 CDF805			AND DIE OIL
0C9E C3930C			; GET NEXT CHR ; RESTORE RC
	843 TYMSG1: POP	B 199 M	THE TOTAL BO
0CR2 C9	844 RET		2 INETORIA
	845 ;		
	846 ;		
	847 ; SIGNON MESSAGE		9075 3888 988 WILL 9075 20 WILL 9075 20 WILL 9075 20 WILL 9075 20 WILL 9075 9075 9075 9075 9075 9075 9075 9075
	848 ;		

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```
OCA3 OD 849 SIGNON: DB
                                                                         CR, '8273 MONITOR 141. 1', CR, 0FFH
       OCA4 38323733 THE SECTION OF THE SEC
        OCR8 204D4F4E
        0CAC 49544F52
        0CB0 20205631
        0CB4 2E31 | 3VP2 0H9 3TV3 9CR T30 |
        0CB6 0D
        OCB7 FF GRAZUB MOST BIVE JIMO TEST
                                       850 ; 302 71 798
                               851 ; = 60 .234
                                       852 ;
MONTH RELIGIOUS 853 RECEIVER INTERRUPT MESSAGES
       4-(0)99 01 32-642398542302 4-(0)99: 38997.3
         93334 W 10392 A 855 ; 42 W 7 00 :
        0CB8 0D 856 RXIMSG: DB
                                                                         CR, 'RX INT - ', OFFH
        0CB9 52582049 and state at 1999
        0CBD 4E54202D
        0CC1 20
                                                                                   H
        0CC2 FF
                                        857
                                       858 ; TRANSMITTER INTERRUPT MESSAGES
                                       859 ; married that .
        0CC3 0D
                                  860 TXIMSG: DB
                                                                         CR, 'TX INT - ', OFFH
        0CC4 54582049
        OCC8 4E54202D
        OCCC 20 8 TOM SCOTADIGMI LIDY YES:
        OCCD FF
                                       861 ; 1000 739
                                        862;
               863 ; TRANSMITTER INTERRUPT ROUTINE
                                       864 ;
        OCCE E5
                                       865 TXI: PUSH
                                                                                                     ; SAVE HL
        OCCF F5
                                    866 PUSH
                                                                         PSW PMG/S
                                                                                                     ; SAYE PSW
        0CD0 C5
                                    867 PUSH
                                                                          В
                                                                                                     ; SAYE BC
        0CD1 D5
                                       868
                                                            PUSH
                                                                          D
                                                                                                     SAVE DE
        0CD2 3E61
                                       869
                                                            MVI
                                                                          A, DTDMA
                                                                                                     ; DISABLE TX DMA
        0CD4 D3A8
                                       870
                                                                          MODE57
                                                            OUT
                                                                                                     ; 8257 MODE PORT
        9CD6 1694
                                   871 MYI
                                                                          D. 04H
                                                                                                     ; SET COUNTER
        9CD8 281929
                                       872 LHLD
                                                                          LDADR
                                                                                                     GET LOAD POINTER
        OCDB E5
                                       873
                                                            PUSH
                                                                          H
                                                                                                     ; SAVE IT : ASA
        OCDC 45
                                       874
                                                            MOA
                                                                          B, L
                                                                                                     ; SAVE LSB IN B
                                                                          CNADR
        0CDD 281320
                                       875 LHLD
                                                                                                  GET CONSOLE POINTER
                                       876 TXI1: INR
        0CE0 04
                                                                                                    ; INC POINTER
        0CE1 78
                                       877
                                                           MOY
                                                                          A, B
                                                                                                    GET SET TO TEST
                                       878 CMP
        OCE2 BD
                                                                          L
                                                                                                    ; LOAD=CONSOLE?
        OCE3 CRE40A
                                       879 JZ
                                                                          BUFFUL MA
                                                                                                    ; YES, BUFFER FULL
        OCE6 15
                                       880 DCR
                                                                          D
                                                                                                    ; NO, TEST NEXT LOCATION
        OCE7 C2EGOC
                                       881 JNZ
                                                                          TXI1
                                                                                                    ; TRY AGAIN
        OCEA E1
                                       882 POP
                                                                          TVMS08 H
                                                                                                     ; RESTORE LOAD POINTER
        OCEB DB92
                                       883 gra qu IN
                                                                          TXIR73
                                                                                                     READ RESULT
        OCED 77
                                       884 MOY
                                                                          MA DEST
                                                                                                     STORE IN BUFFER
        OCEE 2C
                                                                          L Spenyt
                                       885 INR
                                                                                                     ; INR POINTER
        OCEF 3600
                                       886 MVI
                                                                          M. 00H
                                                                                                     ; EXTRA RESULT SPOTS 0
        ØCF1 2C
                                       887
                                                INR
                                                                         L
        0CF2 3600
                                       888
                                                            MVI
                                                                          M. 00H
        0CF4 2C
                                       889
                                                            INR
                                                                         L
        0CF5 3600
                                       899
                                                            MYI
                                                                          M. 00H
        OCF7 2C
                                       891
                                                            INR
                                                                         L
```

2-315

								NTROD						19		la me		
				tito														
							ıl mə											
0CF8 36	99 8	192		MY	TUONON	001	AS Y											
ØCFA 2C		193		IN	D I	3.0												
0CFB 22		94		SH	LD L	DADE	part	man 7.	UPI	DATE LO	OAD POINTE	ER						
OCFE CD		199				XDMF	ng	rmrl	RE	SET DME	CHANNEL							
0001 D1		100		PO			F	1764	RES	STORE D	)E							
0002 C1		101			P		12 T II II	tova:	REG	STORE F	RC.							
0002 C1		102			PARE													
0D04 E1		103			Poolit													
0007 EE		04									ITERRUPTS							
0005 FB		105		RE				Rese			TERROI 15							
9000 C3		106 ;			J sur			Exte	KE	IONI								
		907 ;					Re Re											
				Ye V														
		52 ;				365		fini										
		953 ;		EN	noiti		0 be											
	3	734		EN	Dagyta		dnu.	ern I										
DUDI TO CU	IMPOL C																	
PUBLIC SY	LIBUE2																	
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FIFTEDNIOL	CIMPOL C		11:0.00				QU IT											
EXTERNAL	SYMBULS			E														
			90															
LICED CUMP	101.5						010											
USER SYMB			0000		DI ICC II	0.00	o) m	OLIO ODI		2000	CHOTO	_	0004	0114.000	0.0000	CHATC	^	0003
			09CE		BUFFUL			CHORDE			CHOTC				A 00A2	CH1TC		
CMD51 A			2020		CMDBUF			ACT DO			CMDREC	-			A 0931		-	2013
CNT053 A					CNT253			CNTL5					0003		A 0588	COBR		999C
			OAEA		COMM2						CPBF		0020	CR	A 000D	CRLF		05EB
			2027		DISPY			DISPY			DISPY2				A 0062	DTDMA		0061
			0A1B		ENDMA			GDWN		08FF	GETCH				A 087D			09C4
			2010			A 00		LKBR1			LKBR2				A 9861	MDCNT0		
MDCNT2 R			00CE		MODE53			MODE 57			MONTOR				A 06C7	NSAF		0073
	0B08 PRR2		080D		PARIN			PARIN			PARIN2				A OABC	PARM73		
POLIN A			2015		0.000	A OF	ALK UBILL	R1PT		OAA7	RBCMD				A 0971	RDWN		08AF
			2800		RESL73			ROCMD		095D	RPCMD			RROF	A 0011	RROP		0011
			20CE		RST75			RXBUF		8200	RXD51			RXDMA	A 081A	RXI		9C99
	0C16 RXI2		0C23			A 00		RXI4		0C45	RXI5		0C89	RXI6	A 0C85	RXIMSG		
			0093			A 06		RXS1	A	0A69	RXS2		0A7F	RXS3	A 0880	RXSORC		
RXTC A	41FF SBCM	ID A	0985		SDWN	A 08	307	SIGNO	I A	OCA3	SLCMD	A	098F	SNRMP	A 0093	SOCHD	A	09A6
SPCMD A			09BA		SSCMD	A 05	9B0	START	A	0800	STAT51	A	9989	STAT57	A 00A8	STAT73		
STKSRT A	2000 SW	A	0943		T1 0	A 00	260	TBUFFL	. A	0A24	TBUFL	A	0A07	TBUFL1	A GAGD	TOWN	A	090E
TEST73 A		D A	09EC		TFCMD1	A 09	¥F6	TFRET	A	0A36	TLCMD	A	0999	TRUE	A 0000	TRUE1	A	0000
TXBUF A	8000 TXD5	1 A	9988		TXDMA	A 06	335	TXDMA	L A	<b>0B42</b>	TXI	A	OCCE.	TXI1	A OCEO	TXIMSG	A	0CC3
TXINT A	9984 TXIR	273 A	0092		TXIRA	A 06	991	TXPOL	A	094C	TXRET	A	OC6E	TXSORC	A 0A47	TXTC	A	81FF
TYMSG A	0C92 TYMS	G1 A	OCA1		TYMSG2	A 00	293	YALDG	A	075E								

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ASSEMBLY COMPLETE, NO ERRORS

Asynchronous Communication Contents with the 8274 Multiple Protocol Serial Controller INTRODUCT ION 2-318 Communication Functions System Interface Scope 2-319 SERIAL AS YN CHRONOUS DATA LINKS Characters Framing agent Timing Parity Communication Modes Break Condition MPSC SYSTEM INTERFACE 2-321 Hardware Environment 279092001 20003 Operational Interface 160 Reset Externa<sup>1</sup>/Status Latches Error Reporting Transmitter/Receiver Initial ization Polled Operation Interrupt Driven Operation Interrupt Configurations Interrupt Sources/Priorities Interrupt Initialization Interrupt Service Routines DATA LINK INTERFACE 2-328 Serial Data Interface Data Clocking DRESS SAMBOTZ Modem Control APPENDIX A 2-329 Command/Status Details Per Async OFC) 48 R 0962 Communication STATE & SECTION R APPENDIX B 018C A 2000 I 2-336 MPSC Polled Transmit/Receive Character Routines 2-340 APPENDIX C G250 N Interrupt Driven Transmit/Receive Software SLOW A GROLE APPENDIX D 2-342 Application Example Using SDK-86 TECHD B 695C 2009 R TERKT MORE R THIRT

RESPONSE CONFLETE NO ETRORES

#### ASYNCHRONOUS COMMUNICATION stad sugnordanyaA fatre2 .S

#### A serial asynchronous interface is a metro 47.58 BHT HIW synchronous mode characters may vary in

## of data transmission in which the receiving length from five to eight bits. The charand transmitting systems need no NALLONTHOO LAIRS 1000TONG-LTJUM spends on the coding method

# bit characters noitsuborini for ASCII data, and eight-bit characters and eight-bit characters.

The 8274 Multi-protocol serial controller (MPSC) is a sophisticated dual-channel communications controller that interfaces microprocessor systems to high-speed serial data links (at speeds to 880K bits per second) using synchronous or asynchronous protocols. The 8274 interfaces easily to most common microprocessors (e.g., 8048, 8051, 8085, 8086, amd 8088), to DMA controllers such as the 8237 and 8257, and to the 8089 I/O processor. Both MPSC communication channels are completely independent and can operate in a full-duplex communication mode (simultaneous data transmission and reception.

Communication Functions

The 8274 performs many communications oriented functions, including:

Converting data bytes from a microprocessor system into a serial bit stream for transmission over the data link to a receiving system.

Receiving serial bit streams and reconverting the data into parallel data bytes that can easily be processed by the microprocessor system.

Performing error checking during data transfers. Error checking functions include computing/transmitting error codes (such as parity bits or CRC bytes) and using these codes to check the validity of received data.

Operating independently of the system processor in a manner designed to reduce the system overhead involved in data transfers.

System Interface Transit of TRATE ventions not

The MPSC system interface is extremely flexible, supporting the following data transfer modes:

1. Polled Mode. The system processor periodically reads (polls) an 8274 status register to determine when a

character has been received, when a character is needed for transmission, and when transmission errors are detected.

- 2. Interrupt Mode. The MPSC interrupts the system processor when a character has been received, when a character is needed for transmission, and when transmission errors are detected.
- 3. DMA Mode. The MPSC automatically requests data transfers from system memory for both transmit and receive functions by means of two DMA request signals per serial channel. These DMA request signals may be directly interfaced to an 8237 or 8257 DMA controller or to an 8089 1/0 processor.
- 4. WAIT Mode. The MPSC ready signal is used to synchronize processor data transfers by forcing the processor to enter wait states until the 8274 is ready for another data byte. This feature enables the 8274 to interface directly to an 8086 or 8088 processor by means of string I/O instructions for very high speed data links.

#### Normally the data link is in an idle or equal

This application note describes the use of the 8274 in asynchronous communication modes. Asynchronous communication is typically used to transfer data to/from video display terminals, modems, printers, and other low-to-medium speed peripheral devices. Use of the 8274 in both interrupt driven and polled system environments is described. Use of the DMA and WAIT modes are not described since these modes are employed mainly in synchronous communication systems where extremely high data rates are common. Programming examples are written in PL/M--86 (Appendix B and Appendix C). PL/M-86 is executed by the iAPX-86 and iAPX-88 processor families. In addition, PL/M-86 is very similar to PL/M-80 10 518 10 911 (executed by the MCS-80 and MCS-85 processor families). In addition, Appendix D describes a simple application example using an SDK-86 in an iAPX-86/88 environments delias y fementa at anotasimament

#### 2. Serial Asynchronous Data Links Characters

A serial asynchronous interface is a method and In asynchronous mode characters may vary in of data transmission in which the receiving and transmitting systems need not be synchronized. Instead of transmitting clocking information with the data, locally generated clocks (16, 32 or 64 times as fast as the data transmission rate) are used by the transmitting and receiving systems. When a character of information is sent by the transmitting system, the character data is framed (preceded and followed) by special START and STOP bits. This framing information permits the receiving system to temporarily synchronize with the data transmission. (Refer to Figure 1 during the following discussion of asynchronous data transmission.)

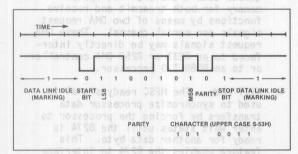


Figure 1. Transmission of a 7-Bit ASCII Character with Even of a Parity untann OVI putate to ansem you

Normally the data link is in an idle or marking state, continuously transmitting a "mark" (binary 1). When a character is to be sent, the character data bits are immediately preceded by a "space" (binary 0 START bit). The mark-to-space transition informs the receiving system that a character of information will immediately follow the start bit. Figure 1 illustrates the transmission of a 7-bit ASCII character (upper case S) with even parity. Note that the character is transmitted immediately following the start bit. Data bits within the character are transmitted from leastsignificant to most-significant. The parity bit is transmitted immediately following the character data bits and the STOP framing bit (binary 1) signifies the end of the character.

Asynchronous interfaces are often used with human interface devices such as CRT/keyboard units where the time between data transmissions is extremely variable.

length from five to eight bits. The character length depends on the coding method used. For example, five-bit characters are used when transmitting Baudot Code, sevenbit characters are required for ASCII data, and eight-bit characters are needed for EBCDIC and binary data. To transmit messages composed of multiple characters, each character is framed and transmitted separately (Figure 2).

This framing method ensures that the receiving system can easily synchronize with the start and stop bits of each character, preventing receiver synchronization errors. In addition, this synchronization method makes both transmitting and receiving systems insensitive to possible time delays between character transmissions.

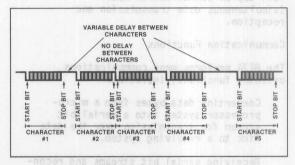


Figure 2. Multiple Character Transmission

#### Framing

Character framing is accomplished by the START and STOP bits described previously. When the START bit transition (mark to space) is detected, the receiving system assumes that a character of data will follow. In order to test this assumption (and isolate noise pulses on the data link), the receiving system waits one-half bit time and samples the data link again. If the link has returned to the marking state, noise is assumed, and the receiver waits for another START bit transition.

When a valid START bit is detected, the receiver samples the data link for each bit of the following character. Character data bits and the parity bit (if required) are sampled at their nominal centers until all required characters are received. Immediately following the data bits, the receiver samples the data link for the STOP bit, indicating the end of the character. Most systems permit specification of 1, 1 1/2, or 2 stop bits.

Floure 3 filustrates typical MPSC con-

## figurations for use with an 8088 micro- gnimit

The transmitter and receiver in an asynchronous data link arrangement are clocked independently. Normally, each clock is generated locally and the clocks are not synchronized. In fact, each clock may be a slightly different frequency. (In practice. the frequency difference should not exceed a few percent. If the transmitter and receiver clock rates vary substantially, errors will occur because data bits may be incorrectly identified as START or STOP framing bits.) These clocks are designed to operate at 16, 32, or 64 times the communications data rate. These clock speeds allow the receiving device to correctly sample the incoming bit stream.

Serial interface data rates are measured in bits/second. The term baud is used to specify the number of times per second that the transmitted signal level can change states. In general, the baud is not equal to the bit rate. Only when the transmitted signal has two states (electrical levels) is the baud rate equal to the bit rate.

Most point-to-point serial data links use RS-232-C, RS-422, or RS-423 electrical interfaces. These specifications call for two electrical signal levels (the baud is equal to the bit rate). Modem interfaces, however, may often have differing bit and baud rates.

While there are generally no limitations on the data transmission rates used in an asynchronous data link, a limited set of rates has been standardized to promote equipment interconnection. These rates vary from 75 bits per second to 38,400 bits per second. Table 1 illustrates typical

Table 1. Communication Data Rates and Associated Transmitter/Receiver Clock Rates

Data Rate (bits/second)	CI	ock Rate (k	Hz)
200	X16	X32	X64
75	1.2	2.4	4.8
150	2.4	4.8	9.6
300	4.8	9.6	19.2
600	9.6	19.2	38.4
1200	19.2	38.4	76.8
2400	38.4	76.8	153.6
4800	76.8	153.6	307.2
9600	153.6	307.2	614.2
19200	307.2	614.4	_
38400	614.4	ref-ens	mait <del>a</del> l i

asynchronous data rates and the associated clock frequencies required for the transmitter and receiver circuits.

## I/O channel responds to two I/O or memory addresses as shown in Table 2. In additiviting

In order to detect transmission errors, and and parity bit may be added to the character data as it is transferred over the data link. The parity bit is set or cleared to make the total number of "one" bits in the character even (even parity) or odd (odd parity). For example, the letter "A" is represented by the seven-bit ASCII code 1000001 (41H). The transmitted data code (with parity) for this character contains eight bits: 01000001 (41H) for even parity and 11000001 (OC1H) for odd parity. Note that a single bit error changes the parity of the received character and is therefore easily detected. The 8274 supports both odd and even parity checking as well as a parity disable mode to support binary data transfers.

#### Communication Modes

Serial data transmission between two devices can occur in one of three modes. In the simplex transmission mode, a data link can transmit data in one direction only. In the half-duplex mode, the data link can transmit data in both directions, but not simultaneously. In the full-duplex mode (the most common), the data link can transmit data in both directions simultaneously. The 8274 directly supports the full-duplex mode and will interface to simplex and half-duplex communication data links with appropriate software controls.

#### Break Condition

Asynchronous data links often include a special sequence known as a break condition. A break condition is initiated when the transmitting device forces the data link to a spacing state (binary 0) for an extended length of time (typically 150 milliseconds). Many terminals contain keys to initiate a break sequence. Under software control, the 8274 can initiate a break sequence when receiving data.

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## 3. MPSC System Interface

Hardware Environment wards reviewed bas restrict

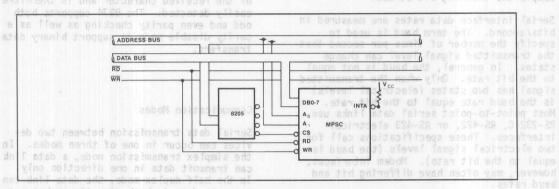
The 8274 MPSC interfaces to the system processor over an 8-bit data bus. Each serial I/O channel responds to two I/O or memory addresses as shown in Table 2. In addition, and the MPSC supports vectored and daisychained interrupts.

Table 2: 8274 Addressing. The 8274 may be configured for memory mapped or I/O mapped operation.

cs	A	A <sub>0</sub>	Read Operation	Write Operation
0	0	0	Ch. A Data Read	Ch. A Data Write
0	1	0	Ch. A Status Read	Ch. A Command/Parameter
0	201	0.00	Ch. B Data Read	Ch. B Data Write
0	1 1	1	Ch. B Status Read	Ch. B Command/Parameter
1	X	X	High Impedence	High Impedence

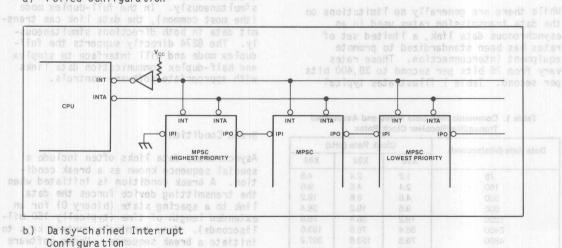
The 8274/processor hardware interface can be configured in a flexible manner, depending on the operating mode selected --polled, interrupt driven, DMA, or WAIT. Figure 3 illustrates typical MPSC configurations for use with an 8088 microprocessor in the polled and interrupt driven modes.

All serial-to-parallel conversion, parallel-to-serial conversion, and parity checking required during asynchronous serial I/O operation is automatically performed by the MPSC.



#### a) Polled Configuration

control, the 8274 can initiate a break



#30400 but \$3.60 pniss many Figure 3: 8274 Hardware Interface for Polled and Interrupt Driven Environments

Operational Interface

Command, parameter, and status information is stored in 22 registers within the MPSC (8 writable registers and 3 readable registers for each channel). These registers are all accessed by means of the command/status ports for each channel. An internal pointer register selects which of

the command or status registers will be written or read during a command/status access of an MPSC channel. Figure 4 diagrams the command/status register architecture for each serial channel. In the following discussion, the writable registers will be referred to as WRO through WR7 and the readable registers will be referred to as RRO through RR2.

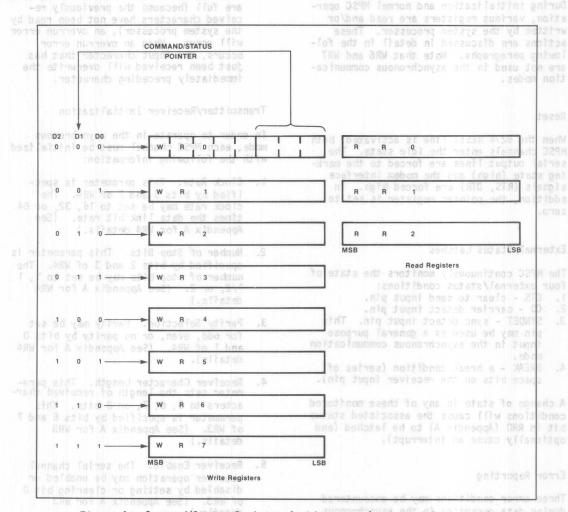


Figure 4: Command/Status Register Architecture (each serial channel)

The least significant three bits of WRO are automatically loaded into the pointer register every time WRO is written. After reset, WRO is set to zero so that the first write to a command register causes the data to be loaded into WRO (thereby setting the pointer register). After WRO is written, the following read or write accesses the

register selected by the pointer. The pointer is reset after the read or write operation is completed. In this manner, reading or writing an arbitrary MPSC channel register requires two I/O accesses. The first access is always a write command. This write command is used to set the pointer register. The second access is

either a read or a write command; the pointer register (previously set) will ensure that the correct internal register is read or written. After this second access, the pointer register is automatically reset. Note that writing WRO and reading RRO does not require presetting of the pointer register.

During initialization and normal MPSC operation, various registers are read and/or written by the system processor. These actions are discussed in detail in the following paragraphs. Note that WR6 and WR7 are not used in the asynchronous communication modes.

#### Reset

When the 8274 RESET line is activated, both MPSC channels enter the idle state. The serial output lines are forced to the marking state (high) and the modem interface signals (RTS, DTR) are forced high. In addition, the pointer register is set to zero.

#### External/Status Latches

The MPSC continuously monitors the state of four external/status conditions:

- CTS clear to send input pin.
- 2. CD carrier detect input pin.
- SYNDET sync detect input pin. This pin may be used as a general purpose input in the asynchronous communication mode.
- BREAK a break condition (series of space bits on the receiver input pin).

A change of state in any of these monitored conditions will cause the associated status bit in RRO (Appendix A) to be latched (and optionally cause an interrupt).

#### Error Reporting

Three error conditions may be encountered during data reception in the asynchronous mode:

1. Parity. If parity bits are computed and transmitted with each character and the MPSC is set to check parity (bit 0 in WR4 is set), a parity error will occur whenever the number of "1" bits within the character (including the parity bit) does not match the odd/even setting of the parity check flag (bit 1 in WR4).

- Framing. A framing error will occur if a stop bit is not detected immediately following the parity bit (if parity checking is enabled) or immediately following the most-significant data bit (if parity checking is not enabled).
- 3. Overrun. If an input character has been assembled but the receiver buffers are full (because the previously received characters have not been read by the system processor), an overrun error will occur. When an overrun error occurs, the input character that has just been received will overwrite the immediately preceding character.

#### Transmitter/Receiver Initialization

In order to operate in the asynchronous mode, each MPSC channel must be initialized with the following information:

- Clock Rate. This parameter is specified by bits 6 and 7 of WR4. The clock rate may be set to 16, 32, or 64 times the data link bit rate. (See Appendix A for WR4 details.)
- Number of Stop Bits. This parameter is specified by bits 2 and 3 of WR4. The number of stop bits may be set to 1, 1 1/2, or 2. (See Appendix A for WR4 details.)
- Parity Selection. Parity may be set for odd, even, or no parity by bits 0 and 1 of WR4. (See Appendix A for WR4 details).
- Receiver Character Length. This parameter sets the length of received characters to 5, 6, 7, or 8 bits. This parameter is specified by bits 6 and 7 of WR3. (See Appendix A for WR3 details.)
- 5. Receiver Enable. The serial channel receiver operation may be enabled or disabled by setting or clearing bit 0 of WR3. (See Appendix A for WR3 details.)
- 6. Transmitter Character Length. This parameter sets the length of transmitted characters to 5, 6, 7, or 8 bits. This parameter is specified by bits 5 and 6 of WR5. (See Appendix A for WR5 details.) Characters of less than 5 bits in length may be transmitted by setting the transmitted length to five bits (set bits 5 and 6 of WR5 to 1).

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The character data byte. The Dits APPLICATIONS Is sed in Appendix b. Figure 5 be transmitted must be right justified in the data byte, the next three bits must be set to 0 and all remaining bits must be set to 1. The following table illustrates the data formats for transmission of 1 to 5 bits of data:

To shorth or admir latency, the 8274 can D7 D6 D5 D4 D3 D2 D1 D0 Bits Transmitted -nevo answards on asm (Character Length) head is required to detarnOneOtio chust of 1 1 10 0 0 0 0 0 c c c c mark 2 courrecter as 1 1 000000ccc coefdees 2 3 boo "rectory 1 0 0 0 0 0 colored cib and add maint their

0 0 0 c c cac c MS8 and 5vd v [fabition

7. Transmitter Enable. The serial channel transmitter operation may be enabled or disabled by setting or clearing bit 3 of WR5. (See Appendix A for WR5 Channel B Character Available(.sliable

For data transmission via a modem or RS-232-C interface, the following information must also be specified: The formand

- 1. Request to Send/Data Terminal Ready. Must be set to indicate status of data terminal equipment. Request to send is controlled by bit ! of WR5 and data terminal ready is controlled by bit 7. (See Appendix A for WR5 details.)
- 2. Auto Enable. May be set to allow the MPSC to automtically enable the channel transmitter when the clear to send signal is active and to automatically enable the receiver when the carrier detect signal is active. Auto Enable is controlled by bit 5 of WR3. (See Appendix A for WR3 details.)

During initialization, it is desirable to quarantee that the external/status latches reflect the latest interface information. Since up to two state changes are internally stored by the MPSC, at least two Reset External/Status Interrupt commands must be issued. This procedure is most easily accomplished by simply issuing this reset command whenever the pointer register is set during initialization. at dourselet

illustrates typical MPSC initialization parameters for use with this procedure.

call MPSC\$RX\$INIT(41, 1,1,0,1, 3,1,1, 3,1,1,0,1);

initializes the 8274 at address 41 as follows:

X16 clock rate Enable transmitter and receiver 1 stop bit Auto enable set Odd parity DTR and RTS set 8-bit characters (Tx and Rx) Break transmission disabled

Figure 5. Sample 8274 initialization procedure for polled officeration, no decembed at partiages application. For example, the receiv-

Polled Operation and and to notestmens of the

In the polled mode, the processor must monitor the MPSC status by testing the appropriate bits in the read register. Data available, status, and error conditions are represented in RRO and RR1 for channels A and B. An example of MPSC polled transmitter/receiver routines are given in Appendix B. The following routines are detailed: of betrogen ers anditaredd to teber

1. MPSC\$POLL\$RCV\$CHARACTER - This procedure receives a character from the serial data link. The routine waits until the character available flag in RRO has been set. When this flag indicates that a character is available, RRI is checked for errors (overrun, parity, or framing). If an error is detected, the character in the MPSC receive buffer must be read and discarded and the error routine (RECEIVESERROR) is called. If no receive errors have been detected, the character is input from the 8274 data port and returned to the calling program.

MPSC\$POLL\$RCV\$CHARACTER requires three parameters - the address of the 8274 channel data port (data\$port), the address of the 8274 channel command port (cmd\$port), and the address of a byte variable in which to store the received character (character\$ptr).

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- 2. MPSC\$POLL\$TRAN\$CHARACTER This procedure transmits a character to the serial data link. The routine waits until the transmitter buffer empty flag has been set in RRO before writing the character to the 8274.

  MPSC\$POLL\$TRAN\$CHARACTER requires three parameters the address of the 8274 channel data port (data\$port), the address of the 8274 channel command port (cmd\$port), and the character of data that is to be transmitted (character).
- 3. RECEIVE\$ERROR This procedure processes receiver errors. First, an Error Reset command is written to the affected channel. All additional error processing is dependent on the specific application. For example, the receiving device may immediately request retransmission of the character or wait until a message has been completed. RECEIVE\$ERROR requires two parameters the address of the affected 8274 command port (cmd\$port) and the error status (status) from 8274 register RR1.

#### Interrupt Driven Operation signske nA .8 bas

In an interrupt driven environment, all based receiver operations are reported to the system processor by means of interrupts. Once a character has been received and assembled, the MPSC interrupts the system processor. The system processor must then read the character from the MPSC data buffer and clear the current interrupt. During transmission, the system processor starts serial I/O by writing the first character of a message to the MPSC. The MPSC interrupts the system processor whenever the next character is required (i.e., when the transmitter buffer is empty) and the processor responds by writing the next character of the message to the MPSC data port for the appropriate channel. ASS and

By using interrupt driven I/O, the MPSC proceeds independently of the system processor, signalling the processor only when characters are required for transmission, when characters are received from the data link, or when errors occur. In this manner, the system processor may continue execution of other tasks while serial I/O is performed concurrently.

#### Interrupt Configurations

The 8274 is designed to interface to 8085and 8086-type processors in much the same manner as the 8259A is designed. When operating in the 8085 mode, the 8274 causes a "call" to a prespecified interrupt service routine location. In the 8086 mode, the 8274 presents the processor with a one-byte interrupt type number. This interrupt type number is used to "vector" through the 8086 interrupt service table. In either case, the interrupt service address or interrupt type number is specified during MPSC initialization.

To shorten interrupt latency, the 8274 can be programmed to modify the prespecified interrupt vector so that no software overhead is required to determine the cause of an interrupt. When this "status affects vector" mode is enabled, the following eight interrupts are differentiated automatically by the 8274 hardware:

- 1. Channel B Transmitter Buffer Empty
- 2. Channel B External/Status Transition
- 3. Channel B Character Available
- 4. Channel B Receive Error as many sist and
- 5. Channel A Transmitter Buffer Empty
- 6. Channel A External/Status Transition
- 7. Channel A Character Available
- 8. Channel A Receive Error ypsey fantmas

#### Interrupt Sources/Priorities

The 8274 has three interrupt sources for each channel:

- 1. Receiver (RxA, RxB). An interrupt is initiated when a character is available in the receiver buffer or when a receiver error (parity, framing, or overrun) is detected.
- 2. Transmitter (TxA, TxB). An interrupt is initiated when the transmitter buffer is empty and the 8274 is ready to accept another character for transmission.
- External/Status (ExTA, ExTB). An interrupt is initiated when one of the external/status conditions (CD, CTS, SYNDET, BREAK) changes state.

The 8274 supports two interrupt priority orderings (selectable during MPSC initialization) as detailed in Appendix A, WR2, CH-A.

Interrupt Initialization A RAHDE BY I BORRES SAM ...

In addition to the initialization parameters required for polled operation, the following parameters must be supplied to the 8274 to specify interrupt operation:

- Transmit Interrupt Enable. Transmitter buffer empty interrupts are separately enabled by bit 1 of WR1. (See Appendix A for WR1 details.)
- 2. Receive Interrupt Enable. Receiver interrupts are separately enabled in one of three modes: a) interrupt on first received character only and on receive errors (used for message oriented transmission systems), b) interrupt on all received characters and on receive errors, but do not interrupt on parity errors, and c) interrupt on all received characters and on receive errors (including parity errors). The ability to separately disable parity interrupts can be extremely useful when transmitting messages. Since the parity error bit in RR1 is latched, it will not be reset until an error reset operation is performed. Therefore, the parity error bit will be set if any parity errors were detected in a multi-character message. If this mode is used, the serial I/O software must poll the parity error bit at the completion of a message and issue an error reset if appropriate. The receiver interrupt mode is controlled by bits 3 and 4 of WR1. (See Appendix A for WR1 details.)
- External/Status Interrupts. External/Status interrupts can be separately enabled by bit 0 of WR!. (See Appendix A for WR! details.)
- Interrupt Vector. An eight-bit interrupt service routine location (8085) or interrupt type (8086) is specified through WR2 of channel B. (See Appendix A for WR2 details). Table 3 lists interrupt vector addresses generated by the 8274 in the "status affects vector" mode.
- Status Affects Vector Mode. The 8274 will automatically modify the interrupt vector if bit 3 of WRl is set. (See Appendix A for WRl details.)

- 6. System Configuration. Specifies the 8274 data transfer mode. Three configuration modes are available: a) interrupt driven operation for both channels, b) DMA operation for both channels, and c) DMA operation for channel A, interrupt driven operation for channel B. The system configuration is specified by means of bits 0 and 1 of WR2 (channel A). (See Appendix A for WR2 details).
- Interrupt Priorities. The 8274 permits software specification of receive/ transmit priorities by means of bit 2 of WR2 (channel A). (See Appendix A for WR2 details.)
- 8. Interrupt Mode. Specifies whether the MPSC is to operate in a non-vectored mode (for use with an external interrupt controller), in an 8086 vectored mode, or in an 8085 vectored mode. This parameter is specified through bits 3 and 4 of WR2 (channel A). (See Appendix A for WR2 details.)

Table 3. MPSC Generated Interrupt Vectors in "Status Affects Vector" Mode

V7 V6 V5 V4 V3	V2 V1 \	Original Vector (specified during initialization)		
8086 Interrupt T	ype	19	8085 Interrupt Location	Interrupt Condition
V7 V6 V5 V4 V3	0 0	0	V7 V6 V5 0 0 0 V1 V0	Channel B Transmitter Buffer Empty
V7 V6 V5 V4 V3	0 0	1	V7 V6 V5 0 0 1 V1 V0	Channel B External/Status Change
V7 V6 V5 V4 V3	0 1	0	V7 V6 V5 0 1 0 V1 V0	Channel B Receiver Character Available
V7 V6 V5 V4 V3	0 1	1	V7 V6 V5 0 1 1 V1 V0	Channel B Receive Error
V7 V6 V5 V4 V3	1 0	0	V7 V6 V5 1 0 0 V1 V0	Channel A Transmitter Buffer Empty
V7 V6 V5 V4 V3	1 0	1	V7 V6 V5 1 0 1 V1 V0	Channel A External/Status Change
V7 V6 V5 V4 V3	1 1	0	V7 V6 V5 1 1 0 V1 V0	Channel A Receiver Character Available
V7 V6 V5 V4 V3	1 1	1	V7 V6 V5 1 1 1 V1 V0	Channel A Receive Error

An MPSC interrupt initialization procedure (MPSC\$INT\$INIT) is listed in Appendix C.

Interrupt Service Routines and meday

Appendix C lists four interrupt service procedures, a buffer transmission procedure, and a buffer reception procedure that illustrate the use of the 8274 in interrupt driven environments. Use of these procedures assumes that the 8086/8088 interrupt vector is set to 20H and that channel B is used with the "status affects vector" mode enabled.

- 1. TRANSMIT\$BUFFER This procedure begins serial transmission of a data buffer. Two parameters are required a pointer to the buffer (buf\$ptr) and the length of the buffer (buf\$length). The procedure first sets the global buffer pointer, buffer length, and initial index for the transmitter interrupt service routine and initiates transmission by writing the first character of the buffer to the 8274. The procedure then enters a wait loop until the I/O completion status is set by the transmit interrupt service routine (MPSC\$TRANSMIT\$CHARACTER\$INT).
- 2. RECEIVESBUFFER This procedure inputs a line (terminated by a line feed) from a serial I/O port. Two parameters are required - a pointer to the input buffer (buf\$ptr) and a pointer to the buffer length variable (buf\$length\$ptr). The buffer length will be set by this procedure when the complete line has been input. The procedure first sets the global buffer pointer and initial index for the receiver interrupt service routine. RECEIVE\$BUFFER then enters a wait loop until the I/O completion status is set by the receive interrupt routine (MPSC\$RECEIVE\$CHAR-ACTERSINT).

- 3. MPSC\$RECEIVE\$CHARACTER\$INT This procedure is executed when the MPSC Tx buffer empty interrupt is acknowledged. If the current transmit buffer index is less than the buffer length, the next character in the buffer is written to the MPSC data port and the buffer pointer is updated. Otherwise the transmission complete status is posted.
- 4. MPSC\$RECEIVE\$CHARACTER\$INT This procedure is executed when a character has been assembled by the MPSC and the MPSC has issued a character available interrupt. If no input buffer has been set up by RECEIVE\$BUFFER, the character is ignored. If a buffer has been set up, but it is full, a receive overrun error is posted. Otherwise, the received character is read from the MPSC data port and the buffer index is updated. Finally, if the received character is a line feed, the reception complete status is posted.
- 5. RECEIVESERRORSINT This procedure is executed when a receive error is detected. First, the error conditions are read from RR1 and the character currently in the MPSC receive buffer is read and discarded. Next, an Error Reset command is written to the affected channel. All additional error procession is application dependent.
- 6. EXTERNAL\$STATUS\$CHANGE\$INT This procedure is executed when an external status condition change is detected. The status conditions are read from RRO and a Reset External/Status Interrupt command is issued. Further error processing is application dependent.

Appendix A for WRI details.)

4. Data Link Interface

Serial Data Interface as mi beau for I brammo 3

Each serial I/O channel within the 8274

MPSC interfaces to two data link lines -one line for transmitting data and one for
receiving data. During transmission, characters are converted from parallel data
format (as supplied by the system processor
or DMA device) into a serial bit stream
(with START and STOP bits) and clocked out
on the TxD pin. During reception, a serial
bit stream is input on the RxD pin, framing
bits are stripped out of the data stream,
and the resulting character is converted to
parallel data format and passed to the system processor or DMA device.

Data Clocking

As discussed previously, the frequency of data transmission/reception on the data link is controlled by the MPSC clock in conjunction with the programmed clock divider (in register WR4). The 8274 is designed to permit all four serial interface lines (TxD and RxD for each channel) to operate at different data rates. Four clock input pins (TxC and RxC for each channel) are available for this function. Note that the clock rate divider specified in WR4 is used for both RxC and TxC on the appropriate channel are independent.

data when the transmit forthood meboM

The following four modem interface signals may be connected to the 8274:

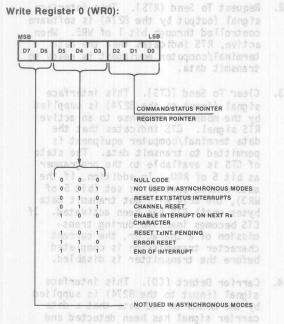
1. Data Terminal Ready (DTR). This interface signal (output by the 8274) is software controlled through bit 7 of WR5. When active, DTR indicates that the data terminal/computer equipment is active and ready to interact with the data communications channel. In addition, this signal prepares the modem for connection to the communication

channel and maintains connections previously established (e.g., manual call origination).

- Request To Send (RTS). This interface signal (output by the 8274) is software controlled through bit 1 of WR5. When active, RTS indicates that the data terminal/computer equipment is ready to transmit data.
- 3. Clear To Send (CTS). This interface signal (input to the 8274) is supplied by the modem in response to an active RTS signal. CTS indicates that the data terminal/computer equipment is permitted to transmit data. The state of CTS is available to the programmer as bit 5 of RRO. In addition, if the auto enable control is set (bit 5 of WR3), the 8274 will not transmit data bytes until RTS has been activated. If CTS becomes inactive during transmission of a character, the current character transmission is completed before the transmitter is disabled.
- 4. Carrier Detect (CD). This interface signal (input to the 8274) is supplied by the modem to indicate that a data carrier signal has been detected and that a valid data signal is present on the RxD line. The state of CD is available to the programmer as bit 3 of RRO. In addition, if the auto enable control is set (bit 5 of WR3), the 8274 will not enable the serial receiver until CD has been activated. If the CD signal becomes inactive during reception of a character, the receiver is disabled, and the partially received character is lost.

In addition to the above modem interface signals, the 8274 SYNDET input pin for channel A may be used as a general purpose input in the asynchronous communication mode. The status of this signal is available to the programmer as bit 4 of status register RRO.

Appendix A: Command/Status Details for Asynchronous Communication



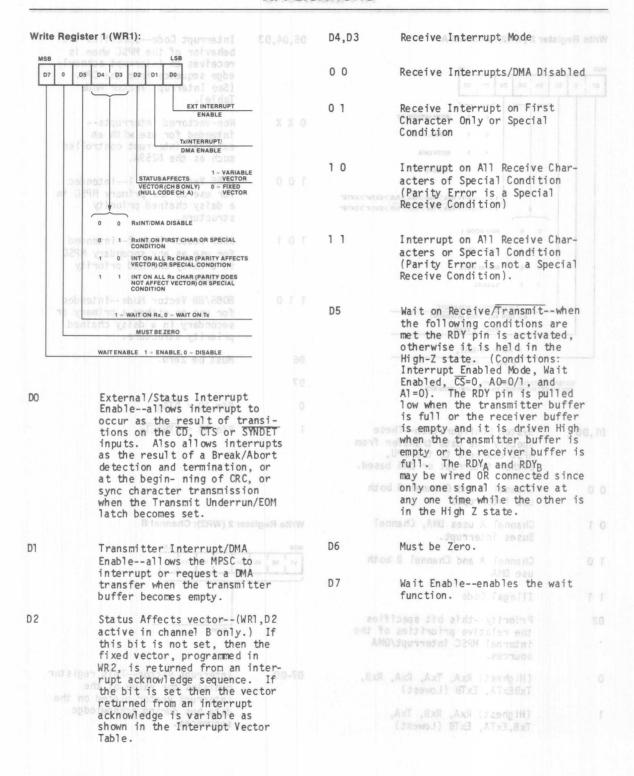
- D2, D1, D0 Command/Status Register Pointer bits determine which writeregister the next byte is to be do and written into, or which read-inu register the next byte is to be read from. After reset, the first byte written into either channel goes into WRO. Following a read or write to any register (except WRO) the pointer will point to WRO.
- D5,D4,D3 Command bits determine which of the basic seven commands are to be performed. register RRO.

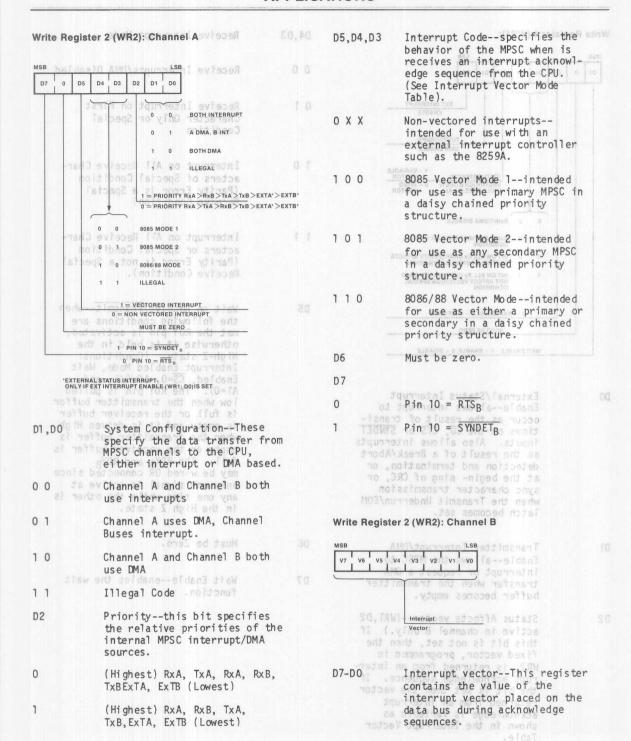
channel A may be used as a general purpose

- Command O Null--has no effect.
- Command 1 Not used in asynchronous modes.
- Command 2 Reset External/Status Inter--- rupts--resets the latched status bits of RRO and re-enables them, allowing sinterrupts to occur again.
- Command 3 Channel Reset--resets the Latched Status bits of RRO, the Targe interrupt prioritization logic and all control registers for the channel. Four extra system clock cycles should be allowed for MPSC reset time before any additional commands or controls are written into the channel.
- Command 4 Enable Interrupt on Next Receive Character--if the Interrupt on First Receive Character mode is selected, this command reactivates that mode after each complete message is received to prepare the MPSC for the next message.
- Command 5 Reset Transmitter Interrupt Pending--if The Transmit state of the state Interrupt mode is selected, the MPSC automatically interrupts data when the transmit buffer about becomes empty. When there are no more characters to be sent, issuing this command prevents further transmitter interrupts until the next character has been completely sent.

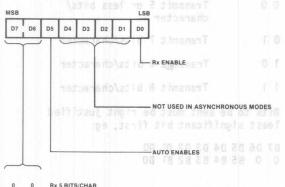
saftware controlled through bit 7 of

- Command 6 Error Reset--error latches, Parity and Overrun errors in - tobs nRR1 are reset and fact nummos at ab
- Command 7 End of Interrupt -- resets the interrupt-in-service latch of the highest-priority internal device under service.





## Write Register 3 (WR3): 355560 3 mens T



0 1 Rx 7 BITS/CHAR

1 0 Rx 6 BITS/CHAR

Rx 8 BITS/CHAR

DO Receiver Enable--A one enables the receiver to begin. This bit should be set only after the receiver has been initialized.

Auto Enables--A one written to this bit caused CD to be auto-matic enable signal for the receiver and CTC to be an automatic enable signal for the transmitter. A zero written to this bit limits the effect of CD and CTS signals to setting/resetting their corresponding bits in the status register (RRO).

D7,D6 Receive Character length

O O Receive 5 Data bits/character

O 1 Receive 7 Data bits/character

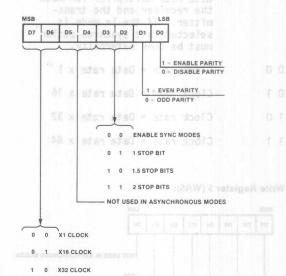
1 O Receive 6 Data bits/character

1 1 Receive 8 Data bits/character

2 is specified. This bit is always zero in Channel 8.

Transmit Buffer Empty--Ihis bit is set whenever the transmit buffer is empty except when CRC characters are being sent in a synchronous mode. This bit is reset when the transmit buffer is loaded. This bit is set after an MAPC reset.

## Write Register 4 (WR4): 192--- short short 3



Parity—a one in this bit causes a parity bit to be added to the programmed number of data bits per character for both the transmitted and received character. If the MPSC is programmed to receive 8 bits per character, the parity bit is not transferred to the microprocessor. With other receiver character lengths, the parity bit is transferred to the microprocessor.

D1 Even/Odd Parity -- if parity is enabled, a one in this bit causes the MPSC to transmit and expect even parity, and zero causes it to send and expect odd parity.

D3,D2 Stop Bits

1 X64 CLOCK

0 0 Selects synchronous modes.

0 1 Async mode, 1 stop bit/character

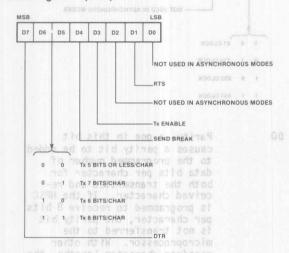
1 0 Async mode, 1-1/2 stop bits/ character

1 1 Async mode, 2 stop bits/character

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D7,D6	Clock modeselects the clock/ data rate multiplier for both the receiver and the trans- mitter. If the lx mode is selected, bit synchronization must be done externally.
0 0	Clock rate = Data rate x 1
0 1	Clock rate = Data rate x 16
1 0	Clock rate = Data rate x 32
11	Clock rate = Data rate x 64

#### Write Register 5 (WR5): 212 MOTES



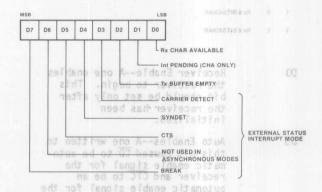
D1 Request to Send—a one in this bit forces the  $\overline{\text{RTS}}$  pin active (10w) and zero in this bit forces the  $\overline{\text{RTS}}$  pin inactive (high).

D3 Transmitter Enable—a zero in this bit forces a marking state on the transmitter output. If this bit is set to zero during data or sync character transmission, the marking state is entered after the character has been sent. If this bit is set to zero during transmission of a CRC character, sync or flag bits are substituted for the remainder of the CRC bits.

D4 Send Break--a one in this bit forces the transmit data low.
A one in this bit allows normal transmitter operation.

D6,D5	Transmit Character length	
0 0	Transmit 5 or less bits/ character	
0 1	Transmit 7 bits/character	
1 0	Transmit 6 bits/character	
11	Transmit 8 bits/character	
	sent must be right justified ificant bit first, eg:	
	4 D3 D2 D1 D0 4 B3 B2 B1 B0	

#### Read Register 0 (RR0):



DO Receive Character Available-this bit is set when the receive FIFO contains data and is proportion of the reset when the FIFO is empty.

Interrupt Pending—This Interrupt—Pending bit is reset when and EO1 command is issued and there is no other interrupt request pending at that time.

In vector mode this bit is set at the falling edge of the second INTA in an INTA cycle for an internal interrupt request. In non-vector mode, this bit is set at the falling edge of RD input after pointer 2 is specified. This bit is always zero in Channel B.

D2 Transmit Buffer Empty—This bit is set whenever the transmit buffer is empty except when CRC characters are being sent in a synchronous mode. This bit is reset when the transmit buffer is loaded. This bit is set after an MPSC reset.

etwalke made this bit is sat	tains the state of the CD pitains the		
D3	Carrier Detect This bit con-		
	tains the state of the CD pin	ceive mode, this bit	is setz di
	at the time of the last change	when a Break sequence	(nullective
	of any of the External/Status	character plus framin	g error)
	bits (CD, CTS, Sync/Hunt,	is detected in the da	ta berosal
	Break/Abort, or Tx Underrun/	stream. The External	
	EOM). Any change of state of	interrupt, if enabled	
	the CD pin causes the CD bit to	when break is detected	
	be latched and causes an Ex-	interrupt service rou	
1,000	ternal/Status interrupt. This	issue the Reset Exter	
	bit indicates current state of	Interrupt command (WR	
	the CD pin immediately follow-	2) to the break detec	tion logic
	ing a Reset External/Status	so the Break sequence	termina-
	Interrupt command.	end solition can be recognized	tosff bas

SYNDET -- In asynchronous modes. 00-70 D4 the operation of this bit is similar to the CD status bit, except that it shows the state of the SYNDET input. Any High-to-Low transition on the SYNDET pin sets this bit, and causes an External/Status interrupt (if enabled). The Reset External/Status Interrupt command is issued to clear the interrupt. A Low-to-High transition clears this bit and sets the External/Status interrupt. When the External/Status interrupt is set by the change in state of any other input or condition, this bit shows the inverted state of the SYNDET pin at time of the change. This bit must be read immediately following a Reset External/Status Interrupt command to read the current state of the SYNDET input.

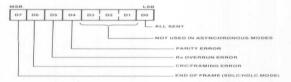
Clear to Send--this bit contains the inverted state of the CTS pin at the time of the last change of any of the External/ Status bits (CD, CTS, Sync/ Hunt, Break/Abort, or Tx Underrun/EOM). Any change of state of the CTS pin causes the CTS bit to be latched and causes an External/Status interrupt. This bit indicates the inverse of the current state of the CTS pin immediately following a Reset External/Status Interrupt command.

D5

.... DIE ASVACHIONOUS Break-in the ASVACHIONO

The Break bit is reset when the termination of the Break sequence is detected in the incoming data stream. The termination of the Break sequence also causes the External/Status interrupt to be set. The Reset External/Status Interrupt command must be issued to enable the break detection logic to look for the next Break sequence. A single extraneous null character is present in the receiver after the termination of a break: it should be read and discarded.

#### Read Register 1 (RR1)

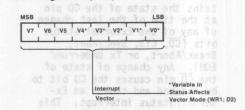


All sent -- this bit is set when all characters have been sent, in asynchronous modes. It is reset when characters are in the transmitter, in asynchronous modes. In synchronous modes, this bit is always set.

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- D4 Parity Error--If parity is enabled, this bit is set for received characters whose parity does not match the programmed sense (Even/Odd). This bit is latched. Once an error occurs, it remains set until the Error Reset command is written. I dans to diquired at
- D5 Receive Overrun Error--this bit indicates that the receive FIFO has been overloaded by the receiver. The last character in the FIFO is overwritten and flagged with this error. Once the overwritten character is read, this error condition is latched until reset by the Error Reset command. If the MPSC is in the status affects vector mode, the overrun causes a special Receive Error Vector.
- D6 Framing Error--In async modes, a one in this bit indicates a receive framing space error. It can be reset by issuing an Error Reset command. an ad b fuel at the sand

Read Register 2 (RR2): -- to at all the install



RR2

Channel B D7-D0 Interrupt vector--contains the interrupt vector programmed into WR2. If the status affects vector mode is selected, it contains the modified vector. (See WR2) RR2 contains the modified vector for the highest priority interrupt pending. If no interrupts are pending, the variable bits in the vector are set to one.

```
APPENDIX B: MPSC Polled Transmit/Receive Character Routines AAD WORLD AD ROUGH
MPSC$RX$INIT: procedure (cmd$port,
                          clock$rate,stop$bits,parity$type,parity$enable,
                          rx$char$length,rx$enable,auto$enable,
                          tx$char$length,tx$enable,dtr,brk,rts);
  declare cmd$port
                          byte.
        clock$rate
                          byte,
        stop$bits
                          byte,
                          while (input (cmoSport) and charSavail) <> 0 do; end; styd
        parity$type
        parity$enable
                          byte,
        rx$char$length
                          byte,
        rx$enable \* I8byte, inlog *\
        auto$enable
                          byte,
        tx$char$length
                          byte.
    * OtxSenable of resobyte; beer *\
        /* clear, etvdiver errors */ tb
/* lieve brkostado on - nibyte, rome */
                          byte:
  /* good return - character avail */
  output(cmd$port) = 30H;
                                  /* channel reset */
                                 /* point to WR4 */ #RETDARAHDEVDAR JJOSEDESM Bas
  output(cmd$port) = 14H;
  /* set clock rate, stop bits, and parity information */
  output(cmd$port) = shl(clock$rate,6) or shl(stop$bits,2) or shl(parity$type,1)
                   or parity$enable;
                   MPSCSPOLLSTRANSCHARROTER: procedure(dataSport,cmdSport,character)
                                  /* point to WR3 */
  output (cmd$port) = 13H;
  /* set up receiver parameters */
  output(cmd$port) = sh1(rx$char$length,6) or rx$enable or sh1(auto$enable,5);
  output(cmd$port)=15H;
                                  /* point to WR5 */
  declare txSbufferSempty literally "4"; * set up transmitter parameters */
  output(cmd$port)=shl(tx$char$length,5) or shl(tx$enable,3) or shl(dtr,7)
                   or shl(brk,4) or shl(rts;1); one refitte buffet buffet for shl(brk,4) or shl(rts;1);
  end MPSC$RX$INIT:
                                                            /* output character */
```

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```
MPSC$POLL$RCV$CHARACTER: procedure(data$port,cmd$port,character$ptr) byte; X10089948
    declare data$port
                                                    byte,
                      cmd$port
                                                    byte,
                      character$ptr pointer,
                      character based character$ptr byte, 51835015
                                               rxScharSlength, rxSenable, auto; stydle,
                      status
                                                   literally '1', literally '70H';
    declare char$avail
                      rcv$error
     /* wait for input character ready */
    while (input(cmd$port) and char$avail) <> 0 do; end;
    /* check for errors in received character */
                                                                                                  /* point to RRl */
    output(cmd$port)=1;
    if (status:=input(cmd$port) and rcv$error)
         then do;
             character=input(data$port);
                                                                                                   /* read character to clear MPSC */
             call RECEIVESERROR (cmdSport, status);
                                                                                                   /* clear receiver errors */
            return 0;
                                                                                                   /* error return - no character avail */
             end;
         else do;
             character=input(data$port);
              return OFFH;
                                                                                                     /* good return - character avail */
             end;
end MPSC$POLL$RCV$CHARACTER;
           output(cmosport)=isa;
/* set clock rate, stop bits, and parity information */
output(cmdSport)=shl(clockSrate,6) or shl(stopSbits,2) or shl(parityStype,1)
MPSC$POLL$TRAN$CHARACTER: procedure(data$port,cmd$port,character);
                                                                      output(cmdSport)=13H; /* point to WR3 */
/* set up receiver parameters */
    declare data$port
                                                      byte,
                (dcmdSport) = all(rxScharSlength, so (a.rxSenatSlength, so ) lde=(araSport) | de=(araSport) | 
                      character
                                                      byte;
                                                                       output(cmdSport)=15H; /* point to WR5 */
/* set up transmitter parameters */ ;'b' yll
    declare tx$buffer$empty literally '4';
                                           output(cmdSport) =sh1(txScharSlength, 5) or sh1(txSenable, 3) or
    /* wait for transmitter buffer empty */ a) Ida to (4, Mad) Ida to
    while not (input(cmd$port) and tx$buffer$empty) do; end;
     /* output character */
    output(data$port) = character;
end MPSC$POLL$TRAN$CHARACTER:
RECEIVE $ERROR: procedure (cmd $port, status);
    declare cmd$port
                                                    byte,
                     status
                                                    byte;
    output(cmd$port) = 30H;
                                                                              /* error reset */
    /* *** other application dependent
                   error processing should be placed here *** */
end RECEIVESERROR:
```

```
TRANSMIT$BUFFER: procedure(buf$ptr,buf$length) # Decode tTWISFETDASANDESVIEDESSEDESM
      declare
              buf$ptr
                                                              pointer,
              buf$length
                                                              byte:
      /* set up transmit buffer pointer and buffer length in global variables for
                  interrupt service */
       tx$buffer$ptr=buf$ptr:
      transmit$length=buf$length;ellud ni seld bns 290m moil research bees *\
       output(data$port) = transmit$buffer(0); /* transmit first character */
      transmit$index=1;ud evieces edabage */ /* first character transmitted */
      /* wait until transmission complete or error detected */ sail soi should */
      while transmit$status = not$complete do; end; beeltent1 = proposado it
      if transmit$status <> complete it is index transmit $ status <> complete it is in it
              then return false:
             else return true:
end TRANSMIT$BUFFER;
RECEIVE$BUFFER: procedure (buf$ptr,buf$length$ptr); aredosind a some not absent a
      declare
             buf$ptr
                                                                 /* Write next character from buffer to MPSC */
              buf$length$ptr pointer (xsbml3imansr) ieliud;imansr==(3roc3sisb) sudjuo
             buf$length old based buf$length$ptr byte; *xebal231manay=xebal231manay
      /* set up receive buffer pointer in global variable for interrupt service */
      rx$buffer$ptr=buf$ptr:
      receiveSindex=0:
      receive$status=not$complete;
                                                                                                                                             /* set status to not complete */
      /* wait until buffer received */
      while receive$status = not$complete do; end; 119441 518050019 :TK1280588828VISOSR
      buf$length=receive$length;
       if receive$status = complete
                                                                                   byte; /* temporary character
              then return true;
              else return false:
end RECEIVESBUFFER:
                                                                                                                                                                   AFRE 01995 AFRE STATES AFRE 01995 ```

```
MPSC$RECEIVE$CHARACTER$INT: procedure interrupt 22H; ud) = rubecord : 99990 ug2TIM2NAST
  /* ignore input if no open buffer */
  if receive$status <> not$complete then return;
  /* check for receive buffer overrun */
  if receive$index = 128 in defer length in 821 = xsindex if
    then receive$status=overrun:
   interrupt service */
    else do:
      /* read character from MPSC and place in buffer - note that the
        parity of the character must be masked off during this step if
  the character is less than 8 bits (e.g., ASCII) */
      receive$buffer(receive$index),character=input(data$port) and 7FH;
    receiveSindex=receiveSindex+1: /* update receive buffer index */
     /* check for line feed to end line */ statement from the */
      if character = line$feed shee tob stelomopeton = autotactinanest elidw
       then do; receive$length=receive$index; receive$status=complete; end;
    end.
end MPSC$RECEIVE$CHARACTER$INT:
MPSC$TRANSMIT$CHARACTER$INT: procedure interrupt 20H:
  /* check for more characters to transfer */d rigglud) elubecolo :8239U823VISCAR
  if transmit$index < transmit$length
     /* write next character from buffer to MPSC */ 1950100
     transmit$index=transmit$index+1; /* update transmit buffer index */
   else transmitSstatus=complete:sv ladolp al refaiog relitud evicoes qui see *\
end MPSC$TRANSMIT$CHARACTER$INT;
        /* set status to not complete */
RECEIVESERRORSINT: procedure interrupt 23H; ejelomoolion = autolelavieser elidw
  declare
                                /* temporary character storage */
   temp
                       byte:
 output(cmd$port)=1;
                                /* point to RR1 */
  receive$status=input(cmd$port);
                                /* discard character */
  temp=input(data$port);
 output(cmd$port)=error$reset; /* send error reset */
  /* *** other application dependent
        error processing should be placed here *** */
end RECEIVE$ERROR$INT;
EXTERNAL$STATUS$CHANGE$INT: procedure interrupt 21H:
  transmit$status=input(cmd$port)
                                   /* input status change information */
 output(cmd$port)=reset$ext$status;
  /* *** other application dependent
        error processing should be placed here *** */
end EXTERNAL$STATUS$CHANGE$INT:
   AFN: 01995A
                                   2-339
```

```
APPENDIX C: Interrupt Driven Transmit/Receive Software
     eclare
/* global variables for buffer manipulation */
declare
     rx$buffer$ptr === * pointer. /* pointer to receive buffer */
      receive$buffer based rx$buffer$ptr(128) byte,
      receive$status byte initial(0), /* indicates receive buffer status */
      tx$buffer$ptr \* psil a pointer, a aid-1 *\ /* pointer to transmit buffer */
      transmit$buffer based tx$buffer$ptr(128) byte,
      transmit$status days byte initial(0), /* indicates transmit buffer status */
      transmit$index and and byte, and bid-1 */* current index into transmit buffer */
transmit$lengthe asend byte, and bid-1 */* length of buffer to be transmitted */
      cmd$port literally '43H', '42H', b$cmd$port literally '43H', '42H', b$cmd$port literally '43H', '43H', '43H', '60H', '60H
      channel$reset
   literally '18H',
  literally '30H',
      error$reset
  literally 10H;
      reset$ext$status
   /* point to WR3 */
             /* set up rec iver parameters */
output (bscmdsort) = shl(rx$char$length,6) or rx$enable or shl(auto$enable,5);
```

```
MPSC$INT$INIT: procedure (clock$rate, stop$bits, parity$type, parity$enable, GMagga
  rx$char$length,rx$enable,auto$enable,
  tx$char$length,tx$enable,dtr,brk,rts,
  ext$en,tx$en,rx$en,stat$affects$vector,
  config,priority,vector$int$mode,int$vector);
   /* global variables for buffer manipulation
       declare
                   clock$rate | byte, | /* 2-bit code for clock rate divisor */ |
  stop$bits byte, /* 2-bit code for number of stop bits */
parity$type byte, /* 1-bit parity type */
parity$enable byte, /* 1-bit parity enable */
rx$char$length byte, /* 2-bit receive character length */
                  rx$enable byte, /* 1-bit receiver enable */
auto$enable flag */ 1-bit auto enable flag */
  byte,
  byte, 2-bit transmit character length */ said
                   txScharSlength
/* 1-bit transmitter enable */ dataimens of the status of DTR pin */ on the status of 
* bejimebrki ed of reflucbyte, ignel */ /* 1-bit data link break enable !*/ imanari
  byte,
  /* 1-bit status of RTS pin */
                   rts
  byte,
  /* 1-bit external/status enable */1002550
                   ext$en
  byte,
  /* 1-bit Tx interrupt enable */
                   tx$en
  byte,
  /* 2-bit Rx interrupt enable/mode */ bmoss
                   rxSen
                   stat$aff$vector byte,
  /* 1-bit status affects vector flag */
                   config
  byte,
  /* 2-bit system config - int/DMA */
  /* 1-bit priority flag */
                   priority
  byte,
                   vectorSintSmode byte,
  /* 3-bit interrupt mode code */
                   int$vector
  byte;
  /* 8-bit interrupt type code */
       output(b$cmd$port) = channel$reset;
  /* channel reset */
       output (b$cmd$port) = 14H:
  /* point to WR4 */
      /* set clock rate, stop bits, and parity information */
output(b$cmd$port)=shl(clock$rate,6) or shl(stop$bits,2) or shl(parity$type,1)
  or parity$enable;
       output(b$cmd$port)=13H;
   /* point to WR3 */
       /* set up receiver parameters */
       output(b$cmd$port)=shl(rx$char$length,6) or rx$enable or shl(auto$enable,5);
       output(b$cmd$port)=15H:
  /* point to WR5 */
       /* set up transmitter parameters */
       output(b$cmd$port)=shl(tx$char$length,5) or shl(tx$enable,3) or shl(dtr,7)
   or shl(brk,4) or shl(rts,1);
       output (b$cmd$port) = 12H;
  /* point to WR2 */
       /* set up interrupt vector */
       output (b$cmd$port) = int$vector;
       output(a$cmd$port)=12H;
  /* point to WR2, channel A */
       /* set up interrupt modes */
       output(a$cmd$port)=shl(vector$int$mode,3) or shl(priority,2) or config;
       output(b$cmd$port)=11H;
  /* point to WRl */
       /* set up interrupt enables */
       output(b$cmd$port)=shl(rx$en,3) or shl(stat$aff$vector,2) or shl(tx$en,1)
  or extSen:
       end MPSCSINTSINIT:
```

### Appendix D

### Application Example Using SDK-86

This application example shows the 8274 in simple iAPX-86/88 system. The 8274 controls two separate asynchronous channels using its internal interrupt controller to request all data transfers. The 8274 driver software is described which transmits and receives data buffers provided by the CPU. Also, status registers are maintained in system memory to allow the CPU to monitor progress of the buffers and error conditions.

### THE HARDWARE INTERFACE

Nothing could be easier than the hardware design of an interrupt-driven 8274 system. Simply connect the data bus lines, a few bus control lines, supply a timing clock for baud rate and, voila, it's done! For this example, the ubiquitous SDK-86 is used as the host CPU system. The 8274 interface is constructed on the wire-wrap area provided. While discussing the hardware interface, please refer to Diagram 1.

Placing the 8274 on the lower 8-bits of the 8086 data bus allows byte-wide data transfers at even I/O addresses. For simplicity, the 8274's CS/ input is generated by combining the M-IO/ select line with address line A7 via a 7432. This places the 8274 address range in multiple spots within the 8086 I/O address space. (While fine for this example, a more complete address decoding is recommended for actual prototype systems.) The 8086's Al and A2 address lines are connected to the AO and Al 8274 register select inputs respectively. Although other port assignments are possible because of the overlapping address spaces, the following I/O port assignments are used in this example:

| Port Function    | I/O Address |
|------------------|-------------|
| Data channel A   | 0000H       |
| Command/status A | 0002H       |
| Data channel B   | 0004H       |
| Command/status B | 000 6H      |

To connect the 8274's interrupt controller into the system an inverter and pull-up resistor are needed to convert the 8274's active-low interrupt request output, IRQ, into the correct polarity for the 8086's INTR interrupt input. The 8274 recognizes interrupt acknowledge bus cycles by connecting the INTA (INTerrupt Acknowledge) lines of the 8274 and 8086 together.

The 8274 ReaD and WRite lines directly connect to the respective 8086 lines. The RESET line requires an inverter. The system clock for the 8274 is provided by the PCLK (peripheral clock) output of the 8284A clock generator.

On the 8274's serial side, traditional 1488 and 1489 RS-232 drivers and receivers are used for the serial interface. The onboard baud rate generator supplies the channel baud rate timing. In this example, both sides of both channels operate at the same baud rate although this certainly is not a requirement. (On the SDK-86, the baud rate selection is hard-wired thru jumpers. A more flexible approach would be to incorporate a 8253 Programmable Interval Timer to allow software-configurable baud rate selection.)

That's all there is to it. This hardware interface is completely general-purpose and supports all of the 8274 features except the DMA data transfer mode which requires an external DMA controller. Now let's look at the software interface.

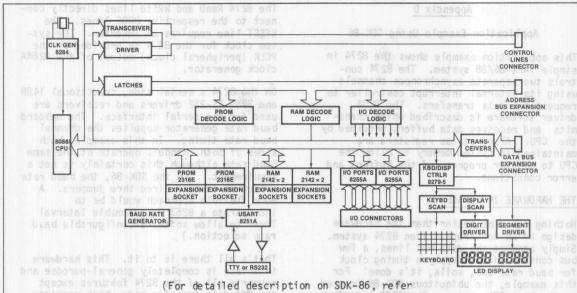
### SOFTWARE INTERFACE

In this example, it is assumed that the 8086 has better things to do rather than continuously run a serial channel. Presenting the software as a group of callable procedures lets the designer include them in the main body of another program. The interrupt-driven data transfers give the effect that the serial channels are handled in the background while the main program is executing in the foreground. There are five basic procedures: a serial channel initialization routine and buffer handling routines for the transmit and receive data buffers of each channel. Appendix D-1 shows the entire software listing. Listing line numbers are referenced as each major routing is discussed.

The channel initialization routine (INITIAL 8274), starting with line #203, simply sets each channel into a particular operating mode by loading the command registers of the 8274. In normal operation, once these registers are loaded, they are rarely changed. (Although this example assumes a simple asynchronous operating mode, the concept is easily extended for the byte and bit-sychronous modes.)

The channel operating modes are contained in two tables starting with line #163. As the 8274 has only one command register per channel, the remaining seven registers are

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(For detailed description on SDK-86, refer to upidu add signals and to SDK-86 MCS-86 System Design Kit Assembly Manual)

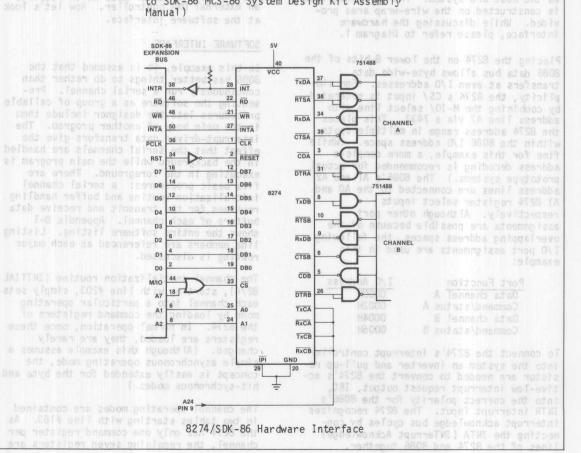


Diagram 1

loaded indirectly through the WRO (Write Register O) register. The first byte of each table entry is the register pointer value which is loaded into WRO and the second byte is the value for that particular register.

The indicated modes set the 8274 for asynchronous operation with data characters 8 bits long, no parity, and 2 stop bits. A X16 baud rate clock is assumend. Also selected is the "interrupt on all RX character" mode with a variable interrupt vector compatible with the 8086/8088. The transmitters are enabled and all model control lines are put in their active state.

In addition to initializing the 8274, this routine also sets up the appropriate interrupt vectors. The 8086 assumes the first 1K bytes of memory contain up to 256 separate interrupt vectors. On the SDK-86 the initial 2K bytes of memory is RAM and therefore must be initialized with the appropriate vectors. (In a prototype system, this initial memory is probably ROM thus the vector set-up is not needed.) The 8274 supplies up to eight different interrupt vectors. These vectors are developed from internal conditions such as data requests, status changes, or error conditions for each channel. The initialization routine arbitrarily assumes that the initial 8274 vector corresponds to 8086 vector location 80H (memory location 200H). This choice is arbitrary since the 8274 initial vector location is programmable.

Finally, the initialization routine sets up the status and flag in RAM. The meaning and use of these locations are discussed later.

Following the initialization routine are those for the transmit commands (starting with line #268). These commands assume that the host CPU has initialized the publically declared variables for the transmit buffer pointer, TX\_POINTER\_CHx, and the buffer length, TX\_LENGTH\_CHx. The transmit command routines simply clear the transmitter empty flag, TX EMPTY CHx, and load the first character of the buffer into the transmitter. It is necessary to load the first character in this manner since transmitter interrupts are generated only when the 8274's transmit data buffer becomes empty. It is the act of becoming empty which generates the interrupt not simply the buffer being empty, thus the transmitter needs one character to start.

The host CPU can monitor the transmitter empty flag, TX\_EMPTY\_CHx, in order to determine when transmission of the buffer is complete. Obviously, the CPU should only call the command routine after first checking that the empty flag is set.

After returning to the main program, all sell transmitter data transfers are handled via the transmitter interrupt service routines starting at lines #360 and #443. These routines start by issuing and End-Of-Interrupt command to the 8274. (This command resets the internal interrupt controller logic of the 8274 for this particular vector and opens the logic for other internal interrupt requests. The routines next check the length count. If the buffer is completely transmitted, the transmitter empty flag. TX EMPTY CHx. is set and a command is issued to the 8274 to reset its interrupt line. Assuming that the buffer is not completely transmitted, the next character is output to the transmitter. In either case, an interrupt return is executed to return to the main CPU program.

The receiver commands start at line #314. Like the transmit commands, it is assumed that the CPU has initialized the receive buffer pointer public variable, RX\_POINTER\_CHx. This variable points to the first location in an empty receive buffer. The command routines clear the receiver ready flag, RX\_READY\_CHx, and then set the receiver enable bit in the 8274 WR3 register. With the receiver now enabled, any received characters are placed in the receive buffer using interrupt-driven data transfers.

The received data service routines, starting at lines #402 and #485, simply place the received character in the buffer after first issuing the EOI command. The character is then compared to a ASCII CR. An ASCII CR causes the routine to set the receiver ready flag, RX\_READY\_CHx, and to disable the receiver. The CPU can interrogate this flag to determine when the buffer contains a new line of data. The receive buffer pointer, RX\_POINTER\_CHx, points to the last received character and the receive counter, RX\_COUNTER\_CHx, contains the length.

That completes our discussion of the command routines and their associated interrupt service routines. Although not used by the commands, two additional service routines are included for completeness. These routines handle the error and status-change interrupt vectors.

The error service routines, starting at lines #427 and #510, are vectored to if a special receive condition is detected by the 8274. These special receive conditions include parity, receiver overrun, and framing errors. When this vector is generated, the error condition is indicated in RRI (Read Register 1). The error service routine issues an EOI command, reads RRI and places it in the ERROR\_MSG\_CHx variable, and then issues a reset error command to the 8274. The CPU can monitor the error message location to detect error conditions. The designer, of course, can supply his own error service routine.

Similarily, the status-change routines (starting lines #386 and #469) are initiated by a change in the modem control status lines CTS/, CD/, or SYNDET/. (Note that WR2 bit 0 controls whether the 8274

generates interrupts based upon changes in these lines. Our WR2 parameter is such that the 8274 is programmed to ignore changes for these inputs.) The service routines simply read RRO, place its contents in the STATUS\_MSG\_CHx variable and then issue a reset external status command. Read Register O contains the state of the modem inputs at the point of the last change.

Well, that's it. This application example has presented useful, abeit very simple, routines showing how the 8274 might be used to transmit and recieve buffers using an asynchronous serial format. Extensions for byte or bit-synchronous formats would require no hardware changes due to the highly programmable nature of the 8294's serial formats.

rate interrupt vectors. On the SDK-88 th initial ZK bytes of memory is RAM and

- TSHO TXBN DAT LEGISTITUTE TO THE TOTAL Appendix D-1

MCS-86 MACRO ASSEMBLER ASYNCB OF Judge of reduce

therefore mapsq be initialized with the appropriate vectors. (In a prototype system, this initial memory is probably ROM

ISIS-II MCS-86 MACRO ASSEMBLER V2.1 ASSEMBLY OF MODULE ASYNCB OBJECT MODULE PLACED IN :F1:ASYNCB. OBJ ASSEMBLER INYOKED BY: ASM86 :F1:ASYNCB. SRC

received character; are placed in the re-

LOC OBJ 24 P SAT OF LINE OF SOURCE ANY STATE AND

vector location 30H (m\*mory location marger program marger program as thin set the re-

8274 initial vector location is ter. With the retirvet now enabled, any

6 ;\* \*
7 ;\* THE 8274 IS INITIALIZED FOR SIMPLE ASYNCHRONOUS SERIAL \*
8 ;\* FORMAT AND VECTORED INTERRUPT-DRIVEN DATA TRANSFERS.
9 ;\* THE INITIALIZATION ROUTINE ALSO LOADS THE 8086'S INTERRUPT \*

10 ;\* VECTOR TABLE FROM THE CODE SEGMENT INTO LOW RAM ON THE
11 ;\* SDK-96. THE TRANSMITTER AND RECEIVER ARE LEFT ENABLED.

12 ;\*

13 ;\* FOR TRANSMIT, THE CPU PASSES IN MEMORY THE POINTER OF A \*

14 ;\* BUFFER TO TRANSMIT AND THE BYTE LENGTH OF THE BUFFER. \*

15 ;\* THE DATA TRANSFER PROCEED USING INTERRUPT-DRIVEN TRANSFERS. \*

16 ;\* A STATUS BIT IN MEMORY IS SET WHEN IF BUFFERS IS EMPTY. \*

17 ;\*

18 ;\* FOR RECEIVE, THE CPU PASSES THE POINTER OF A BUFFER TO FILL. \*

19 ;\* THE BUFFER IS FILLED UNTIL A 'CR\_CHR' CHARACTER IS RECEIVED. \*

20 ;\* A STATUS BIT IS SET AND THE CPU MAY READ THE RX POINTER TO \*

21 ;\* DETERMINE THE LOCATION OF THE LAST CHARACTER. \*

22 ;\* \*
23 ;\* ALL ROUTINES ARE ASSUMED TO EXIST IN THE SAME CODE SEGMENT. \*
24 ;\* CALL'S TO THE SERVICE ROUTINES ARE ASSUMED TO BE "SHORT" OR \*
25 ;\* INTRASFRMENT (ONLY THE PETIEN ADDRESS IP IS ON THE STACK) \*

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| MCS-86 MACRO ASSEMBLER | ASYNCB   |                   |                   |                                     |           | PRGE 2      |
|------------------------|----------|-------------------|-------------------|-------------------------------------|-----------|-------------|
| LOC OBJ                | LINE     | SOURCE            |                   |                                     |           |             |
|                        |          |                   |                   |                                     |           |             |
|                        | 31<br>32 |                   |                   | NAME (SO SO RESIDUE SE SOCIORE)     |           |             |
|                        | 33       |                   |                   | CONTROL START LOCATION RID C        |           |             |
|                        | 34       | ; PUBLIC DECLARE  | ATIONS FOR COMMAN | ID ROUTINES                         |           |             |
|                        | 35<br>36 | DUDI TO           | INITIO 0274       | ; INITIALIZATION ROUTINE            |           |             |
|                        | 37       |                   |                   | ; TX BUFFER COMMAND CHANNEL B       |           |             |
|                        | 38       |                   |                   | ; TX BUFFER COMMAND CHANNEL A       |           |             |
|                        | 39       | PUBLIC            | RX_COMMAND_CHB    | RX BUFFER COMMAND CHANNEL B         |           |             |
|                        | 40       |                   |                   | ; RX BUFFER COMMAND CHANNEL A       |           |             |
|                        | 41       | · PHID TO DECLODE |                   | VARIABLES WIS SECURITION            |           |             |
|                        | 43       | ) FODE TO DECEME  | IIIONS FOR SINIUS | YHKIHDLE3                           |           |             |
|                        | 44       | PUBLIC            | RX_READY_CHB      | ; RX READY FLAG CHB                 |           |             |
|                        | 45       |                   |                   | RX READY FLAG CHA                   |           |             |
|                        | 46<br>47 |                   |                   | TX EMPTY FLAG CHB                   |           |             |
|                        | 48       |                   |                   | RX BUFFER COUNTER CHB               |           |             |
|                        | 49       | PUBLIC            | RX_COUNT_CHA      | ; RX BUFFER COUNTER CHA             |           |             |
|                        | 50       |                   |                   | ERROR FLAG CHB                      |           |             |
|                        | 51<br>52 |                   |                   | FRROR FLAG CHA                      |           |             |
|                        |          |                   |                   | STATUS FLAG CHA                     |           |             |
|                        | 54       |                   |                   | STS_CS_CHA DM B                     |           |             |
|                        | 55       |                   |                   | BLES PASSED TO THE TRANSMIT         |           |             |
|                        | 56<br>57 | ; AND RECEIVE CO  | MINIHNUS.         |                                     |           |             |
|                        | 58       | PUBLIC            | TX_POINTER_CHB    | ; TX BUFFER POINTER FOR CHB         |           |             |
|                        | 59       |                   |                   | ; TX LENGTH OF BUFFER FOR CHB       |           |             |
|                        | 60       |                   |                   | TX BUFFER POINTER FOR CHA           |           |             |
|                        | 61<br>62 |                   |                   | TX LENGTH OF BUFFER FOR CHA         |           |             |
|                        | 63       |                   |                   | RX BUFFER POINTER FOR CHA           |           |             |
|                        | 64       |                   |                   |                                     |           |             |
|                        | 65<br>66 | ; I/O PORT ASSIG  |                   |                                     |           |             |
|                        | 67       | CHANNEL A PORT    | ASSIGNMENTS       |                                     |           |             |
|                        | 68       |                   |                   |                                     |           |             |
| 9999                   | 69       | DATA_PORT_CHA     | EQU               | 0 s so so DATA                      |           |             |
| 9992<br>9992           | 70<br>71 |                   | HA EQU            | 2 ; COMM<br>COMMAND_PORT_CHA ; STAT |           |             |
|                        | 72       |                   | STATUS CHINE      |                                     |           |             |
|                        |          | CHANNEL B PORT    | ASSIGNMENTS       |                                     |           |             |
| 0004                   | 74<br>75 | DATA_PORT_CHB     | EQU               | 4                                   | 7.40 DODT |             |
| 9996                   | 76       | COMMAND_PORT_CI   |                   | 4 ATZ GRA ZMETATOM R LEGIDATA       | AND PORT  |             |
| 9996                   | 77       |                   | B EQU             | COMMAND_PORT_CHB STAT               |           |             |
|                        | 78       |                   | FIX BUFFER LON    |                                     |           |             |
|                        | 79<br>80 | ; MISC. SYSTEM E  |                   | 8 NO RECEPTION ON 8                 |           |             |
| 0000                   | 81       | CR_CHR            | EQU ØDH           | ; ASCII CR CHARACTER CODE           |           |             |
| 0200                   | 82       | INT_TABLE_BASE    |                   | ; INT. VECTOR BASE ADDRESS          |           |             |
| 0500                   | 83       | CODE_START        |                   | START LOCATION FOR CODE             |           |             |
|                        |          | 1 \$EJECT         |                   |                                     |           |             |
|                        | 86       | - PLULUI          |                   |                                     |           |             |
|                        | 87       | RAM ASSSIGNMEN    | NTS FOR DATA SEGN |                                     |           |             |
|                        | 88       |                   | CEOUENE           |                                     |           |             |
|                        | 89<br>90 | DATA              | SEGMENT           |                                     |           |             |
|                        | 20       |                   |                   | 0.40                                |           | AFN: 01995A |

| MCS-86 MACRO ASSEMBLER | ASYNCB     |                   |           |           | 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | OMVER   | PAGE 3  |
|------------------------|------------|-------------------|-----------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------|
| LOC OBJ                | LINE       | SOURCE            |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 3/[J    | 180 301 |
|                        | 91         | ; YECTOR INTERRU  | JPT TABLE | - ASSU    | ME INITIAL 8274 INTERRUPT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |         |         |
|                        | 92         | ; VECTOR IS NUME  | BER 80 (8 | 200H).    | FOR EACH VECTOR, THE TABLE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |         |         |
|                        | 93         | CONTAINS START    | LOCATIO   | N AND C   | DDE SEGMENT REGISTER VALUE.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |         |         |
|                        | 94         | THE TABLE IS L    | OADED FR  | OM PROM.  | PUBLIC DEGLARATIONS FOR CONTIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 3.6     |         |
|                        | 95         |                   |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 0200                   | 96         | ORG               | INT_TAB   | LE_BASE   | PUBLIC INITIAL 8274                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 35      |         |
|                        | 97         | B JEWIND CHRISTER | PFER COM  |           | PUBLIC TX_COMMAND_CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 32      |         |
| 0200 0000              | 98         | TX_YECTOR_CHB     | DW 933    | 0         | TX INTERRUPT VECTOR FOR CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 38      |         |
| 0202 0000              | 99         |                   |           |           | PUBLIC PY_COMMIND_CHE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 52      |         |
|                        | 100        | PAND CHAMMEL A    |           | 18K BU    | PUBLIC RX_COMMEND_CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 69      |         |
| 0204 0000              | 101        | STS_VECTOR_CHB    | DW        | 0         | STATUS INTERRUPT VECTOR FOR CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 0206 0000              | 102        | STS_CS_CHB        | DW 23     | 0         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 25      |         |
|                        | 103        |                   |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 0208 0000              | 104        | RX_VECTOR_CHB     | DW        | 0         | ; RX INTERRUPT VECTOR FOR CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |         |         |
| 020A 0000              | 105        | RX_CS_CHB PHO     | DW Y      | 0         | PURLIC RX_READY_CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |         |         |
|                        | 106        |                   | PIY FLAG  |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 3Þ      |         |
| 020C 0000              | 107        | ERR_VECTOR_CHB    | DM        | 0         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 020E 0000              | 108        | ERR_CS_CHB        |           |           | PUBLIC ROLCOUNT_CHS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |         |         |
|                        | 109        |                   |           |           | PUBLIC RALEGUNTLOHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 49      |         |
| 0210 0000              | 110        | TX_VECTOR_CHA     |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 0212 0000              | 111        | TX_CS_CHA         | DW        | 0         | PUBLIC ERROR_MSG_CHR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |         |         |
|                        | 112        |                   | FLAG CH   |           | BHD_DENLEUTE STATUS_CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |         |         |
| 0214 0000              | 113        |                   |           |           | STATUS INTERRUPT VECTOR FOR CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 0216 0000              | 114        | STS_CS_CHA        | DM        | 0         | ANNOUN AND REPORTED TO THE PARTY.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 8E      |         |
| 0040 0000              | 115        |                   |           |           | STUBLIC DECLINATIONS FOR VARIOUS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 36      |         |
| 0218 0000              | 116        | RX_VECTOR_CHA     | 7.00      | 0         | ; RX INTERRUPT VECTOR FOR CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 25      |         |
| 021A 0000              | 117        | RX_CS_CHA         | DM        | 0         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 2040, 2000             | 118        |                   |           |           | PUBLIC TX_POINTER_CHE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         |         |
| 021C 0000<br>021E 0000 | 119        |                   |           |           | ERROR INTERRUPT VECTOR FOR CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 88      |         |
| 021F 0000              | 120<br>121 |                   |           |           | PUBLIC TXLENDINGSCOM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 19      |         |
|                        | 122        |                   |           |           | STATUS AND POINTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |         |         |
|                        | 123        |                   |           |           | AND POINTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |         |         |
|                        | 124        | CHANNEL B POIN    |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
|                        | 125        | OHIMALL DIOI      | TIERS THE | 3111103   | LIAD PORT RESIGNATORS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         |         |
| 0220 0000              | 126        | TX_POINTER_CHB    | DM        | 0         | ; TX BUFFER POINTER FOR CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |         |         |
| 0222 0000              | 127        | TX_LENGTH_CHB     |           | 9         | TX BUFFER LENGTH FOR CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |         |         |
| 0224 0000              | 128        | RX_POINTER_CHB    |           | 0         | RX BUFFER POINTER FOR CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |         |         |
| 0226 0000              | 129        | RX_COUNT_CHB      |           | 0 0       | and the second s |         |         |
| 0228 00                | 130        | TX_EMPTY_CHB      | DB        | 0 9       | TX DONE FLAG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |         | 9892    |
| 0229 00                |            | RX_READY_CHB      |           | Later and | The second secon | ELSE 0) |         |
| 922R 99                | 132        | STATUS_MSG_CHB    |           | 0         | STATUS CHANGE MESSAGE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 22      |         |
| 022B 00                | 133        | ERROR_MSG_CHB     |           | 0         | ERROR STATUS LOCATION (0 IF NO E                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | RROR)   |         |
|                        | 134        |                   |           | 1         | 2001 211102 20011101 (0 1) 110 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | and a   |         |
|                        | 135        | CHANNEL A POIN    | ITERS AND | STATUS    | DATA_PORT_CHS EEU                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |         | 4688    |
|                        |            |                   |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 022C 0000              | 137        | TX_POINTER_CHA    | DW        | 0110      | ; TX BUFFER POINTER FOR CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |         |         |
| 022E 0000              | 138        | TX_LENGTH_CHA     | DW        | 0         | ; TX BUFFER LENGTH FOR CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |         |         |
| 0230 0000              | 139        | RX_POINTER_CHA    | DW        | 0         | RX BUFFER POINTER FOR CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 62      |         |
| 0232 0000              | 140        | RX_COUNT_CHA      | DW        | 0         | RX LENGTH COUNTER FOR CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |         |         |
| 0234 00                | 141        | TX_EMPTY_CHA      |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 81      |         |
| 0235 00                | 142        | RX_READY_CHA      |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
| 0236 00                | 143        |                   |           |           | A STATE OF STREET                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |         |         |
| 0237 00                | 144        | ERROR_MSG_CHA     | DB        | 0         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
|                        | 145        |                   |           |           | TOBUSE 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |         |         |
|                        | 146        | DATA              | ENDS      |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
|                        | 147        |                   |           |           | FRAN ASSSTOWNENTS FOR DATA SECH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
|                        | 148 +1     | \$EJECT           |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |
|                        |            |                   |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |         |

AFN: 01995A

| MCS-86 MACRO ASSEMBLER | ASYNCB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |               | PAGE 4            |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------------|
| NGS-00 PHCKU POSERBLEK | пэтка                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |               | TIGE              |
| LOC OBJ                | LINE SOURCE 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | FDS 3411      |                   |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                   |
|                        | 149 230171001 (019100) 10 139                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |                   |
|                        | 150 ABC SEGMENT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                   |
| 0000                   | 151 ASSUME CS: ABC, DS: DATA, SS: DATA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 134 July      |                   |
| 9599                   | 152 ORG CODE_START                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               |                   |
|                        | INTERLIZATION COMMIND FOR THE 8274 - THE 8274 - 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | #4 REL        |                   |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | okokokokok    |                   |
|                        | 155 ;* (we 8 (2009)) 903 907300 TA BUTTOUTZ 30099 MD99                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | * 801         |                   |
|                        | 156 ;* PARAMETERS FOR CHANNEL INITIALIZATION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | * 883         |                   |
|                        | 157 ;*                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | # 88S         |                   |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | pjojojojoje   |                   |
|                        | 159                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               |                   |
|                        | 160 ; CHANNEL B PARAMETERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                   |
|                        | 161 HOS OT HOSE MOSES SOLUTION SO ONE SE SOCIOUS PROSECTION VIOLATION OF THE SECRET VIOLATION OF THE S |               |                   |
|                        | 162 ; MR1 - INTERRUPT ON ALL RX CHR, VARIABLE INT VECTOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | TX INT ENABLE | 0518 C70639428906 |
| 0500 01                | 163 CMDSTRB DB 1,16H 23 380 23 XI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |               |                   |
| 0501 16                | HOW STS., VECTOR, CHES. STRING STRING VECTOR CHE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |               |                   |
|                        | 164 ; WR2 - INTERRUPT VECTOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |               |                   |
| 0502 02                | 165 DB 2, (INT_TABLE_BASE/4)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |               |                   |
| 9593 89                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                   |
|                        | 166 ; WR3 - RX 8 BITS/CHR, RX DISABLE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |               |                   |
| 0504 03                | 167 DB 3, 0C0H 20, 28 00 20 WA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |               |                   |
| 0505 C0                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                   |
|                        | 168 ; MR4 - X16 CLOCK, 2 STOP BITS, NO PARITY                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |                   |
| 0506 04                | 169 40 90 90 DB 4, 4CH 90 90 90 90 90 90 90 90                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |               |                   |
| 0507 4C                | 22 JBJD 22 272 VIW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               |                   |
|                        | 170 ; MR5 - DTR ACTIVE, TX 8 BITS/CHR, TX ENABLE, RTS AC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | CTIVE TIS     |                   |
| 0508 05                | 171 DB 5, ØEAH 23 380 23 38                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                   |
| 0509 EA                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                   |
|                        | 172 ; WR6 AND WR7 NOT REQUIRED FOR ASYNC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |               |                   |
| 950A 99                | 173 DB 0.0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                   |
| 959B 99                | EA ZELLE LUGITE EMBONELIEUS BULO 8554                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |               |                   |
|                        | 174                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               |                   |
|                        | 175 ; CHANNEL A PARAMETERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                   |
|                        | 176 SRO_TROS_QUERROO_USGUSU                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                   |
|                        | 177 ; MR1 - INTERRUPT ON ALL RX CHR, TX INT ENABLE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               |                   |
| 050C 01                | 178 CMDSTRA DB 1, 12H 000000 732300 10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |               |                   |
| 050D 12                | 10Y 50 COMMEND_PORT_CHE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                   |
|                        | 179 ; WR2 - VECTORED INTERRUPT FOR 8086                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               | 605283 2256       |
| 050E 02                | 180 DB 2, 30H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |                   |
| 050F 30                | HIT FALL 22 STATUS BYTES BAD PLAGS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               |                   |
|                        | 181 ; WR3 - RX 8 BITS/CHR, RX DISABLE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |               |                   |
| 0510 03                | 182 DB 3, 9C9H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |               |                   |
| 0511 C0                | NOV ERROR HEQ. CAS. AL : CLEAR ERROR FLAG CAS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |                   |
|                        | 183 ; WR4 - X16 CLOCK, 2 STOP BITS, NO PARITY                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |                   |
| 0512 04                | 184 SIO SALIA DB ATE 94,4CH IN GROUNGAL BUTHTE WOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               |                   |
| 0513 4C                | NOV STRINGLYSGLERN, NO. LOLERN STRING PLAS CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |               |                   |
| 0544.05                | 185 SING SING HIRS - DTR ACTIVE, TX 8 BITS/CHR, TX ENABLE, RTS AC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | TIVE          |                   |
| 0514 05                | 186 AND SET DB VS 5, OEAH VS AND THEOLOGY VON                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |                   |
| 0515 EA                | 407 UPC OND UPT NOT DECUTOES FOR ACTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                   |
| 0546 00                | 187 JUNE AND WRY NOT REQUIRED FOR ASYNC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                   |
| 0516 00<br>0517 00     | 188 AND THE DB AND TO BE AND THE SECOND THE SECOND  |               |                   |
| 0517 00                | HOW TXLENETYLERS RL 1SET TX HONE FLAS CH8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |               |                   |
|                        | 189 AND BREF SHOUNT TSE: LR GROUNTNEGERT WOM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 244           |                   |
|                        | 190 +1 \$EJECT ASSAULT BARRES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |                   |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                   |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                   |
|                        | SELLINGS ENTAGES SELECTED SELECTED SOUTH AND S |               |                   |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |                   |

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| MCS-86 MACRO ASSEMBLER             | RSYNCB     |                                                    |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         | PAGE 35 5 STATE OF THE PAGE |
|------------------------------------|------------|----------------------------------------------------|-------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------------------|
| LOC OBJ                            | LINE       | SOURCE                                             |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 301.1   |                             |
|                                    | 191        |                                                    |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
|                                    | 192        | START OF COMM                                      | AND ROUTINES                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
|                                    | 193        |                                                    |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 130     |                             |
|                                    | 194        | ; alajojajajajajajajajajajajajajajajajajaj         |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
|                                    | 195        | ;*                                                 |                                           | M1573000 530                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | * 551   |                             |
|                                    | 196        | first in the party present executively distribute  | LIZATION COMMAND FOR TH                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 158     |                             |
|                                    | 197        |                                                    | UP ACCORDING TO THE PARI                  | a contract of the contract of  | * 551   |                             |
|                                    | 198        |                                                    | BOYE STARTING AT CHSTRB<br>FOR CHANNEL A. |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | * 361   |                             |
|                                    | 199<br>200 | ;* CMSTRA                                          | FUR CHINNEL H.                            | 4.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 157     |                             |
|                                    | 201        | bern or death or death or to the or destroy of the | iakakakakakakakakakakakakakakakakakakak   | olokokolokokokokokokokokokokokokokokoko                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 158 *   |                             |
|                                    | 202        | ,                                                  |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 159     |                             |
| 9518                               | 203        | INITIAL_8274:                                      |                                           | CHARLE & PROPRETEES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |         |                             |
|                                    | 204        |                                                    | INTERRUPT VECTOR IP AND                   | CS VALUES FROM PROM TO RAM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 161     |                             |
| 0518 C70600020806                  | 205        | MOY                                                | TX_YECTOR_CHB, OFFSET                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
| 051E 8C0E0202                      | 206        | MOV                                                | TX_CS_CHB, CS                             | CHRISTING OR 1.16H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |         |                             |
| 0522 C70604023506                  | 207        | YOM                                                | STS_VECTOR_CHB, OFFSE                     | T STAINB ; STATUS VECTOR (                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |         |                             |
| 0528 8C0E0602                      | 208        | YOM                                                |                                           | The World Co., St. Co | 164     |                             |
| 052C C70608024906                  | 209        | VOM                                                |                                           | RCVINB RX DATA VECTOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | CHB     | 8592 82                     |
| 0532 8C0E0R02                      | 210        | MOA                                                | RX_CS_CHB, CS                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
| 0536 C7060C027706                  | 211        | MOV                                                | ERR_VECTOR_CHB/ OFFSE                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | B SOI   |                             |
| 053C 8C0E0A02                      | 212        | MOV                                                | RX_CS_CHB, CS                             | HOUSE SU                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |         |                             |
| 0540 C70610028C06<br>0546 8C0E1202 | 213<br>214 | MOV                                                | TX_VECTOR_CHA, OFFSET TX_CS_CHA, CS       | XMTINA ; TX DATA VECTOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | CHH     |                             |
| 0548 C7061402B906                  | 214        | MOA                                                |                                           | T STAINA ; STATUS VECTOR (                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | (69 aur |                             |
| 9559 8C0E1602                      | 216        | MOV                                                | STS_CS_CHA, CS                            | i Sinimn /Sinius Vector (                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | ,nn     |                             |
| 0554 C7061802CD06                  | 217        | STANDA STAND                                       |                                           | RCVINA RX DATA VECTOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | CHA     |                             |
| 055A 8C0E1A02                      | 218        | MOY                                                | RX_CS_CHA, CS                             | DB 5, 059H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 171     |                             |
| 055E C7061C02FB06                  | 219        | MOV                                                | ERR_VECTOR_CHA, OFFSE                     | T ERRINA ; ERROR VECTOR CI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | HA .    |                             |
| 0564 8C0E1E02                      | 220        | MOV                                                | ERR_CS_CHA, CS                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
|                                    | 221        |                                                    |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
|                                    | 222        | COPY SETUP TA                                      | BLE PARAMETERS INTO 827                   | 4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |         |                             |
|                                    | 223        |                                                    |                                           | DETERMINATION AND STORY                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 174     |                             |
| 0568 BF0005                        | 224        | MOV                                                | DI, OFFSET CMDSTRB                        | ; INITIALIZE CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |         |                             |
| 056B BA0600                        | 225        | MOV CALL                                           | DX, COMMAND_PORT_CHB                      | COPY CHB PARAMETERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |         |                             |
| 056E E82E00<br>0571 BF0C05         | 226<br>227 | MOV                                                | DI, OFFSET CMDSTRA                        | INITIALIZE CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                             |
| 0574 BA0200                        | 228        | MOV                                                | DX, COMMAND_PORT_CHA                      | ) INTITICIZE OINT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |         | 6560 12                     |
| 0577 E82500                        | 229        | CALL                                               |                                           | COPY CHA PARAMETERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |         |                             |
| 0011 202000                        | 230        | VII.E.                                             | 20.01                                     | HBE & 20.38H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |         |                             |
|                                    | 231        | INITIALIZE ST                                      | ATUS BYTES AND FLAGS                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
|                                    | 232        |                                                    | VEHRO RX DISABLE                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
| 057A B80000                        | 233        | MOV                                                | AX, 0                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
| 057D A22B02                        | 234        | YOM                                                | ERROR_MSG_CHB, AL                         | ; CLEAR ERROR FLAG CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |         |                             |
| 0580 A23702                        | 235        | MOV                                                |                                           | CLEAR ERROR FLAG CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |         |                             |
| 0583 A22A02                        | 236        | MOV                                                | STATUS_MSG_CHB, AL                        | CLEAR STATUS FLAG CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         |                             |
| 0586 R23602                        | 237        | VOM                                                | STATUS_MSG_CHA, AL                        | CLEAR STATUS FLAG CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         |                             |
| 0589 A32602                        | 238<br>239 | MOY                                                | RX_COUNT_CHA, RX                          | CLEAR RX COUNTER CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |         |                             |
| 058C A33202<br>058F B001           | 249        | MOV                                                | AL, 1                                     | FOLERK KA COUNTER CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         |                             |
| 0591 A22902                        | 241        | YOM                                                |                                           | SET RX DONE FLAG CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |         |                             |
| 0594 R23502                        | 242        | VOM                                                | RX_READY_CHA, AL                          | ; SET RX DONE FLAG CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |         |                             |
| 0597 A22802                        | 243        | MOV                                                | TX_EMPTY_CHB, AL                          | SET TX DONE FLAG CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |         |                             |
| 059A A23402                        | 244        | MOV                                                | TX_EMPTY_CHA, AL                          | SET TX DONE FLAG CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |         |                             |
| 0590 FB                            | 245        | STI                                                |                                           | ; ENABLE INTERRUPTS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 190 H   |                             |
| 059E C3                            | 246        | RET                                                |                                           | ; RETURN - DONE WITH SET                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |         |                             |
|                                    | 247        |                                                    |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
| 059F 8A05                          | 248        | SETUP: MOY                                         | AL, [DI]                                  | ; PARAMETER COPYING ROUT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | INE     |                             |
| 05A1 3C00                          | 249        | CMP                                                | AL, 0                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                             |
| 05A3 7404                          | 250        | JE                                                 | DONE                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         | AFN: 01995A                 |
|                                    |            |                                                    |                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         | AL 14. 01000A               |

AFN: 01

| MCS-86 MACRO ASSEMBLER | ASYNCB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | ACVAICS.       | PAGE 1322 6 OTOM 38-20M |
|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-------------------------|
| LOC OBJ                | LINE SOURCE 209403                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 3/11           | 180 30.1                |
| OFOE FF                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 111            |                         |
| 9585 EE<br>9586 47     | 231 OUT DAT TE TOUTFUL PRENINCIER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                |                         |
|                        | 252 INC DI POINT AT NEXT PARAMETE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | EME EME        |                         |
| 05A7 EBF6              | 253 JMP SETUP ; GO LOAD IT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                | 5/800                   |
| 05A9 C3                | 254 DONE: RET ; DONE - SO RETURN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                | 9009                    |
|                        | 255 SIETZIOSA SMR2 ( XR 1219                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 315            | 8806 56                 |
|                        | 256 +1 \$EJECT XG 152V9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 9.62           | 3507 52                 |
|                        | 257 GALF YORES XF SHELD: 8 SHOLYGRESLXS VON                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 7.17           | 5508 C686296289         |
|                        | 258 ; ***********************************                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                | 2500 C79626628888       |
|                        | 259 ;*RO9 GHERROS TA TREOPA SHOLTROPA_GRAPHROS AND YORK                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | * 615          | BEE3 BR9699             |
|                        | 260 ;* TX CHANNEL B COMMAND ROUTINE - ROUTINE IS CALLED TO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | * 625          | 5888 935                |
|                        | 261 ;* TRANSMIT A BUFFER. THE BUFFER STARTING ADDRESS.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | * 132          | 33 83C                  |
|                        | 262 ;* TX_POINTER_CHB, AND THE BUFFER LENGTH, TX_LENGTH_CHB,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | * 272          | 1389 8801               |
|                        | 263 ;* MUST BE INITIALIZED BY THE CALLING PROGRAM. TWO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | * 525          | 33 830                  |
|                        | 264 ;* BOTH ITEMS ARE WORD VARIABLES.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | * \$25         | AG 3366                 |
|                        | 265 ;*                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | * 335          | 82 (38)                 |
|                        | 266 ; solutolatotatotatatatatatatatatatatatatatata                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | olok 382       | ED 330                  |
|                        | 267                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 122            |                         |
| 95AA                   | 268 TX_COMMAND_CHB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 328            |                         |
| 85AA 50                | 269 PUSH AX ; SAVE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 329            |                         |
| 95AB 57                | 278 * TPUSHATADI DALLEG SAT - A LEMBRO SON GARRAGO XX . *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                |                         |
| 05AC 52                | 271 * PUSHCER DXT TO THIS OF AND STIMIOUS SELECTIFIE *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                |                         |
| 05AD C606280200        | 272 * MOV TX_EMPTY_CHB, 0 ; CLEAR EMPTY FLAG *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                |                         |
| 05B2 BB0400            | 273 * MOV DX, DATA_PORT_CHB ; SETUP PORT POINTER *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                |                         |
| 0585 8B3E2002          | 274 MOV DI, TX_POINTER_CHB ; GET TX BUFFER POINTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                |                         |
| 05B9 8A05              | 275 MOY AL, [DI] ; GET FIRST CHARACTER TO TX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 375            |                         |
| 05BB EE                | 276 OUT DX, AL ; OUTPUT IT TO 8274 TO GET IT S'                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                | 3325                    |
| 05BC 5A                | 277 POP DXTE1899 3M2 MA HEUR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 337            | 30EF 58                 |
| 95BD 5F                | 278 POP DI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 328            | 2578 52                 |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 339            | 30F1 C696358298         |
| 05BE 58<br>05BF C3     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 348            | 88888833873 3708        |
| and ra                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 345            | SOFE BARRES             |
|                        | 281 TROP (UMPRIO TR TUTOR) AND TROPO MODERNICO AND VOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                |                         |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                | 13FF B983               |
|                        | 283 ;* 284 ;* TX CHANNEL A COMMAND ROUTINE - ROUTINE IS CALLED TO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | * 242          | 33 1836                 |
|                        | 285 ;* TRANSMIT A BUFFER. THE BUFFER STARTING ADDRESS.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 177.6          | 3692 BBC1               |
|                        | 286 ;* TX_POINTER_CHA, AND THE BUFFER LENGTH, TX_LENGTH_CHA,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 345 *          | 33 4826                 |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 41             | 3685 SA                 |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 347 *          | 3686 58                 |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                | 9697 C3                 |
|                        | 289 ;* 290 ;************************************                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                |                         |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 111,0611 10110 |                         |
| 0000                   | 291                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 331            |                         |
| 9509                   | 292 TX_COMMAND_CHA:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                |                         |
| 0500 50                | 293 PUSH AX ; SAVE REGISTERS *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                |                         |
| 05C1 57                | 294 * PUSH 23DITUDR 301V/932 T9U9RSTRI 90 T9RT2 *:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                |                         |
| 0502 52                | 295 * PUSH DX *:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 385            |                         |
| 05C3 C606340200        | 296 MOY TX_EMPTY_CHA, 0 ; CLEAR EMPTY FLAG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                         |
| 05C8 BA0000            | 297 MOV DX, DATA_PORT_CHA ; SETUP PORT POINTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                |                         |
| 05CB 8B3E2C02          | 298 MOV DI, TX_POINTER_CHA GET TX_BUFFER POINTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                |                         |
| 05CF 8A05              | 299 MOV AL, [DI] ; GET FIRST CHARACTER TO TX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 359            |                         |
| 05D1 EE                | 300 OUT DX, AL 3002 ; OUTPUT IT TO 8274 TO GET IT S                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | TARTEDES       | 3688 32                 |
| 05D2 5A                | 301 POP DX 10 H209                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 361            | 3683 57                 |
| 05D3 5F                | 302 POP DI NO HENT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 362            | 9698 SB                 |
| 95D4 58                | 303 470PPT 0MPAX00 103 0M32 183 JURG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                | 8698 ES8284             |
| 9505 C3                | 304 SCRETCHO THEM BY THEM RETURN BOLLYT ONE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 364            | 960E FF852982           |
|                        | 385 RETHURO HIGHELLER 320                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 365            | 9612 FF9E2282           |
|                        | 306 ; which is a constructive and a constructive | ***            | 861.6 748E              |
|                        | 307 JOSH (*TXSH TSD - BROQ TOW). SHOLTROYLETER XXX WORL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | * 295          | 8949R8 3139             |
|                        | 308 ;* RX COMMAND FOR CHANNEL B - THE CALLING ROUTINE MUST                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | * 898          | 9818 8B3E2882           |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                |                         |
|                        | 309 ;* INITIALIZE RX_POINTER_CHB TO POINT AT THE RECEIVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | * 695          | 961F 3R85               |
|                        | 309 ;* INITIALIZE RX_POINTER_CHB TO POINT AT THE RECEIVE 310 ;* BUFFER BEFORE CALLING THIS ROUTINE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | * 695          | 961F 8R85<br>9621 EE    |

| MCS-86 MACRO ASSEMBLER | ASYNCB       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | SCHOOL | PAGE 12-27 OXORN 36-231 |
|------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------|
| LOC OBJ                | LINE         | SOURCE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 361.1  |                         |
|                        | 311          | * GOT STORAGE THAT HE SEE SEE SEE SEE SEE SEE SEE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | AES .  |                         |
|                        | 312          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
|                        | 313          | TI 0901 08: 90732 900                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |        |                         |
| <b>0506</b>            | 314          | RX_COMMAND_CHB:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| 0506 50                | 315          | PUSH RX ; SAYE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |        |                         |
| 0507 52                | 316          | PUSH DX TOURS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |        |                         |
| 05D8 C606290200        | 317          | MOV RX_READY_CHB, 0 ; CLEAR RX READY FLAG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |        |                         |
| 05DD C70626020000      | 318          | MOV RX_COUNT_CHB, 0 ; CLEAR RX COUNTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |                         |
| 05E3 BA0600            | 319          | MOV DX, COMMAND_PORT_CHB ; POINT AT COMMAND PORT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |        |                         |
| 05E6 B003              |              | MOY IN AL, 3 1 199 - 31; SET UP FOR WR3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 269    |                         |
| 05E8 EE                |              | OUT AND DX ALMAR REPORT OF SETTING A THEOREM IN THE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |                         |
| 05E9 B0C1              |              | MOV AL, 9C1H ; WR3 - 8 BITS/CHR, ENABLE RX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |        |                         |
| 05EB EE                |              | * OUT DX AL DMILBO BUT YE CEST BUTTEN BE TOWN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |        |                         |
| 05EC 5A                |              | * POP DX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 264    |                         |
| 05ED 58                |              | POP AX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |                         |
| 05EE C3                |              | ; RETURN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |        |                         |
|                        | 327          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
|                        | 328          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
|                        | 329          | * PUSH PK ** SRVE REGISTERS *:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |                         |
|                        | 330          | * RX COMMAND FOR CHANNEL A - THE CALLING ROUTINE MUST                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |        |                         |
|                        | 331          | * INITIALIZE RX_POINTER_CHA TO POINT AT THE RECEIVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |                         |
|                        | 332          | ;* BUFFER BEFORE CALLING THIS ROUTINE.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 272    | 995985363C GR26         |
|                        | 333          | ** PETTLE PORT LONG LONG LONG PORT POLICER *;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 528    |                         |
|                        | 334 8<br>335 | ; waterialist in a state of the |        |                         |
| OECC                   |              | XT OT SETOINEN TEST TESTED E ELGI JA VON<br>SERX_COMMEND_CHR:SE OT TESTED JE AG TEO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |                         |
| 05EF<br>05EF 50        | 336 337      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| 05F0 52                | 338          | PUSH AX ; SAVE REGISTERS PUSH DX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 875    |                         |
| 05F1 C606350200        | 339          | MOV RX_READY_CHR. 0 ; CLEAR RX READY FLAG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |        |                         |
| 95F6 C79632929999      | 340          | MOV RX_COUNT_CHA, 0 ; CLEAR RX COUNTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |                         |
| 05FC BR0206            | 341          | MOV DX COMMAND_PORT_CHA ; POINT AT COMMAND PORT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 183    |                         |
| 05FF B003              |              | MOV AL, 3 /SET UP FOR WR3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 282    |                         |
| 9691 EE                |              | * OUT DX AL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |        |                         |
| 0602 B0C1              | 344          | 이 보고 있는 것이 되었다. 이번째 하는 것이 하면 하면 하면 되었다. 그는 이 그는 사람들은 사람들은 사람들이 되었다. 그는 사람들은 그는 것이 되었다.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |                         |
| 0604 EE                | 345          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| 0605 5A                | 346          | THE POPPELL DX ATTORES SHE BUTTER SHE PROTECTION OF THE PROTECT OF |        |                         |
| 9696 58                | 347          | POP MERK DRY BALLERO BAT VE GESTARTITAL BE TEUR *V                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 297    |                         |
| 0607 C3                | 348          | RET RETURN A 398 24311 HTGB *.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |                         |
|                        | 349          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
|                        | 350 +1       | ESEJECT ASSESSED TO A TOTAL TO A TOTAL ASSESSED TO A TOTAL ASSESSE |        |                         |
|                        | 351          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 291    |                         |
|                        | 352          | j where the transfer of the state of the     |        |                         |
|                        | 353          | * PUBH RX SPACE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |        |                         |
|                        | 354          | * START OF INTERRUPT SERVICE ROUTINES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |        |                         |
|                        | 355          | ;* X0 H2U3 4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |                         |
|                        | 356          | j stantoletras de televista televista de la circia del circia de la circia del la |        | 9503 CS95749289         |
|                        | 357          | PETRICO TORY SETUP PORTLESS AND SETUP PORT POINTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        |                         |
|                        | 358 R        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| 9698 52                | 360          | XMTINB: PUSH DX ; SAVE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |        |                         |
| 0609 57                | 361          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| 969R 59                | 362          | PUSH DI<br>PUSH 6X                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        |                         |
| 969B E89291            | 363          | CALL EOI ; SEND EOI COMMAND TO 8274                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |                         |
| 060E FF062002          | 364          | INC TX_POINTER_CHB ; POINT TO NEXT CHARACTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |                         |
| 0612 FF0E2202          | 365          | DEC TX_LENGTH_CHB ; DEC LENGTH COUNTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |                         |
| 0616 740E              | 366          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| 0618 BR0400            | 367          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| 061B 8B3E2002          | 368          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 388    |                         |
| 061F 8R05              | 369          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| 9621 EE                | 370          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |                         |
| AFN: 01925A            |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        | AFN: 01995A             |

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| MCS-86 MACRO ASSEMBLER | RSYNCE | 3          |         |       |              |                   |                             |            | PAGE 8        |
|------------------------|--------|------------|---------|-------|--------------|-------------------|-----------------------------|------------|---------------|
| LOC OBJ                | LINE   | SOURCE     |         |       |              |                   |                             | E Bill     |               |
|                        |        | 300.102    |         |       | St. W. THAT  | A 10              | 1000                        |            | 1056 PC10     |
| 0622 58                | 371    |            | POP     | AX    |              | RESTORE REGISTE   |                             | 437        | 967F 8885     |
| 0623 5F                | 372    |            | POP     | DI    | 2.00         | - MI 450          |                             |            |               |
| 0624 5A                | 373    |            | POP     | DX    | ESSE OFFER   |                   |                             |            |               |
| 9625 CF                | 374    |            | IRET    |       | ARE: J       | RETURN TO FOREG   | ROUND                       |            |               |
| 0626 BR0600            | 375    | XIB:       | MOV     | DX,   | COMMAND_POR  |                   | RACTERS HAVE I              | BEEN SEND  |               |
| 9629 B928              | 376    |            | MOY     | AL    | 28H          | DECET TROUGHTTT   |                             |            |               |
| 062B EE                | 377    |            | OUT     | DX.   | AL           | 200               | 9,19                        | 25%        | 6689 58       |
| 962C C696289291        | 378    |            | MOV     | TX    | EMPTY CHR. 1 | ; DONE - SO SET T | X EMPTY FLAG                | CHR        |               |
| 0631 58                | 379    |            | POP     |       |              | RESTORE REGISTE   |                             | 627        | 35 8936       |
| 9632 5F                | 380    |            | POP     | DI    |              | /NESTONE NESTSTE  |                             | 644        |               |
| 0633 5A                | 381    |            | POP     | DX    | ROUTINE      |                   |                             |            |               |
| 9634 CF                | 382    |            | IRET    | Un    |              | RETURN TO FOREG   | DUIND                       |            |               |
| 0034 CI                | 383    |            | INL     |       | SHVE REGIST  | THE TORNE         |                             |            |               |
|                        | 384    | · CHOKRIC  | D CTO   | THE C | HANGE SERVI  | E DOUTINE         | HEU9                        |            |               |
|                        |        | ) Unnivine | T D DIU |       |              |                   |                             |            | 9636 58       |
| 0CDE E0                | 385    | CTOTHE     | DUCK    | DU    | 0 103 dH32:  | COUR DECLETERS    |                             |            |               |
| 9635 52<br>9636 57     | 386    | STAINB     |         | אט פא | POINT TO N   | ; SAVE REGISTERS  |                             |            |               |
|                        | 387    |            | PUSH    | DI    | ADEC LENGTH  |                   |                             |            |               |
| 0637 50                | 388    |            | PUSH    | HX    | 00 31 7237 : | CENE EST SERVICE  |                             |            |               |
| 0638 E80500            | 389    |            | CALL    |       |              |                   |                             |            |               |
| 963B BR9699            | 390    |            | MOV     |       | COMMAND_POR  | (1_GIID           |                             |            |               |
| 063E EC                | 391    |            | IN      |       |              | READ RRO          |                             |            |               |
| 063F R22R02            | 392    |            | HUY     | 2 III | ITUS_MSG_CHB |                   | IN STATUS ME                |            |               |
| 0642 B010              | 393    |            | MOV     | AL    | 10H<br>AL    | ; SEND RESET STAT | us int commani              | D TO 8274  |               |
| 0644 EE                | 394    |            | OUT     | DX    | AL           |                   | nc 909                      |            |               |
| 0645 58                | 395    |            | POP     | HX    |              | RESTORE REGISTE   | RS                          |            |               |
| 0646 5F                | 396    |            | POP     | DI    |              |                   |                             |            |               |
| 0647 5A                | 397    |            | POP     | DX    |              |                   |                             |            |               |
| 0648 CF                |        |            | IRET    |       |              | HES JA            |                             |            |               |
|                        | 399    |            |         |       |              |                   |                             |            |               |
|                        | 400    |            |         |       | DATA SERVI   | E KUUIINE         |                             |            |               |
|                        | 401    |            |         | STEEL | 96 - 5900 c  |                   |                             |            |               |
| 0649 52                | 402    | RCVINB:    |         |       | SEPTONE RE   | ; SAVE REGISTERS  |                             |            |               |
| 064R 57                | 403    |            | PUSH    | DI    |              |                   |                             |            |               |
| 064B 50                | 404    |            | PUSH    | RX    |              |                   |                             |            |               |
| 064C E8C100            | 405    |            | CALL    |       |              |                   |                             |            |               |
| 064F 8B3E2402          | 406    |            | YOM     |       | RX_POINTER.  |                   | CHB BUFFER PO               | INTER TALL |               |
| 0653 BA0400            | 407    |            | MOV     |       | DATA_PORT_0  |                   | NOW IT THE PERSON IN COLUMN |            |               |
| 9656 EC                | 408    |            | IN      |       |              | READ CHARACTER    |                             |            |               |
| 9657 8895              | 409    |            | YOM     |       | 1 AL         | STORE IN BUFFER   |                             |            |               |
| 0659 FF062402          | 410    |            | INC     | RX_   | POINTER_CHB  | BUMP THE BUFFER   | POINTER                     |            |               |
| 065D FF062602          | 411    |            | INC     |       | COUNT_CHB    | BUMP THE COUNTE   |                             |            |               |
| 9661 3C9D              | 412    |            | CMP     | AL    | CR_CHR       | ; TEST IF LAST CH | aracter to be               | RECEIVED?  |               |
| 0663 750E              | 413    |            | JNE     | RIE   | 000 7000     |                   |                             |            |               |
| 0665 C606290201        | 414    |            | MOY     | RX_   | READY_CHB, 1 | L; YES, SET READY |                             |            |               |
| 066A BA0600            | 415    |            | MOV     | DX,   | COMMAND_POR  | RT_CHB ; POINT A  | T COMMAND POR               |            |               |
| 066D B003              | 416    |            | YOM     | AL    | 3            | POINT AT WR3      |                             | 476        |               |
| 066F EE                | 417    |            | OUT     | DX,   | AL<br>ACAH   |                   |                             |            |               |
| 0670 B0C0              | 418    |            | MOY     | AL.   | 9C9H         | ; DISABLE RX      |                             |            |               |
| 0672 EE                | 419    |            | OUT     | DX,   | AL           |                   |                             |            |               |
| 0673 58                | 420    | RIB:       | POP     | AX    |              | EITHER WAY, RES   | TORE REGISTERS              | 5 884      |               |
| 0674 5F                | 421    |            | POP     | DI    |              |                   |                             | 481        |               |
| 9675 5A                | 422    |            | POP     | DX    |              |                   |                             | 482        |               |
| 0676 CF                | 423    |            | IRET    |       |              | RETURN TO FOREG   | ROUND                       |            |               |
|                        | 424    |            |         |       |              |                   |                             |            |               |
|                        | 425    | ; CHANNE   | L B ERR | OR SE | RVICE ROUTIN | E X0              |                             |            |               |
|                        | 426    |            |         |       | 1100/11      | 10                |                             |            |               |
| 0677 52                | 427    | ERRINB:    | PUSH    | DX    |              | SAVE REGISTERS    |                             | 48%        |               |
| 0678 50                | 428    |            | PIICH   | BX    |              | ; SAVE REGISTERS  |                             |            |               |
| 0679 E89400            | 429    |            | CALL    | EOI   |              | ; SEND EOI COMMAN | D TO 8274                   |            | 28853588 E096 |
| 067C BR0600            | 430    |            | MOV     |       | COMMAND_POR  |                   | 10 0214                     |            | 06998 5030    |
|                        |        |            |         |       |              | 352               |                             |            | AFN: 01995A   |

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| LOC OBJ                                                    | LINE       | SOURCE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 3617     |
|------------------------------------------------------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| 967F B001                                                  | 431        | MOV AL 1 ;POINT AT RR1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
| 681 EE                                                     | 432        | UUI DX, HL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |          |
| 3682 EC                                                    | 433        | IN AL, DX ; READ RR1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |          |
| 1683 A22B02                                                | 434        | MOV ERROR_MSG_CHB, AL ; SAVE IT IN ERROR FLAG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |
| 1686 B030                                                  | 435        | THUY TILL SON SEND RESEL EKKUK CUMMIND 10 86                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 274      |
| 688 EE                                                     | 436        | DA) DL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
| 689 58                                                     | 437        | POP AX RESTORE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |          |
| 68A 5A                                                     | 438        | POP DX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
| 168B CF                                                    | 439        | IRET ; RETURN TO FOREGROUND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |          |
|                                                            | 440        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |          |
|                                                            | 441        | ; CHANNEL A TRANSMIT DATA SERVICE ROUTINE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |
|                                                            | 442        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |          |
| 68C 52                                                     | 443        | XMTINA: PUSH DX ; SAVE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |          |
| 68D 57                                                     | 444        | PUCH NT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |
| 68E 50                                                     | 445        | PUSH AX SALTHON SOUNCES SHARE SOLINIES & TENNEROS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |          |
| 68F E87E00                                                 | 446        | CALL EOI ; SEND EOI COMMAND TO 8274                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |          |
| con FERCACO                                                | 447        | INC TX_POINTER_CHA ; POINT TO NEXT CHARACTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |          |
| 696 FEREZER2                                               | 448        | DEC TX_LENGTH_CHA ; DEC LENGTH COUNTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
| 1698 740E                                                  | 449        | JE XIA ; TEST IF DONE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |          |
| 1696 FF0E2E02<br>1696 FF0E2E02<br>1698 740E<br>169C BR0000 | 450        | MOV DX, DATA_PORT_CHA ; NOT DONE - GET NEXT CH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | JODOCTED |
| 69F 8B3E2C02                                               | 451        | MOV DI, TX_POINTER_CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | HINTUIER |
| 6A3 8A05                                                   | 452        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |          |
| 16A2 EE                                                    |            | MOV AL [DI] ; PUT CHARACTER IN AL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |          |
| 16A6 58                                                    | 453<br>454 | 001 DA) TR. (1010PH) 11 111 82/4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |          |
|                                                            |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |          |
| 688 58                                                     | 455        | POP SESTED STOTES AND SESTED AND SESSION |          |
| 6R9 CF                                                     | 456<br>457 | 101 00                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
| COO DO0200                                                 | 457        | IRET ; RETURN TO FOREGROUND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 292      |
| 16AA BA0200<br>16AD B028                                   | 458<br>459 | XIA: MOV DX, COMMAND_PORT_CHA ; ALL CHARACTERS HAVE BE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | EN SEND  |
|                                                            |            | MOV AL, 28H ; RESET TRANSMITTER INTERRUPT PE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | :ND1NG   |
| 6AF EE<br>16B0 C606340201                                  | 460        | OUT DX, AL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |          |
| 16B2 28                                                    | 461        | MUV IX_EMPTY_CHR, 1 ; DONE - SO SET TX EMPTY FLAG O                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 4P       |
| 1686 5F                                                    | 462        | POP AX ; RESTORE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |          |
| 16B7 5A                                                    | 463        | 701 01                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
| 1688 CF                                                    | 464        | FUF UA 1993                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |          |
| ODO CF                                                     | 465        | IRET ; RETURN TO FOREGROUND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |          |
|                                                            | 466        | A TOTAL PROPERTY AND ADDRESS OF THE PARTY AND |          |
|                                                            | 467        | CHANNEL A STATUS CHANGE SERVICE ROUTINE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |
| CDO EO                                                     | 468        | CTOTNO. DUCH TO THE COURSE PROTECTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |          |
| 1689 52<br>1699 57                                         | 469        | SIMINM: PUSH UX SHVE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |          |
| 6BA 57                                                     | 470        | PUSH DI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |
| 6BB 50                                                     | 471        | PUSH HX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |
| 6BC E85100                                                 | 472        | CALL EOI ; SEND EOI COMMAND TO 8274                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |          |
| 6BF BA0200                                                 | 4/3        | MOY DX, COMMIND_PORT_CHR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |          |
| 6C2 EC                                                     | 474        | THE TIEF OF THE REPUBLIE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |          |
| 603 A23602                                                 | 475<br>476 | MOV STATUS_MSG_CHA, AL ; PUT RRO IN STATUS MESS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | SAGE     |
|                                                            | 110        | MOV AL, 10H ; SEND RESET STATUS INT COMMAND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | TO 8274  |
| 6C8 EE                                                     | 477        | OUT DX AL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |
| 609 58                                                     | 478        | POP AX RESTORE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |          |
| IGCA SF                                                    | 479        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |          |
| 6CB 5A                                                     | 480        | POP DX NA STATES AND THE STATES AND |          |
| 6CC CF                                                     | 481        | IREI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |          |
|                                                            | 482        | 10 909                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
|                                                            | 483        | CHANNEL A RECEIVED DATA SERVICE ROUTINE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |
|                                                            | 484        | Tall                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |          |
| 6CD 52                                                     | 485        | RCVINA: PUSH DX SAVE REGISTERS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |          |
| 6CE 57                                                     | 486        | PUSH DI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |
| 6CF 50                                                     | 487        | PUSH AX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |
| 6D0 E83D00                                                 | 488        | PUSH AX CALL EOI ;SEND EOI COMMAND TO 8274                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |          |
| 6D3 8B3E3002                                               | 489        | MOV DI, RX_POINTER_CHA ; GET RX CHA BUFFER POIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | лер      |
| 6D7 BR0000                                                 | 490        | MOV DX, DATA PORT CHA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | UEK      |
|                                                            |            | THE DAY DITTILL ON LICHE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |          |

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| MCS-86 MACRO ASSEMBLER | ASYNCB |          |          |        |           | asomerels PAGE 18                                            |  |
|------------------------|--------|----------|----------|--------|-----------|--------------------------------------------------------------|--|
|                        |        |          |          |        |           | 8274 Maiti-Protocol Sadal Controller (MPSC) Data             |  |
| LOC OBJ                | LINE   | SOURCE   |          |        |           | Sheet, Intel Corporation, California, 1980.                  |  |
| 06DA EC                | 491    |          | IN       | AL,    | DX        | Basics of Data Communication, Electronics Book               |  |
| 96DB 8895              | 492    |          | MOV      | CDT    | 1 01      | READ CHARACTER STOP DOOY WOULD HIM WAS DOM, ESTIGE           |  |
| 06DD FF063002          | 493    |          | INC      | DA b   | OUNTED C  | Telecommunications and the Cotton parting part and a         |  |
| 06E1 FF063202          | 494    |          | INC      | DV C   | COUNT_CHA | Prentice-Hall, New Jersey, 1976. STRIVER PATHOLOGY PIN MINES |  |
| 96E5 3C9D              | 495    |          | CMP      |        | CR_CHR    | ; TEST IF LAST CHARACTER TO BE RECEIVED? stoogsA isolandooT  |  |
|                        |        |          |          |        | UK_UNK    | McNamara, DEC Preso, Massachusetta, 1977.                    |  |
| 96E7 759E              | 496    |          | JNE      | RIA    | CODU. OUO |                                                              |  |
| 06E9 C606350201        | 497    |          | MOY      |        |           | Miscellaneous Data Communication PAG FLASS, 11.              |  |
| 06EE BA0200            | 498    |          | YOM      |        |           | PORT_CHA BOG; POINT AT COMMAND PORT SSEA AT ATE O-SSS OF ATE |  |
| 06F1 B003              | 499    |          | YOM      | AL,    | -         | :POINT AT WR3 .D.CD.C. sales.                                |  |
| 06F3 EE                | 500    |          | OUT      | DX,    |           |                                                              |  |
| 06F4 B0C0              | 501    |          | MOV      |        | 0C0H      | ; DISABLE RX                                                 |  |
| 06F6 EE                | 502    |          | OUT      | DX,    | AL        |                                                              |  |
| 06F7 58                | 503    | RIA:     | POP      | AX     |           | ; EITHER WAY, RESTORE REGISTERS                              |  |
| 06F8 5F                | 504    |          | POP      | DI     |           |                                                              |  |
| 06F9 5A                | 505    |          | POP      | DX     |           |                                                              |  |
| 06FA CF                | 506    |          | IRET     |        |           | RETURN TO FOREGROUND                                         |  |
|                        | 507    |          |          |        |           |                                                              |  |
|                        | 508    | ; CHANNE | L A ERRO | OR SER | RVICE ROU | TINE                                                         |  |
|                        | 509    |          |          |        |           |                                                              |  |
| 06FB 52                | 510    | ERRINA:  | PUSH     | DX     |           | ; SAVE_REGISTERS                                             |  |
| 96FC 59                | 511    |          | PUSH     | AX     |           |                                                              |  |
| 06FD E81000            | 512    |          | CALL     | EOI    |           | SEND EOI COMMAND TO 8274                                     |  |
| 0700 BA0200            | 513    |          | MOY      | DX.    | COMMAND_  | PORT_CHA                                                     |  |
| 0703 B001              | 514    |          | YOM      | AL,    | 1         | ; POINT AT RR1                                               |  |
| 0705 EE                | 515    |          | OUT      | DX,    | AL        |                                                              |  |
| 0706 EC                | 516    |          | IN       | AL,    | DX        | ; READ RR1                                                   |  |
| 0707 A23702            | 517    |          | MOY      | ERRO   | OR_MSG_CH | A, AL ; SAVE IT IN ERROR FLAG                                |  |
| 070A B030              | 518    |          | MOV      | AL.    | 30H       | ; SEND RESET ERROR COMMAND TO 8274                           |  |
| 070C EE                | 519    |          | OUT      | DX.    | AL        |                                                              |  |
| 070D 58                | 520    |          | POP      | AX     |           | RESTORE REGISTERS                                            |  |
| 070E 5A                | 521    |          | POP      | DX     |           |                                                              |  |
| 070F CF                | 522    |          | IRET     |        |           | ; RETURN TO FOREGROUND                                       |  |
|                        | 523    |          |          |        |           |                                                              |  |
|                        | 524    | ; END-OF | -INTERRU | JPT RO | DUTINE -  | SENDS EOI COMMAND TO 8274.                                   |  |
|                        | 525    | ; THIS   | COMMAND  | ) MUST | T ALWAYS  | TO ISSUED ON CHANNEL A.                                      |  |
|                        | 526    |          |          |        |           |                                                              |  |
| 0710 50                | 527    | E01:     | PUSH     | θX     |           | ; SAVE_REGISTERS                                             |  |
| 0711 52                | 528    |          | PUSH     | DX     |           |                                                              |  |
| 0712 BA0200            | 529    |          | MOV      | DX,    | COMMAND_  | PORT_CHA ; ALWAYS FOR CHANNEL A !!!                          |  |
| 0715 B038              | 530    |          | MOV      | AL,    | 38H       |                                                              |  |
| 0717 EE                | 531    |          | OUT      | DX,    | AL        |                                                              |  |
| 0718 5A                | 532    |          | POP      | DX     |           |                                                              |  |
| 0719 58                | 533    |          | POP      | θX     |           |                                                              |  |
| 071A C3                | 534    |          | RET      |        |           |                                                              |  |
|                        | 535    |          |          |        |           |                                                              |  |
|                        | 536    | END OF   | CODE RO  | OUTIN  | E         |                                                              |  |
|                        | 537    |          |          |        |           |                                                              |  |
|                        | 538    |          | ABC      | END:   | 5         |                                                              |  |
|                        | 539    |          | END      |        |           |                                                              |  |
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| 82 3889 References                                                                                                    |          |                           |            |      | 83WYZA | SLIBSERS OSCIONARIO   |      |
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| ifly the typical communication protocol for<br>tims of instruments. So in 1972, Hewlett-                                                                                                                                                                                                      | GPIB/IEEE 488 OVERVIEW AND DELIGIOUS AND                                                                                                                                                    | 2-357                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
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| ormance.<br>Allow different manufacturers' equipment to be                                                                                                                                                                                                                                    | INTERRUPT AND DMA CONSIDERATIONS                                                                                                                                                                                                | 2-383                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
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| agong the GPIB was originally designed for<br>rumentation systems, it became obvious that<br>of these systems would be controlled by a<br>ulator or computer. With this in mind several<br>difications were made to the original proposal<br>are its final adoption as an international stan- | ned his her own interface from scratch.  was inconsistent in terms of electrical most uts on connector, and types of concalc calc ary time they built a system they had to most                                                 | igner designach one vers, pin-o<br>ectors, pin-o                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

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AFN-01380A

### INTRODUCTION

The Intel® 8292 is a preprogrammed UPI™-41A that implements the Controller function of the IEEE Std 488-1978 (GPIB, HP-IB, IEC Bus, etc.). In order to function the 8292 must be used with the 8291 ceiver logic such as a pair of Intel 8293s. In this configuration the system has the potential to be a so complete GPIB Controller when driven by the appropriate software. It has the following capa- 8847 bilities: System Controller, send IFC and Take Charge, send REN, Respond to SRO, send Interface messages, Receive Control, Pass Control, Parallel Poll and Take Control Synchronously. Raving 39AW

This application note will explain the 8292 only in the system context of an 8292, 8291, two 8293s and the driver software. If the reader wishes to learn more about the UPI-41A aspects of the 8292, Intel's Application Note AP-41 describes the hardware and a second features and programming characteristics of the louing device. Additional information on the 8291 may be applied obtained in the data sheet. The 8293 is detailed in its data sheet. Both chips will be covered here in the details that relate to the GPIB controller.

The next section of this application note presents an overview of the GPIB in a tutorial, but comprehensive nature. The knowledgable reader may wish to skip this section; however, certain basic semantic concepts introduced there will be used throughout soon this note.

Additional sections cover the view of the 8292 from the CPU's data bus, the interaction of the 3 chip types (8291, 8292, 8293), the 8292's software protocol and the system level hardware/software protocol. A brief description of interrupts and DMA will be followed by an application example. Appendix A contains the source code for the system and tance interconnections. driver software.

## **GPIB/IEEE 488 OVERVIEW**

### **DESIGN OBJECTIVES**

### What is the IEEE 488 (GPIB)?

The experience of designing systems for a variety of applications in the early 1970's caused Hewlett-Packard to define a standard intercommunication mechanism which would allow them to easily assemble instrumentation systems of varying degrees of complexity. In a typical situation each instrument designer designed his/her own interface from scratch. Each one was inconsistent in terms of electrical levels, pin-outs on a connector, and types of connectors. Every time they built a system they had to invent new cables and new documentation just to specify the cabling and interconnection procedures.

Based on this experience, Hewlett-Packard began to define a new interconnection scheme. They went further than that, however, for they wanted to specify the typical communication protocol for systems of instruments. So in 1972, Hewlett-Talker/Listener and suitable interface and transwhich since has been modified and standardized by a committee of several manufacturers, coordinated through the IEEE, to perfect what is now known as the IEEE 488 Interface Bus (also known as the HP-IB, the GPIB and the IEC bus). While this bus specification may not be perfect, it is a good compromise of the various desires and goals of instrumentation and computer peripheral manufacturers to produce a common interconnection mechanism. It fits most instrumentation systems in use today and also fits very well the microcomputer I/O bus requirements. The basic design objectives for the GPIB were to:

- 1. Specify a system that is easy to use, but has all of the terminology and the definitions related to that system precisely spelled out so that everyone uses the same language when discussing the GPIB.
- 2. Define all of the mechanical, electrical, and functional interface requirements of a system, yet not define any of the device aspects (they are left up to the instrument designer).
- 3. Permit a wide range of capabilities of instruments and computer peripherals to use a system simultaneously and not degrade each other's per-ARETMI formance.
  - 4. Allow different manufacturers' equipment to be connected together and work together on the
  - 5. Define a system that is good for limited dis-
- epoliteid source 6. Define a system with minimum restrictions on performance of the devices.
  - a xiguage 7. Define a bus that allows asynchronous communication with a wide range of data rates.
  - 8. Define a low cost system that does not require OXIGNASSA extensive and elaborate interface logic for the low cost instruments, yet provides higher capability for the higher cost instruments if desired.
    - 9. Allow systems to exist that do not need a central controller; that is, communication directly from one instrument to another is possible.

Although the GPIB was originally designed for instrumentation systems, it became obvious that most of these systems would be controlled by a calculator or computer. With this in mind several modifications were made to the original proposal before its final adoption as an international standard. Figure 1 lists the salient characteristics of the

GPIB as both an instrumentation bus and as a one talker to many listeners. ... ... sud O/I ratuqmoo

mismatched data rates. Howevertag PIB can support this mode of oxygens, maxo lo shom sitt troques end to eno 250k bytes/s, typ redtien at retugmoo Multiple Devices 15 devices, max (electrical limit) 8 devices, typ (interrupt flexibility) Bus Length Data Eus 20 m, max The lines Diol through qyt soiveb/m2d to transfer addresses, control informat betrain o styleta. The formats for addresses anabnammos fid-8s are defined by the IEEE 488 standard (seatsbirid-8dix C). Data formats are undefined and payalqifluM Molla (with or

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Interrupt Driven

Serial poll (slower devices) Parallel poll (faster devices) management

ed t ve beDirect Memory Access and month - VTA

Controller : One DMA facility at controller : Tollowing control byte on sud no serves all devices on bus no styd formos

allow the assigned Talker to rauonordanyaAr data on

I his signal has two uses as

One talker 33-wire handshake

with the handshake to srafener (O/I of O/I between

Talker and listeners need not bas louinos include microcomputer/controller

Figure 1. Major Characteristics of data. The contract a Paranel Poll Although many

The bus can be best understood by examining each of these characteristics from the viewpoint of a general microcomputer I/O bus.

Data Rate - Most microcomputer systems utilize peripherals of differing operational rates, such as floppy discs at 31k or 62k bytes/s (single or double density), tape cassettes at 5k to 10k bytes/s, and cartridge tapes at 40k to 80k bytes/s. In general, the only devices that need high speed I/O are 0.5" (1.3cm) magnetic tapes and hard discs, operational at 30k to 781k bytes/s, respectively. Certainly, the 250k-bytes/s data rate that can be easily achieved by the IEEE 488 bus is sufficient for microcomputers and their peripherals, and is more than needed for typical analog instruments that take only a few readings per second. The 1M-byte/s maximum data rate is not easily achieved on the GPIB and requires special attention to considerations beyond the scope of this note. Although not required, data buffering in each device will improve the overall bus performance and allow utilization of more of the bus poll capability in the IEEE 488 allows htbiwbned

Multiple Devices — Many microcomputer systems used as computers (not as components) service from three to seven peripherals. With the GPIB, up to 8 devices can be handled easily by 1 controller; with some slowdown in interrupt handling, up to 15 devices can work together. The limit of 8 is imposed by the number of unique parallel poll responses available; the limit of 15 is set by the electrical drive characteristics of the bus. Logically, the IEEE 488 Standard is capable of accommodating more device addresses (31 primary, each potentially with 31 secondaries), it this With the can be obtained using DMA. With the

Bus Length — Physically, the majority of microcomputer systems fit easily on a desk top or in a standard 19" (48-cm) rack, eliminating the need for extra long cables. The GPIB is designed typically to have 2 m of length per device, which accommodates most systems. A line printer might require greater cable lengths, but this can be handled at the lower speeds involved by using extra dummy terminaon the bus by allowing each device to transfer agnoit

Byte Oriented — The 8-bit byte is almost universal in I/O applications; even 16-bit and 32-bit computers use byte transfers for most peripherals. The 8bit byte matches the ASCII code for characters and is an integral submultiple of most computer word sizes. The GPIB has an 8-bit wide data path that may be used to transfer ASCII or binary data, as well as the necessary status and control bytes.

Block Multiplexed — Many peripherals are block oriented or are used in a block mode. Bytes are transferred in a fixed or variable length group; then there is a wait before another group is sent to that device, e.g., one sector of a floppy disc, one line on a printer or tape punch, etc. The GPIB is, by nature, a block multiplexed bus due to the overhead involved in addressing various devices to talk and listen. This overhead is less bothersome if it only occurs once for a large number of data bytes (once per block). This mode of operation matches the needs of microcomputers and most of their peripherals. Because of block multiplexing, the bus works best with buffered memory devices.

Interrupt Driven — Many types of interrupt systems exist, ranging from complex, fast, vectored/priority networks to simple polling schemes. The main tradeoff is usually cost versus speed of response. The GPIB has two interrupt protocols to help span the range of applications. The first is a single service request (SRQ) line that may be asserted by all interrupting devices. The controller then polls all devices to find out which wants service. The polling mechanism is well defined and can be easily

automated. For higher performance, the parallel poll capability in the IEEE 488 allows up to eight devices to be polled at once — each device is assigned to one bit of the data bus. This mechanism provides fast recognition of an interrupting device. A drawback is the frequent need for the controller to explicitly conduct a parallel poll, since there is no equivalent of the SRQ line for this mode.

Direct Memory Access (DMA) — In many applications, no imediate processing of I/O data on a byte-by-byte basis is needed or wanted. In fact, programmed transfers slow down the data transfer rate unnecessarily in these cases, and higher speed can be obtained using DMA. With the GPIB, one DMA facility at the controller serves all devices. There is no need to incorporate complex logic in each device.

Asynchronous Transfers — An asynchronous bus is desirable so that each device can transfer at its own rate. However, there is still a strong motivation to buffer the data at each device when used in large systems in order to speed up the aggregate data rate on the bus by allowing each device to transfer at top speed. The GPIB is asynchronous and uses a special

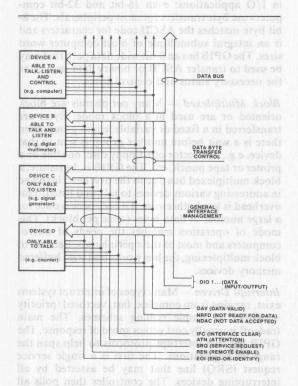


Figure 2. Interface Capabilities and Bus Structure

3-wire handshake that allows data transfers from one talker to many listeners.

I/O To I/O Transfers — In practice, I/O to I/O transfers are seldom done due to the need for processing data and changing formats or due to mismatched data rates. However, the GPIB can support this mode of operation where the microcomputer is neither the talker nor one of the listeners.

### GPIB SIGNAL LINES

### Data Bus

The lines DI01 through DI08 are used to transfer addresses, control information and data. The formats for addresses and control bytes are defined by the IEEE 488 standard (see Appendix C). Data formats are undefined and may be ASCII (with or without parity) or binary. DI01 is the Least Significant Bit (note that this will correspond to bit 0 on most computers).

## Management Bus was recent line listers

ATN — Attention This signal is asserted by the Controller to indicate that it is placing an address or control byte on the Data Bus. ATN is de-asserted to allow the assigned Talker to place status or data on the Data Bus. The Controller regains control by reasserting ATN; this is normally done synchronously with the handshake to avoid confusion between control and data bytes.

EOI — End or Identify This signal has two uses as its name implies. A talker may assert EOI simultaneously with the last byte of data to indicate end of data. The Controller may assert EOI along with ATN to initiate a Parallel Poll. Although many devices do not use Parallel Poll, all devices should use EOI to end transfers (many currently available ones do not).

SRQ — Service Request This line is like an interrupt: it may be asserted by any device to request the Controller to take some action. The Controller must determine which device is asserting SRQ by conducting a Serial Poll at its earliest convenience. The device deasserts SRQ when polled.

IFC — Interface Clear This signal is asserted only by the System Controller in order to initialize all device interfaces to a known state. After deasserting IFC, the System Controller is the active controller of the system.

REN — Remote Enable This signal is asserted only by the System Controller. Its assertion does not place devices into Remote Control mode; REN only enables a device to go remote when addressed to listen. When in Remote, a device should ignore its front panel controls.

## Transfer Busing a data for a data from Transfer Busing and Transfe

NRFD — Not Ready For Data This handshake line is asserted by a listener to indicate it is not yet ready for the next data or control byte. Note that the Controller will not see NRFD deasserted (i.e., ready for data) until all devices have deasserted NRFD.

NDAC — Not Data Accepted This handshake line is asserted by a Listener to indicate it has not yet accepted the data or control byte on the DIO lines. Note that the Controller will not see NDAC deasserted (i.e., data accepted) until all devices have deasserted NDAC.

DAV — Data Valid This handshake line is asserted by the Talker to indicate that a data or control byte has been placed on the DIO lines and has had the minimum specified settling time.

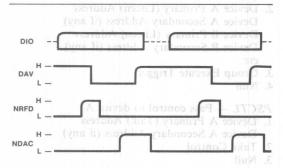


Figure 3. GPIB Handshake Sequence

### **GPIB INTERFACE FUNCTIONS**

There are ten (10) interface functions specified by the IEEE 488 standard. Not all devices will have all functions and some may only have partial subsets. The ten functions are summarized below with the relevant section number from the IEEE document given at the beginning of each paragraph. For further information please see the IEEE standard.

- SH Source Handshake (section 2.3) This function provides a device with the ability to properly transfer data from a Talker to one or more Listeners using the three handshake lines.
- AH Acceptor Handshake (section 2.4) This
  function provides a device with the ability to
  properly receive data from the Talker using the
  three handshake lines. The AH function may
  also delay the beginning (NRFD) or end
  (NDAC) of any transfer.
- T Talker (section 2.5) This function allows a device to send status and data bytes when addressed to talk. An address consists of one (Primary) or two (Primary and Secondary)

- bytes. The latter is called an extended Talker.
- L Listener (section 2.6) This function allows a device to receive data when addressed to listen. There can be extended Listeners (analogous to extended Talkers above).
- SR Service Request (section 2.7) This function allows a device to request service (interrupt) the Controller. The SRQ line may be asserted asynchronously.
- RL Remote Local (section 2.8) This function allows a device to be operated in two modes: Remote via the GPIB or Local via the manual front panel controls.
- PP Parallel Poll (section 2.9) This function allows a device to present one bit of status to the Controller-in-charge. The device need not be addressed to talk and no handshake is required.
- 8. DC Device Clear (section 2.10) This function allows a device to be cleared (initialized) by the Controller. Note that there is a difference between DC (device clear) and the IFC line (interface clear).
- 9. DT Device Trigger (section 2.11) This function allows a device to have its basic operation started either individually or as part of a group.

  This capability is often used to synchronize several instruments.
- 10. C Controller (section 2.12) This function allows a device to send addresses, as well as universal and addressed commands to other devices. There may be more than one controller on a system, but only one may be the controller-in-charge at any one time.

At power-on time the controller that is handwired to be the System Controller becomes the active controller-in-charge. The System Controller has several unique capabilities including the ability to send Interface Clear (IFC — clears all device interfaces and returns control to the System Controller) and to send Remote Enable (REN — allows devices to respond to bus data once they are addressed to listen). The System Controller may optionally Pass Control to another controller, if the system software has the capability to do so.

### GPIB CONNECTOR

The GPIB connector is a standard 24-pin industrial connector such as Cinch or Amphenol series 57 Micro-Ribbon. The IEEE standard specifies this connector, as well as the signal connections and the mounting hardware.

The cable has 16 signal lines and 8 ground lines. The maximum length is 20 meters with no more than two meters per device.

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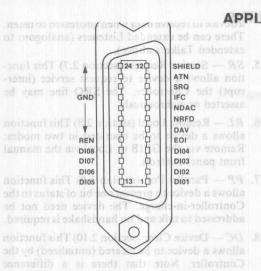


Figure 4. GPIB Connector

## GPIB SIGNAL LEVELS SOLVED A SWOTE HOLD

The GPIB signals are all TTL compatible, low true signals. A signal is asserted (true) when its electrical voltage is less than 0.5 volts and is deasserted (false) when it is greater than 2.4 volts. Be careful not to become confused with the two handshake signals, NRFD and NDAC which are also low true (i.e. > 0.5 volts implies the device is Not Ready For Data).

The Intel 8293 GPIB transceiver chips ensure that all relevant bus driver/receiver specifications are met. Detailed bus electrical specifications may be found in Section 3 of the IEEE Std 488-1978. The Standard is the ultimate reference for all GPIB questions.

## GPIB MESSAGE PROTOCOLS

The GPIB is a very flexible communications medium and as such has many possible variations of protocols. To bring some order to the situation, this section will discuss a protocol similar to the one used by Ziatech's ZT80 GPIB controller for Intel's MULTIBUS™ computers. The ZT80 is a complete high-level interface processor that executes a set of high level instructions that map directly into GPIB actions. The sequences of commands, addresses and data for these instructions provide a good example of how to use the GPIB (additional information is available in the ZT80 Instruction Manual). The 'null' at the end of each instruction is for cosmetic use to remove previous information from the DIO lines.

APPLICATIONS

- Device A Secondary Address (if any) 2. Universal Unlisten
- 3. Device B Primary (Listen) Address Device B Secondary Address (if any) Device C Primary (Listen) Address accepted the data or control byte outling etc
- 4. First Data Byte Second Data Byte

To Last Data Byte (EOI) To Just Both and Dollars

control byte has been algoed on the D10 lilluNa.5

has had the minimum specified settling time TRIGR — Trigger devices A, B,... to take action

- 1. Universal Unlisten
- 2. Device A Primary (Listen) Address Device A Secondary Address (if any) Device B Primary (Listen) Address Device B Secondary Address (if any)
- 3. Group Execute Trigger
- 4 Null

PSCTL — Pass control to device A

- 1. Device A Primary (Talk) Address Device A Secondary Address (if any)
- 2. Take Control
- 3 Null

CLEAR — Clear all devices

- 1 Device Clear
- 2. Null

REMAL — Remote Enable

1. Assert REN continuously

GOREM — Put devices A, B,...into Remote 1. Assert REN continuously

- 2. Device A Primary (Listen) Address Device A Primary (Listen) Address

  Device B Primary (Listen) Address

  (if any) Device B Primary (Listen) Address Device B Secondary Address (if any)
- function provides a device with the abigin properly transfer data from a Talker IcliuM 9.8

GOLOC — Put devices A, B,...into Local

- 1. Device A Primary (Listen) Address
  - Device A Secondary Address (if any)
  - Device B Primary (Listen) Address
  - Device B Secondary Address (if any) etc.
- 2. Go To Local and (Section 2.5) This last T T
- device to send status and data bytes willing, S.

LOCAL — Reset all devices to Local 1. Stop asserting REN 19) over 10 (vismin)

LLKAL — Prevent all devices from returning to Local

1. Local Lock Out

2. Null

SPOLL — Conduct a serial poll of devices A, B,...

1. Serial Poll Enable

2. Universal Unlisten

3. ZT 80 Primary (Listen) Address ZT 80 Secondary Address

4. Device Primary (Talk) Address Device Secondary Address (if any)

5. Status byte from device

6. Go to Step 4 until all devices on list have been polled

7. Serial Poll Disable

8. Null

PPUAL — Unconfigure and disable Parallel Poll response from all devices

1. Parallel Poll Unconfigure

2. Null

ENAPP — Enable Parallel Poll response in devices A, B,...

1. Universal Unlisten

2. Device Primary (Listen) Address Device Secondary Address (if any)

3. Parallel Poll Configure

4. Parallel Poll Enable

5. Go to Step 2 until all devices on list have been configured.

6. Null-

DISPP - Disable Parallel Poll response from devices A. B....

1. Universal Unlisten

2. Device A Primary (Listen) Address Device A Secondary Address (if any) Device B Primary (Listen) Address Device B Secondary Address (if any)

3. Disable Parallel Poll

4. Null

This Ap Note will detail how to implement a useful subset of these controller instructions.

## HARDWARE ASPECTS OF THE SYSTEM

### 8291 GPIB TALKER/LISTENER 884 FIRST odd

The 8291 is a custom designed chip that implements many of the non-controller GPIB functions. It provides hooks so the user's software can implement additional features to complete the set. This chip is discussed in detail in its data sheet. The major features are summarized here; news noiseologis aids al

—Designed to interface microprocessors to the GPIB

—Complete Source and Acceptor Handshake

—Complete Talker and Listener Functions with extended addressing

-Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local functions

Programmable data transfer rate

Maskable interrupts

On-chip primary and secondary address recogni-

1-8 MHz clock range

-16 registers (8 read, 8 write) for CPU interface

-DMA handshake provision

—Trigger output pin

On-chip EOS (End of Sequence) recognition

The pinouts and block diagram are shown in Fig. 5. One of eight read registers is for data transfer to the CPU; the other seven allow the microprocessor to monitor the GPIB states and various bus and device conditions. One of the eight write registers is for data transfer from the CPU; the other seven control various features of the 8291.

The 8291 interface functions will be software configured in this application example to the following subsets for use with the 8292 as a controller that does not pass control. The 8291 is used only to provide the handshake logic and to send and receive data bytes. It is not acting as a normal device in this mode, as it never sees ATN asserted.

| SHI                 | Source Handshake moississib tetal         |
|---------------------|-------------------------------------------|
|                     | Acceptor Handshake As as a Secretary      |
| T3 <sub>iomem</sub> | Basic Talk-only nos 1 UTO metava nism     |
| Lianthov            | Basic Listen-only                         |
| SR0                 | No Service Requests 190 dily betalooms    |
| RLO                 | No Remote/Local MAN gids                  |
| PPO SV S            | No Parallel Poll response of and to state |
| DC0                 | No Device Clear world and singly land to  |
| DT0                 | No Device Trigger and saff moderntolaid   |
|                     |                                           |

If control is passed to another controller, the 8291 must be reconfigured to act as a talker/listener with the following subsets:

Source Handshake SH1 AHI Acceptor Handshake Basic Talker and Serial Poll T5, bas y Basic Listener engal (A14-1910) COCS L3 Service Requests SRI Remote/Local with Lockout PP2 Preconfigured Parallel Poll information to the master Clear Device Clear DTI to am Device Trigger at Tutalizant TUOSSO affi CO and Not a Controller to abrow strike and to

Most applications do not pass control and the controller is always the system controller (see 8292 commands below). A series 198018100 1981 10113 Counter Status or Time Out Status

## 8292 GPIB CONTROLLER die gewissen MISSO

The 8292 is a preprogrammed Intel® 8041A that provides the additional functions necessary to

**BLOCK DIAGRAM** 

### PIN CONFIGURATION

D7 19

VSS

#### 40 TVCC T/R1 8291 T/R2 39 EOI 38 NDAC CLOCK [ 3 derupts GPIB DATA 37 NRFD RESET ta airb-a( 36 DAV TRIG 5 INTERFACE DREQ 35 DIO8 **FUNCTIONS** 8 READ 34 DI07 GPIB CONTROL DACK TO NON-INVERTING REGISTERS ROCESSOR DATA B CST 33 DIO6 AH BUS TRANSCEIVERS TE 32 DIO5 RDF LE WRT 10 8291 31 DIO4 SR RNAL 30 0103 RL INT 11 T/R CONTROL 29 DIO2 D0 12 000 DC 28 DIO1 D1 13 Status byte from device 8 WRITE D2 14 27 SRQ REGISTERS 26 ATN 6. Go to Step 4 until all devices of D3 15 ofleight 25 REN 040 the oth 24 DIFC D5 17 MESSAGE D6 18 211 2110 23 RS2 201612 F monitor the (

Figure 5, 8291 Pin Configuration and Block Diagram

implement a GPIB controller when used with an 8291 Talker/Listener. The 8041A is documented in both a user's manual and in AP-41. The following description will serve only as an outline to guide the later discussion.

21 RS0

conditions. Or ear the eights

transfer from the CPU

The 8292 acts as an intelligent slave processor to the main system CPU. It contains a processor, memory, I/O and is programmed to perform a variety of tasks associated with GPIB controller operation. The onchip RAM is used to store information about the state of the Controller function, as well as a variety of local variables, the stack and certain user status information. The timer/counter may be optionally used for several time-out functions or for counting data bytes transferred. The I/O ports provide the GPIB control signals, as well as the ancillary lines necessary to make the 8291, 2, 3 work together.

The 8292 is closely coupled to the main CPU through three on-chip registers that may be independently accessed by both the master and the 8292 (UPI-41A). Figure 6 shows this Register Interface. Also refer to Figure 12.

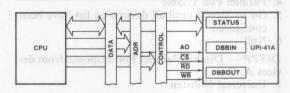
The status register is used to pass Interrupt Status information to the master CPU (A0 = 1 on a read).

The DBBOUT register is used to pass one of five other status words to the master based on the last command written into DBBIN. DBBOUT is accessed when A0 = 0 on a Read. The five status words are Error Flag, Controller Status, GPIB Status, Event Counter Status or Time Out Status.

DBBIN receives either commands (A0 = 1 on a Write) or command related data (A0 = 0 on a write) from the master. These command related data are Interrupt Mask, Error Mask, Event Counter or Time Out.

PPUAL - Unconfigure an

DECODER



| CS | AO      | RD | WR      | REGISTER              |
|----|---------|----|---------|-----------------------|
| 0  | 0       | 0  | (maisin | READ DBBOUT           |
| 0  | 1 f v n | 0  | A fidee | READ STATUS           |
| 0  | 0       | 1  | 0       | WRITE DBBIN (DATA)    |
| 0  | 1       | 1  | 0       | WRITE DBBIN (COMMAND) |
| 1  | X       | X  | X       | NO ACTION             |

Figure 6. UPI-41A Registers

#### 8293 GPIB TRANSCEIVERS

The 8293 is a multi-use HMOS chip that implements the IEEE 488 bus transceivers and contains the additional logic required to make the 8291 and 8292 work together. The two option strapping pins are used to internally configure the chip to perform the specialized gating required for use with 8291 as a device or with 8291/92 as a controller.

In this application example the two configurations used are shown in Fig. 7a and 7b. The drivers are set to open collector or three state mode as required and the special logic is enabled as required in the two modes.

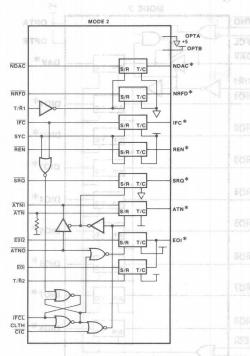


Figure 7a. 8293 Mode 2

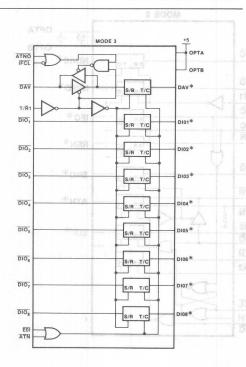


Figure 7b. 8293 Mode 3

### 8291/2/3 CHIP SET

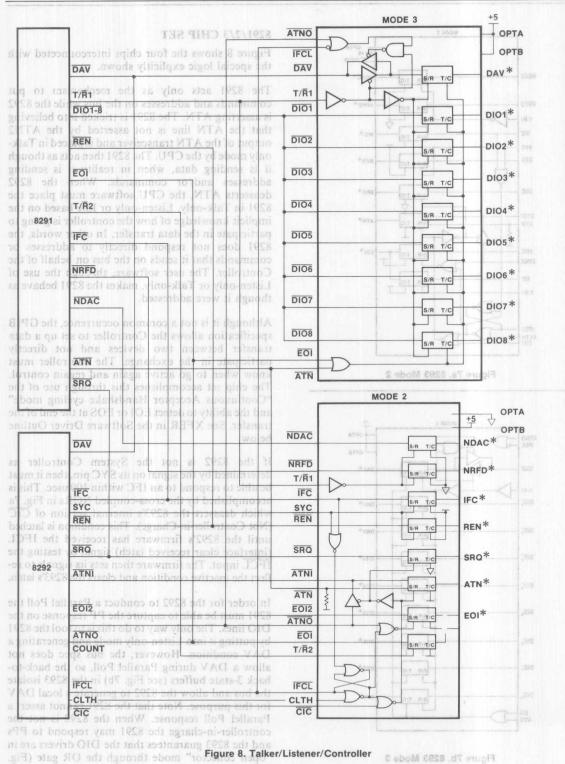
Figure 8 shows the four chips interconnected with the special logic explicitly shown.

The 8291 acts only as the mechanism to put commands and addresses on the bus while the 8292 is asserting ATN. The 8291 is tricked into believing that the ATN line is not asserted by the ATN2 output of the ATN transceiver and is placed in Talkonly mode by the CPU. The 8291 then acts as though it is sending data, when in reality it is sending addresses and/or commands. When the 8292 deasserts ATN, the CPU software must place the 8291 in Talk-only, Listen-only or Idle based on the implicit knowledge of how the controller is going to participate in the data transfer. In other words, the 8291 does not respond directly to addresses or commands that it sends on the bus on behalf of the Controller. The user software, through the use of Listen-only or Talk-only, makes the 8291 behave as though it were addressed.

Although it is not a common occurrence, the GPIB specification allows the Controller to set up a data transfer between two devices and not directly participate in the exchange. The controller must know when to go active again and regain control. The chip set accomplishes this through use of the "Continuous Acceptor Handshake cycling mode" and the ability to detect EOI or EOS at the end of the transfer. See XFER in the Software Driver Outline below.

If the 8292 is not the System Controller as determined by the signal on its SYC pin, then it must be able to respond to an IFC within 100 usec. This is accomplished by the cross-coupled NORs in Fig. 7a which deassert the 8293's internal version of CIC (Not Controller-in-Charge). This condition is latched until the 8292's firmware has received the IFCL (interface clear received latch) signal by testing the IFCL input. The firmware then sets its signals to reflect the inactive condition and clears the 8293's latch.

In order for the 8292 to conduct a Parallel Poll the 8291 must be able to capture the PP response on the DIO lines. The only way to do this is to fool the 8291 by putting it into Listen-only mode and generating a DAV condition. However, the bus spec does not allow a DAV during Parallel Poll, so the back-to-back 3-state buffers (see Fig. 7b) in the 8293 isolate the bus and allow the 8292 to generate a local DAV for this purpose. Note that the 8291 cannot assert a Parallel Poll response. When the 8292 is not the controller-in-charge the 8291 may respond to PPs and the 8293 guarantees that the DIO drivers are in "open collector" mode through the OR gate (Fig. 7b).



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Figure 7b. 8293 Mode 3

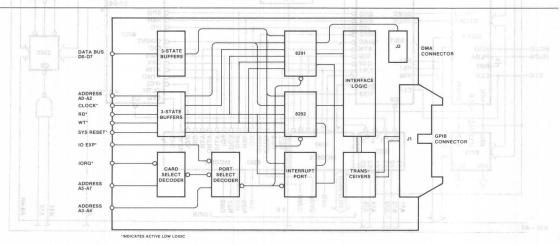
### **ZT7488/18 GPIB CONTROLLER**

Ziatech's GPIB Controller, the ZT7488/18 will be used as the controller hardware in this Application Note. The controller consists of an 8291, 8292, an 8 bit input port and TTL logic equivalent to that shown in Figure 8. Figure 9 shows the card's block diagram. The ZT7488/18 plugs into the STD bus, a 56 pin 8 bit microprocessor oriented bus. An 8085 CPU card is also available on the STD bus and will be used to execute the driver software.

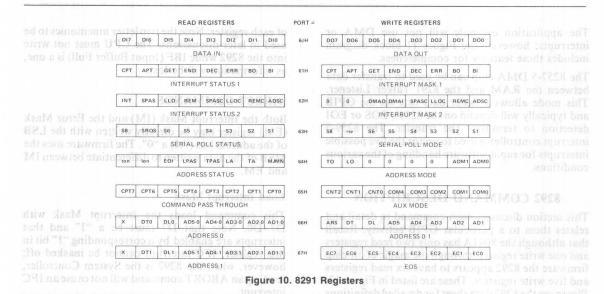
The 8291 uses I/O Ports 60H to 67H and the 8292 uses I/O Ports 68H and 69H. The five interrupt lines are connected to a three-state buffer at I/O Port

6FH to facilitate polling operation. This is required for the TCI, as it cannot be read internally in the 8292. The other three 8292 lines (SPI, IBF, OBF) and the 8291's INT line are also connected to minimize the number of I/O reads necessary to poll the devices.

NDAC is connected to COUNT on the 8292 to allow byte counting on data transfers. The example driver software will not use this feature, as the software is simpler and faster if an internal 8085 register is used for counting in software.



mangsi G Figure 9. ZT7488/18 GPIB Controller



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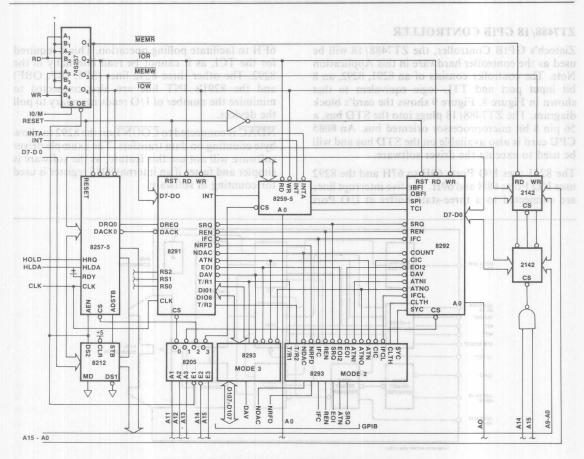


Figure 11. DMA/Interrupt GPIB Controller Block Diagram

The application example will not use DMA or interrupts; however, the Figure 11 block diagram includes these features for completeness.

The 8257-5 DMA chip can be used to transfer data between the RAM and the 8291 Talker/Listener. This mode allows a faster data rate on the GPIB and typically will depend on the 8291's EOS or EOI detection to terminate the transfer. The 8259-5 interrupt controller is used to vector the five possible interrupts for rapid software handling of the various conditions.

### 8292 COMMAND DESCRIPTION

This section discusses each command in detail and relates them to a particular GPIB activity. Recall that although the 8041A has only two read registers and one write register, through the magic of on-chip firmware the 8292 appears to have six read registers and five write registers. These are listed in Figure 12. Please see the 8292 data sheet for detailed definitions

of each register. Note the two letter mnemonics to be used in later discussions. The CPU must not write into the 8292 while IBF (Input Buffer Full) is a one, as information will be lost.

#### DIRECT COMMANDS

Both the Interrupt Mask (IM) and the Error Mask (EM) register may be directly written with the LSB of the address bus (A0) a "0". The firmware uses the MSB of the data written to differentiate between IM and EM.

### Load Interrupt Mask

This command loads the Interrupt Mask with D7-D0. Note that D7 must be a "1" and that interrupts are enabled by a corresponding "1" bit in this register. IFC interrupt cannot be masked off; however, when the 8292 is the System Controller, sending an ABORT command will not cause an IFC interrupt.

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|                 |                | R            | EAD FI   | ROM 82  | 292               |                   |                   | PORT | on the             |                  | V metron          | RITE   | TO 829  | 2 0 0               |                   |                  |
|-----------------|----------------|--------------|----------|---------|-------------------|-------------------|-------------------|------|--------------------|------------------|-------------------|--------|---------|---------------------|-------------------|------------------|
|                 |                | IN           | TERRU    | PT STAT | US                | ) = bm            |                   |      | stepped            |                  | o man             | OMMA   | ND FIEL | DION                |                   |                  |
| SYC             | ERR            | SRQ          | EV       | X       | IFCR              | IBF               | OBF               | 69H  | Tawai s            | tor1to           | dots n            | OP     | si C i  | С                   | /08C              | 88 C             |
| D7              | is "l"         | set to       | ERROF    | R FLAG* | DBB               | opy in<br>interr  | Do sic            |      | lo each<br>be able | e to d<br>t must | iay tak<br>Ime ou | ITERRU |         | SK 3101             | n hov<br>There    | mili c           |
| х               | X              | USER         | ×        | ×       | TOUT <sub>3</sub> | TOUT <sub>2</sub> | TOUT <sub>1</sub> | 68H  | ofur rug           | SPI              | TCI               | SYC    | OBFI    | IBFI                | 0                 | SRQ              |
|                 |                | CON          | NTROLL   | ER STA  | TUS*              | Real              | RERF -<br>Comma   |      | 8292's             |                  | mented            |        |         |                     |                   |                  |
| CSBS            | CA             | I X 3 I a    | ooxad    | SYCS    | IIIFC             | REN               | SRQ               | 68H  | 101101             | ji 010           | USER              | Is 0.0 | 0.0     | TOUT4               | TOUT <sub>3</sub> | TOUT             |
| nware<br>ed on, | ne rer<br>mask | i ją GF      | PIB (BUS | S) STAT | US*               | Sucrate<br>= lan  | ets TCI           |      | ad by a            | disable<br>comi  | abled/o           |        |         | R <sub>3</sub> m 10 | ne Err            | aluc.<br>dt in t |
| REN             | DAV            | EOI          | Х        | SYC     | IFC               | ANTI              | SRQ               | 68H  | D                  | D                | D                 | D      | D       | D <sub>an</sub>     | Dig               | D                |
| ni ")"          | of le          | EVEN         | T COUN   | TER ST  | ATUS*             |                   | comman            |      |                    |                  | Status            | TIME   | OUT*    | vā ba               |                   | ŽEVC             |
| D               | D              | D            | D        | eRno    | I Par             | P.ne              | P                 | 68H  | D                  | D                | D                 | D      | D       | D                   | D                 | D                |
| -enide          | rop ze         | S   1)<br>IT | ME OU    | T STATU |                   |                   | Comma<br>Dais con |      | mware<br>rupt if   |                  |                   |        |         |                     |                   | ounte<br>nen se  |
| SDC             | ( D            | 1/D          | in Dire  | uniDJ®  | 2 Dvi             | -Di               | lo Diroi          | 68H  |                    |                  | gisters ar        |        |         | a special           |                   |                  |

RIVM — Read Interrupt Mask Register stational September 12.829 September 10 the corresponding bit in the Interrupt Status Register. The command

## Load Error Mask selection acknowledge skeM rorr back

This command loads the Error Mask with D7-D0. Note that D7 must be a zero and that interrupts are enabled by a corresponding "1" bit in this register.

## UTILITY COMMANDS AMMOD KOITARISO

These commands are used to read or write the 8292 registers that are not directly accessible. All utility commands are written with A0 = 1, D7 = D6 = D5 = 1, D4 = 0. D3 - D0 specify the particular command. For writing into registers the general sequence is:

- 1. wait for IBF = 0 in Interrupt Status Register
- 2. write the appropriate command to the 8292,
- 3. write the desired register value to the 8292 with A0 = 1 with no other writes intervening.
- 4. wait for indication of completion from 8292 (IBF = 0).

For reading a register the general sequence is:

- 1. wait for IBF = 0 in Interrupt Status Register
- 2. write the appropriate command to the 8292
- 3. wait for a TCI (Task Complete Interrupt)
- 4. Read the value of the accessed register from the 8292 with A0 = 0.

WEVC — Write to Event Counter (Command = 0E2H)

The byte written following this command will be loaded into the event counter register and event counter status for byte counting. The internal

counter is incremented on a high to low transition of the COUNT (T1) input. In this application example NDAC is connected to count. The counter is an 8 bit register and therefore can count up to 256 bytes (writing 0 to the EC implies a count of 256). If longer blocks are desired, the main CPU must handle the interrupts every 256 counts and carefully observe the timing constraints.

Because the counter has a frequency range from 0 to 133 kHz when using a 6 MHz crystal, this feature may not be usable with all devices on the GPIB. The 8291 can easily transfer data at rates up to 250 kHz and even faster with some tuning of the system. There is also a 500 ns minimum high time requirement for COUNT which can potentially be violated by the 8291 in continuous acceptor handshake mode (i.e., TNDDV1 + TDVND2-C = 350 + 350 = 700 max). When cable delays are taken into consideration, this problem will probably never occur.

When the 8292 has completed the command, IBF will become a "0" and will cause an interrupt if masked on.

WTOUT — Write to Time Out Register (Command = 0E1H)

The byte written following this command will be used to determine the number of increments used for the time out functions. Because the register is 8 bits, the maximum time out is 256 time increments. This

OPIB but is not enough for a manually stepped operation using a GPIB logic analyzer like Ziatech's ZT488. Also, the 488 Standard does not set a lower limit on how long a device may take to do each action. Therefore, any use of a time out must be able to be overridden (this is a good general design rule for service and debugging considerations).

The time out function is implemented in the 8292's firmware and will not be an accurate time. The counter counts backwards to zero from its initial value. The function may be enabled/disabled by a bit in the Error mask register. When the command is complete IBF will be set to a "0" and will cause an interrupt if masked on.

REVC — Read Event Counter Status (Command = 0E3H)

This command transfers the content of the Event Counter to the DBBOUT register. The firmware then sets TCI = 1 and will cause an interrupt if masked on. The CPU may then read the value from the 8292 with A0 = 0.

RINM — Read Interrupt Mask Register (Command = 0E5H)

This command transfers the content of the Interrupt Mask register to the DBBOUT register. The firmware sets TCI = 1 and will cause an interrupt if masked on. The CPU may then read the value.

RERM — Read Error Mask Register (Command = 0EAH)

This command transfers the content of the Error Mask register to the DBBOUT register. The firmware sets TCI = 1 and will cause an interrupt if masked on. The CPU may then read the value.

RCST — Read Controller Status Register (Command = 0E6H)

This command transfers the content of the Controller Status register to the DBBOUT register. The firmware sets TCI = 1 and will cause an interrupt if masked on. The CPU may then read the value.

RTOUT — Read Time Out Status Register (Command = 0E9H)

This command transfers the content of the Time Out Status register to the DBBOUT register. The firmware sets TCI = 1 and will cause an interrupt if masked on. The CPU may then read the value.

If this register is read while a time-out function is in process, the value will be the time remaining before time-out occurs. If it is read after a time-out, it will be zero. If it is read when no time-out is in process, it will be the last value reached when the previous timing occurred.

(Command = UE/H) Are 1909 Harrier

This command causes the firmware to read the GPIB management lines, DAV and the SYC pin and place a copy in DBBOUT. TCI is set to "1" and will cause an interrupt if masked on. The CPU may read the value.

RERF — Read Error Flag Register (Command = 0E4H)

This command transfers the content of the Error Flag register to the DBBOUT register. The firmware sets TCI = I and will cause an interrupt if masked on. The CPU may then read the value.

This register is also placed in DBBOUT by an IACK command if ERR remains set. TCI is set to "1" in this case also

IACK — Interrupt Acknowledge (Command = A1 A2 A3 A4 1 A5 1 1)

This command is used to acknowledge any combinations of the five SPI interrupts (A1-A5): SYC, ERR, SRQ, EV, and IFCR. Each bit A1-A5 is an individual acnowledgement to the corresponding bit in the Interrupt Status Register. The command clears SPI but it will be set again if all of the pending interrupts were not acknowledged.

If A2 (ERR) is "1", the Error Flag register is placed in DBBOUT and TCI is set. The CPU may then read the Error Flag without issuing an RERF command.

### **OPERATION COMMANDS**

The following diagram (Fig. 13) is an attempt to show the interrelationships among the various 8292 Operation Commands. It is not meant to replace the complete controller state diagram in the IEEE Standard.

RST — Reset (Command = 0F2H)

This command has the same effect as an external reset applied to the chip's pin #4. The 8292's actions are:

- All outputs go to their electrical high state. This
  means that SPI, TCI, OBFI, IBFI, CLTH will be
  TRUE and all other GPIB signals will be FALSE.
- 2. The 8292's firmware will cause the above mentioned five signals to go FALSE after approximately 17.5 usec. (at 6 MHz).
- 3. These registers will be cleared: Interrupt Status, Interrupt Mask, Error Mask, Time Out, Event Counter, Error Flag.
- 4. If the 8292 is the System Controller (SYC is TRUE), then IFC will be sent TRUE for approximately 100 usec and the Controller function will end up in charge of the bus. If the 8292 is not the

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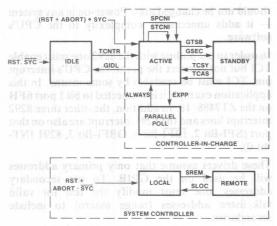


Figure 13. 8292 Command Flowchart

System Controller then it will end up in an Idle state.

5. TCI will not be set.

RSTI — Reset Interrupts (Command = 0F3)

This command clears all pending interrupts and error flags. The 8292 will stop waiting for actions to occur (e.g., waiting for ATN to go FALSE in a TCNTR command or waiting for the proper handshake state in a TCSY command). TCI will not be set.

ABORT — Abort all operations and Clear Interface (Command = 0F9H)

If the 8292 is not the System Controller this command acts like a NOP and flags a USER ERROR in the Error Flag Register. No TCI will occur.

If the 8292 is the System Controller then IFC is set TRUE for approximately  $100^{\circ}$  µsec and the 8292 becomes the Controller-in-Charge and asserts ATN. TCI will be set, only if the 8292 was NOT the CIC.

STCNI — Start Counter Interrupts (Command = 0FEH)

Enables the EV Counter Interrupt. TCI will not be set. Note that the counter must be enabled by a GSEC command.

SPCNI — Stop Counter Interrupts (Command = 0F0H)

The 8292 will not generate an EV interrupt when the counter reaches 0. Note that the counter will continue counting. TCI will not be set.

SREM — Set Interface to Remote Control (Command = 0F8H)

If the 8292 is the System Controller, it will set REN

and TCI TRUE. Otherwise it only sets the User Error Flag.

SLOC — Set Interface to Local Mode (Command = 0F7H)

If the 8292 is the System Controller, it will set REN FALSE and TCI TRUE. Otherwise, it only sets the User Error Flag.

EXPP — Execute Parallel Poll
(Command = 0F5H)

If not Controller-in-Charge, the 8292 will treat this as a NOP and does not set TCI. If it is the Controller-in-Charge then it sets IDY (EOI & ATN) TRUE and generates a local DAV pulse (that never reaches the GPIB because of gates in the 8293). If the 8291 is configured as a listener, it will capture the Parallel Poll Response byte in its data register. TCI is not generated, the CPU must detect the BI (Byte In) from the 8291. The 8292 will be ready to accept another command before the BI occurs; therefore the 8291's BI serves as a task complete indication.

GTSB — Go To Standby (Command = 0F6H)

If the 8292 is not the Controller-in-Charge, it will treat this command as a NOP and does not set TCI TRUE. Otherwise, it goes to Controller Standby State (CSBS), sets ATN FALSE and TCI TRUE. This command is used as part of the Send, Receive, Transfer and Serial Poll System commands (see next section) to allow the addressed talker to send data/status.

If the data transfer does not start within the specified Time-Out, the 8292 sets TOUT2 TRUE in the Error Flag Register and sets SPI (if enabled). The controller continues waiting for a new command. The CPU must decide to wait longer or to regain control and take corrective action.

GSEC — Go to Standby and Enable Counting (Command = 0F4H)

This command does the same things as GTSB but also initializes the event counter to the value previously stored in the Event Counter Register (default value is 256) and enables the counter. One may wire the count input to NDAC to count bytes. When the counter reaches zero, it sets EV (and SPI if enabled) in Interrupt Status and will set EV every 256 bytes thereafter. Note that there is a potential loss of count information if the CPU does not respond to the EV/SPI before another 256 bytes have been transferred. TCI will be set at the end of the command.

TCSY — Take Control Synchronously (Command = 0FDH)

If the 8292 is not in Standby, it treats this command as a NOP and does not set TCl. Otherwise, it waits for the proper handshake state and sets ATN TRUE. The 8292 will set TOUT3 if the handshake never assumes the correct state and will remain in this command until the handshake is proper or a RSTI command is issued. If the 8292 successfully takes control, it sets TCI TRUE.

This is the normal way to regain control at the end of a Send, Receive, Transfer or Serial Poll System Command. If TCSY is not successful, then the controller must try TCAS (see warning below).

### TCAS — Take Control Asynchronously O ton H (Command = 0FCH)

If the 8292 is not in Standby, it treats this command as a NOP and does not set TCI. Otherwise, it arbitrarily sets ATN TRUE and TCI TRUE. Note that this action may cause devices on the bus to lose a data byte or cause them to interpret a data byte as a command byte. Both Actions can result in anomalous behavior. TCAS should be used only in emergencies. If TCAS fails, then the System Controller will have to issue an ABORT to clean things up.

### GIDL — Go to Idle (Command = 0F1H) 8 3 4 1

If the 8292 is not the Controller in Charge and Active, then it treats this command as a NOP and does not set TCI. Otherwise, it sets ATN FALSE, becomes Not Controller in Charge, and sets TCI TRUE. This command is used as part of the Pass Control System Command.

# TCNTR — Take (Receive) Control (Command = 0FAH)

If the 8292 is not Idle, then it treats this command as a NOP and does not set TCI. Otherwise, it waits for the current Controller-in-Charge to set ATN FALSE. If this does not occur within the specified Time Out, the 8292 sets TOUT1 in the Error Flag Register and sets SPI (if enabled). it will not proceed until ATN goes false or it receives an RSTI command. Note that the Controller in Charge must previously have sent this controller (via the 8291's command pass through register) a Pass Control message. When ATN goes FALSE, the 8292 sets CIC, ATN and TCI TRUE and becomes Active.

### SOFTWARE DRIVER OUTLINE

The set of system commands discussed below is shown in Figure 14. These commands are implemented in software routines executed by the main CPU.

The following section assumes that the Controller is the System Controller and will not Pass Control. This is a valid assumption for 99+% of all controllers. It also assumes that no DMA or Interrupts will be used. SYC (System Control Input)

should not be changed after Power-on in any system
— it adds unnecessary complexity to the CPU's software.

In order to use polling with the 8292 one must enable TCI but not connect the pin to the CPU's interrupt pin. TCI must be readable by some means. In this application example it is connected to bit 1 port 6FH on the ZT7488/18. In addition, the other three 8292 interrupt lines and the 8291 interrupt are also on that port (SPI-Bit 2, IBFI-Bit 4, OBFI-Bit 3, 8291 INT-Bit 0).

These drivers assume that only primary addresses will be used on the GPIB. To use secondary addresses, one must modify the test for valid talk/listen addresses (range macro) to include secondaries.

| Talker/Listener                               |                                                                                                                                                           |
|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| SEND<br>RECV                                  | SEND DATA RECEIVE DATA TRANSFER DATA                                                                                                                      |
| Controller                                    | or flags. The 8292 will stop waiting to c.e.r. waiting for ATN to c.                                                                                      |
| TRIG<br>DCLR<br>SPOL<br>PPEN<br>PPDS          | GROUP EXECUTE TRIGGER DEVICE CLEAR SERIAL POLL PARALLEL POLL ENABLE PARALLEL POLL UNCONFIGUR PARALLEL POLL PASS CONTROL RECEIVE CONTROL SERVICE REQUESTED |
| System Controlle                              |                                                                                                                                                           |
| then ISMAR set<br>c and JOOL 992<br>IFCL JOHN | REMOTE ENABLE<br>LOCAL<br>ABORT/INTERFACE CLEAR                                                                                                           |

Figure 14. Software Driver Routines

#### INITIALIZATION

8292 — Comes up in Controller Active State when SYC is TRUE. The only initialization needed is to enable the TCI interrupt mask. This is done by writing 0A0H to Port 68H.

8291 — Disable both the major and minor addresses because the 8291 will never see the 8292's commands/addresses (refer to earlier hardware discussion). This is done by writing 60H and 0E0H to Port 66H.

Set Address Mode to Talk-only by writing 80H to Port 64H.

Set internal counter to 3 MHz to match the clock input coming from the 8085 by writing 23H to Port 65H. High speed mode for the handshakes will not be used here even though the hardware uses threestate drivers.

No interrupts will be enabled now. Each routine will enable the ones it needs for ease of polling operation. The INT bit may be read through Port 6FH. Clear both interrupt mask registers.

Release the chip's initialization state by writing 0 to Port 65H.

INIT:

Enable-8292 Enable TCI Enable-8291

Disable major address Disable minor address

Clock frequency All interrupts off

Immediate execute pon

:Set up Int. pins for Port 6FH ;Task complete must be on

;In controller usage, the 8291

:Is set to talk only and/or listen only

:Talk only is our rest state

;3 MHz in this ap note example

:Releases 8291 from init. state

### TALKER/LISTENER ROUTINES

### Send Data

SEND < listener list pointer > < count > < EOS > < data buffer pointer >

This system command sends data from the CPU to one or more devices. The data is usually a string of ASCII characters, but may be binary or other forms as well. The data is device-specific.

My Talk Address (MTA) must be output to satisfy the GPIB requirement of only one talker at a time (any other talker will stop when MTA goes out). The MTA is not needed as far as the 8291 is concerned it will be put into talk-only mode (ton).

This routine assumes a non-null listener list in that it

always sends Universal Unlisten. If it is desired to send data to the listeners previously addressed, one could add a check for a null list and not send UNL. Count must be 255 or less due to an 8 bit register. This routine also always uses an EOS character to terminate the string output; this could easily be eliminated and rely on the count. Items in brackets () are optional and will not be included in the actual code in Appendix A.

Figure 16, SEND to "1", "2" ">"; ": GW72 EOS = "D"

Output-to-8291 MTA, UNL Put EOS into 8291 While  $20H \le listener \le 3EH$ output-to-8291 listener Increment listen list pointer Output-to-8292 GTSB Enable-8291

Output EOI on EOS sent If count < > 0 then

While not (end or count = 0) of isages blue (could check tout 2 here) chapter X

od 11 oca od Output-to-8291 data Increment data buffer pointer Decrement count

enoted previo Output-to-8292 TCSYoutis reduction ed videdorg (If tout3 then take control async) ed

left in a strange state and 1928 aldard be cleared by No output EOI on EOS sent therefore used as an error nrutaRion in most

;We will talk, nobody listen :End of string compare character GPIB listen addresses are "space" thru ">" ASCII :Address all listeners

;8292 stops asserting ATN, go to standby

;Send EOI along with EOS character

;Wait for EOS or end of count Optionally check for stuck bus-tout 2 Output all data, one byte at a time ;8085 CREG will count for us

;8292 asserts ATN, take control sync. ;If unable to take control sync. Restore 8291 to standard condition

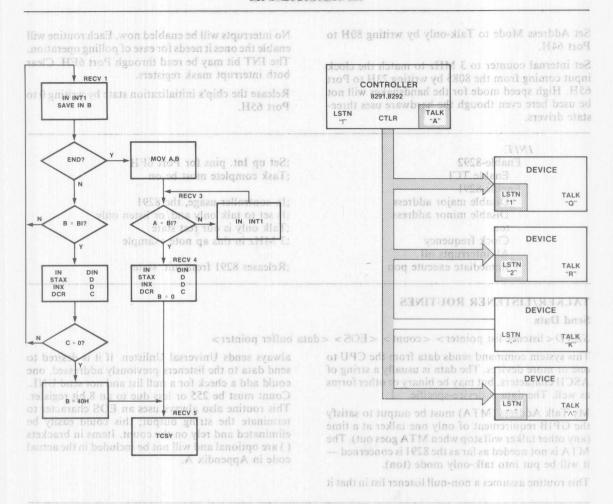


Figure 15. Flowchart For Receive Ending Conditions

We will talk, nobody listen F. and of string compare char (GPIB listen addresses are "space" thru ">" ASCII (Address all listeners (S292 stops asserting ATN).

#### Receive Data

RECV < talker > < count > < EOS > < data buffer pointer >

This system command is used to input data from a device. The data is typically a string of ASCII characters.

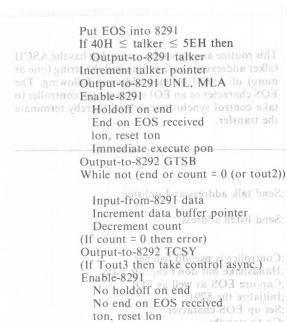
This routine is the dual of SEND. It assumes a new talker will be specified, a count of less than 257, and an EOS character to terminate the input. EOI received will also terminate the input. Figure 15 shows the flow chart for the RECV ending conditions. My Listen Address (MLA) is sent to keep the GPIB transactions totally regular to

Figure 16. SEND to "1", "2", ">"; "ABCD"; EOS = "D"

Put FOS into 8291
While 20H ≤ listener ≤ 3EH
output-to-8291 listener
Increment listen list pointer
Output-to-8292 GTSB
Enable-8291
Output EOI on EOS sent
If count < > 0 then

facilitate analysis by a GPIB logic analyzer like the Ziatech ZT488. Otherwise, the bus would appear to have no listener even though the 8291 will be listening.

Note that although the count may go to zero before the transmission ends, the talker will probably be left in a strange state and may have to be cleared by the controller. The count ending of RECV is therefore used as an error condition in most situations.



Finish handshake

Figure 17. RECV from "R"; EOS = 0DH

Immediate execute pon

Return error-indicator lorinos control

;End of string compare character :GPIB talk addresses are I his system command is used to IDSA "A" and to "";" and to "";" ;Do this for consistency's sake one to ano or realist Everyone except us stop listening lours of 2005 data. This is accomplished through the use of the Stop when EOS character is our sucurimos 21908 :Detected by 8291 :Listen only (no talk) ;8292 stops asserting ATN, go to standby :wait for EOS or EOI or end of count optionally check for stuck bus-tout2

input data, one byte at a time :Use 8085 C register as counter ;Count should not occur before end ;8292 asserts ATN take control sloans :If unable to take control sync. ;Put 8291 back as needed for

;Complete holdoff due to end, if any ;Needed to reset lon

;Clear holdoff due to end

:Controller activity and

Finish handshake NOT END ON ECHANDONTHOO CONTROLLER 8291,8292 8291.8292 CTLR STITALK LSTN LSTN TALK CTLR DEVICE DEVICE IOS TALK LSTN TALK DEVICE DEVICE oup execute TALK ent to all device n the listener DEVICE DEVICE LSTN LSTN TALK TALK :Everybody stop listening DEVICE ck fogoivage listen address LSTNE NO STITALK LSTN TALK "\/"

2-374

Figure 18. XFER from " \" to "1", "2", "+"; EOS = 0DH

This system command is used to transfer data from a talker to one or more listeners where the controller does not participate in the transfer of the ASCII data. This is accomplished through the use of the 8291's continuous acceptor handshake mode while in listen-only.

This routine assumes a device list that has the ASCII talker address as the first byte and the string (one or more) of ASCII listener addresses following. The EOS character or an EOI will cause the controller to take control synchronously and thereby terminate the transfer. bovisos 203 no ball

wait for EOS or EOI of end of exact XFER: Output-to-8291: Talker, UNL While  $20H \le listen \le 3EH$ Output-to-8291: Listener Increment listen list pointer Enable-8291 TA Present COLS

lon, no ton If unable to take cont Continuous AH mode Immediate execute PON End on EOS received Put EOS into 8291 Output-to-8292: GTSB blod stellamo

Upon end (or tout2) then Take control synchronously Enable-8291 Finish handshake Not continuous AH mode Not END on EOS received

Immediate execute pon Return

;Send talk address and unlisten

;Send listen address

;Controller is pseudo listener ;Handshake but don't capture data ;Capture EOS as well as EOI :Initialize the 8291 ;Set up EOS character :Go to standby ;8292 waits for EOS or EOI and then

:Regains control ;Go to Ready for Data

#### CONTROLLER

Group Execute Trigger

TRIG < Listener list >

This system command causes a group execute trigger (GET) to be sent to all devices on the listener

list. The intended use is to synchronize a number of instruments.

#### TRIG:

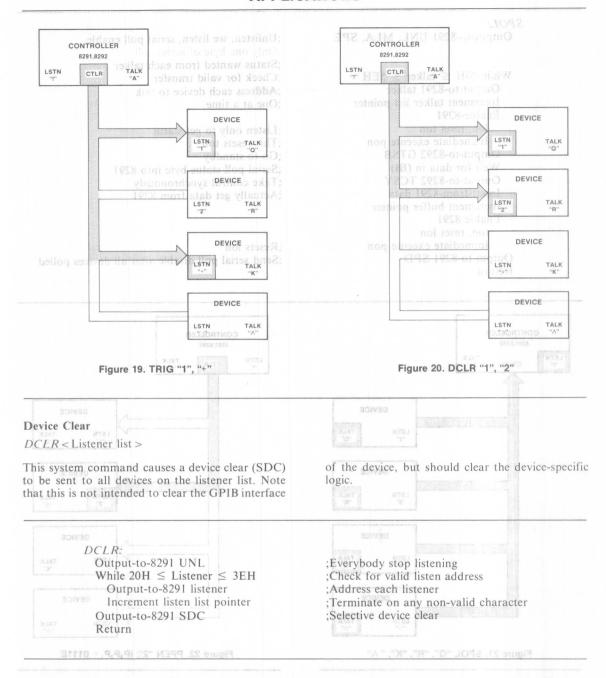
Output-to-8291 UNL While 20H ≤ listener ≤ 3EH Output-to-8291 Listener Increment listen list pointer Output-to-8291 GET Return

:Everybody stop listening :Check for valid listen address

:Address each listener

Terminate on any non-valid character

;Issue group execute trigger



#### Serial Poll

SPOL < Talker list > < status buffer pointer >

This system command sequentially addresses the designated devices and receives one byte of status from each. The bytes are stored in the buffer in the

same order as the devices appear on the talker list. MLA is output for completeness.

#### SPOL:

Output-to-8291 UNL, MLA, SPE

While 40H ≤ talker ≤ 5EH
Output-to-8291 talker
Increment talker list pointer
Enable-8291
lon, reset ton
Immediate execute pon
Output-to-8292 GTSB
Wait for data in (BI)
Output-to-8292 TCSY
Input-from-8291 data
Increment buffer pointer
Enable 8291

Increment buffer pointer Enable 8291 ton, reset lon Immediate execute pon Output-to-8291 SPD Return ;Unlisten, we listen, serial poll enable;Only one byte of serial poll

;Status wanted from each talker

;Check for valid transfer ;Address each device to talk

One at a time

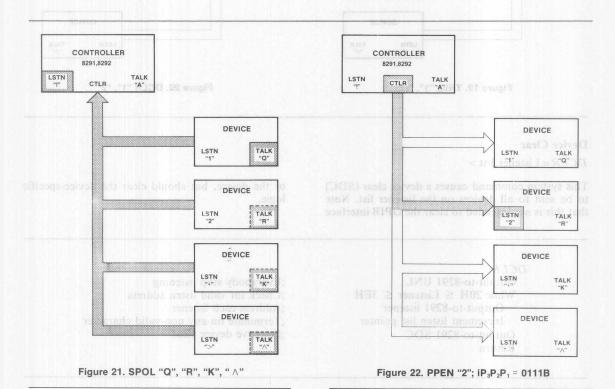
;Listen only to get status ;This resets ton ;Go to standby

;Serial poll status byte into 8291 ;Take control synchronously

Actually get data from 8291

:Resets lon

;Send serial poll disable after all devices polled



#### Parallel Poll Enable

PPEN < Listener list > < Configuration Buffer pointer >

This system command configures one or more devices to respond to Parallel Poll, assuming they implement subset PP1. The configuration information is stored in a buffer with one byte per device in the same order as devices appear on the listener

list. The configuration byte has the format XXXXIP3P2P1 as defined by the IEEE Std. P3P2P1 indicates the bit # to be used for a response and I indicates the assertion value. See Sec. 2.9.3.3 of the Std. for more details

#### PPEN:

Output-to-8291 UNL While  $20H \le Listener \le 3EH$ Output-to-8291 listener Output-to-8291 PPC, (PPE or data) Increment listener list pointer Increment buffer pointer Return

:Universal unlisten

:Check for valid listener

;Stop old listener, address new

;Send parallel poll info vd control lls lo senonces

:Point to next listener One configuration byte per listener

## Parallel Poll Disable

PPDS < listener list >

This system command disables one or more devices from responding to a Parallel Poll by issuing a Parallel Poll Disable (PPD). It does not deconfigure the devices. As possess between no matters shift

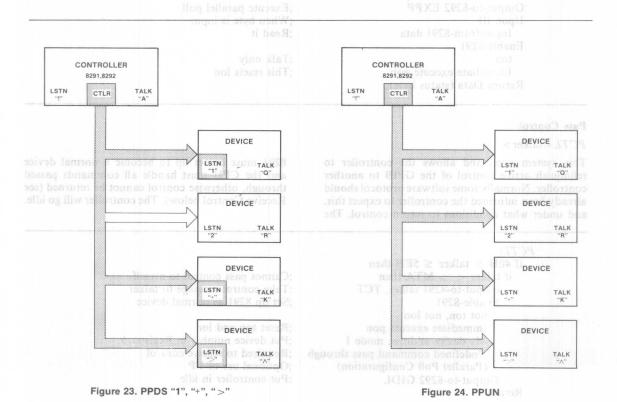
will still be set when the next Pacally Poll occurs.
This command recent the byte SQAP is. Output-to-8291 UNL brismmos and T While  $20H \le Listener \le 3EH$ Output-to-8291 listener Increment listener list pointer Output-to-8291 PPC, PPD/Ino notal 1 Return

;Universal Unlisten

;Check for valid listener

:Address listener

;Disable PP on all listeners



#### Parallel Poll Unconfigure

#### PPUN

This system command deconfigures the Parallel Poll response of all devices by issuing a Parallel Poll Unconfigure message.

#### PPUN:

Output-to-8291 PPU Return

#### :Unconfigure all parallel poll

#### Conduct a Parallel Poll

## Parallel Poll Disable (PPD). It does not JOSA

This system command causes the controller to conduct a Parallel Poll on the GPIB for approximately 12.5 usec (at 6 MHz). Note that a parallel poll does not use the handshake; therefore, to ensure that the device knows whether or not its positive response was observed by the controller, the CPU should explicitly acknowledge each device by a devicedependent data string. Otherwise, the response bit will still be set when the next Parallel Poll occurs. This command returns one byte of status.

#### PPOL:

Enable-8291

Immediate execute pon

Output-to-8292 EXPP

Upon BI

Input-from-8291 data

Enable-8291

Immediate execute pon Return Data (status byte) Output-to-8291 PPC, PPLylno notice.

This resets ton

Execute parallel poll

;When byte is input

:Read it

:Talk only

;This resets lon

#### Pass Control

#### PCTL < talker >

This system command allows the controller to relinquish active control of the GPIB to another controller. Normally some software protocol should already have informed the controller to expect this, and under what conditions to return control. The 8291 must be set up to become a normal device and the CPU must handle all commands passed through, otherwise control cannot be returned (see Receive Control below). The controller will go idle.

#### PCTL:

If  $40H \le talker \le 5EH$  then if talker < > MTA then output-to-8291 talker, TCT

Enable-8291

not ton, not lon

Immediate execute pon

My device address, mode 1 Undefined command pass through

(Parallel Poll Configuration)

Output-to-8292 GIDL

Return 99 . AS supia

:Cannot pass control to myself

;Take control message to talker

Set up 8291 as normal device

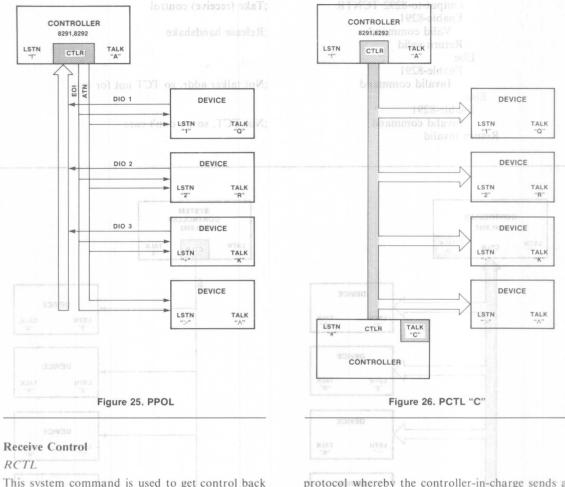
:Reset ton and lon

;Put device number in Register 6

Required to receive control

:Optional use of PP

;Put controller in idle



This system command is used to get control back from the current controller-in-charge if it has passed control to this inactive controller. Most GPIB systems do not use more than one controller and therefore would not need this routine.

To make passing and receiving control a manageable event, the system designer should specify a

protocol whereby the controller-in-charge sends a data message to the soon-to-be-active controller. This message should give the current state of the system, why control is being passed, what to do, and when to pass control back. Most of these issues are beyond the scope of this Ap Note.

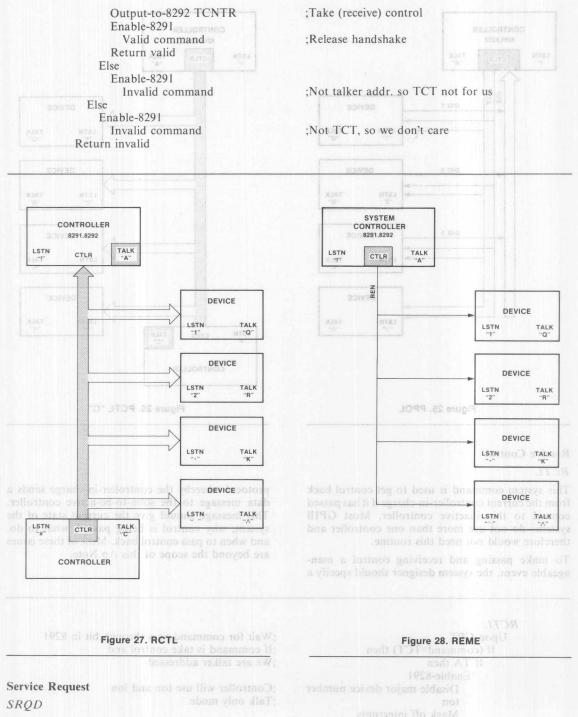
```
RCTL:
Upon CPT
If (command=TCT) then
If TA then
Enable-8291
Disable major device number ton
Mask off interrupts
Immediate execute pon
```

;Wait for command pass through bit in 8291 ;If command is take control and

;We are talker addressed

;Controller will use ton and lon ;Talk only mode

This system command is used to detect the occurrence of a Service Request on the GPIB. One or



This system command is used to detect the occurrence of a Service Request on the GPIB. One or more devices may assert SRQ simultaneously, and

the CPU would normally conduct a Serial Poll after calling this routine to determine which devices are SRQing.

SROD: If SRQ then :Test 92 status bit Output-to-8292 IACK.SRQ ;Acknowledge it Return SRO Else return no SRQ SYSTEM CONTROLLER Remote Enable REMEremote until they are later addressed to listen by This system command asserts the Remote Enable line (REN) on the GPIB. The devices will not go some other system command. REME: Output-to-8292 SREM :8292 asserts remote enable line nrutan In, etc. The only difficulty lies un integ routines into the overall system's interrupt strulated This is highly situation executic and is bey 1301 This system command deasserts the REN line on the GPIB. The devices will go local immediately. code and provide for the corresponding interrupt to bring the control back to the nex LOOL not GPIB ;8292 stops asserting remote enable and radio made Output-to-8292 SLOC 8291) would be replaced by hay arrupa BO interrupt STRUCTURE WIll then be act valed act water such things as 8292 Tasi SYSTEM CONTROLLER 8291,8292 LSTN TALK LSTN TALK CTLB CTLB DEVICE DEVICE LSTN TALK LSTN TALK 761 -<sub>4</sub> DEVICE DEVICE LSTN LSTN TALK TALK DEVICE DEVICE

Figure 29. LOCL O to wolf enthur 8 content 8190 .18 stuffigure 30. IFCL

LSTN

LSTN

DEVICE

TALK

TALK

TALK

LSTN

LSTN

DEVICE

#### Interface Clear/Abort

**IFCL** 

This system command asserts the GPIB's Interface Clear (IFC) line for at least 100 microseconds. This causes all interface logic in all devices to go to a known state. Note that the device itself may or

may not be reset, too. Most instruments do totally reset upon IFC. Some devices may require a DCLR as well as an IFCL to be completely reset. The (system) controller becomes Controller-in-Charge.

IFCL:
Output-to-8292 ABORT
Return

;8292 asserts Interface Clear :For 100 microseconds

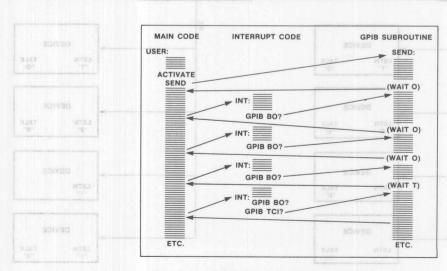
#### INTERRUPTS AND DMA CONSIDERATIONS

The previous sections have discussed in detail how to use the 8291, 8292, 8293 chip set as a GPIB controller with the software operating in a polling mode and using programmed transfer of the data. This is the simplest mode of use, but it ties up the microprocessor for the duration of a GPIB transaction. If system design constraints do not allow this, then either Interrupts and/or DMA may be used to free up processor cycles.

The 8291 and 8292 provide sufficient interrupts that one may return to do other work while waiting for such things as 8292 Task Completion, 8291 Next Byte In, 8291 Last Byte Out, 8292 Service Request

In, etc. The only difficulty lies in integrating these various interrupt sources and their matching routines into the overall system's interrupt structure. This is highly situation-specific and is beyond the scope of this Ap Note.

The strategy to follow is to replace each of the WAIT routines (see Appendix A) with a return to the main code and provide for the corresponding interrupt to bring the control back to the next section of GPIB code. For example WAITO (Wait for Byte Out of 8291) would be replaced by having the BO interrupt enabled and storing the (return) address of the next instruction in a known place. This co-routine structure will then be activated by a BO interrupt. Fig. 31 shows an example of the flow of control.



1071 66 Stuffigure 31. GPIB Interrupt & Co-Routine Flow of Control . 65 Stup 13

DMA is also useful in relieving the processor if the average length of a data buffer is long enough to overcome the extra time used to set up a DMA chip. This decision will also be a function of the data rate of the instrument. The best strategy is to use the DMA to handle only the data buffer transfers on SEND and RECV and to do all the addressing and control just as shown in the driver descriptions.

Another major reason for using a DMA chip is to increase the data rate and therefore increase the overall transaction rate. In this case the limiting factor becomes the time used to do the addressing and control of the GPIB using software like that in Appendix A. The data transmission time becomes insignificant at DMA speeds unless extremely long buffers are used.

Refer to Figure 11 for a typical DMA and interrupt based design using the 8291, 8292, 8293. A system we like this can achieve a 250K byte transfer rate while under DMA control.

## APPLICATION EXAMPLE TS no sess, 1858 1911

This section will present the code required to operate a typical GPIB instrument set up as shown in Fig. 32. The HP5328A universal counter and the HP3325 function generator are typical of many GPIB devices; however, there are a wide variety of software protocols to be found on the GPIB. The Ziatech ZT488 GPIB analyzer is used to single step the bus to facilitate debugging the system. It also serves as a training/familiarization aid for new-comers to the bus.

This example will set up the function generator to each terms output a specific waveform, frequency and ampli-

tude. It will then tell the counter to measure the frequency and Request Service (SRQ) when complete. The program will then read in the data. The assembled source code will be found at the end of Appendix A.

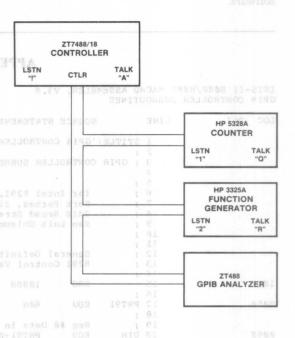


Figure 32. GPIB Example Configuration

#### SEND

LSTN: "2", COUNT: 15, EOS: 0DH, DATA: "FUIFR37KHAM2VO (CR)" :SETS UP FUNCTION GEN. TO 37 KHZ SINE. 2 VOLTS PP

COUNT EQUAL TO # CHAR IN BUFFER

;EOS CHARACTER IS (CR) = 0DH = CARRIAGE RETURN

#### SEND

LSTN: "1", COUNT: 6, EOS: "T" DATA: "PR4G7T"

;SETS UP COUNTER FOR P:INITIALIZE, F4: FREQ CHAN A

; vino mater G7:0.1 HZ RESOLUTION, T:TRIGGER AND SRO WOT

COUNT IS EQUAL TO # CHAR

#### WAIT FOR SRO not polasenbbs I show

SPOL TALK: "Q", DATA: STATUS 1

;CLEARS THE SRO - IN THIS EXAMPLE ONLY FREQ CTR ASSERTS SRQ

RECV TALK: "Q", COUNT: 17, EOS: 0AH,

DATA: " + 37000.0E+0" (CR) (LF)

GETS 17 BYTES OF DATA FROM COUNTER

COUNT IS EXACT BUFFER LENGTH

DATA SHOWN IS TYPICAL HP5328A READING THAT WOULD BE RECEIVED.

#### and conclusion of CONCLUSION of the of the

This Application Note has shown a structured way to view the IEEE 488 bus and has given typical code sequences to make the Intel 8291, 8292, and 8293's behave as a controller of the GPIB. There are other ways to use the chip set but whatever solution is chosen, it must be integrated into the overall system software

0023

The ultimate reference for GPIB questions is the IEEE Std 488, -1978 which is available from IEEE. 345 East 47th St., New York, NY, 10017. The ultimate reference for the 8292 is the source listing for it (remember it's a pre-programmed UPI-41A) which is available from INSITE. Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051.

factor becomes the time used to do the address XIDNAPPAA and control of the GPIB using software like the XIDNAPPAA Appendix A. The data transmission time becomes ISIS-II 8080/8085 MACRO ASSEMBLER, V3.0 insignificant at DMA speeds unless extremely long GPIB CONTROLLER SUBROUTINES OBJ LINE SOURCE STATEMENT based design using the 8291, 8292, 8290's SUTTUORBUS RELIGIOR OF BITTE 2 GPIB CONTROLLER SUBROUTINES 3 5 for Intel 8291, 8292 on ZT 7488/18 A FORTADIAGA 6 Bert Forbes, Ziatech Corporation 7 . GENERATOR 8 San Luis Obispo, CA, USA 93461 28 Qui 152 Insmuniami 8190 (spidy) 8 9 10 : General Definitions & Equates 11 12 : General Definitions & Estaples 3 and General G 13: 14 : For ZT7488/18 w/8085 Jane 3190 884TE dostal 1000 V AMA 800 15 ORG the bus to facilitate debugging the Port # 1 2012 and the 1829; 16: 0050 17 PRT91 FOU 60H serves as a training familiarization aid 18 ; 19 ; Reg #Ø Data in & Data out 9969 20 DIN FOU PRT91+0 ;91 Data in reg This example will set up the functionation out of 1919 at 1919 This example will set up the functional set up the function of the set up the function of the set up the function of the set up the set 0060 21 DOUT EQU 22 3 8190 23 ; Reg # 1 Interrupt 1 Constants 9951 24 INT1 EOU PRT91+1 :INT Reg 1 0061 25 INTM1 EOU PRT91+1 ; INT Mask Reg. 1 9992 02 ;91 BO INTRP Mask 01 ;91 BI INTRP Mask 10H ;91 END INTRP Mask 26 BOM EQU. agai 27 BIM EOU 28 ENDMK EOU 0010 0080 29 CPT EQU 80H 93:91 command pass thru int bit EOS CHARACTER IS (CR) = ODH = CARRIAGE 2# pag 30 ; 31 : 9962 32 INT2 EQU PRT91+2 33 ; 34 : Reg #4 Address Mode Constants PRT91+4 ;91 address mode register # 30 2132 9964 35 ADRMD EQU aasa 36 TON OS EOU 80H ;91 talk only mode & not listen only 0040 37 LON ;91 listen only & not ton 2 TAUOD: EOU 4 aH SOCO 38 TLON EQU ØCØH ;91 talk & listen only 0001 39 MODE 1 EQU 01 ; mode 1 addressing for device 07 TIAW 40 41 ; Reg #4 (Read) Address Status Register 0064 OSE AT 42 ADRST PRT91+4 ; reg #4 2HHT MI - ORS 3HT SRAEJD; EOUS 0020 43 EOIST EOU 2ØH 0002 44 TA EQU 0001 45 LA EOU ; listener active ( ) ANTE 46; 47 ; Reg #5 (Write) Auxillary Mode Register PRT91+5 ;91 auxillary mode register # 0065 48 AUXMD EQU

CHANGE AND CLIKET WEOUT 23H A 1913 Mhz clock input WOHE ATAC

```
03 MMOO will finingh handshake command
                  50 FNHSK
                            EOU
                                06 ;91 send EOI with next byte
83H ;91 aux. req A pattern
9996
                  51 SDEOI
                            FOU
   ;91 aux. reg A pattern
0280
                  52 AXRA
                            EOU
                            EQU :91 hold off handshake on all bytes
EQU :91 hold off handshake on end
                  53 HOHSK
9991
                 54 HOEND
                            EQU 2
0002
0003
                55 CAHCY
56 EDEOS
                            EQU 3
  ;91 continuous AH cycling
   ;91 end on EOS received
9994
                            EQU 4
                            EQU 8
EQU ØFH
   ;91 output EOI on EOS sent
aaaa
                  57 EOIS
agar
                  58 VSCMD
   ;91 valid command pass through
                59 NVCMD
                                SISO Ø7H
9997
   ;91 invalid command pass through
                            EOU
                                07H
0A0H
   ; Aux. reg. B pattern
BABB
                  60 AXRB
                            EQU
                                    Ø1H
                  51 CPTEN
9991
                            EQU
  ; command pass thru enable
                  62 iphalwor
                            Reg #5 (Read) H88 U03 XDAI 381
                  54 CPTRG
0265
                            EQU PRT91+5
                  65 ;
66 ;
                            Reg #6 Address 0/1 reg. constants
                 67 ADRØ1 EQU
68 DTDL1 EQU
0065
                                   PRT91+6
                                    60H ;Disable major talker & listener
9969
     70 FOUL PRT91+7 HAS USA THE FOLLOWING THE PRT91+7
                  69 DTDL2 EQU MEMH Disable minor talker & listener
           0067
          UO3 (980 in til 08) 8292 CONTROL VALUES
                  76;
                  77 ;
                  78 ;
                          EQU PRT91+8 ;8292 Base Port # (CS7)
                  79 PRT92
0068
                  80 :
                            EQU 1993 PRT92+0 ;92 INTRP Mask Reg JVU NACL
                  81 INTMR
0068
MANN
                  82 INTM
                            EQU NANH ;TCI
                  83 .
                            EQU
                  84 ERRM
                                    PRT92+0 ;92 Error Mask Reg
9968
                                    01 ;92 Time Out for Pass Control
02 ;92 Time Out for Standby
04 ;92 Time Out for Take Control Sync
                  85 TOUT1
                            EOU
                  86 TOUT?
0002
                            EOU
                  87 TOUT3
0004
                            EOU
                                    PRT92+0 ;92 Event Counter Pseudo Reg
9968
                  88 EVREG
                            EOU
                  89 TOREG
2068
                                PRT92+0 ;92 Time Out Pseudo Reg
                            EQU
                  90 ;
                            EQU
               91 CMD92
                                    PRT92+1 ;92 Command Register
                  92;
                                    PRT92+1 ;92 Interrupt Status Reg
0069
                  93 INTST
0010
                  94 EVBIT
                            EQU
                                    10H ; Event Counter Bit
   ;Input Buffer Full Bit
0002
                  95 IBFBT
                            EQU
                                    02
  ;Seq bit MACRO STEE 801
0020
                  95 SROBT
                            EQU
                                    20H
                  97 ;
                                    PRT92+0 ;92 Error Flag Pseudo Reg
9968
                  98 ERFLG
                            EQU
9968
                  99 CLRST
                            EQU
                                    PRT92+0 ;92 Controller Status Pseudo Reg
9968
                 100 BUSST
                            EQU
                                    PRT92+0 ;92 GPIB (Bus) Status Pseudo Reg
0068
                            EOU
                                    PRT92+0 ;92 Event Counter Status Pseudo Reg
                 101 EVCST
0068
                 102 TOST EQU
                                   PRT92+0 ;92 Time Out Status Pseudo Reg
                 103 : 300 8292
                      OPERATION COMMANDS ST TTI
                 105 ; nisps
                 106 ;
                                    ØFØH ;Stop Counter Interrupts
ggra
                 107 SPCNI EQU
OOFI
                 108 GIDL
                            EQU
                                    ØF1H
  ;Go to idle am TTTAW 181
             109 RSET
00F2
                                    ØF2H
   ;Reset
                            EQU
   Reset Interrupts
aaF3
                                ог эн
Ог эн
               110 RSTI
                            EOU
ØØF4
                111 GSEC
                            EOU
                                    ØF4H
   ;Goto standby, enable counting
   Execute parallel pollagi
00F5
                112 EXPP
                            EQU ØF5H
               113 GTSB
                                ØF6H
   ;Goto standby
;Set local mode , TRI
ØØF6
                            EOU
               114 SLOC
ØØF7
                                    ØF7H
                            EQU
               115 SREM
gars.
                                    ØF8H
  ;Set interface to remote
                            EOU
                                ØF9H
gar9
            116 ABORT
117 TCNTR
  ;Abort all operation, clear interface
                            EQU
   ; Take control (Receive control)
ØØFA
                                    ØFAH
                            EOU
                            EQU 0FAH ;Take control (Receive cont
EQU 0FCH ;Take control asyncronously
EQU 0FEH ;Take control syncronously
EQU 0FEH ;Start counter interruots
ØØFC
                 118 TCASY
   ; Take control asyncronously
MAFD
                 119 TCSY
                 120 STCNI
                 121 ;
                 122 ;
```

```
00E1
00E2
127 WEVC EQU 0E2H ;Write to event counter
00E3
128 REVC EQU 0E3H ;Read event counter status
00E4
129 RERF EQU 0E4H ;Read error flag reg
00E5
130 RINM EQU 0E5H ;Read interrupt mask reg
00E6
131 RCST EQU 0E6H ;Read controller status reg
00E7
00E9
132 RBST EQU 0E7H ;Read GPIB Bus status reg
00E9
133 RTOUT EQU 0E9H ;Read timeout status reg
00EA
134 RERM EQU 0EAH ;Read error mask reg
00EA
135 IACK EQU 0BH ;Interrupt Acknowledge
136;
137;
138; PORT F BIT ASSIGNMENTS
139;
140;
                       67 ADRW1 EQU PRT91+6 ; 041 ; 041 58 DTDL1 EQU 588 rDisable major talker; 141stener
                      142 PRTF EQU PRT91+0FH ;ZT7488 port 6F for interrupts
  MASE
                      142 PRTF EQU PRT91+0FH ; ZT7488 port 6F for interr 143 TCIF EQU 02H ; Task complete interrupt 144 SPIF EQU 04H ; Special interrupt 145 OBFF EQU 08H ; 92 Output (to CPU) Buffer full 146 IBFF EQU 10H ; 92 Input (from CPU) Buffer empty 147 BOF EQU 01H ; 91 Int line (BO in this case) 148 ; GPIB MESSAGES (COMMANDS)
  0002
 0004
 0008
 0010
 9991
                150;
151 MDA EQU 1 ;My device address is 1
152 MTA EQU MDA+40H; My talk address is 1 ("A")
153 MLA EQU MDA+20H; My listen address is 1 ("!")
154 UNL EQU 3FH; Universal unlisten
155 GET EQU 08 ;Group Execute Trigger
156 SDC EQU 04H; Device Clear
157 SPE EQU 18H; Serial poll enable
158 SPD EQU 19H; Serial poll disable
159 PPC EQU 05; Parallel poll configure
160 PPD EQU 70H; Parallel poll disable
161 PPE EQU 60H; Parallel poll disable
162 PPU EQU 69; Take control (pass control)
164
165; MACRO DEFINITIONS
                                150;
 0001
 9941
  0021
 003F
 2008
 0004
 0018
 0019
 0005
 0070
 0060
 0015
  0009
                                  168 ;
169 SETF MACRO ;Sets flags on A register
                      173 WAITO MACRO
LOCAL WAITL
175 WAITL: IN INT1 ;Get Intl status
176 ANI BOM ;Check for byte out
177 JZ WAITL ;If not, try again
179 ;
                                 :Step Counter Interru; 081
                                  181 WAITI MACRO
  ;Wait for 91 hyte to be input
                         182 LOCAL WAITL
183 WAITL: IN INT1
184 MOV B,A
185 ANI BIM
  Get INTl status ITEM UII
  ;Save status in B
;Check for byte in
  ;Check for byte in ;If not, just try again ;until it is
                                  186 JZ WAITL
                                 187 ENDM
            189 WAITX MACRO
190 LOCAL WAITL
191 WAITL: IN PRTF
192 ANI TCIF
  ;Wait for 92's TCI to go false
  119 TONE EQU DECH
                                  193 JNZ WAITL
                                 194 ENDM
                                 195 ;
```

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```
MACRO
   196 WAITT
   197
  LOCAL WAITL
  198 WAITL: IN PRTF ;Get task complete int,etc.
   ANI TCIF ; Mask it J. WAITL ; Wait for task to be complete
   199
                    cause tidate to be sent
  JZ
  201 wilos --
  ENDM sold d
  MACRO LOWER, UPPER, LABEL
   203 RANGE
   Checks for value in range
  204
  ; branches to label if not
  205
  206
  ; in range. Falls through if
  207
  ;lower <= ( (H)(L) ) <= upper.
  208
209 MOV AA, M
210 CPI LOWER TUO TUO
   A, MOST TUCK TUCK TO ESC.
   210 CPI LOWER
211 JM LABEL
212 CPI UPPER+1
213 JP LABEL
214 ENDM
  ENDM
   218
   219
   219;
220; All of the following routines have these common
221; assumptions about the state of the 8291 & 8292 upon entry
  222; to the routine and will exit the routine in an identical state.
  223 :> ( (J) (H) ) => rewol
  224 ;
   8291: BO is or has been set,
  All interrupts are masked off
TON mode, not LA
No holdoffs in effect or enabled to the state of 
  225 ;
  226 ;
  227 ;
  228 ;
   229;
   No holdoffs waiting for finish command
   230 steer previous
  None
  1000 3EA0 248 INIT: MVI A,INTM ;Enable TCI 1002 D368 249 OUT ADR01 1006 D366 251 OUT ADR01 1008 3EE0 252 MVI A,DTDL1;Disable major talker/lister 1006 D366 253 OUT ADR01 1008 3EE0 252 MVI A,DTDL2;Disable minor talker/lister 1000 3E80 254 MVI A,DTDL2;Talk only mode 1000 D364 255 OUT ADR01 ;Talk only mode 1000 D364 255 OUT ADR01 1000 D365 257 
  OUT
  1014 AF
    1015 D361
    1017 D362
    1019 D355
   262 OUI STANDS THE POWER STANDS THE POWE
    101B C9
   268 ; SEND ROUTINE 269 :
```

```
276; OUTPUTS: none CALLS: none DESTROYS: A, C, DE, HL, F
  gin range. Falls through
  OUT DOUT ; Send MTA to turn off any previous talker

284 WAITO
285+??0001: IN INT1 ; Get Intl status
286+ ANI BOM ; Check for byte out
287+ JZ ??0001 ; If not, try again
288 MVI A,UNL ; Send MTA to turn off any previous talker

289 OUT DOUT ; To stop previous listeners
290 MOV A,B ; Get EOS character
291 OUT EOSR ; Output it to door
      101C 3E41
      101E D350
      1020 DB61
       1022 E602
       1024 CA2010
      1027 3E3F
       1029 D360
       1028 78
      102C D357
292 SEND1: RANGE 20H,3EH,SEND2 ;Check next listen address now 2944 and send of the control of th
  297+
   ;lower <= ( (H)(L) ) <= upper.
     | 102E 7E | 299+ | MOV = 09A, M = 116 | 11A | 11
   303+ JP SEND2
304 WAITO
305+??0002: IN INT1 ,Get Intl status
306+ ANI BOM ;Check for byte out
307+ JZ ??0002; If not, try again
308 GOUT DOUT ;Get this listener
309 OUT DOUT ;Output to GPIB
310 INX H
311 JMP SENDI ;Increment listener list pointer
312 ;Enable 91 ending conditions
313 SEND2: WAITO ;Wait for lstn addr accepted
314+??0003: IN INT1 ;Get Intl status
       103B E602
       103D CA3910
       1040 7E
        1041 D360
       1043 23
      1044 C32E10
  313 SEND2: WAITO
314+??0003: IN INT1 ;Get Intl status
315+ ANI BOM ;Check for byte out
316+ JZ ??0003 ;If not, try again
317 ;WAITO required for early versions
318 ;of 8292 to avoid GTSB before DAC
      1047 DB61
      1049 E502
       104B CA4710
  104E 3EF6
   1050 D369
      1052 3E88
   322 OUT AUXMD ; Wait for TCI to go false 324+??9994: IN PRTF 325+ ANI TCIF 1326+ JNZ ??9994
      1054 D365
      1055 DB6F
      1058 E602
      105A C25510
   327 WAITT ; Wait for TCI on GTS8
328+??0005: IN PRTF ; Get task complete int,etc.
      105D DB6F
  329+ ANI TCIF ; Mask it 330+ JZ ??0005 ; Wait for task to be complete
      105F E602
      1061 CA5D10
   330+
331

332; delete next 3 instructions to make count of 0=256
333; delete next 3 instructions to make count of 0=256
334 MOV A,C ;GetTcount TUO RAS
33511 JANES SETFIC SIGNATURE ;SetTflags
3361 JANES SETFIC SIGNATURE ;SetTflags
3361 JANES SETFIC SIGNATURE ;SetTflags
      1064 79
       1065 B7
  337 JZ SEND6 ; If count=0, send no data
       1065 CA8810
  338 SEND3: LDAX D ;Get data byte
339 OUT DOUT ;Output to GPIB
340 CMP B ;Test EOS ...this is faster
       1069 1A
        105A D350
        106C B8
  341
  ;and uses less code than using
   :91's END or EOI bits
   342
```

| -       |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | - to - to to - to - to - to - to - to - |
|---------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|
| 1060    | CA7F10         | 343 aJZ made [GSEND5 of; If char = EOS ), go finish [A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                         |
| TNOD    | CATEIN         | 344 SEND4: WAITO TUOD TUO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                         |
| 1070    | DB61           | 345+??0006: IN pointlews: Get wintl status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                         |
| 1972    | E692           | 346+ ANI TO BOM 203; Check for byte out                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                         |
|         | CA7010         | 347+ JZ ??0006 ; If not, try again                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                         |
| 1077    |                | 348 INX Day Day; Increment buffer pointer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | #CA D861                                |
| 1078    |                | 349 DCR C Decrement count                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                         |
|         | C26910         | JNZ SEND3 ; If count < > 0, go send                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                         |
|         | C38810         | JMP SEND6 ; Else go finish                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                         |
| 107F    |                | 352 SEND5: INX D ; for consistency                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                         |
| 1080    |                | 353 MODCRAY and Thammars; " ARAD 354                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                         |
| 1000    | OD             | 426 CLRA" "; Immedî Dre xFROQN 626<br>4274 XRA A ; A XOR A = # OTIÁW 426                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | RDS AR                                  |
|         |                | ;This ensures that the standard e                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                         |
| 1 0 0 1 | DB61           | 355+??0007: IN value INTh to De; Get Tinth status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                         |
|         | E602           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | BDA D349                                |
|         | CA8110         | 356+ ANI BOM ; Check for byte out 357+ JZ 107 ??0007 ; If not, try again                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                         |
| LNOS    | CHOIIN         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | ino aro mot                             |
| 1 000   | 2000           | 358 ;assumptions for the next subrout                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | .Ine are met                            |
|         | 3 EFD          | 359 SEND6: MVI A,TCSY ;Take control syncronously 1 360 OUT CMD92 EERRSS SMC + NCB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | D1000 000                               |
|         | D369           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                         |
|         | 3E8Ø           | 361 MVI TOT A, AXRA W; Reset send EOI on EOS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                         |
| INSE    | D365           | 436+220014: IN PRIF GedMXUAR comTUDe int, ec 266                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                         |
|         | 2000           | 363 WAITX #1 NabM; Wait for TCI false +VE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | GES DEGE<br>GES EGG2<br>GEA OBS1        |
|         | DB6F           | (18 364+??0008: IN an IPRTF 180; ITMI WI LIVOSA PE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                         |
|         | E 502          | 440 MOV - B.A SavaIDT in BIAC BI chet Clater                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                         |
| 1094    | C29010         | 365+ 16 JNZ 2?20088 1MA 1 TCIF 364 1MA 365+ 18 JNZ 2?20088 1MA 1 1 TCIF 364 1MA 1 1 TCIF 364 1MA 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | MT53 G3W                                |
|         |                | 367 and sight the say; Wait for TCI NU CAA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                         |
|         | DB6F           | 368+??0009; IN Syst PRTF OM; Get task complete int, etc.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                         |
|         | E602           | 369+ ANIIS TOTCIFORD; Mask Mit IMA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                         |
| 109B    | CA971Ø         | IN 1370+ rentie JZ] tisw??0009 m; Wait for task to be complete                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | OFS CASALD                              |
| 109E    | C9             | 371 SIGRET IE SEY: MIC MI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 02EG 830                                |
|         |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                         |
|         |                | 448 INX D Increment buffer points 676                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | FE 13                                   |
|         |                | 374; RECEIVE ROUTINE D SOC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                         |
|         |                | 158 . JNZ RECVI :If count < > 8 go back is 576it                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | OFD CREALS                              |
|         |                | SS JNZ RECVI JIE count < > 8 go back % 576 t<br>NVI 8,408 ;Else set error indicate, 376<br>JMP rathroq rayletglHtake cont;TUPUNI; 776                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 100 0540                                |
|         |                | 377 ; INPUT: 1000 axia HL talker pointer 9ML                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 102 031711                              |
|         |                | 378 : DE data buffer pointer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                         |
|         |                | 379; C. count (max buffer size) 0 implies 256                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                         |
|         |                | 380; B EOS character TMA EVOSE 330                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 106 8501                                |
|         |                | 381 ;OUTPUT: Fills buffer pointed at by DE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                         |
|         |                | 382 ; CALLS: 101 j None 11 17 NI 17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 108 DB61                                |
|         |                | 383 : DESTROYS: A BC DE HI F                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                         |
|         |                | 384; elyd sish iso. WI : AVOSH 02-                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                         |
|         |                | 385 ; RETURNS: A=0 normal termination-EOS detected                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 112 12                                  |
|         |                | 385; A=40 Error count overrun                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                         |
|         |                | 385 ; RETURNS: A=0 normal termination—EOS detected 385 ; A=40 Error—— count overrun 387 is sud source A<40 or A>5EH Error—— bad talk address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                         |
|         |                | 463 MVI B.W Set normal completion in 886 store                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 115 0600                                |
|         |                | 389 ;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                         |
| 109F    | 78             | 390 RECV: 10 MOV 1013 A,B 3 3 T; Get EQS character : 2003 A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                         |
| 10A0    | D367           | 391 OUT EOSR ;Output it to 91                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 119 0369                                |
|         |                | 202 A CONCESS AGU FEU DECUG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                         |
|         |                | 393+ ;Checks for value in range ;branches to label if not ;checks for value in range ;checks for value ;checks  |                                         |
|         |                | 394+ ; branches to label if noted                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                         |
|         |                | 395+ ;in range, Falls through if                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                         |
|         |                | 395+ ;in range. Falls through if 396+ f=IDT not diswi;lower <= (T(H)(L)) <= upper.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                         |
|         |                | 397+ ++ and father than the terminal by the te |                                         |
| 10A2    | 7 E            | 4724920016: IN styd fran 199; Get task complete int.e+798.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                         |
|         | FE4Ø           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                         |
|         | FA3911         | 400+ JM RECV6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                         |
|         | FE5F           | 476; if timeout 3 is to be checil+H3che alqoe WAITT +1041d                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                         |
|         | F23911         | 402+m no xyP of eRECV6 singong set & bettime ed; TT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                         |
|         |                | 403 ; valid if 40H<= talk <=5EH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                         |
| IØAD    | D360           | 404 OUT DOUT ;Output talker to GPIB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                         |
| 10AF    |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                         |
| - C/11  | 23             | and 11405 GMS IP INX of H reflect; Increpointer for consistency                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                         |
| apa     | DB61           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                         |
|         |                | 407+2:20010: IN Seq INTlast; Get Intl status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                         |
|         | ESØ2<br>CABØ1Ø | 408+ ANI MOTBOM CHICAGO SCHECK for byte out                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                         |
|         |                | 409+ JZ about ?? 0010 ; If not, try again                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                         |
|         | 3 E 3 F        | 410 MVI A, UNL ; Stop other listeners                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                         |
|         |                | 411 OUT DOUT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                         |
| 1089    | D 3 . 10       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                         |
|         |                | 412 WAITO R= A SOX A4 A ASX 4733                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 135 AF                                  |
| 10BB    | DB61           | 413+??0011: IN INTL Get Intl status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                         |
| 10BD    |                | 412 wall's and the status and the st |                                         |

| 1.000 0001  | 416                 | UT A MIASS       | :For completeness                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |
|-------------|---------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| 10C2 3E21   |                     |                  | ;For completeness                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |
| 10C4 D360   | 417 0               | UI DUUI          | HOEND+EDEOS ; End when                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |
| 10C6 3E86   |                     |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 10C8 D365   |                     |                  | , bob of bot a nothori                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 874 CA7816 |
|             |                     | AITO II IOO II   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 10CA DB61   | 421+??0012:         | IN INTI          | ; det litt status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |
| 10CC E502   | 422+ A              | NI BOM           | ; check for byte out                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |
| 10CE CACA10 |                     |                  | ; II not, try again                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |            |
| 10D1 3E40   | 424 M               | VI A, LON        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 10D3 D364   | 425 0               | UT SADRMD        | 152 SENDS: INX D                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |
|             | 426 C               | LRA              | ;Immediate XEO PON                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 10D5 AF     | 427+ X              | RA A             | ; A XOR A =0 TIAM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |
| 10D6 D365   | e bas428 de edd deo | UT AUXMD         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 10D8 3EF6   | 429 M               | VI A, GTSB       | Goto standby I : TWRMST + 228                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | - 1990 IBA |
| 10DA D359   | 430                 | U'T CMD92        | 355+ ANI BOM +                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |            |
|             |                     |                  | ;Wait for TCI=0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | NIIBAD 288 |
| 10DC DB6F   | 432+??0013: I       |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 10DE E602   |                     | NIJOTATCIE       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 10E0 C2DC10 |                     | NZ ??0013        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| TOES CZDCIS | 4347 3              | NZ ::0713        | ;Wait for TCI=1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 1002 0000   | 435                 | AITT             | ;walt for TCI=I                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 10E3 DB6F   | 436+??ØØ14: I       |                  | ;Get task complete int,etc.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |            |
| 10E5 E602   |                     |                  | ;Mask it                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |            |
| 10EA DB61   | 439 RECV1: I        |                  | Get 91 Int status (END &/or BI)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 10EC 47     |                     | OV B, A          | ;Save it in B for BI check later                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |
| 10ED E610   | 441 A               | NI ENDMK         | :Check for EOS or EOI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |            |
| 10EF C20511 | 442 J               | NZ RECV2         | :Yes end go wait for BI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |
| 10F2 78     | 443 de dai edm      | OV A,B           | ;NO, retrieve status &                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 197 DB6F   |
| 10F3 E601   |                     | NI BIM           | ; check for BI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |            |
| 10F5 CAEA10 | 445 amon ad cJ      |                  | ;NO, go wait for either END or BI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 038 CA9710 |
| 10F8 DB50   |                     | N DIN            | ;YES, BI get data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |
| 10FA 12     | 447                 |                  | Store it in buffer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 10FB 13     |                     | NX D             | ;Increment buffer pointer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |
| 10FC 0D     |                     |                  | ;Decrement counter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 10FD C2EA10 |                     |                  | ;If count < > 0 go back & wait                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |            |
| 1100 0640   |                     |                  | ;Else set error indicator                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |
| 1102 C31711 |                     |                  | ;And go take control                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |
| 1102 031/11 |                     | uffer pointer    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 1105 78     | 454 RECV2: M        |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 1106 E601   | 455 RECV3: A        | NT DIM           | Check for BI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |            |
| 1108 C21011 |                     |                  | ;If BI then go input data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |
| 1108 DB61   |                     |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 110D C30611 |                     | N INT1           | ;In loop                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |            |
| 1110 DB60   |                     |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 1112 12     | 459 RECV4: I        | N DIN            | ;Get data byte<br>;Store it in buffer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |            |
|             | 460                 | TAX              | ;Incr data pointer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 1113 13     | 461 I               | NX D             | ;Incr data pointer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 1114 ØD     |                     |                  | ;Decrement count, but ignore it                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 1115 Ø6ØØ   |                     | VI B,Ø           | ;Set normal completion indicators                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |
| 1115 2000   | 464 ;               |                  | The state of the s |            |
| 1117 3EFD   | 465 RECV5: M        | VI A, TCSY       | ;Take control synchronously                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |            |
| 1119 D369   |                     |                  | 3 91 OUT 805R                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |
|             |                     |                  | ;Wait for TCI=0 (7 tcy)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |
| 1118 DB6F   |                     | New rolparts and |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 111D E602   | 469+ A              | NI OF TCIF       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 111F C21B11 |                     | NZ ??0915        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
|             | 471 W               | lower (= (TTIA   | ;Wait for TCI=1 4000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |
| 1122 DB6F   | 472+??0016: I       | N STYN SPRTF 190 | ;Get task complete int,etc.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |            |
| 1124 E602   | 473+ A              | NI TCIF          | ;Mask it VOM +808                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |
| 1126 CA2211 | 474+ J              | Z ??ØØ16         | ;Wait for task to be complete                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |
|             | 475 ;               |                  | 400+ JM RECVG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |
|             | 476 ; if timeo      | ut 3 is to be    | checked, the above WAITT should                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
|             |                     |                  | priate code to look for TCI or                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |            |
|             |                     | serted here.     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
|             | 479 ; 4190 63       | Output talker    | TUOG TUO NAS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |            |
| 1129 3E80   |                     |                  | ;Pattern to clear 91 END condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | BAF 23 P   |
| 1128 D365   |                     |                  | eriak 31 man domittion                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |
| 112D 3E8Ø   |                     |                  | ;This bit pattern already in "A"                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |
| 112F D364   |                     | UT ADRMD         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 1131 3E Ø3  |                     |                  | ;Finish handshake                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |
| 1133 D365   |                     | UT AUXMD         | , I Ill Isi Hallusliake                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |
|             |                     | LRA              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
| 1135 AF     |                     |                  | ; A XOR A =0 OTIAN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 1136 D365   | 487+ X              | RA A             | THE AUR A SU                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |            |
| 1138 78     | 488 O<br>489 M      | OV AUXMU         | ;Immediate execute PON-Reset LON<br>;Get completion character                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | GBD E602   |
| 1139 C9     | 100 DECVE           | ET A,B           | Get completion character                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | BBF CABBIS |
| 1139 69     | 490 KECVO: R        | E1               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
|             |                     |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |

2-391 AFN-01380A

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494 ; 495 ; BOT TOT TOTAL TOTAL TOTAL 888
  530 XFER1: RANGE 20H, 3EH, XFER2 ; Check for valid listener
   531+ ;Checks for value in range
  532+
   ; branches to label if not
  533+
   ; in range. Falls through if
   | 153 | 153 | 153 | 153 | 154 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 | 155 
  534+
  ;lower <= ( (H)(L) ) <= upper.
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WAITX
    566+ ANI TCIF SWITTOON HANK ERP
567+ JNZ ??0020
568 WAITT ;Wait for TCS
    1187 E602
    1189 C28511
   118C DB6F
118E E602
1190 CA8C11
1193 DB61
1195 E610
1197 CA931
   568
569+??0021: IN PRTF ; Mask it
570+ ANI TCIF ; Mask it
571+ JZ ??0021 ; Wait for task to be complete
572 XFER3: IN INT1 ;Get END status bit
573 ANI ENDMK ;Mask it
574 JZ XFER3
575 MVI A,TCSY ;Take control syncronously
576 OUT CMD92
577 WAITX
578+??0022: IN PRTF
579+ ANI TCIF
580+ JNZ ??0022
581 WAITT ;Wait for TCI
582+??0023: IN PRTF ;Get task complete int,etc.
ANI TCIF ;Mask it
-Wait for task to be complete
    1195 E610
1197 CA9311
119A 3EFD
119C D369
    119C D369
    119E DB6F
11AØ E6Ø2
    11A2 C29E11
 581 WAITT ; Wait for TC1
582+??0023: IN PRTF ; Get task complete int,etc.
583+ ANI TCIF ; Mask it
584+ JZ ??0023 ; Wait for task to be complete
  589 MVI A, TON ; Talk only
590 OUT ADRMD
591 CLRA ; Normal return A=0
592+ XRA A ; A XOR A =0
593 OUT AUXMD ; Immediate XEQ PON
594 XFFR4: RET
595;
    11B8 AF
    11B9 D365
     11BB C9
   595 ; 596 ;*******************************
  in range. Falls through; 806
  608 TRIG: MVI A,UNL ;
609 OUT DOUT ;Send univ
    11BC 3E3F
  ;Send universal unlisten
    11BE D350
   610 TRIG1: RANGE 20H, 3EH, TRIG2 ; Check for valid listen ; Checks for value in range
| Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | Sil+ | 
  511+
512+
   11D9 DB61
11DB E602
11DD CAD911
11E0 3E08
11E2 D350
  630 TRIG2: WAITU
630+270025: IN INTI ;Get Intl status
631+ ANI BOM ;Check for byte out
632+ JZ ??0025 ;If not, try again
633 MVI A,GET ;Send group execute trigger
634 OUT DOUT ;to all addressed listeners
635 WAITO
636+??0026: IN INTI ;Get Intl status
    11E2 D350
  ;Get Intl status
    11E4 DB61
  636+??ØØ26: IN INT1
637+ ANI BOM
  ;Get Intl status
;Check for byte out
    11E6 E692
```

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| 11E8 CAE411                                                     | 638+ Juo JZ vd 10 ??0026 ; If not, try again                                                                     | 711+   |                              |
|-----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|--------|------------------------------|
| 11EB C9                                                         |                                                                                                                  |        | 23A CA3513                   |
|                                                                 | SPOLL: RANGE 404,5RH,SPOL2 ;Check for valid 040 ker                                                              |        |                              |
|                                                                 | 641 ;*********************                                                                                       |        |                              |
|                                                                 | 642 cr il ledel of aedonard;                                                                                     | 71.5+  |                              |
|                                                                 | 643 ; DEVICE CLEAR ROUTINE                                                                                       |        |                              |
|                                                                 |                                                                                                                  |        |                              |
|                                                                 |                                                                                                                  |        |                              |
|                                                                 |                                                                                                                  |        |                              |
|                                                                 | · · · · · · · · · · · · · · · · · · ·                                                                            | +927   | 23E FERD                     |
|                                                                 |                                                                                                                  |        |                              |
|                                                                 |                                                                                                                  | 122+   | 243 FESF                     |
|                                                                 |                                                                                                                  |        |                              |
| 1100 2020                                                       |                                                                                                                  |        |                              |
| llec 3E3F                                                       | 652 DCLR: MVIRIAD A, UNLES: TUOO TUO                                                                             |        |                              |
| 11EE D360                                                       | INX H :InTUODINET TUOK pointe 653                                                                                | 726    |                              |
|                                                                 | 654 DCLR1: RANGE TO 20H, 3EH, DCLR2 A                                                                            | 727    |                              |
|                                                                 | 655+ ;Checks for value in rar<br>elegan 656+ searches also and staw; ;branches to label if no                    | ige    | 24E D364                     |
|                                                                 | eldmobb+ aserbbe xisi not fish; ; branches to label if no                                                        | t      |                              |
|                                                                 | 657+ suisiz Iidl idl; ;in range. Falls through                                                                   | if     |                              |
|                                                                 | => ((H)(L)) => lower ((H)(L)) <=                                                                                 |        |                              |
| 1100 75                                                         |                                                                                                                  |        |                              |
| 11FØ 7E                                                         | 660+ MOV A,M                                                                                                     | 733    |                              |
| llF1 FE2Ø                                                       | 201                                                                                                              | 7344   |                              |
| 11F3 FAØ912                                                     |                                                                                                                  |        | 258 0365                     |
| llF6 FE3F                                                       | SSS! CFI SERTI                                                                                                   |        |                              |
| 11F8 F20912                                                     | JF DCLKZ                                                                                                         |        |                              |
| IIPD DOCI                                                       | 665 DELEWAITO TOT JIEW: XTIAW                                                                                    |        |                              |
| llFB DB61                                                       | 666+??0027: IN INT1 ;Get Intl status                                                                             |        |                              |
| 11FD E602                                                       | 667+ ANI BOM ; Check for byte out                                                                                |        |                              |
| l1FF CAFB11<br>1202 7E                                          |                                                                                                                  |        |                              |
| 1202 /E                                                         |                                                                                                                  |        |                              |
| 1205 23                                                         | 670 DOUT ;Send listener to GPIB                                                                                  |        |                              |
| 1205 23<br>1206 C3F011                                          | 0,1                                                                                                              |        |                              |
| 1200 CSFUII                                                     | U/Z JAP DCERT                                                                                                    |        |                              |
| 1209 DB61                                                       |                                                                                                                  |        |                              |
| 1209 E602                                                       | 674+??0028: IN INTI ;Get Intl status                                                                             |        |                              |
| 120D CA0912                                                     | 675+ ANI BOM ; Check for byte out                                                                                |        |                              |
| 1210 3E04                                                       | 677 JZ ??0028 ; If not, try again                                                                                |        | 271 CARCI                    |
| 1212 D360                                                       | 676+ JZ 10270028; If not, try again<br>677 MVI A,SDC; Send device clear<br>678 OUT JOUT; To all addressed lister |        | 274 36FD                     |
| LELE DOOD                                                       | 679 WAITO ;To all addressed lister                                                                               | iers   |                              |
| 1214 DB61                                                       | 680+??0029: IN INT1 ;Get Intl status                                                                             |        |                              |
| 1216 E602                                                       | 681+ ANI BOM ; Check for byte out                                                                                | 754    |                              |
| 1218 CA1412                                                     |                                                                                                                  |        |                              |
| 121B C9                                                         | 683 BET                                                                                                          | 2 756- |                              |
|                                                                 |                                                                                                                  | 757    |                              |
|                                                                 | 685 : ********************                                                                                       | 227.   |                              |
|                                                                 | 686 · Ji Mask TCIF IMA                                                                                           | 159    | 281 8682                     |
|                                                                 | 91687 TO BE OCCUPATION TO DOMESTIC NO.                                                                           |        | 283 CATEL                    |
|                                                                 | IN DIN Get Serial poli status 8826                                                                               |        |                              |
|                                                                 | 688 ; HL talker list pointer 690 ; DE status buffer pointer                                                      |        |                              |
|                                                                 | 690; DE status buffer pointer                                                                                    | 763    |                              |
|                                                                 | fills buffer pointed to by DF                                                                                    | 35.50  |                              |
|                                                                 | 692 ;CALLS: None                                                                                                 |        |                              |
|                                                                 | 693 ; DESTROYS: A. BC. DE. HI. F. ARJO                                                                           |        |                              |
|                                                                 |                                                                                                                  |        | 28E AF                       |
| 121C 3E3F                                                       | 695 SPOL: MVI A,UNL ;Universal unlisten                                                                          |        |                              |
| 121E D360                                                       | ngh Olly Dolly                                                                                                   |        |                              |
|                                                                 | 697 00 solve WAITO of no ob; IJO98 9ML                                                                           |        | Ser caspi                    |
| .220 DB61                                                       | 698+??0030: IN INT1 ;Get Intl status                                                                             |        |                              |
| 222 E602                                                        | 699+ ANI BOM ; Check for byte out                                                                                | 772    |                              |
|                                                                 | 700+ JZ ??0030 ; If not, try again                                                                               |        |                              |
| 227 3E21                                                        | 701 MVT A MIA . M 1: 22                                                                                          | 774    |                              |
| 229 D360                                                        | 702 OUT DOUT                                                                                                     |        | 298 DB61                     |
|                                                                 | 703 WAITO STANDER AND THA                                                                                        |        | 29A E602                     |
|                                                                 | 704+??0031: IN INT1 ;Get Intl status                                                                             |        | 29C CA981                    |
|                                                                 | 705+ ANI BOM :Check for byte out                                                                                 | 778    |                              |
| 22D E602                                                        |                                                                                                                  |        |                              |
| .22D E602<br>.22F CA2B12                                        | 706+ 17 220021 15 576                                                                                            | 779    |                              |
| 122D E602<br>122F CA2B12<br>1232 3E18                           | 706+ JZ ??0031 ; If not, try again                                                                               | 780    | 2A@ D365                     |
| 122B DB61<br>122D E602<br>122F CA2B12<br>1232 3E18<br>1234 D360 | 706+ JZ ??0031 ;If not, try again 707 MVI A,SPE ;Serial poll enable                                              | 780    | 286 D365                     |
| 122D E602<br>122F CA2B12<br>1232 3E18                           | 706+ JZ ??0031 ;If not, try again 707 MVI A,SPE ;Serial poll enable 708 OUT DOUT ;To be formal about it          | 780    | 29F AF<br>2AG D365<br>2A2 C9 |

```
:Checks for value in range
                              714+
                              715+
  ; branches to label if not
                              716+
  ; in range. Falls through if
   ; lower <= ( (H)(L) ) <= upper.
                              717+
                            718+
719+
MOV A,M
720+
CPI 40H
721+
JM SPOL2
722+
CPI 5EH+1
723+
JP SPOL2
724
MOV A,M ;Get talker
725
OUT DOUT ;Send to GPIB ym ;SIDG $23
   ;Get next byte.
123D 7E
123E FE40
1240 FA9412
1243 FE5F
1245 F29412
1248 7E
   OUT DOUT ;Send to GPIB
INX H ;Incr talker list pointer
MVI A,LON ;Listen only
1249 D360
124B 23
                              726
124C 3E40
                              727
124E D364
                              728 ADRMD
                             729 WAITO associate; Wait for talk address to complete
1250 DB61
                             730+??0033: IN INTI GET INTL STATUS
                         1252 E502
1254 CA5012
1257 AF
1258 D365
125A 3EF6
   WAITX
125C D369
                             739+??0034: IN 14 14PRTF 00; ITHI WI STERRES + 222
125E DB6F
   1260 E602
                             740+ ANI TCIF
  ??0034
   JNZ
1262 C25E12
                              741+
                              742
  WAITT
                             743+??0035: IN PRTF ;Get task complete int,etc.
744+ ANI TCIF ;Mask it
745+ JZ ??0035 ;Wait for task to be complete
746 WAITI ;Wait for status byte input
1265 DB6F
1267 E602
   ??0935 ;Wait for task to be complete
1269 CA5512
                             745+
                             745+
746 WAITI ;Wait for status byte input
747+??0036: IN INTI ;Get INTI status
748+ MOV B,A ;Save status in B
749+ ANI BIM ;Check for byte in
750+ JZ ??0036 ;If not, just try again
126C DB61
126E 47
                             749+ ANI
750+ JZ
126F E691
1271 CA6C12
1274 3EFD
  A,TCSY ;Take control sync
                              751 MVI
752 OUT
1276 D359
  CMD92
                             753
  WAITX
  PRTF ;Wait for TCI false RCC 1880
                             754+??0037: IN
1278 DB6F
                              755+ ANI
756+ JNZ
757 WAIT'T
127A E602
  # 4880
; Wait for TCI # 4880
127C C27812
  ??0037
                              757
  TTIAW
127F DB6F
                             758+??0038: IN PRTF ;Get task complete int,etc.
                              759+ ANI
1281 E602
  TCIF
   ;Mask it
                            760+ JZ
761 IN
762 STAX
763 INX
1283 CA7F12
                            760+
  ??0038 ; Wait for task to be complete
1286 DB60
  DIN
  ;Get serial poll status byte
1288 12
   D
1289 13
  D
  ;Incr pointer
                              764
765
  A, TON
128A 3E8Ø
  ;Talk only for controller
  MVI
128C D364
  TUO
  ADRMD
  692 ;CALLS: None
  CLRA
                              765
  A JA . SO
  ; A XOR A =9 *8YORTESO; ERA
128E AF
                              767+
  XRA
   AUXMD
                              768
128F D365
  TUOSten
   ;Immeditate XEQ PON OGG 300
                              769
1291 C33D12
                              770
  JMP
   SPOL1
   ;Go on to next device on list
                              771 ;
  OUT A, SPD
  ;Serial poll disable
                              772 SPOL2: MVI
1294 3E19
                              773
774
  DOUT
1296 D360
   ; We know BO was set (WAITO above) STASAD ASSI
                             775+??0039: IN INT1 ;Get Intl status
776+ ANI BOM ;Check for byte out
  WAITO
1298 DB61
  JZ ??0039 ;If not, try again
CLRA
XRA
A ;A XOR A -0
129A E602
129C CA9812
                              777+
                              778
   ; A XOR A =0
  XRA A ;A XOR A = 0
OUT AUXMD ;Immediate XEQ PON to clear LA
129F AF
                              779+
                              780 9Ide
12AØ D365
                              780 SIGNATURE ANALYSIS FINITE AND THE SET OF 12A2 C9
```

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```
PARALLEL POLL ENABLE ROUTINE TO BE NOT ASSI
                  785;
787;INPUTS: HL listener list pointer
788;
DE configuration byte pointer
789;OUTPUTS: None
790;CALLS: None
                  12A3 3E3F
                  795 PPEN1: RANGE 20H,3EH,PPEN2 ;Check for valid listener
797+
798+
798+
799+
ibranches to label if not
799+
in range Falle through ;
12A5 D360
   ; branches to label if not
; in range. Falls through if
                  800+
   ;lower <= ( (H)(L) ) <= upper.
                 12A7 7E
12A8 FE2Ø
12AA FAD812
12AD FE3F
12AF F2D812
                  12E2 D350
                  844 PPDS1: RANGE 20H, 3EH, PPDS2 ; Check for valid listener
                  845+ 41808 (1) Jan ; Checks for value in range 846+ (branches to label if not
                 ; branches to label if not
; in range. Falls through if
848+
849+
850+ MOV A,M
851+ CPI 20H
852+ JM PPDS2
853+ CPI 3EH+1
854+ JP PPDS2
12E4 7E
12E5 FE20
12E7 FAFD12
12EA FE3F
12EC F2FD12
                 854+ JP PPDS2
855 WAITO
856+??0044: IN INT1 ;Get Intl status
857+ ANI BOM ;Check for byte out
858+ JZ ??0044 ;If not, try again
12EF DB61
12F1 E602
12F3 CAEF12
```

```
12F6 7E
   MOV
                                    859
   A,M SIE;Get listener ASAG DOUT
                                   861
862
12F7 D360
   OUT
   H ;Incr pointer
PPDS1 ;Loop until invalid listener
12F9 23
   INX
12FA C3E412
   JMP
                                    862
863 PPDS2:
   INT1 ;Get Intl status 2109100; 881
   WAITO
                                     854+??0745: IN
12FD D861
   BOM ;Check for byte out
??0045 ;If not, try again
                                    865+
866+
12FF E592
   ANI
                                    856+ JZ
867 MVI
868 OUT
859 WAITE
1301 CAFD12
  A, PPC ; Parallel poll configure
1304 3E05
1305 D350
  DOUT JUNE A, UML JUNE THORY
   WAITO
   INT1 ;Get Intl status
80M ;Check for byte out
220046 ;If not, try again
13Ø8 DB61
                                     870+??0046: IN
871+ ANI
                                    871+ ANI
872+ JZ
130A E602
130C CA0813
                                    872+ JZ
873 MVI
  A,PPD ;Parallel poll disable
130F 3E70
                                    874 OUT
875 WAITO
  DOUT
1311 D350
                                    875 WAITO
876+??0047: IN INTI ;Get Intl status
877+ ANI BOM ;Check for byte out
878+ JZ ??0047 ;If not, try again
879 RET
880 ;
881 ; PARALLEL POLL UNCONFIGURE ALL ROUTINE
1313 DB61
1315 E602
1317 CA1313
131A C9
                                     808+278046: IN INTI ;Get Intl Status ; 288
889+ AMI BOM ;Check for byte out
                                   131B 3E15
131D D360
131F DB61
1321 E602
1323 CA1F13
                                    891 ANI BOM TCDECK for DyeTISHUE ; 898
1326 C9
                                     897 ; ***************
                                    906; RETURNS: A= parallel poll status byte
907;
908 PPOL: MVI A,LON; Listen only
909 OUT ADRMD ADDMD ADRMD ADDMD ADRMD ADDMD ADRMD ADDMD ADRMD ADDMD A
1327 3E40
                                   1329 D364
132B AF
132C D365
132E 3EF5
1330 D369
                                    916+??0049: IN INTIDITY GET INTI STATUS
917+ MOV B,A ;Save status in B
918+ ANI BIM G;Check for byte in
1332 DB61
1334 47
1335 E601
1337 CA3213
                                    919+ JZ ??0049 ;If not, just try again
920 MVI A,TON ;Talk only
921 OUT ADRMD
133A 3E8Ø
133C D364
                                     922 CLRA ) => rewol; Immediate XEQ PON
                                    923+ XRA A 3 A XOR A =0
924 OUT AUXMD ;Reset LON 925 IN DIN ;Get PP byte 193
926 RET 927;
133F D355
1341 DB50
1343 C9
                                     928 ;*********************
                                    929 ; PASS CONTROL ROUTINE OTIAN 930 ;
                                    930;
931;INPUTS: HL pointer to talker 1MA 4788
932;OUTPUTS: None 11 ABBET 1MA 4788
```

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```
933 ;CALLS: VII GIBLE None COME LITTOR SIME PARTY 1934 ;DESTROYS: 18 280 Å, HL, FT 1890 M1
  935 PCTL: RANGE 40H, 5EH, PCTLl ; Is it a valid talker ?
935 PCTL: RANGE 40H,5EH,PCTL1 ;Is it a valid talker ?
936+ ;Checks for value in range
937+ ;branches to label if not
938+ ;in range. Falls through if
939+ ;lower <= ((H)(L)) <= upper.
940+ ;Get next byte.

1344 7E 941+ MOV A,M
1345 FE40 942+ CPI 40H
1347 FA8A13 943+ JM PCTL1
134A FE5F 944+ CPI 5EH+1
134C F28A13 945+ JP PCTL1
134F FE41 946 CPI MTA ;Is it my talker address
1351 CA8A13 947 JZ PCTL1 ;Yes, just return
1354 D360 948 OUT DOUT ;Send on GPIB
949 WAITO
1356 DB61 950+??0050: IN INT1 ;Get Intl status
948 OUT DOUT ;Send on GPIB
949 WAITO

1356 DB61 950+??0050: IN INT1 ;Get Intl status
1358 E60? 951+ ANI BOM ;Check for byte out
135A CA5613 952+ JZ ??0050 ;If not, try again
135D 3E09 953 MVI A,TCT ;Take control message
135F D360 954 OUT DOUT
955 WAITO
1361 DB61 956+??0051: IN INT1 ;Get Intl status
1363 E602 957+ ANI BOM ;Check for byte out
1365 CA6113 958+ JZ ??0051 ;If not, try again
1368 3E01 959 MVI A,MODE1 ;Not talk only or listen only
136A D364 960 OUT ADRMD ;Enable 91 address mode 1
136C AF 962+ XRA A ;A XOR A =0
136D D365 963 OUT AUXMD ;Immediate XEO PON
136F 3E01 964 MVI A,MDA ;My device address
1371 D366 965 OUT ADRM1 ;enabled to talk and listen
1373 3EA1 966 MVI A,AXRB+CPTEN ;Command pass thru enable
1375 D365 967 OUT AUXMD
968 ;*********optional PP configuration goes here*******
                                  968 ;********optional PP configuration goes here*******

969 MVI A,GIDL ;92 go idle command

970 OUT CMD92

971 WAITX

972+??0052: IN PRTF

973+ ANI TCIF

3 974+ JNZ ??0052

975 WAITT

976+??0053: IN PRTF ;Get task complete int,etc.

977+ ANI TCIF ; Mask it

978+ JZ ??0053 :Wait for task to be complete
   968 ;******optional PP configuration goes here******
 1377 3EF1
 1379 D369
 1378 DB6F
  137D E602
 137F C27B13
  1382 DB6F
  978+ 32 ??0053 ; Wask it 978+ JZ ??0053 ; Wait for task to be complete 980 PCTL1: RET 981 ;
   977+ ANI
978+ JZ ANI
979 INX
 1384 E602
  1385 CA8213
 1389 23
  138A C9
   982 ;
  986 ;
   986;
987; INPUTS:
988; OUTPUTS:
None
989; CALLS:
990; DESTROYS:
991; RETURNS:
99 invalid (not take control to us or CPT bit not on)
992;
(> 0 = valid take control-- 92 will now be in control
993; NOTE:
994; THIS CODE MUST BE TIGHTLY INTEGRATED INTO ANY USER
994; SOFTWARE THAT FUNCTIONS WITH THE 8291 AS A DEVICE.
995; NORMALLY SOME ADVANCE WARNING OF IMPENDING PASS
996; CONTROL SHOULD BE GIVEN TO US BY THE CONTROLLER
997; WITH OTHER USEFUL INFO. THIS PROTOCOL IS SITUATION
  997; WITH OTHER USEFUL INFO. THIS PROTUCUL IS
998; Idea signal specific and WILL NOT BE COVERED HERE.
999;
1000;
The local specific and Will red (i.e. CPT etc.)
   999;
1000;
1001 RCTL: IN INTl ;Get INTl req (i.e. CPT etc.)
1002 ANI CPT ;Is command pass thru on ?
1003 JZ RCTL2 ;No, invalid-- go return
1004 IN CPTRG ;Get command
1005 CPI TCT ;Is it take control ?
 138B DB51
 138D E680
 138F CACF13
 1392 DB65
 1394 FE09
```

```
A.DTDL1 :Disable talker listener
13A0 3E60
  1010
1011 OUT
   ADRØ1
A,TON ;Talk only
 13A2 D355
 13A4 3E80
  1012 MVI
1013 OUT
 13A6 D354
  1013 OUT ADRMD
1014 CLRA
1015+ XRA A ;A XOR A = 0
1016 OUT INT1 ;Mask off INT bits
1017 OUT INT2
1018 OUT AUXMD
1019 MAY A TOWN 
  ADRMD
 13A8 AF
 13A9 D361
   13AB D352
 13AD D365
  1019 MVI A,TCNTR; Take (receive) control 92 command
1020 OUT CMD92
1021 MVI A,VSCMD; Valid command pattern for 91
1022 OUT AUXMD
 13AF 3EFA
 13B1 D369
 1383 3EØF
 1385 D355
  1023 ;****** optional TOUT1 check could be put here ******

1024 WAITX

1025+??0054: IN PRTF

1026+ ANI TCIF

1027+ JNZ ??0054

1028 WAITT ;Wait for TCI

1029+??0055: IN PRTF
  1387 DBSF
  1389 E602
  13BB C2B713
   1028
1029+??0055: IN PRTF ; Get task complete int,etc.
1030+ ANI TCIF ; Mask it
1031+ JZ ??0055 ; Wait for task to be complete
1032 MVI A,TCT ; Valid return pattern
1033 JMP RCTL2 ; Only one return per routine
1034 RCTL1: MVI A,VSCMD ; Acknowledge CPT
1035 OUT AUXMD
1036 CLRA ; Error return pattern
1037+ XRA A ; A XOR A = 0
1039;
 138E DB6F
 13C0 E602
  13C2 CABE13
  13C5 3E09
  13C7 C3CF13
   13CA 3EØF
   13CC D365
   13CE AF
   13CF C9
   1048; A < > 0 SRO occured
   1049 PRITE FOR LOSS COMPLETE INT. STREET I
  1050;
1051 SRQD: IN INTST ;Get 92's INTRO status
1052 ANI SRQBT ;Mask off SRQ
1053 JZ SRQD2 ;Not set--- go return
1054 ORI IACK ;Set--- must clear it with IACK
1055 OUT CMD92
1056 SRQD1: IN INTST ;Get IBF
 13DØ DB69
   13D2 E620
   13D4 CAE213
   13D7 F60B
   13D9 D359
  13DB DB69
   1057 ANI IBFBT ; Mask it
1058 JZ SRQD1 ; Wait if not set avgaces as
1059 SRQD2: RET
   13DD E602
   13DF CADB13
   13E2 C9
1059 | 1061 | 1061 | 1061 | 1062 | 1063 | 10661 | 1062 | 1063 | 10662 | 1063 | 10662 | 10663 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 | 10666 |
  1070 REME.

1071 OUT

1072 WAITX

1073+??0056: IN
   ;Wait for TCI = 0

PRTF
TCIF
??0056

;Wait for TCI
PRTF
;Get task complete int.etc.
13E7 DB6F
13E9 E602
13EB C2E713
 13E7 DB6F
   1074+ ANI
1075+ JNZ
1076 WAITT
 13EE DB6F 1077+??0057: IN
13F0 E502 1078+ ANI
13F2 CAEE13 1079+ JZ
  PRTF ;Get task complete int,etc.
TCIF ;Mask it
??0057 ;Wait for task to be complete
```

2-399 AFN-01380A

```
1133 ; APPLICATION EXAMPLE CODE FOR 8885 TES
13F5 C9
    1089
    1081 ;
   1104 ;*********************
    1105;
    1106 ; INTERFACE CLEAR / ABORTOROUTINE WOLTOWUY 90738; 1211
    1113 ;
1114 ;
1125 ; Delete both WAITX & WAITT if this routine
141B C9
```

```
1133 ; APPLICATION EXAMPLE CODE FOR 8985
                    1134 :
                    1135 FGDNL EQU '2' ;Func gen device num "2" ASCII,lstn
                    1136 FCDNL EQU '1' ;Freq ctr device num "1" ASCII,lstn
9931
                                   1137 FCDNT EQU
1138 CR EQU
9951
                    1138 CR
agan
ARRE
                    1139 LF
GGFF
                    1140 LEND
0040
                    1141 SROM
                                  EQU
                    1142 ;
141C 46553146
                    1143 FGDATA: DB 'FUlfr37KHAM2VO',CR ;Data to set up func. gen
1420 5233374B
1424 48414D32
1428 564F sldene emote emable 7466 8241
1146 LIM2 EQUIOT 163 118W:
   13FE CZFA13 1897+ JNZ
Halter length
142F 3754
0006
1431 31
                   1147 LL1: 4 DB GMOS FCDNL, LEND 3199
  Listen list for freq ctr [MA]
1432 FF
1433 32
                   1148 LL2: ad DB year FGDNL, LEND
  :Listen list for func. gen 2011
1434 FF
                    1149 TL1: DB FCDNT, LEND
   ; Talk list for freq ctr
1435 51
1435 FF
                    1150;
                   1150;
1151; SETUP FUNCTION GENERATOR GOAD RABBO SCAPERTY: 3811
1152 MVI B,CR; EOS
1153 MVI C,LIM1; Count
1154 LXI D,FGDATA; Data pointer FI; EBII
1155 LXI H,LL2 m; Listen list pointer FI; EBII
1156 CALL SENDAMON 12303 1111
1157;
1158; SETUP FREO COUNTER
1437 9690
1439 ØEØF
143B 111C14
143E 213314
1441 CD1C10
                    1157;
1158; SETUP FREO COUNTER
                   1160 MVI B,'T' ; EOSBA A IVM 11091 2111
1161 MVI C,LIM2 ; Count O THO 1116
1162 LXI D,FCDATA ; Data pointer Till
1163 LXI H,LL1 ; Listen list pointer RECEPTION 11165 ;
  1409 3EF9
1444 Ø554
1446 ØEØ6
1448 112814
                   1162 LXI D,FCDATA ;Data pointer
1163 LXI H,LLI ;Listen list pointer
1164 CALL SEND
1165;
1166; WAIT FOR SRO FROM FREO CTR
1167; Has SRO occurred ?
1168 LOOP: CALL SRODEM; Has SRO occurred ?
1169 DOOS JZ LOOPIN; No, wait for it
1170;
1171; SERIAL POLL TO CLEAR SRO of the ballon decided 2511
144B 213114
  BARD CRAI
144E CD1C10
1451 CDD913
1454 CA5114
                    1172; controller-in-Charge. If not C.I.C. then
1173 (IPCIXI sent) BYSAS, G (IPCIXI sent)
1178 (IPCIXI sent)
1457 11003C
                   145A 213514
145D CD1C12
                                  CALL SPOL
DCX D ;Backup buffer pointer to ctr byte
LDAX D ;Get status byte
ANI SROM ;Did ctr assert SRQ ?
JZ ERROR ;Ctr should have said yes
1460 1B
1461 1A
1462 E640
1464 CA7714
                    1180 ;
                    1181 ; RECEIVE READING FROM COUNTER
                    1182 ;
                    1183 MVI B,LF ;EOS

1184 MVI C,LIM3 ;Count

1185 LXI H,TL1 ;Talk list pointer

1186 LXI D,FCDATI ;Data in bu

1187 CALL RECV
1467 Ø6ØA
1469 ØE11
146B 213514
146E 11013C
  D,FCDATI ;Data in buffer pointer
1471 CD9F10
                    1188
1474 C27714
                                   JNZ
   ERROR
                    1189 ;
                    1190 ;***** rest of user processing goes here *****
                    1191;
                    1192 ;
1477 00
  ;User dependant error handling
                    1193 ERROR: NOP
                    1194 ; ETC.
                   1195 ORG 3C00H
1196 SPBYTE: DS 1 ;Location for serial poll byte
1197 LIM3 EQU 17 ;Max freq counter input
3000
0211
```

| 3CØ1                                                                                                                                                                                                                                                                                                      | 1198 FCDATI:<br>1199                                                                                                                                                                                                                                                                                         | END                                                                                                                                                                                                                                                                                                                                                                                                         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| BIM A 9801 BOF CLRST A 9868 CMD92 DCLR A 11EC DCLR1 EDEOS A 9804 ENDMK ERRORA A 1477 EVBIT FCDNL A 9831 FCDNT GSEC A 1864 GTS8 IFCL A 1489 INIT INTST A 9869 LA LL1 A 1431 LL2 MODEI A 0801 MTA PPD A 08778 PPDS PPEN2 A 12D8 PPDL RANGE + 8985 RECV2 RENF A 9864 SEND SEND6 A 1888 SETF SPIF A 8884 SETF | A 0010 BOIS A 0011 BOIS A 0011 BOUST A 0051 BOIS A 0051 BOIS A 0071 BOIS A 1007 BOIS A 1007 BOIS A 1071 BOIS A 1072 BOIS BOIS A 1072 BOIS BOIS A 1072 BOIS BOIS BOIS A 1072 BOIS BOIS A 1072 BOIS BOIS BOIS BOIS BOIS BOIS BOIS BOIS | A 0992 A 0999 A 1209 A 0998 A 0998 A 141C A 0095 A 0097 A 12E4 A 0015 A 0025 A | ADRST A 6 8 9 USST A 6 6 USST A 6 6 USST A 6 6 USST A 6 0 USST A 6 | MASE CAHCY MAGNITURE MAGNI | A 9955               | AXRA A 0988 CLKRT A 00023 CR A 00001 DDL1 A 0750 ERFLG A 2058 FCDATA A 1428 FCDATA A 1428 FCDATA A 0003 IBFBT A 128 IBFBT A 138 IBFBT A 0003 IB | AXRB A 00A0 CLRA + 20077 OCL A 0014 DTDL2 A 0068 FGDATI A 3C01 GJDL A 00F1 IBFF A 0010 INTMR A 0021 PPC A 0005 PPEN1 A 12A7 PRTF A 005F RECV A 109F RECV A 109F RECV A 109F RENE A 13E3 RTOUT A 00E9 SEND5 A 107F SPE A 0018 SROD A 13D0 TCIF A 0002 T |
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# TEST CASES FOR THE SOFTWARE DRIVERS

The following test cases were used to exercise the software routines and to check their action. To provide another device/controller on the GPIB a ZT488 GPIB Analyzer was used. This analyzer

acted as a talker, listener or another controller as needed to execute the tests. The sequence of outputs are shown with each test. All numbers are hexadecimal.

3E73

#### SEND TEST CASES

| B = 44<br>C = 30<br>DE = 3E80<br>HL = 3E70<br>3E70: 20 30 3E 3F<br>3E80: 11 44<br>GPIB output: 41 ATN<br>3F ATN<br>20 ATN<br>30 ATN<br>3E ATN<br>11 | PRES A RECOMENTAL A 1704 A 170 | 44<br>2<br>3E80<br>3E70<br>41 ATN<br>3F ATN<br>20 ATN<br>30 ATN<br>3E ATN | DCLEAR   A   1889 | 44<br>0<br>3E80<br>3E70<br>41 ATN<br>3F ATN<br>20 ATN<br>30 ATN<br>3E ATN | 7211 A 2001 A 20 |
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| 44 EOI                                                                                                                                              | XPERS A 1103                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 44 EOI                                                                    | XFERL + SERS      |                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Ending B = 44<br>Ending C = 2E<br>Ending DE = 3E82                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 44<br>0<br>3E82                                                           |                   | 3 04 0<br>3E80                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

3E73

# Ending HL = 3E73 RECEIVE TEST CASES

| B = 44              | 44     | 44     | 44   | 44     | 44     | 44     |
|---------------------|--------|--------|------|--------|--------|--------|
| C = 30              | 30     | 30     | 30   | 4      | 4      | 0=256  |
| DE = 3E80           | 3E80   | 3E80   | 3E80 | 3E80   | 3E80   | 3E80   |
| HL = 3E70           | 3E70   | 3E70   | 3E70 | 3E70   | 3E70   | 3E70   |
| 3E70: 40            | 50     | 5E     | 5F   | 40     | 40     | 40     |
| GPIB output: 40 ATN | 50 ATN | 5E ATN |      | 40 ATN | 40 ATN | 40 ATN |
| 3F ATN              | 3F ATN | 3F ATN |      | 3F ATN | 3F ATN | 3F ATN |
| 21 ATN              | 21 ATN | 21 ATN |      | 21 ATN | 21 ATN | 21 ATN |
| ZT488 Data 1        | 1      | 1      |      | 1      | 11     | 1      |
| In 2                | 2      | 2      |      | 2      | 22     | 2      |
| 3                   | 3      | 3      |      | 3      | 33     | 3      |
| 4                   | 4      | 44,EOI |      | 4      | 44     | 44     |
| 44                  | 5,EOI  |        |      |        |        |        |
| Ending $A = 0$      | 0      | 0      | 5F   | 40     | 0      | 0      |
| Ending $B = 0$      | 0      | 0      | 44   | 40     | 0      | 0      |
| Ending $C = 2B$     | 2B     | 2C     | 30   | 0      | 0      | FC     |
| Ending DE = 3E85    | 3E85   | 3E84   | 3E80 | 3E84   | 3E84   | 3E84   |
| Ending HL = 3E71    | 3E71   | 3E71   | 3E70 | 3E71   | 3E71   | 3E71   |

#### SERIAL POLL TEST CASES

| C = 30    | C =          | 30            |
|-----------|--------------|---------------|
| DE = 3E80 | DE =         | 3E80          |
| HL = 3E70 | HL =         | 3E70          |
| 3E70: 40  | 3E70:        | 5F            |
| 50        | GPIB output: | 3F ATN        |
| 5E        |              | 21 ATN        |
| 5F        |              | <b>18 ATN</b> |

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19 ATN A 78
GPIB output: 3F ATN
    output: 21 ATN
                             Ending C = 30
    output: 18 ATN
                             Ending DE = 3E80
    output: 40 ATN
                             Ending HL = 3E70
     input*: 00
    output:
           50 ATN
     input*: 41
    output: 5E ATN
     input*: 7F
    output: 19 ATN
Ending C = 30
 Ending DE = 3E83
 Ending HL = 3E73
Ending 3E80: 00 41 7F
PASS CONTROL TEST CASES
       HL = 3E70
                                  3E70
                       3E70
      3E70: 40
                                  5F
                       41(MTA)
GPIB output: 40 ATN
            09 ATN
            -\overline{ATN}
  Ending HL = 3E71
                       3E70
                                  3E70
 Ending A = 02
                       41(MTA)
                                  5F
RECEIVE CONTROL TEST CASES
GPIB input
                      10 ATN
                                 40 ATN
  41 ATN
                      ATN
                                 09 ATN
  09 ATN
Run Receive Control
GPIB Input
                                 ATN
  ATN
Ending A =
                                 0
  09
PARALLEL POLL ENABLE TEST CASES
       DE = 3E80
                             3E80
       HL = 3E70
                             3E70
      3E70: 20 30 3E 3F
                             3F
      3E80: 01 02 03
GPIB output:
           3F ATN
                             3F ATN
            20 ATN
            05 ATN
            61 ATN
            30 ATN
            05 ATN
            62 ATN
            3E ATN
            05 ATN
            63 ATN
 Ending DE = 3E83
                             3E80
 Ending HL = 3E73
                             3E70
PARALLEL POLL DISABLE TEST CASES
       HL = 3E70
                             3E70
      3E70: 20 30 3E 3F
                             3F
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AFIN-01380A

|                                                                                         | The second secon | Control of the Contro |                 |                                                                                            |
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| GPIB output: 3F ATN 20 ATN 30 ATN 3E ATN 05 ATN 70 ATN                                  | E80 NIA 07                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | nding C = 3<br>nding DE = 3<br>nding HL = 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | a               | GPIB output: 3F ATN output: 21 ATN output: 18 ATN output: 40 ATN input*; 00 output: 50 ATN |
| Ending HL = 3E73                                                                        | 3E70                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                 | input*; 41 output: 5E ATN input*; 7F output: 19 ATN                                        |
| PARALLEL POLL UNCONFIGURE                                                               | TEST CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | even on input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | le step mode    | NOTE: leave ZT488 in sing                                                                  |
| GPIB output: 15 ATN                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                 | Ending C = 30<br>Ending DE = 3E83<br>Ending HL = 3E73<br>Ending 3E80: 00 41 7F             |
| PARALLEL POLL TEST CASES                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                 |                                                                                            |
| Set DIO # 1 2 3 4 5 6 7                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | VSES            | PASS CONTROL TEST CA                                                                       |
| Ending A 1 2 4 8 10 20 40  SRQ TEST                                                     | 80 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 3E70<br>5F                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 3E70<br>41(MTA) | HL = 3E70<br>3E70: 40<br>GPIB output: 40 ATN<br>09 ATN                                     |
| Set SRQ momentarily<br>Ending A = 02                                                    | Reset SRQ<br>00                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 3E70<br>5F                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 3E70<br>41(MTA) | Ending HL = 3E71<br>Ending A = 92                                                          |
|                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | TCASES          | RECEIVE CONTROL TES                                                                        |
| TRIGGER TEST                                                                            | 41 ATN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 40 ATN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | IO ATN          | GPIB input                                                                                 |
| HL = 3E70<br>DE = 3E80                                                                  | 09 ATN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 09 ATN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | ATN             | Run Receive Control                                                                        |
| BC = 4430<br>3E70: 20 30 3E 3F<br>GPIB output: 3F ATN<br>20 ATN                         | ATN<br>09                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | ATN<br>0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 0               | GPIB Input<br>Ending A =                                                                   |
| 30 ATN                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                 | PARALLEL POIL ENABI                                                                        |
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| PSIR<br>ORFE<br>IQCN<br>XXXX<br>XXXX<br>XXXX<br>XXXX<br>XXXX<br>XXXX<br>XXXX<br>X                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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| PARE OR FERENCE OR FER | 52<br>33 10<br>48<br>48<br>41<br>4D<br>32<br>56<br>4F<br>0D EOI<br>41 ATN<br>3F ATN<br>31 ATN<br>50                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           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| PARECE OF RESTRICT | 52<br>33<br>48<br>48<br>41<br>4D<br>32<br>56<br>4F<br>0D EOI<br>41 ATN<br>3F ATN<br>31 ATN<br>50<br>46<br>34<br>47<br>37                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          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| PREPARE OR FERENCE OR  | 52<br>33<br>48<br>48<br>41<br>4D<br>32<br>56<br>4F<br>0D EOI<br>41 ATN<br>3F ATN<br>31 ATN<br>50<br>46<br>34<br>47<br>37<br>54 EOI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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| R S I R O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N O R F G N 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O R F G N O R F G N O R F G N O R F G N O R F G  | 52<br>33<br>48<br>48<br>41<br>4D<br>32<br>56<br>4F<br>0D EOI<br>41 ATN<br>31 ATN<br>50<br>46<br>34<br>47<br>37<br>54 EOI<br>SRQ                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       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| CHARGE CHARGE IN CORREST IN CORRE | 52<br>33<br>48<br>48<br>41<br>4D<br>32<br>56<br>4F<br>0D EOI<br>41 ATN<br>31 ATN<br>50<br>46<br>34<br>47<br>37<br>54 EOI<br>SRQ<br>3F ATN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          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| R S I R S I R O R S I R O R S I R O R S I R O R S I R O R S I R O R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R 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R S I R S I R S I R S I R S I R S I R S I R S I  | 52<br>33<br>48<br>48<br>41<br>40<br>32<br>56<br>4F<br>0D EOI<br>41 ATN<br>3F ATN<br>31 ATN<br>50<br>46<br>34<br>47<br>37<br>54 EOI<br>SRQ<br>3F ATN<br>21 ATN<br>18 ATN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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| R S I R S I R O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F E S I N O R P F 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O R P F E S I N O R P F E S I N O R P F E S I N  | 52<br>33<br>48<br>48<br>41<br>4D<br>32<br>56<br>4F<br>0D EOI<br>41 ATN<br>31 ATN<br>50<br>46<br>34<br>47<br>37<br>54 EOI<br>SRQ<br>3F ATN<br>21 ATN<br>18 ATN<br>51 ATN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                       |                                         | (Notes 2, 9) (Notes 2, 9)          | addressed command group attention data byte data secepted data valid device clear end end of string group execute trigger identify interface clear listen address group my listen address my listen address my listen address      | ACG DAB DAC DAV DAC DAV DCL DAV COL COL LEC LEC LEC LEC LEC LEC LEC MLA                 |
| R S I R S I R O R S I R O R S I R O R S I R O R S I R O R S I R O R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R S I R 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R S I R S I R S I R S I R S I R S I R S I R S I  | 52<br>33<br>48<br>48<br>41<br>4D<br>32<br>56<br>4F<br>0D EOI<br>41 ATN<br>31 ATN<br>50<br>46<br>34<br>47<br>37<br>54 EOI<br>SRQ<br>3F ATN<br>21 ATN<br>18 ATN<br>51 ATN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                       | M M M M M M M M M M M M M M M M M M M   | (Notes 2, 9) (Notes 2, 9) (Note 3) | addressed command group attention data byte data scepted data valid device clear end end of string group execute trigger identify interface clear listen address my listen address my talk address my talk address my talk address | ACG DAB DAC DAC DAV DAC DAV DAC DAV DCL DAV END EOS END EOS END LAC LAC LAC LAC MLA MLA |

|               | 3F ATN<br>21 ATN | XFER TEST                                                 |
|---------------|------------------|-----------------------------------------------------------|
| GPIB input:   | 20               | B = 44                                                    |
| Of the input. | 2B               | HL = 3H70                                                 |
|               | 20               | 3E70: 40 20 30 3E 3F                                      |
|               | 20               | GPIB output: 40 ATN                                       |
|               | 20               | 3F ATN                                                    |
|               | 33               | 20 ATN                                                    |
|               | 37               | 30 ATN                                                    |
|               | 30               | JE ATN                                                    |
|               | 30               |                                                           |
|               | 30               |                                                           |
|               | 2E               |                                                           |
|               | 30               |                                                           |
|               | 45               |                                                           |
|               | 2B               | Ending A = 0                                              |
|               | 30               | B = 44                                                    |
|               | 0D               | HL = 3E74                                                 |
|               | 0A               |                                                           |
| GPIB output   | XX ATN           |                                                           |
| 1             |                  | THE THREE RESIDENCE THE PARTY AND ADDRESS OF THE PARTY AS |

APPLICATION EXAMPLE GPIS OUTPUT/INPUT

GPIB output: 41 ATN 3F ATN 32 ATN

## APPENDIX C

|         |                         |              |                  | c           |                 |        |        |        |        | Coc    | ling<br>Va | g Tl             | al Line(s)<br>hat Asser<br>of the N | ts t | he |   |               |
|---------|-------------------------|--------------|------------------|-------------|-----------------|--------|--------|--------|--------|--------|------------|------------------|-------------------------------------|------|----|---|---------------|
| Mnemoni | c                       | Message Name | T<br>y<br>p<br>e | l<br>a<br>s | I)<br>I ()<br>8 | 7      | 6      | 5      | 4      | 3      |            | D<br>1<br>O<br>1 | NN<br>DRD A<br>AFA T<br>VDC N       | 0    | R  | F |               |
| ACG     | addressed command group |              | М                | AC          | Y               | Ø      | Ø      | Ø      | X      | X      | Х          | Х                | XXX 1                               | Х    | X  | X | X             |
| ATN     | attention               |              | U                | UC          | X               | X      | X      | X      | X      | X      | X          | Х                | XXX 1                               | X    | X  | X | X             |
| DAB     | data byte               | (Notes 1, 9) | M                | DD          |                 | D<br>7 |        | D<br>5 | D<br>4 | D<br>3 | D<br>2     |                  | XXX Ø                               | X    | X  | X | X             |
| DAC     | data accepted           |              | U                | HS          | X               | X      | X      | X      | X      | X      | X          | X                | XXØ X                               | X    | X  | X | X             |
| DAV     | data valid              |              | U                | HS          | X               | X      | X      | X      | X      | X      | X          | X                | 1XX X                               | Х    | X  | X | X             |
| DCL     | device clear            |              | M                | UC          | Y               | Ø      | Ø      | 1      | Ø      | 1      | Ø          | Ø                | XXX 1                               | X    | X  | X | X             |
| END     | end                     |              | U                | ST          | X               | X      | X      | X      | X      | X      | X          | X                | XXX Ø                               | 1    | X  | X | X             |
| EOS     | end of string           | (Notes 2, 9) | M                | DD          | E<br>8          | E 7    | E<br>6 | E<br>5 | E<br>4 | E<br>3 | E 2        | E<br>1           | XXX Ø                               | X    | X  | X | X             |
| GET     | group execute trigger   |              | M                | AC          | Y               | Ø      | Ø      | Ø      | 1      | Ø      | Ø          | 0                | XXX 1                               | X    | X  | X | X             |
| GTL     | go to local             |              | M                | AC          | Y               | Ø      | Ø      | Ø      | Ø      | Ø      | Ø          | 1                | XXX 1                               | X    | X  | X | X             |
| IDY     | identify                |              | U                | UC          | X               | X      | X      | X      | X      | X      | X          | X                | XXX X                               | 1    | X  | Х | X             |
| IFC     | interface clear         |              | U                | UC          | X               | X      | X      | X      | X      | X      | X          | X                | XXX X                               | X    | X  | 1 | X             |
| LAG     | listen address group    |              | M                | AD          | Y               | Ø      | 1      | X      | X      | X      | X          | X                | XXX 1                               | X    | X  | X | X             |
| LLO     | local lock out          |              | M                | UC          | Y               | Ø      | Ø      | 1      | Ø      | Ø      | Ø          | 1                | XXX 1                               | X    | X  | X | X             |
| MLA     | my listen address       | (Note 3)     | M                | AD          | Y               | Ø      | 1      | L<br>5 | L<br>4 |        |            |                  | XXX 1                               | X    | X  | X | X             |
| MTA     | my talk address         | (Note 4)     | M                | AD          | Y               | 1      | Ø      | T<br>5 | T<br>4 | T<br>3 | T 2        | T<br>1           | XXX 1                               | X    | X  | X | X             |
| MSA     | my secondary address    | (Note 5)     | M                | SE          | Y               | 1      | 1      | S<br>5 | S<br>4 | S<br>3 | S<br>2     | 1                | LAXXX<br>19 AT                      |      |    |   | XIQC<br>PIB c |

Bus Signal Line(s) and Coding That Asserts the True Value of the Message D NN DRD A E S I R a AFA T O R F E 0 p 0 VDC N I Q C N Mnemonic Message Name 6 5 3 2 1 4 NUL null byte M DD 0 0 0 0 0 0 0 0 0 XXX X X X X X OSA other secondary address M  $(OSA = SCG \land MSA)$ OTA other talk address M  $(OTA = TAG \land MTA)$ PCG (PCG = ACG V UCG V LAG V TAG) primary command group M PPC parallel poll configure M AC Y Ø Ø Ø Ø 1 Ø 1 XXX 1 X X X X (Note 6) SPPP PPE parallel poll enable M 1 Ø XXX 1 X X X X 3 2 1 SE Y 1 1 1 D D D D PPD parallel poll disable (Note 7) M XXX 1 X X X X 4 3 2 PPR1 parallel poll response 1 U ST X X X X X X X 1 XXX 1 1 X X X PPR2 parallel poll response 2 U ST X X X X X X 1 X XXX 1 1 X X X PPR3 parallel poll response 3 (Note 10) U X X X X X X 1 X XXXX 1 1 X X X PPR4 parallel poll response 4 U ST X X X X 1 X X X XXX 1 1 X X X PPR5 parallel poll response 5 U ST X X X 1 X X X X XXX 1 1 X X X PPR6 ST X X 1 X X X X X XXX 1 1 X X X parallel poll response 6 U PPR7 (Note 10) XXX 1 1 X X X parallel poll response 7 U X 1 X X X X X XPPR8 XXX 1 1 X X X parallel poll response 8 U 1 X X X X X X X PPU XXX 1 X X X X parallel poll unconfigure M UC Y Ø Ø 1 Ø 1 Ø 1 REN remote enable H  $\mathsf{UC}\ \mathsf{X}\ \mathsf{X}\ \mathsf{X}\ \mathsf{X}\ \mathsf{X}\ \mathsf{X}\ \mathsf{X}\ \mathsf{X}\ \mathsf{X}$ XXX X X X X 1 RFD ready for data U X X X X X X X XXØX X X X X X HS XXX Q X X X X RQS request service (Note 9) U X 1 X X X X X XSCG XXX 1 X X X X secondary command group 1 X X X X X M 1 SDC selected device clear M 000100 XXX 1 X X X X AC Y Ø SPD serial poll disable M 0 0 1 1 0 0 1 XXX 1 X X X X SPE XXX 1 X X X X serial poll enable M Y 0 0 1 1 0 0 0 SRQ U ST X X X X X X X X XXX X X 1 X X service request STB XSSSSSS XXX Ø X X X X status byte (Notes 8, 9) M S 6 5 4 3 2 1 8 TCT take control AC Y Ø Ø Ø 1 Ø Ø 1 XXX 1 X X X X M X X X X XXXX 1 X X X X TAG talk address group M AD Y 1 Ø UCG universal command group M UC Y 0 Ø 1 X X X X XXX 1 X X X X 1 1 1 1 1 1 XXX 1 X X X X UNL unlisten M Y 1 Ø 1 1 1 1 1 XXX 1 X X X X UNT untalk (Note 11) M AD

The  $1/\emptyset$  coding on ATN when sent concurrent with multiline messages has been added to this revision for interpretive convenience.

#### NOTES

- (1) D1-D8 specify the device dependent data bits.
- (2) E1-E8 specify the device dependent code used to indicate the EOS message.
- (3) L1-L5 specify the device dependent bits of the device's listen address.
- (4) T1-T5 specify the device dependent bits of the device's talk address.
- (5) S1-S5 specify the device dependent bits of the device's secondary address.
  - (6) S specifies the sense of the PPR.

| S | Response |
|---|----------|
| Ø | 0        |
| 1 | 1        |

P1-P3 specify the PPR message to be sent when a parallel poll is executed.

| P3 | P2 | Pl | PPR Message |
|----|----|----|-------------|
| Ø  | θ  | Ø  | PPR1        |
| 10 |    | 8  |             |
|    |    |    |             |
| 9  |    |    |             |
| 1  | 1  | 1  | PPR8        |

- (7) D1-D4 specify don't-care bits that shall not be decoded by the receiving device. It is recommended that all zeroes be sent.
- (8) S1-S6, S8 specify the device dependent status. (DIO7 is used for the RQS message.)
- (9) The source of the message on the ATN line is always the C function, whereas the messages on the DIO and EOI lines are enabled by the T function.
- (10) The source of the messages on the ATN and EOI lines is always the C function, whereas the source of the messages on the DIO lines is always the PP function.
- (11) This code is provided for system use, see 6.3.

# Controllers

|       | null byte                  |           |      |    |     |     |     |     | 0.6 | 1 6 |     |       |   |   |   |   |   |
|-------|----------------------------|-----------|------|----|-----|-----|-----|-----|-----|-----|-----|-------|---|---|---|---|---|
|       | other secondary address    |           |      |    |     |     |     |     |     |     | (A) |       |   |   |   |   |   |
|       | other talk address         |           |      |    |     |     |     |     | AT  |     |     |       |   |   |   |   |   |
|       | primary command group      |           |      |    | (PC |     |     | V D |     |     |     |       |   |   |   |   |   |
| 7,449 |                            |           | - 3/ | -  | 1   | 9   | 0   | 4   | -   | -   |     | 25.25 | - | - | - | - | - |
|       | parallel poll enable       |           | M    |    |     |     | 0   |     |     |     | d,  |       |   |   |   | × |   |
|       |                            |           |      |    | I Y |     |     | D   |     |     |     |       |   |   |   |   |   |
|       | parallel poll response 1   |           |      | ST | X   |     |     |     |     |     | Ĭ   | XXX   |   |   |   |   |   |
| PPR2  | parallel poll response 2   |           | U    |    |     |     |     |     |     |     |     | XXX   |   |   |   |   |   |
| PPRS  | parallel poll response 3 } | (Note 10) |      |    |     |     | X 2 |     |     | X   |     |       |   | 1 |   |   |   |
|       | parallel poll response 4   |           |      |    |     |     |     |     |     |     | X   |       |   |   |   |   |   |
|       | parallel poll response 5 / |           |      | TE |     |     | 1.2 |     |     | X   |     |       |   |   |   |   |   |
|       | parallel poll response 6   |           |      |    | c x |     |     |     |     |     |     |       |   |   | X |   |   |
| PPRT  | parallel pull response 7   | (Note 10) |      |    |     |     |     |     |     |     |     | XXX   |   |   |   |   |   |
| PPRS  | parallel poli response 8   |           |      |    | 1 2 | X 2 | X X |     |     | ×   |     |       |   |   |   |   | X |
| Ugg   | parallel poll unconfigure  |           |      |    |     | 0 6 |     | 0   | 1   | 6   |     | XXX   |   |   |   |   |   |
| REN   | yemote enable              |           |      |    |     |     |     |     |     | X   |     |       |   |   |   |   |   |
|       | ready for data             |           | 0    |    | X   | X X |     |     |     |     |     |       |   |   |   |   |   |
|       | request service            | (Note 9)  |      |    | X   |     |     | X   |     |     |     |       |   |   |   |   |   |
|       | secondary command group    |           |      |    |     |     |     |     | X   |     |     |       |   |   |   |   |   |
|       | selected device clear      |           |      |    |     |     |     |     |     | 67  |     |       |   |   |   |   |   |
| SPD   | serial poll disable        |           | 141  |    |     |     |     | . 1 |     |     |     |       |   |   |   |   |   |
|       |                            |           | 3/4  |    |     | 0 8 |     |     | 0   |     | 0   |       |   |   |   |   |   |
|       | service request            |           |      |    |     |     | X X |     | Х   |     |     |       |   |   |   |   |   |
|       |                            |           |      |    |     |     |     |     |     | 8   |     |       |   |   |   |   |   |
|       | take control               |           | M    |    | Y   |     |     |     |     | 0   |     |       |   |   |   |   |   |
| DAT   | talk address group         |           | M    |    |     | 0 1 |     |     |     | X   |     |       |   |   |   |   |   |
|       | universal command group    |           |      |    | Y   | 0 0 | 1 6 |     |     |     |     |       |   |   |   |   |   |
|       |                            |           |      |    | Y   | 1 8 | 1 1 |     |     |     |     |       |   | X |   |   |   |
|       |                            |           | 挺    |    |     |     |     |     | 1   |     |     |       |   |   |   |   |   |

The 1.0 coding on ATN when sent concurrent with multiline messages has been added to this revision for interpre-

# 8255A Programmable and Contents Peripheral Interface INTRODUCTION enoits User's User's 014-2 system designer is presented with **OVERVIEW** task of selection a microprocessor for a design, the 8080 CPU MODULE INTERFACE COLUMN AND TO 2-410 PERIPHERAL INTERFACE SECTION of A to Improve 2-412 of INTERNAL LOGIC SECTION aved doing assisted 2-413ag directly address and solve the problems 'noisinifed aboM Logic Bit Set/Reset INTERRUPT CONTROL LOGIC STATUS WORDS 2-415 SOFTWARE CONSIDERATIONS VISITED IN TROUBLE OF 2-417 MODE 0-STATUS DRIVEN PERIPHERAL INTERFACE at villidization myissbor 8255A to Peripheral Hardware Interface comos lo sudmin 8080 CPU Module to 8255A Interface Mode 0 Interface Software band and mort selemans points of view Since the 8255A snoisulandaylyrammuZ MODE 1—INTERRUPT DRIVEN itanugitare bas anoit2-424 PRINTER INTERFACE CPU Module to 8255A Interface hoogs littled of benilbons 8255A to Peripheral Interface Mode 1 Software Driver Summary/Conclusions MODE 2-8080 TO 8080 INTERFACE 2 080 2-429 ule, memory module, and the Hardware Discussion Software Discussion Summary/Conclusions APPENDIX 2-436 8255A Quick Reference 8228 System Controller. The system shown in Figure 3 utilizes a linear select scheme which dedi-

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by the two port select signals  $(A_1, A_0)$ . These signals  $(A_1$  and  $A_0)$  are driven by the least significant bits of the address bus. The 1/O port select

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# INTRODUCTION

Microprocessor-based system designs are a costeffective solution to a wide variety of problems. When a system designer is presented with the task of selecting a microprocessor for a design, the capabilities of the microprocessor should not be the only consideration. The microprocessor should be an element of a compatible family of devices. The MCS-80 component family is a group of compatible devices which have been designed to directly address and solve the problems of microprocessor-based system design. One member of the MCS-80 component family is Intel's 8255A programmable peripheral interface chip. This device replaces a significant percentage of the logic required to support a variety of byte oriented Input/ Output interfaces. Through the use of the 8255A, the I/O interface design task is significantly simplified, the design flexibility is increased, and the number of components required is reduced.

This application note presents detailed design examples from both the hardware and software points of view. Since the 8255A is an extremely flexible device, it is impossible to list all of the applications and configurations of the device. A number of designs are presented which may be modified to fulfill specific user interface requirements.

Detailed design examples are discussed within the context of the 8080 system shown in Figure 1. The basic 8080 system is composed of the CPU module, memory module, and the I/O module. CPU module and memory module design are discussed

within other Intel publications. This application note deals exclusively with I/O module design.

It is assumed that the reader is familiar with the MCS-80 User's Manual and/or the MCS-85 User's Manual, particularly the 8255A device description.

# **OVERVIEW OF THE 8255A**

The 8255A block diagram shown in Figure 2 has been divided into three sections: 8080 CPU Module Interface, Peripheral Interface, and the Internal Logic.

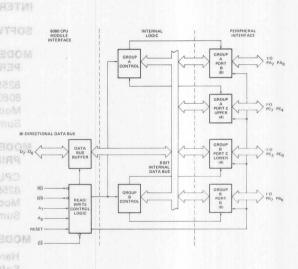


Figure 2. 8255A Block Diagram

# DATA BUS (8 LINES) CONTROL BUS (6 LINES) ADDRESS BUS (16 LINES)

# 8080 CPU MODULE INTERFACE

The 8255A is a compatible member of the MCS-80 component family and, therefore, may be directly interfaced to the 8080. Figure 3 displays one method of interconnecting the 8255A and an 8080 CPU module. The 8080 CPU module consists of the 8080A CPU, the 8224 Clock Generator, and the 8228 System Controller. The system shown in Figure 3 utilizes a linear select scheme which dedicates an address line as an exclusive enable (chip select) for each specific I/O device. The chip select signal is used to enable communication between the selected 8255A and the 8080 CPU. I/O Ports A, B, C, or the Control Word Register are selected by the two port select signals (A1, A0). These signals (A<sub>1</sub> and A<sub>0</sub>) are driven by the least significant bits of the address bus. The I/O port select characters required by this configuration are shown in Figure 4.

When a system utilizing the linear select scheme is implemented, a maximum of six I/O devices may be selected. If more than six I/O devices must be addressed, the six device select bits must be encoded to generate a maximum of 64 device select lines. Note that when large systems are implemented, bus loading considerations may require that bus drivers be included in the CPU module. The MCS-80 component family contains parts which are designed to perform this function (8216, 8226).

The 8255A I/O read (\$\overline{RD}\$) and I/O write (\$\overline{WR}\$) signals may be directly driven by the 8228. This results in an isolated I/O architecture where 8080 Input/Output instructions are used to reference an independent I/O address space. An alternate approach is memory mapped I/O. This architecture treats an area of memory as the I/O address space. The memory mapped I/O architecture utilizes 8080 memory reference instructions to access the I/O address space. Interfacing with the 8080 is outlined in Chapter 3 of the "8080 Microcomputer User's Manual".

The most important feature of the 8255A to 8080 CPU Module Interface is that for small system designs the 8255A may be interfaced directly to

the standard MCS-80 component family with no external logic. Minimum external logic is required in large system designs.

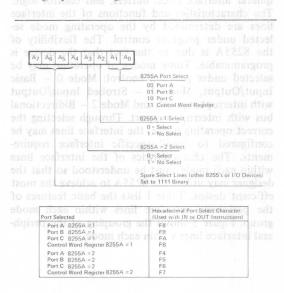
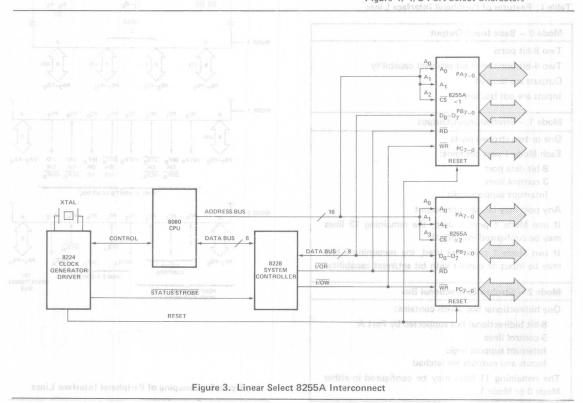


Figure 4. I/O Port Select Characters



ipheral interface lines, buffers, and control logic. The characteristics and functions of the interface lines are determined by the operating mode selected under program control. The flexibility of the 8255A is due to the fact that the device is programmable. Three modes of operation may be selected under program control: Mode 0 - Basic Input/Output, Mode 1 - Strobed Input/Output with interrupt support, and Mode 2 – Bidirectional bus with interrupt support. Through selecting the correct operating mode, the interface lines may be configured to fulfill specific interface requirements. The characteristics of the interface lines within each mode must be understood so that the designer may utilize the 8255A to achieve the most efficient design. Table I lists the basic features of the peripheral interface lines within each mode group. Figure 5 shows the grouping of the peripheral interface lines within each mode.

Table I. Features of Peripheral Interface Lines

# Mode 0 - Basic Input/Output

Two 8-bit ports

Two 4-bit ports with bit set/reset capability

Outputs are latched

Inputs are not latched

# Mode 1 - Strobed Input/Output

One or two strobed ports

Each Mode 1 port contains:

8-bit data port

3 control lines

Interrupt support logic

Any port may be input or output

If one Mode 1 port is used, the remaining 13 lines may be configured in Mode 0.

If two Mode 1 ports are used, the remaining 2 bits may be input or output with bit set/reset capability.

# Mode 2 - Strobed Bidirectional Bus

One bidirectional bus which contains:

8-bit bidirectional bus supported by Port A

5 control lines

Interrupt support logic

Inputs and outputs are latched

The remaining 11 lines may be configured in either Mode 0 or Mode 1.

Through the use of this teature, device strobes may be easily generated by software without utilizing external logic. The Mode 1 and Mode 2 configurations use a number of the Port C lines for interrupt control lines. Thus, the 8255A contains a large portion of the logic required to implement an interrupt driven I/O interface. This feature simplifies interrupt driven hardware design and saves a significant amount of the external logic that is normally required when less powerful I/O chips are used. In fact, the design examples contained in this application note describe how interrupt driven interfaces may be designed such that the only interrupt control logic required is that contained in the 8255A.

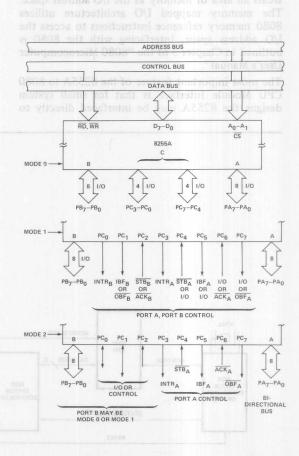


Figure 5. Grouping of Peripheral Interface Lines

# Control word (see Front Sac Signal Language)

The internal logic section manages the transfer of data and control information on the internal data bus (refer to Figure 2). If the port select lines (A1 and A<sub>0</sub>) specify Ports A, B, or C, the operation is an I/O port data transfer. The internal logic will select the specified I/O port and perform the data transfer between the I/O port and the CPU interface. As was previously mentioned, both the functional configuration of each port and bit set/reset on Port C are controlled by the system's software. When the control word register is selected, the internal logic performs the operation described by the control word. The control word contains an opcode field which defines which of the two functions are to be performed (mode definition or bit set/reset).

# Mode Definition JORTHOD 1- AMESS:

When the opcode field (Bit 7) of the control word is equal to a one, the control word is interpreted by the 8255A as a mode definition control word. The mode definition control word (shown in Figure 6) is used to specify the configuration of the

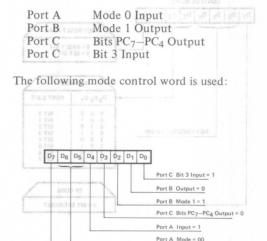
control word into the A register Since it is known that the set bit cor-D7 D6 D5 D4 D3 D2 D1 D0 A 9 00 A 9 00 A GROUP B PORT C (LOWER - PC3-PC0 TO ORESET BIT 3 1 = INPUT 1 0 = OUTPUT PORT B 1 = INPUT 0 = OUTPUT MODE SELECTION 0 = MODE 0 1 = MODE 1 his example demonstrates Example rforming a bit set/reset opera-B. The state of any output PORT C (UPPER - PC7-PC4) reading the port 1 = INPUT od VENT J pg of beau s peram which may b PORT A reset Port Tugni = 1 MODE SELECTION 00 = MODE 0 01 = MODE 1 1X = MODE 2 OPCODE 1 = MODE SET

Figure 6. Mode Definition Control Word

24 8255A peripheral interface lines. The system's software may specify the modes of Port A and Port B independently. Port C may be treated independently or divided into two portions as required by the Port A and Port B mode definitions.

Example #1: This example demonstrates how a mode control word is constructed and issued to an 8255A. The mode control word is passed to the device through the use of an output instruction that references an 8080 I/O port address. The value of the I/O port address is determined by the 8080 CPU interface implemented. This example references the I/O port addresses realized by the simple 8080 to 8255A interface shown in Figure 3.

If an 8255A is to be configured through the use of the mode control word interface as:



Opcode Mode Set = 1

The assembly language program is:

Mode Control Word = 10010101 Binary

Example #2: This example demonstrates how a Port C bit set/reset control word is constructed and issued to an MCZ-SA The bit set/reset control word is set/reset control word is set/reset control word in the set of the se

# Bit Set/Reset and sectional interface from teaching ASSSA 45

When the opcode field (Bit 7) of the control word is equal to a zero, the control word is interpreted by the 8255A as a Port C bit set/reset command word (see Figure 7). Through the use of the bit set/reset command, any of the 8 bits on Port C may be independently set or reset. Note that control word bits 6-4 are not used. Bits 6-4 should be set to zero.

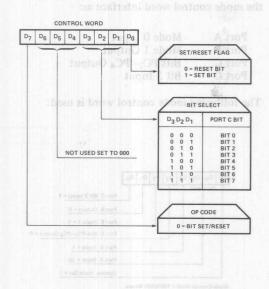
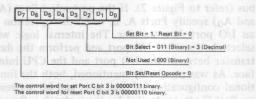


Figure 7. Bit Set/Reset Control Word

Example #2: This example demonstrates how a Port C bit set/reset control word is constructed and issued to an 8255A. The bit set/reset control word is passed to the device through the use of an output instruction that references an 8080 I/O port address. The value of the I/O port address is determined by the 8080 CPU interface implemented. This example references the I/O port addresses realized by the simple 8080 to 8255A interface shown in Figure 3.

Control word (see Figure 7).



The control word for reset Port C bit 3 is 00000110 binary.

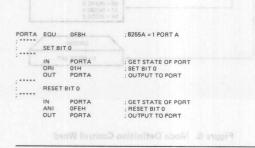
The assembly language program is:



NOTE: An MVI instruction is used to load the reset bit 3 control word into the A register. Since it is known that the set bit control word is already in the A register, a "DCR A" Instruction could be used to generate the correct control word and save one byte of code.

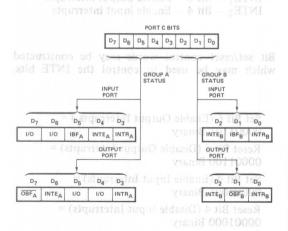
00000111 - 1 = 00000110 (RESET BIT 3 CONTROL WORD)

Example #3: This example demonstrates one simple method of performing a bit set/reset operation on Ports A and B. The state of any output port may be determined by reading the port. The assembly language program which may be used to set/reset Port A or B bits is:



# 

As previously mentioned, the 8255A Mode 1 and Mode 2 configurations support interrupt control logic. If a read of Port C is issued when the 8255A is configured in Mode 1, the software will receive the Mode 1 status word shown in Figure 8. The bits in the status word correspond to the state of the associated Port C lines (buffer full, interrupt request, etc.). The INTE bit shown in the status word corresponds to the interrupt enable flip-flop contained in the 8255A. This signal is not available externally. The structure of the Mode 1 status word varies as a function of the mode of the 8255A. Example #4 shows the status word which results from reading Port C from an 8255A which is configured with Port A Mode 1 input and Port B Mode 1 output.



The control words shown were constructed from the standard bit set/riset format shown in Fig.

Figure 8. Mode 1 Status Word

# Example #4 - MODE 1 STATUS WORD

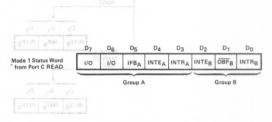
If an 8255A is to be configured through the use of the mode control word interface as:

Port A Mode 1 Input
Port B Mode 1 Output
Port C Bits 6 & 7 Output

The following mode control word is used:

The training and the state of the second and the state of the second and the seco

After the 8255A mode control word has been issued, a READ of Port C will obtain the following Mode 1 status word:



NOTE: The Port C I/O bits D<sub>7</sub> and D<sub>6</sub> should be modified through the use of the Port C bit set/reset command word. If a write to Port C is issued, the INTE<sub>A</sub> and INTE<sub>B</sub> bits may be inadvertently modified by the user. The IBF<sub>A</sub>, INTR<sub>A</sub>, OBF<sub>B</sub>, and INTR<sub>B</sub> bits will not be modified by either a write to Port C or a bit set/reset command. These four bits always reflect the state of the interrupt control logic.

Port A Mode 2 Bidirectional Bus
Port B Mode 1 Input
he following mose control word is used:

Note that the Mode 2 status word (shown in Figure 9) differs from the Mode 1 status word. The format of the status word data bits  $D_2$ – $D_0$  are defined by the specification of the Port B configuration. Example #5 shows the structure of the Mode 2 status word when the 8255A is configured with Port A Mode 2 (bidirectional bus) and Port B Mode 1 input.

The Mode 1 and Mode 2 status words reflect the state of the interrupt logic supported by the 8255A.

ples provide a more detailed explanation of the use of the Port C status word in the Mode 1 and Mode 2 configurations.

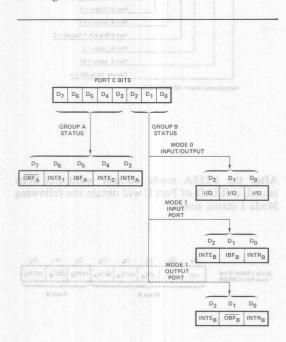


Figure 9. Mode 2 Status Word

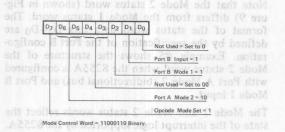
Example #5 – MODE 2 STATUS WORD

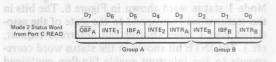
If the 8255A is to be configured as follows:

Port A Mode 2 Bidirectional Bus

Port B Mode 1 Input

The following mode control word is used:





Example #6 - MODE 2 INTERRUPT ENABLE/DISABLE

The Mode 2 status word shown in Figure 9 contains two interrupt enable bits:

INTE<sub>1</sub> - Bit 6 - Enable output interrupts INTE<sub>2</sub> - Bit 4 - Enable input interrupts

Bit set/reset control words may be constructed which may be used to control the INTE bits.

Set Bit 6 (Enable Output Interrupts ) = 00001101 Binary

Reset Bit 6 (Disable Output Interrupts) = 00001100 Binary

Set Bit 4 (Enable Input Interrupts) = 00001001 Binary

Reset Bit 4 (Disable Input Interrupts) = 00001000 Binary

The control words shown were constructed from the standard bit set/reset format shown in Figure 7.

The value of CWR used in the following program example corresponds to the 8080 configuration shown in Figure 3.

| EQU   | OFBH                | ; 8255A = 1 CONTROL WORD REGISTER                                                  |
|-------|---------------------|------------------------------------------------------------------------------------|
| ENABL | E INTERRUPTS FO     | OR MODE 2 OUTPUT (SET PORT C BIT 6)                                                |
|       |                     |                                                                                    |
|       | A, 00001101B        | ; GET SET BIT 6 CONTROL WORD                                                       |
| OUT   | CWR                 | : OUTPUT TO 8255 =1 CONTROL WORD REGISTER                                          |
|       |                     |                                                                                    |
| DISAB | LE INTERRUPTS F     | OR MODE 2 OUTPUT (RESET PORT C BIT 6)                                              |
|       |                     | THE U TO SEE STATE OF THE SECOND STATES                                            |
| MVI   | A 00001100B         | : GET RESET BIT 6 CONTROL WORD                                                     |
|       |                     | OUTPUT TO 8255A = 1 CONTROL WORD REGISTER                                          |
|       | ENABI<br>MVI<br>OUT | ENABLE INTERRUPTS FOR MVI A, 00001101B CWR DISABLE INTERRUPTS FOR MVI A, 00001100B |

always issue the correct mode control word after a reset of the device. Generally, an initialization routine is constructed which issues the correct mode control word, sets up the initial state of the control lines, and initializes any program internal data.

Many of the software requirements of the 8255A vary as a function of the mode selected. The simplest mode supported by the device is Mode 0 (Basic Input/Output). Generally, Mode 0 is used for simple status driven device interfaces (no interrupts). Figure 10 illustrates sample software that could be used to support such interfaces. Most devices support a BUSY or READY signal which is used to determine when the device is ready to input or output data and a DATA STROBE which is used to request data transfer (DATA STROBE may easily be generated with the Port C bit set/ reset feature). In the Mode 0 configuration, Ports A and B are used to input/output byte oriented data. Port C is used to input 8255A status, peripheral status and to drive peripheral control lines. When the Mode 1 and Mode 2 configurations are used, the software is generally required to support interrupts. Software routines written for an interrupt driven environment tend to be more complex than status driven routines. The added complexity is due to the fact that interrupt driven systems are constructed such that other software tasks are run while the I/O transaction is in progress. A software routine that controls a peripheral device is generally referred to as a device driver. One method of implementing an interrupt driven device driver is to partition the device driver into a "Command Processor" and an "Interrupt Service Routine". The command processor is the module that validates

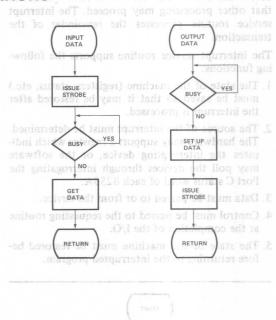


Figure 10. Sample Status Driven Software Flowchart

and initiates user program requests to the device driver. A common method of passing information between the various software programs is to have the requesting routine provide a device control block in memory. A sample device control block is shown in Table II.

Table II. Sample Device Control Block

| NAME                        | DESCRIPTION                                                                                                                     |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| Status                      | This 1-byte field is used to transmit the status of the I/O transaction (busy, complete, etc.).                                 |
| Opcode                      | This 1-byte field defines the type of I/O (READ, WRITE, etc.).                                                                  |
| Buffer Address              | This 2-byte field specifies the source/destination of the data block.                                                           |
| Character Count             | This 1-byte field is a count of the number of characters involved in the transaction.                                           |
| Character Transferred Count | This 1-byte count of the number of characters which were actually transferred.                                                  |
| Completion Address          | This 2-byte field is the address of the user supplied completion routine which will be called after the I/O has been performed. |

The command processor validates the transaction and initiates the operation described by the control block. Control is then returned to the requestor so that other processing may proceed. The interrupt service routine processes the remainder of the transaction.

The interrupt service routine supports the following functions:

- 1. The state of the machine (registers, status, etc.) must be saved so that it may be restored after the interrupt is processed.
- 2. The source of the interrupt must be determined. The hardware may support a register which indicates the interrupting device, or the software may poll the devices through interrogating the Port C status word of each 8255A.
- 3. Data must be passed to or from the device.
- 4. Control must be passed to the requesting routine at the completion of the I/O.
- 5. The state of the machine must be restored be-

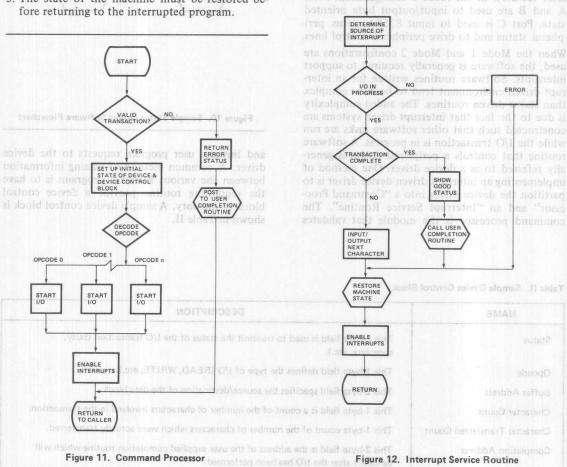
Figures 11 and 12 are simplified flowcharts of one of the many methods of implementing command processor and interrupt service routine modules. The rest of this application note presents specific application examples. All of the 8080 assembly language programs supplied with the application examples use the standard Intel 8080 assembly language mnemonics. The programs discussed use the program equate statement to specify all hard-

ware related data. Equate statements are used so that all references to an I/O port may be changed through a simple reassignment of the port address in the equate statement.

devices support a BUSY or READ THURRATHI WHICH IS

used to determine when the deviceV

STATE



# MODE 0 – STATUS DRIVEN PERIPHERAL INTERFACE

This design example shows how a single 8255A in Mode 0 may be used to develop a status driven interface (no interrupts) for the Centronics 306 character printer, the Remex paper tape punch, and the Remex paper tape reader.

# 8255A To Peripheral Hardware Interface

The first step in the design is to examine the specification for the peripheral devices and identify the control and data signals which must be supported by the interface. Table III lists the signals which were chosen to be supported by the 8255A interface. All three of the devices support the standard

Table III. Peripheral Interface Signals

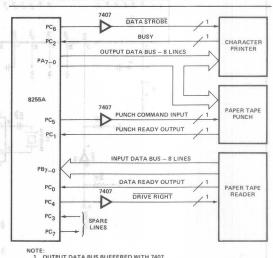
| Name:       | DATA 0-DATA 7                                                                                                                                   |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| Definition: | Input data levels. A high signal represents binary 1 and a low signal represents a bina 0. These eight lines are the data lines to the printer. |
| Name:       | DATA STROBE                                                                                                                                     |
| Definition: | A 0.5 µsec pulse (minimum) used to transfer data from the 8255A to the printer.                                                                 |
| Name:       | BUSY                                                                                                                                            |
| Definition: | The level indicating that the printer canno receive data.                                                                                       |
| PER TAPE P  | PUNCH                                                                                                                                           |
| Name:       | TRACKS 1-8 DATA INPUT                                                                                                                           |
| Definition: | Input data levels. A high signal causes a hole to be punched on the associated tracl These eight lines are the data lines to the printer.       |
| Name:       | PUNCH COMMAND INPUT                                                                                                                             |
| Definition: | A true condition moves the tape and initiates punching the tape. This signal is actually a data strobe.                                         |
| Name:       | PUNCH READY OUTPUT                                                                                                                              |
| Definition: | True signal indicates that the punch is rea to accept a punch command. This is the punch busy line.                                             |
| PER TAPE F  | READER                                                                                                                                          |
| Name:       | DATA TRACK OUTPUTS                                                                                                                              |
| Definition: | True signal indicates data track hole. The eight lines are the data lines from the pund                                                         |
| Name:       | DRIVE RIGHT                                                                                                                                     |
| Definition: | True signal drives the tape to the right and reads a character. This signal is actually the data strobe (initiate read signal).                 |
| Name:       | DATA READY OUTPUT                                                                                                                               |
| Definition: | True signal indicates data track outputs ar<br>in "On character" condition. This signal is<br>the reader busy line.                             |

BUSY/DATA STROBE interface discussed previously (see Figure 10). Figure 13 is a block diagram of the interface design. The 8255A Port A is configured as a Mode 0 output port which is used to support the printer and the paper tape punch data bus. Port B is configured as a Mode 0 input port and is used to input the paper tape reader data. Three of the Port C lower bits (PC<sub>2</sub>-PC<sub>0</sub>) configured in input mode are used to input the device busy indications. Three of the Port C upper bits (PC<sub>6</sub>-PC<sub>4</sub>) configured in output mode are used to support the device strobe signals required by each device.

The drive requirements of the interface lines are a function of the peripheral interface circuitry, the length of the interface cable, and the environment in which the unit is running. In this particular design example, all output lines from the 8255A to the peripherals were buffered through a 7407 buffer/driver. The input lines from the peripherals were fed directly into the Port C and Port B inputs.

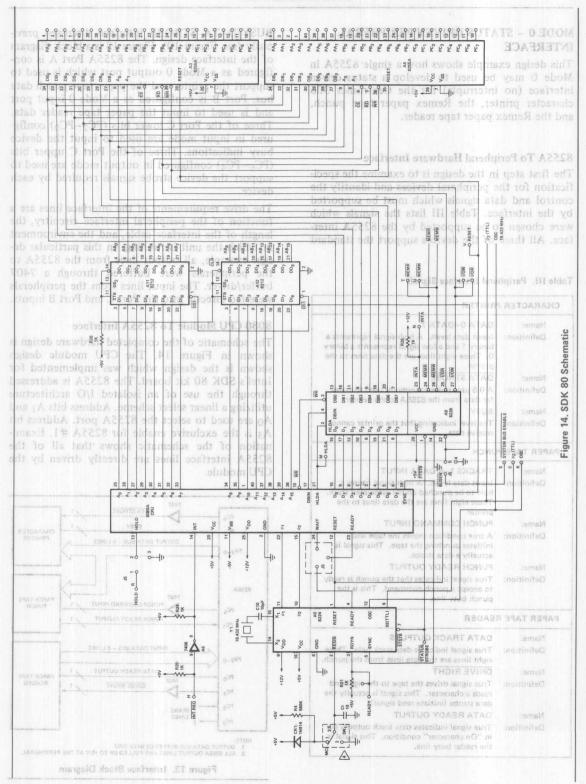
# 8080 CPU Module To 8255A Interface

The schematic of the completed hardware design is shown in Figure 14. The CPU module design shown is the design which was implemented for Intel's SDK 80 kit board. The 8255A is addressed through the use of an isolated I/O architecture utilizing a linear select scheme. Address bits A<sub>1</sub> and A<sub>0</sub> are used to select the 8255A port. Address bit A<sub>3</sub> is the exclusive enable for 8255A #1. Examination of the schematic shows that all of the 8255A interface lines are directly driven by the CPU module.



OUTPUT DATA BUS BUFFERED WITH 7407.
 ALL 8255A OUTPUT LINES ARE PULLED UP TO +5 V AT THE PERIPHERAL.

Figure 13. Interface Block Diagram



# Mode 0 Interface Software

An initialization routine and three device drivers (one for each peripheral device) are required to support the peripheral interface. The I/O port addresses implemented by the hardware are shown in Figure 15. The unused chip select bits are set to one so that chip select conflicts will not result if the unused bits are required by an expanded system.

8255A Port Select

8255A Port Select

90 Port A

10 Port B

10 Port C

11 Control Word Register

8261S A et al.

9 Select

10 Port B

10 Port C

11 Control Word Register

9 Select

11 No Select

12 No Select

12 No Select

13 No Select

14 No Select

15 No Select

16 No Select

17 No Select

18 No Select

18 No Select

19 No Select

19 No Select

10 Post B

10 Port B

11 Port B

12 Port B

13 Port B

14 Port B

15 Port B

16 Port B

17 Port B

18 
| Port Selected                   | Port Select Character<br>(In Hexadecimal) |
|---------------------------------|-------------------------------------------|
| Port A 8255A #1                 | F4                                        |
| Port B 8255A #1                 | F5                                        |
| Port C 8255A #1                 | F6                                        |
| Control Word Register 8255A = 1 | F7                                        |
| Port A 8255A #2                 | EC                                        |
| Port B 8255A #2                 | ED                                        |
| Port C 8255A #2                 | EE                                        |
| Control Word Register 8255A #2  | EF                                        |

Figure 15. I/O Port Addresses

Note that the initialization routine issues the mode control word (shown in Figure 16). It also sets the low true DATA STROBE signals to an inactive (high) state.

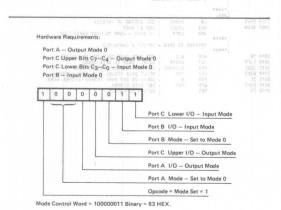
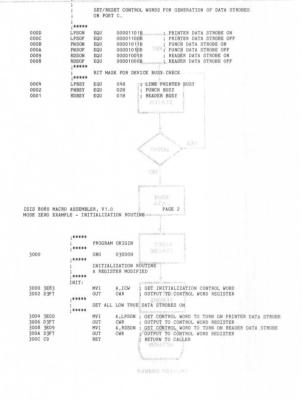


Figure 16. Mode Control Word

The three peripheral drivers which follow all have the basic structure discussed previously. Consider the printer routine. Here the user routine places an ASCII data character in the C-register and passes control to the LPST location through a subroutine call. The printer driver interrogates the status of the printer by reading Port C. If the printer is busy, the routine will loop until the printer is idle. When the routine will loop until the printer is idle. When the printer is ready to accept a data character, the character is placed on the Port A lines and a DATA STROBE, the driver ready cutes a soliv subsessions for the collections of the collection of the collection of the collection of the collections of the collections of the collection of the collections 
The DATA STROEE SHAME ONE ZERO EXAMPLE STROES ATE CHARACTER PRINTER, PAPER TAPE PUNCH, PAPER TAPE READER 1519 193 reset feature. The bit set/reset control awards used ..... PROGRAM FOUNTES ..... end software required bond control word being e device USED TO CONFIGURE THE 8255 AS FOLLOWS: accommodate a PORT A - OUTPUT MODE ZERO
PORT B - INPUT MODE ZERO Tional interface Tupks - (ASPRA) 2 TROP od by the peripheral .... ICW EQU 0083 100000118 : INITIALIZATION CONTROL WORD



The three peripheral drivers which follow all have the basic structure discussed previously. Consider the printer routine. Here the user routine places an ASCII data character in the C-register and passes control to the LPST location through a subroutine call. The printer driver interrogates the status of the printer by reading Port C. If the printer is busy, the routine will loop until the printer is idle. When the printer is ready to accept a data character, the character is placed on the Port A lines and a DATA STROBE is generated. After generating the DATA STROBE, the driver executes a subroutine return to the caller.

The DATA STROBE signals to the devices are generated through the use of the Port C bit set/reset feature. The bit set/reset control words used are shown in Figure 17.

# Summary/Conclusions

This design example discussed the basic hardware and software required to handle a simple device interface. The 8255A will easily accommodate a more complex interface design which utilizes additional interface lines supported by the peripheral.

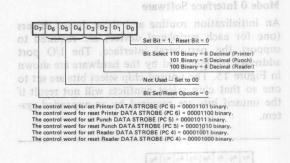
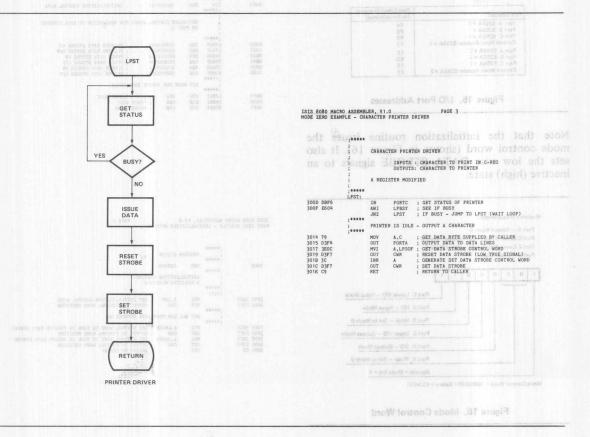


Figure 17. Bit Set/Reset Control Words

For instance, one of the spare Port C output lines may be used to control the punch direction. Support of this additional feature would require minor modification of the device driver so that the punch direction line could be specified by the user routine.

Through consideration of this example, the use of the 8255A in Mode 0 should become evident.





ISIS 8080 MACRO ASSEMBLER, VI.O PAGE 4
MODE ZERO EXAMPLE - PAPER TAPE PUNCH DRIVER of believing PAPER TAPE PUNCH DRIVER PAPER TAPE PUNCH DRIVER

INPUTS: DATA TO PUNCH IN C-REGISTER

OUTPUTS: DATA TO PUNCH

A REGISTER MODIFIED

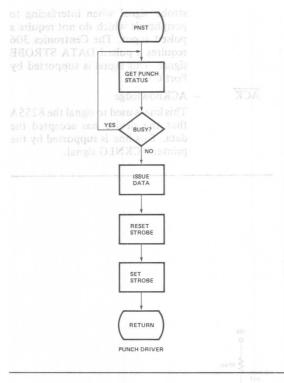
A REGISTER MODIFIED IN PORTC : GET STATUS OF PUNCH
ANI PREST : SEE IF BUST
JUE PRST : IF BUST JUMP TO PNST (MAIT LOOP) PNST: 3021 E602 3023 C21F30 ..... acter printer. PUNCH IS IDLE - OUTPUT A CHARACTER \*\*\*\*\* MOV A,C ; GET DATA BYTE SUPPLIED BY CALLER
OUT PORTA ; OUTPUT DATA TO DATA LINES.
WYI A; PRSOW SET DATA STROBE CONTROL WORD
OUT CWR : SET DATA STROBE
OUT CWR : SET DATA STROBE
OUT CWR : SET DATA STROBE
OUT CWR : RESET DATA STROBE
OUT : RESET DATA STROBE
OUT : RESET DATA STROBE
OUT : RESET DATA STROBE 3026 79 3029 3E0B 302B D3F7 ampic is the same as the Mode 0 example with the

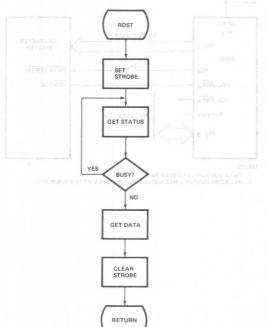
ISIS 8080 MACRO ASSEMBLER, VI.0 PAGE 5

LEMBLE C THOPAPER TAPE READER DRIVER OF CONTROL OF THE SHIP SHIP PAPEN TAPE MEADEN DRIVEN

INPUTS: DATA FROM READER
OUTPUTS: CHARACTER TO USER IN C-REGISTER

A AND C REGISTER MODIFIED ACK inter-RDST: MVI A,ROSOF; GET STROBE CONTROL WORD (LOW TRUE SIGNAL)
CWR ; SET DATA STROBE
PORTC ; GET STATUS OF DEVICE 3031 3E08 3033 D3F7 3035 DBF6 RDBSY ; SEE IF BUSY RDLP ; IF BUSY - LOOP UNTIL IDLE 3037 E601 3039 C23530 ..... READER NOT BUSY - GET CHAR AND CLEAR STROBE DIN PORTB : GET CHARACTER
NYI C,A SAVE CHARACTER
OUT CWR : TURN OFF STROBE SET CONTROL MORD (LOW TRUE SIGNAL) THE negaus: END OF MODE ZERO EXAMPLE





READER DRIVER

ONS ANATOR INTERIOR DESCRIPCE IN THE PREVIOUS ous example required the software driver to poll the device status for completion. An alternate approach is to construct the device interface such that an interrupt is used to signal the completion of the operation. When an interrupt driven interface is utilized, the time that was dedicated to polling can be used to perform other functions and the effective processor through-put is increased. This example demonstrates how an 8255A configured in Mode 1 may be used to develop an interrupt driven interface for the Centronics 306 character printer.

# CPU Module To 8255A Interface

The 8080 bus interface implemented for this example is the same as the Mode 0 example with the addition of interrupt support. Interrupt support is implemented through the use of a special feature of the 8228 System Controller. If only one interrupt vector is required (such as in small systems), the 8228 can automatically assert an RST 7 instruction onto the data bus at the proper time. This option is selected by connecting the INTA output of the 8228 to the +12-volt supply through a 1K ohm series resistor.

The Mode 1 interrupt support logic of the 8255A provides an interrupt request line for each port. The 8255A interrupt request line (INTRA) must be connected to the INT line of the 8080. A 10K ohm pullup resistor is used to insure that the VIH requirements of the 8080 are met.

# 8255A To Peripheral Interface

The interrupt driven configuration control signal interface to the printer is different than the status driven interface. Instead of a BUSY/DATA STROBE interface, a DATA STROBE/ACK interface is supported. The ACK signal notifies the 8255A that a character transferred to the printer by a DATA STROBE has been accepted. After an ACK is issued the printer is considered idle. The block diagram shown in Figure 18 displays the interface signals used.

The Mode 1 interrupt driven peripheral support signals used are:

PA<sub>7</sub>-PA<sub>0</sub> - Output Data

Used to support the printer data port.

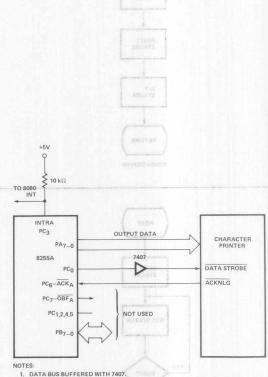
OBF

- Output Buffer Full

This line goes low when data is placed in the output buffer. The OBF signal may be used as a data partie input. The Controlles 200 requires a pulsed DATA STROBE signal. This signal is supported by Port C bit 0.

ACK ACKnowledge

> This line is used to signal the 8255A that the device has accepted the data. This line is supported by the printer ACKNLG signal.



ALL 8255A OUTPUT LINES ARE PULLED UP TO +5 V AT THE PERIPHERAL



Figure 18. Interface Block Diagram

# Mode 1 Software Driver

The software driver implemented for this example utilizes the typical interrupt driven software structure outlined previously. The initialization routine issues the mode control word (shown in Figure 19) to the 8255A after reset of the device. The initialization routine also places a jump to the interrupt service routine in the interrupt location for RST 7. The command processor is started by the user routine through a subroutine call to PSTRT, with the address of the control block in the D and E registers (the control block format is shown in Table IV). The command processor insures that an I/O operation is not already in progress, starts the I/O, enables interrupts, and returns to the caller so that other processing may proceed.

After a character is placed in the output buffer, the DATA STROBE signal is generated through the use of the Port C bit set/reset feature. When the ACK is generated by the printer, the buffer full indication is cleared and the 8255A generates an interrupt. If interrupts are enabled, the interrupt request is serviced by the 8080 CPU through disabling processor interrupts and then executing the instruction at location 38 hexadecimal in program memory. The interrupt service routine saves the processor state and polls the 8255A to determine the source of the interrupt. Once the interrupting device is located, the control block is used to locate the next data character for transfer to the 8255A output buffer. After the entire buffer has been printed, the interrupt service routine passes control to the user-supplied completion routine. Before returning from the interrupt, the state of the processor is restored.

Hardware Requirements:

Port A — Input Mode 1
Port C (Upper)
Port B Port C (Upper)
Not Used
Port B Not Used Set to Input Mode
Port B Not Used Set to Input Mode
Port A I/O Set to Input Mode
Port A I/O Set to Input Mode
Port A I/O Set to Output
Port B Mode Not Used Set to Opcode = Mode Set

Mode Control Word = 10101010 Binary = AA HEX.

Figure 19. Mode Control Word

Table IV. Printer Software Control Block

| NAME THE SECOND SECOND         | POSITION  | THE PROPERTY OF THE PROPERTY O |
|--------------------------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Status                         | Byte 0    | A 1-byte field which defines the completion status of an I/O.  00 = Good completion 01 = Error – command already in progress                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Buffer Address                 | Byte 1, 2 | Pointer to the start of the data to print.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Character Count                | Byte 3    | Count of the number of characters to print.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Character<br>Transferred Count | Byte 4    | The number of characters transferred.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Completion<br>Address          | Byte 5, 6 | Address of a user supplied routine which will be called after the I/O has been performed.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

## NOTES:

- 1. An opcode field is not required because WRITE is the only operation performed.
- 2. The control block must reside above location FF Hex.

There are a number of error conditions which may occur, such as an interrupt from a device which does not have a control block in progress, or an interrupt when polling establishes that no device requires service. Neither of these errors should occur, but if they do, the driver should perform in a consistent fashion. The recovery routines implemented to handle error conditions are determined by the particular applications environment.

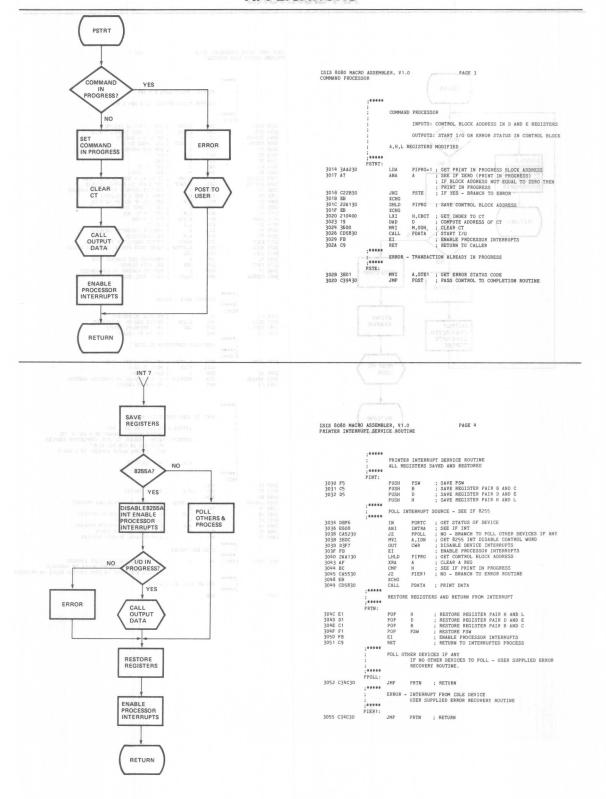
# Summary/Conclusions

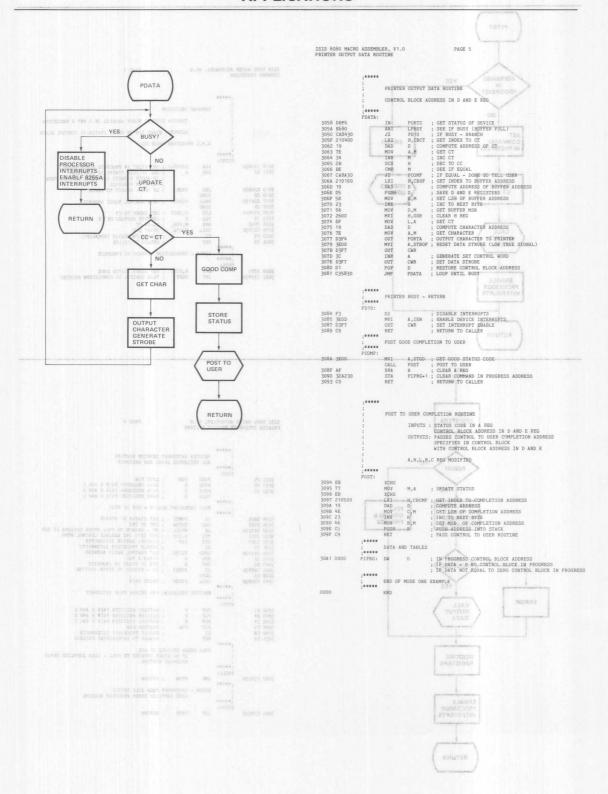
When utilized in a small system design, the 8255A interrupt support logic provides all of the capabilities required to implement an interrupt driven hardware interface without the use of external logic. In larger system designs, the designer may chose to use additional hardware to determine the source of interrupt requests without software polling. The software design required by an interrupt driven system is inherently more complex than the status driven interface. If an interrupt driven system is required the added complexity is a small price to pay for a significant increase in system through-put.

ISIS 8080 MACRO ASSEMBLER, V1.0 MODE ONE EXAMPLE The software driver implemented for this example utilizes the typical interrupt driven software struc-CHARACTER PRINTER - INTERRUPT DRIVEN ON SMITH SILL issues the mode control word (shown in Figure 19) routine through a subroutine call to ParillT, with INITIALIZATION CONTROL WORD THE TIME OF THE 8255 AS FOLLOWS: PORT A - OUTPUT MODE 1
PORT B - INPUT MODE 0 (NOT USED)
PORT C LOWER - OUTPUT 88AA IOW EQU 18181818B ; INITIALIZATION CONTROL WORD ; SET/RESET CONTROL WORDS BALL STILLS SOCIED 18 410 18 41 0001 STBON EQU 00000001B ; SET STACBE 0000 STBOC EQU 0000000B ; RESET STACBE ; 8255 ENABLE/DISABLE INTERRUPT CONTROL WORDS 800D IEN EQU 00001101B ; EMBLE INTESSUPTS 000C IDN EQU 00001100B ; DISABLE INTERSUPTS DEVICE STATUS EQUATES | MING BELL VO DESTRETON SE 8888 LPBSY EQU 888H ; BUFFER FULL (LINE PRINTER BUSY)
8888 INTRA EQU 88H ; INTERRUPT REQUEST ISIS 8880 MACRO ASSEMBLER, V1.0 PAGE 2 processor state and polls the 8255A to d algument and adom the source of the interrupt Once the interrupting device is located, the cearmon xous corms ... ; COMPLETION STATUS EQUATES 8888 STGD EQU 88H ; GOOD COMPLETION 8881 STEI EQU 81H ; ERBOR - COMMAND ALREADY IN PROGRESS PROGRAM ORIGIN ..... 3000 ORG 03000H ,\*\*\*\* INITIALIZATION ROUTINE A.H.L. REGISTERS MODIFIED A, TON ; GET MODE CONTROL MONE RELISTER
ONE , CUTFLY TO CONTROL MONE RELISTER
A, STECK ; GET SET DATA STREET CONTROL MONE

AS EL DATA STREET (LOW TRUE SIGNAL) SET UP RESTART 7 LOCATION WITH JUMP TO PINT ..... A,8C3H ; GET "JMP" ; PLACE IN RST7 LOCATION H,PINT ; GET ADDRESS OF INTERRUPT SERVICE ROUTINE RST7+1 ; STORE ADDRESS

Mode I Software Drit spag





# MODE 2 - 8080 TO 8080 INTERFACE

Due to the drastic reduction of hardware costs, system designs which utilize multiple CPU Modules are becoming more common. An 8080 may be configured as a master CPU and used to control multiple 8080 slave modules which act as intelligent I/O controllers. When multiple CPUs are utilized, a method of processor intercommunication must be supported. Figure 20 is a block diagram of one method of implementing a master/slave interface through the use of the 8255A Mode 2 bidirectional bus.

# Hardware Discussion

Two complete 8080 systems are required for this example. Intel's SBC 80/10 OEM board is used as the master CPU module and Intel's SDK 80 board is used as the slave CPU. The SBC 80/10 supports an 8255A which is configured in Mode 2. The 8255A is selected through the use of a decoded select scheme. Through the use of the 8228 RST 7 interrupt feature, a simple interrupt structure is supported. The SDK 80 is configured without interrupts for this example. The external logic required for this example is associated with the slave CPU. Simple logic is implemented which allows the slave CPU to generate the ACK and STB signals required to READ from and WRITE to the 8255A-bidirectional bus with a single I/O instruction.

The system shown in Figure 20 utilizes SSI logic to read the 8255A IBF and OBF signals. If two spare 8255A input lines are available they could be used to input the IBF and OBF signals and eliminate the SSI logic.

# Software Discussion

Two sets of software are required to support the processor to processor interface. The master resident software which follows conforms to the simple interrupt driven software structure outlined previously. The initialization routine issues the Mode 2 control word to the 8255A after device reset. The command processor accepts READ/WRITE control blocks which provide a simple user interface for transferring data to/from the slave CPU. The master software is capable of processing both a read and a write control block simultaneously. The slave resident software shown at the end of this example utilizes the status driven approach.

# Summary/Conclusions

It is important to note that this design may be expanded to include more slave CPUs by simply adding another 8255A to the master module for each slave. The software drivers discussed address only the passing of data between the two processors. Specific applications generally dictate a software protocol be implemented for information transfer.

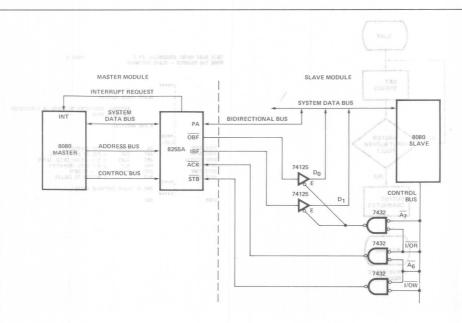
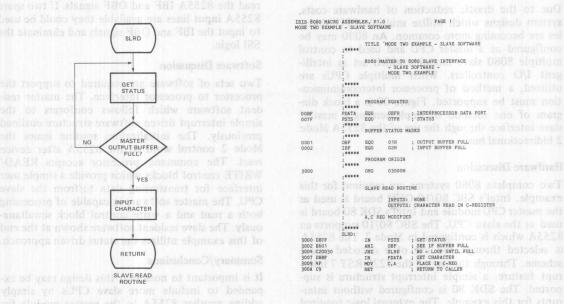
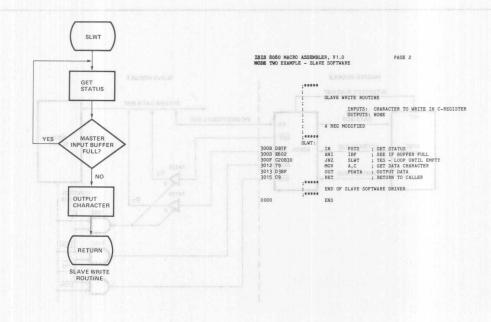


Figure 20. Interface Block Diagram





ISIS 8080 MACRO ASSEMBLER, V1.0 MODE TWO EXAMPLE - MASTER SOFTWARE PAGE 1 TITLE 'MODE TWO EXAMPLE - MASTER SOFTWARE' 8080 MASTER TO 8080 SLAVE INTERFACE - MASTER SOFTWARE -MODE TWO EXAMPLE \*\*\*\*\* \*\*\*\*\* PROGRAM EQUATES PORTA PORTB PORTC CWR RST7 0E4H 0E5H 0E6H 0E7H 038H ; 8255 PORT A ; 8255 PORT B ; 8255 PORT C ; 8255 CONTROL WORD REGISTER ; RESTART 7 ADDRESS ..... INITIALIZATION CONTROL WORD USED TO CONFIGURE THE 8255 AS FOLLOWS: USED TO CONFIGURE THE 8255 AS FOLLOWS:

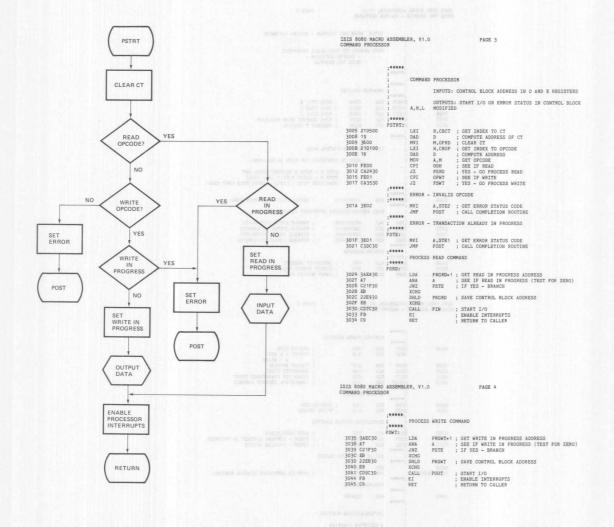
USED TO CONFIGURE THE 8255 AS FOLLOWS:

USED TO CONFIGURE THE 8255 AS FOLLOWS:

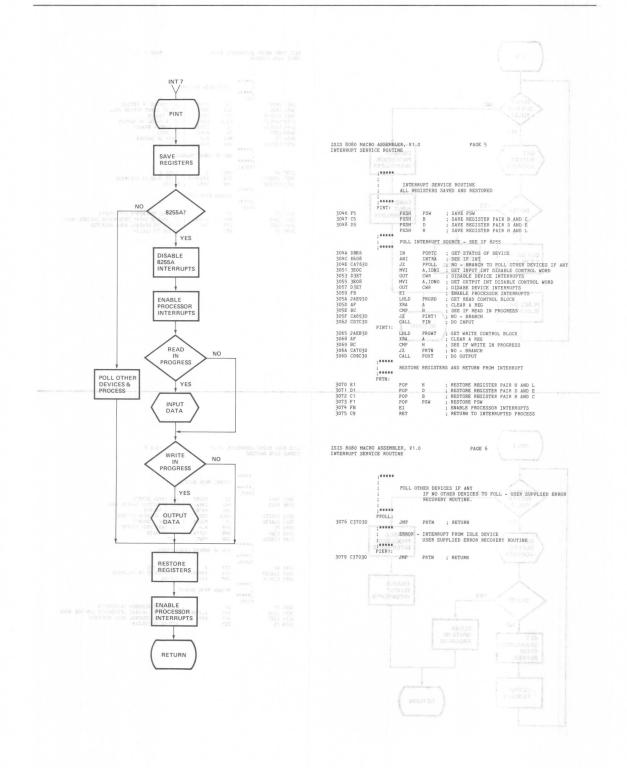
POST B - INDUT MODE OR LOT USED)

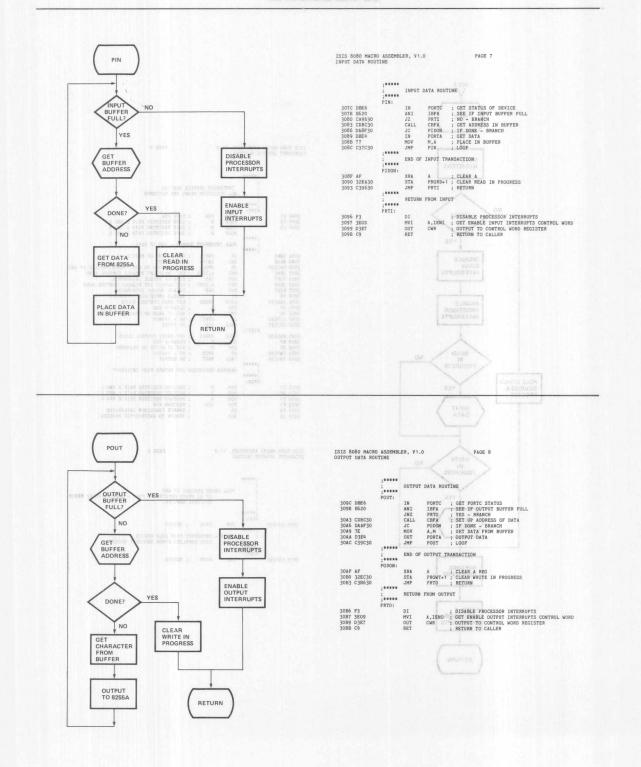
REMAINING FORT C LINES - INPUT MODE (NOT USED) 8255 ENABLE/DISABLE INTERRUPT CONTROL WORDS \*\*\*\*\* 00001101B 00001001B 00001100B 00001000B ; ENABLE INPUT INTERRUPTS ; ENABLE OUTPUT INTERRUPTS ; DISABLE INPUT INTERRUPTS ; DISABLE OUTPUT INTERRUPTS IENI IENO IDNI EQU EQU EQU STATUS EQUATES ..... ; INTERRUPT REQUEST ; OUTPUT BUFFER FULL ; INPUT BUFFER FULL ISIS 8080 MACRO ASSEMBLER, V1.0 MODE TWO EXAMPLE - MASTER SOFTWARE CONTROL BLOCK EQUATES
CBST EQU OOH
CBOP EQU ; STATUS BYTE
; OPCODE = 0 READ
; = 1 WRITE
; BUFFER ADDRESS
; CHARACTER COUNT
; CHARACTER TRANSFERD COUNT
; COMPLETION SERVICE ADDRESS 0000 EQU 02H EQU 04H EQU 05H EQU 06H OPCODE EQUATES \*\*\*\*\* EQU 00H ; READ OPCODE EQU 01H ; WRITE OPCODE OPRD OPWT STGD STE1 STE2 EQU 00H EQU 01H EQU 02H ; GOOD COMPLETION ; ERROR - COMMAND ALREADY IN PROGRESS ; ERROR - INVALID OPCODE 0000 0001 0002 SET UP INTERRUPT VECTOR \*\*\*\*\* 0038 0038 C34630 ORG RST7 JMP PINT ; JUMP TO INTERRUPT SERVICE ROUTINE ..... PROGRAM ORIGIN \*\*\*\*\* 3000 ..... INITIALIZATION ROUTINE A REGISTER MODIFIED INIT: A,ICW ; GET MODE CONTROL WORD
CMR ; OUTPUT TO CONTROL WORD REGISTER
; RETURN TO CALLER 3000 3ECB 3002 D3E7 3004 C9

2-431

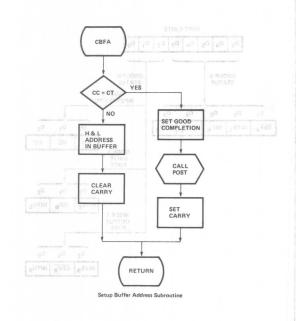


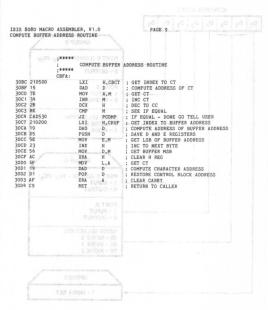
2-432





# APPLICATIONS XIGHTS APPLICATIONS



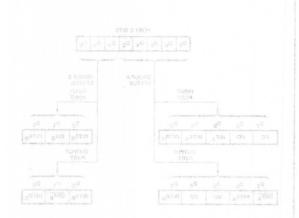


# MODE 1 STATUS WORD

MODE CONTROL WORD

PAGE 10

ISIS 8080 MACRO ASSEMBLER, V1.0 POST TO USER COMPLETION ROUTINE

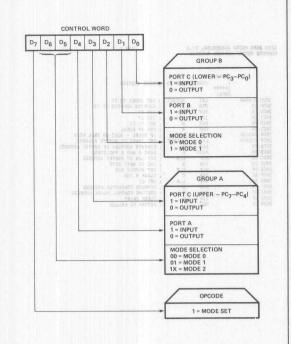


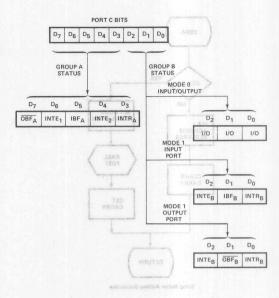
```
.....
   POST GOOD COMPLETION TO USER
                              ****
                             PCOMP:
   MVI
CALL
STC
RET
  A,STGD ; GET GOOD STATUS CODE
; CALL USER ROUTINE
; SET CARRY
; RETURN TO CALLER
30D5 3E00
30D7 CDDC30
30DA 37
30DB C9
   POST TO USER COMPLETION ROUTINE
   INPUTS: STATUS CODE IN A REG
CONTROL BLOCK ADDRESS IN D AND E REG
OUTPUTS: PASSES CONTROL TO USER COMPLETION ADDRESS
SPECIFIED IN CONTROL BLOCK
                            POST:
30DC EB
30DD 77
30DE EB
30DF 210600
30E2 19
30E3 4E
30E4 23
30E5 46
30E6 C5
30E7 C9
30E8 C9
   XCHG
MOV
XCHG
LXI
DAD
MOV
INX
MOV
PUSH
RET
RET
   M.A
  : UPDATE STATUS
  H, CBCMP ; GET INDEX TO COMPLETION ADDRESS
  GET INDEX TO COMPLETION ADDRESS
COMPUTE ADDRESS.
GET LSS OF COMPLETION ADDRESS
INC TO MEXT BYTE OF
GET MSB BYTE OF COMPLETION ADDRESS
PUSH ADDRESS INTO STACK
PASS COMPROL TO USER ROUTINE
RETURN TO CALLER
  D
C,M
H
B,M
B
                             .....
   DATA AND TABLES
   IF DATA NON ZERO CONTROL BLOCK IN PROGRESS
   ; IN PROGRESS READ CONTROL BLOCK
; IN PROGRESS WRITE CONTROL BLOCK
   END OF MASTER SOFTWARE DRIVER
                             .....
0000
   END
```

MODE 2 STATUS WORD

BIT SETABLESET CONTROL WORD

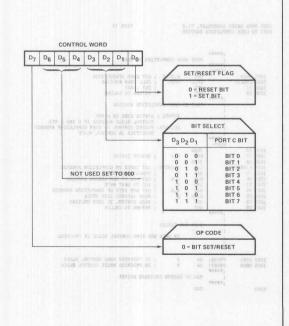
# APPENDIX A - 8255A QUICK REFERENCE

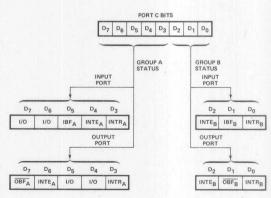




# MODE CONTROL WORD

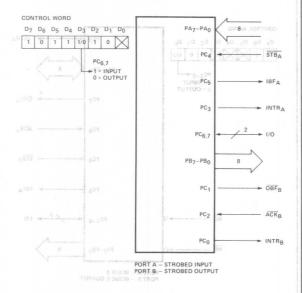
# **MODE 1 STATUS WORD**

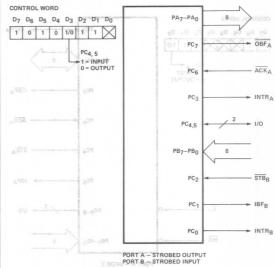


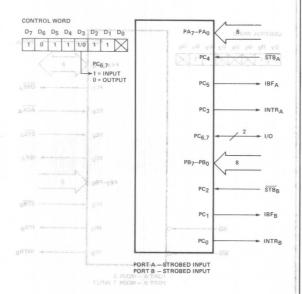


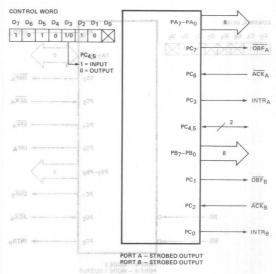
BIT SET/RESET CONTROL WORD

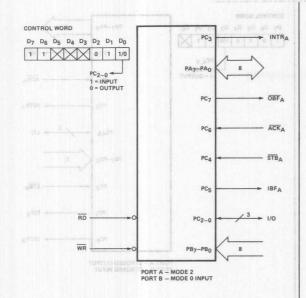
**MODE 2 STATUS WORD** 

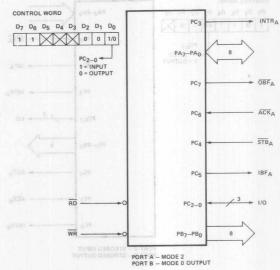


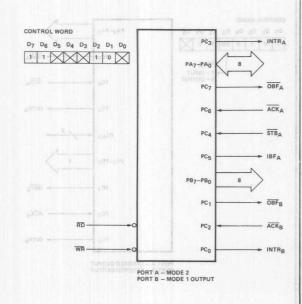


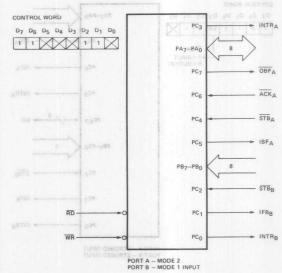












| A Low Cost CRT Terminal                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Contents                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | DEFENDANTING :                                                       |
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| Using the 8275                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 1. INTRODUCTION of a state of more state of the state of | 2-440 2-040                                                          |
| AND COMMENT AND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | design concepts and factual tools ato Intel peripherals and microSSICSB TRO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2-440                                                                |
| The second secon | 3. 8275 DESCRIPTION ston not bodge bedge 3.1 CRT Display Refreshing not tolog and a 3.2 CRT Timing about the ston not bodge 3.3 Special Functions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | reviously publication. This a                                        |
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| cously operating independent circuits control the tical and horizontal movement of the beam.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | CYCLEW COLLMAND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 2-454<br>Appendix                                                    |
| the electron beam meres across the face of the T, a third circuit controls the current flowing in beam. By varying the current in the electron in the image on the CRT can be made to be as                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 6.3 Memory Pointers and Scrolling 6.4 Software Timing                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | There is no que<br>peripherals have<br>tion of CRT<br>allowed design |
| ght or as dark as the user desires. This allows any sired pattern to be displayed.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | CRT Terminal Schematics                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | were previously                                                      |
| the beam reaches the end of a line, it is sught back to the beginning of the next line at a chart is much fester than was used to generate                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | APPENDIX 72                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | oqmoo 12-460                                                         |
| line This action is referred to as "retrace".                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | MSI packages, and of soatraful braodysM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | and 70 SSI and                                                       |
| iring the retrace period the electron beam is saffy shut off so that it doesn't appear on the                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | APPENDIX (13) a unionider of nothible of se                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2-40                                                                 |
| .пээ                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | and increase the reliability of design.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                      |
| the electron beam is moving across the screen                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | nects increases mechanical reliab.7 XIDNAPPA s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 2-462                                                                |
| rizontally, it is also moving downward. Because this, each successive line starts slightly below the                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | overall reliability of the design. The of                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | and beace the                                                        |
| evious line. When the beam finally reaches the ttom right hand corner of the screen, it retraces                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | mponents also yields a circuit 6.7 XIDNA99A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | oo to no 2-463                                                       |
| windly back to the total of hand comer. The time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Offaracter deficiator                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                      |
| takes for the beam to move from the top of the ren to the bottom and back again to the top is                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | APPENDIX 7.6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2-464                                                                |
| nally referred to as a "frame". In the United                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | HEX Dump of Character Generator                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | CRT terminal                                                         |
| ates, commercial television broadcast use 15,750 r. as the horizontal sweep frequency (63.5 microconds per horizontal line) and 60 Hz as the vertical sep frequency or "frame" (16.67 milliseconds per                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | opped this component count 7.7 XIQPAPAPAPAPAPAPAPAPAPAPAPAPAPAPAPAPAPAPA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | tween 30 and                                                         |
| rtical frame).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | APPENDIX 7.8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2-465                                                                |
| though, the 60 Hz vertical frame and the 15,750 Hz rizontal line are the standards used by commercial ondeasts, they are by no means the only requency which CRT's can operate, in act, many CRT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | a display gets its name from the race displayed on the CRT is built up by ho he case of ines (raster) across the face of br                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | The raster scar<br>that the image<br>generating a se                 |

2-439

moves left to right and top to bottom to put a series

# 1. INTRODUCTION

The purpose of this application note is to provide the reader with the design concepts and factual tools needed to integrate Intel peripherals and microprocessors into a low cost raster scan CRT terminal. A previously published application note, AP-32, presented one possible solution to the CRT design question. This application note expands upon the theme established in AP-32 and demonstrates how to design a functional CRT terminal while keeping the parts count to a minimum.

For convenience, this application note is divided into seven general sections:

- 1. Introduction
- 2. CRT Basics
- 3. 8275 Description
- 4. Design Background
- 5. Circuit Description
- 6. Software Description
- 7. Appendix

There is no question that microprocessors and LSI peripherals have had a significant role in the evolution of CRT terminals. Microprocessors have allowed design engineers to incorporate an abundance of sophisticated features into terminals that were previously mere slaves to a larger processor. To complement microprocessors, LSI peripherals have reduced component count in many support areas. A typical LSI peripheral easily replaces between 30 and 70 SSI and MSI packages, and offers features and flexibility that are usually not available in most hardware designs. In addition to replacing a whole circuit board of random logic, LSI circuits also reduce the cost and increase the reliability of design. Fewer interconnects increases mechanical reliability and fewer parts decreases the power consumption and hence, the overall reliability of the design. The reduction of components also yields a circuit that is easier to debug during the actual manufacturing phase of a product.

Until the era of advanced LSI circuitry, a typical CRT terminal consisted of 80 to 200 or more SSI and MSI packages. The first microprocessors and peripherals dropped this component count to between 30 and 50 packages. This application note describes a CRT terminal that uses 20 packages.

# 2. CRT BASICS

The raster scan display gets its name from the fact that the image displayed on the CRT is built up by generating a series of lines (raster) across the face of the CRT. Usually, the beam starts in the upper left hand corner of the display and simultaneously moves left to right and top to bottom to put a series

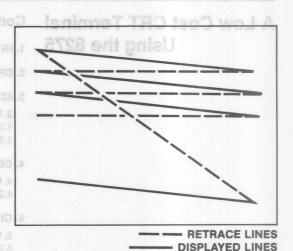


Figure 2-1. Raster Scan

of zig-zag lines on the screen (Fig. 2.1). Two simultaneously operating independent circuits control the vertical and horizontal movement of the beam.

As the electron beam moves across the face of the CRT, a third circuit controls the current flowing in the beam. By varying the current in the electron beam the image on the CRT can be made to be as bright or as dark as the user desires. This allows any desired pattern to be displayed.

When the beam reaches the end of a line, it is brought back to the beginning of the next line at a rate that is much faster than was used to generate the line. This action is referred to as "retrace". During the retrace period the electron beam is usually shut off so that it doesn't appear on the screen.

As the electron beam is moving across the screen horizontally, it is also moving downward. Because of this, each successive line starts slightly below the previous line. When the beam finally reaches the bottom right hand corner of the screen, it retraces vertically back to the top left hand corner. The time it takes for the beam to move from the top of the screen to the bottom and back again to the top is usually referred to as a "frame". In the United States, commercial television broadcast use 15,750 Hz as the horizontal sweep frequency (63.5 microseconds per horizontal line) and 60 Hz as the vertical sweep frequency or "frame" (16.67 milliseconds per vertical frame).

Although, the 60 Hz vertical frame and the 15,750 Hz horizontal line are the standards used by commercial broadcasts, they are by no means the only frequency at which CRT's can operate. In fact, many CRT displays use a horizontal scan that is around 18 KHz to 22 KHz and some even exceed 30 KHz. As the

horizontal frequency increases, the number of horizontal lines per frame increases. Hence, the resolution on the vertical axis increases. This increased resolution is needed on high density graphic displays and on special text editing terminals that display many lines of text on the CRT.

Although many CRT's operate at non-standard horizontal frequencies, very few operate at vertical frequencies other than 60 Hz. If a vertical frequency other than 60 Hz is chosen, any external or internal magnetic or electrical variations at 60 Hz will modulate the electron beam and the image on the screen will be unstable. Since, in the United States, the power line frequency happens to be 60 Hz, there is a good chance for 60 Hz interference to exist. Transformers can cause 60 Hz magnetic fields and power supply ripple can cause 60 Hz electrical variations. To overcome this, special shielding and power supply regulation must be employed. In this design, we will assume a standard frame rate of 60 Hz and a standard line rate of 15,750 Hz.

By dividing the 63.5 microsecond horizontal line rate into the 16.67 millisecond vertical rate, it is found that there are 262.5 horizontal lines per vertical frame. At first, the half line may seem a bit odd, but actually it allows the resolution on the CRT to be effectively doubled. This is done by inserting a second set of horizontal lines between the first set (interlacing). In an interlaced system the line sets are not generated simultaneously. In a 60 Hz system, first all of the even-numbered lines are scanned: 0, 2, 4,...524. Then all the odd-numbered lines: 1, 3, 5,... 525. Each set of lines usually contains different data (Fig. 2.2).

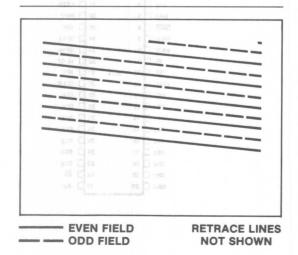


Figure 2-2. Interlaced Scan

Although interlacing provides greater resolution, it also has some distinct disadvantages. First of all, the circuitry needed to generate the extra half horizontal line per frame is quite complex when compared to a noninterlaced design, which requires an integer number of horizontal lines per frame. Next, the overall vertical refresh rate is half that of a noninterlaced display. As a result, flicker may result when the CRT uses high speed phosphors. To keep things as simple as possible, this design uses the noninterlaced approach.

The first thing any CRT controller must do is generate pulses that define the horizontal line timing and the vertical frame timing. This is usually done by dividing a crystal reference source by some appropriate numbers. On most raster scan CRT's the horizontal frequency is very forgiving and can vary by around 500 Hz or so and produce no ill effects. This means that the CRT itself can track a horizontal frequency between 15250 Hz and 16250 Hz, or in other words, there can be 256 to 270 horizontal lines per vertical frame. But, as mentioned earlier, the vertical frequency should be 60 Hz to insure stability.

The characters that are viewed on the screen are formed by a series of dots that are shifted out of the controller while the electron beam moves across the face of the CRT. The circuits that create this timing are referred to as the dot clock and character clock. The character clock is equal to the dot clock divided by the number of dots used to form a character along the horizontal axis and the dot clock is calculated by the following equation:

DOT CLOCK (Hz) = (N + R) \* D \* L \* Fwhere N is the number of displayed characters per row,

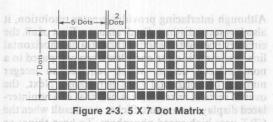
R is the number of retrace character time increments,

D is the number of dots per character,

L is the number of horizontal lines per frame and F is the frame rate in Hz.

In this design N = 80, R = 20, D = 7, L = 270, and F = 60 Hz. If the numbers are plugged in, the dot clock is found to be 11.34 MHz.

The retrace number, R, may vary from system to system because it is used to establish the margins on the left and right hand sides of the CRT. In this particular design R=20 was empirically found it be optimum. The number of dots per character may vary depending on the character generator used and the number of dot clocks the designer wants to place between characters. This design uses a 5 X 7 dot matrix and allows 2 dot clock periods between characters (see Fig. 2.3); since 5+2 equals 7, we find that D=7.



The number of lines per frame can be determined by The first thing any CRT:noitaups gniwollof add

where. H is the number of horizontal lines per character, of source source at the character, of source source or the character, of source source or the character, or source or the character or the characte

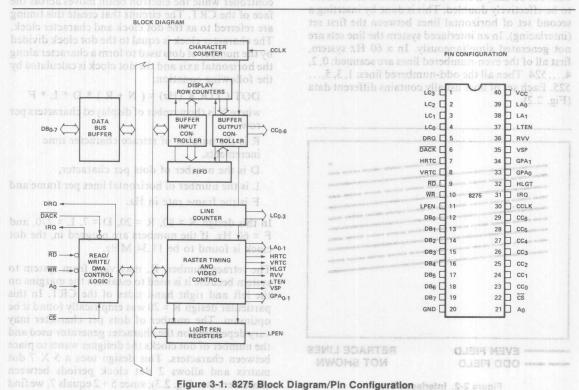
Z is the number of character lines per frame and V is the number of horizontal lines during vertical retrace. In this design, a 5 X 7 dot matrix is to be placed on a 7 X 10 field, so H = 10. Also, 25 lines are to be displayed, so Z = 25. As mentioned before, V = 20. When the numbers are plugged into the equation, L is found to be equal to 270 lines per frame.

The designer should be cautioned that these numbers

are interrelated and that to guarantee proper operation on a standard raster scan CRT, L should be between 256 and 270. If L does not lie within these bounds the horizontal circuits of the CRT may not be able to lock onto the driving signal and the image will roll horizontally. The chosen L of 270 yields a horizontal frequency of 16,200 KHz on a 60 Hz frame and this number is within the 500 Hz tolerance mentioned earlier.

The V number is chosen to match the CRT in much the same manner as the R number mentioned earlier. When the electron beam reaches the bottom right corner of the screen it must retrace vertically to the top left corner. This retrace action requires time, usually between 900-1200 microseconds. To allow for this, enough horizontal sync times must be inserted during vertical retrace. Twenty horizontal sync times at 61.5 microseconds yield a total of 1234.5 microseconds, which is enough time to allow the beam to return to the top of the screen.

The choices of H and Z largely relate to system design preference. As H increases, the character size along the vertical axis increases. Z is simply the number of lines of characters that are displayed and this, of course, is entirely a system design option.



# 3. 8275 DESCRIPTION

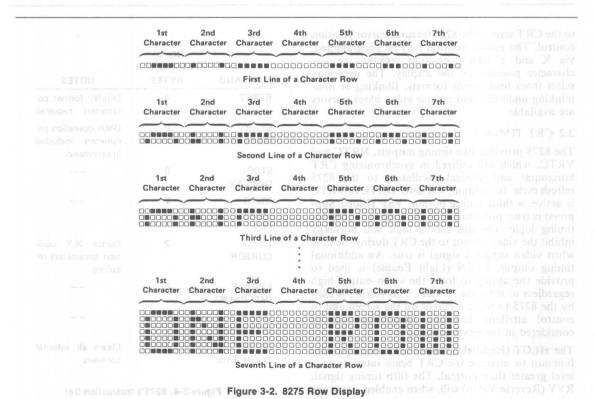
A block diagram and pin configuration of the 8275 are shown in Fig. 3.1. The following is a description of the general capabilities of the 8275.

# 3.1 CRT DISPLAY REFRESHING

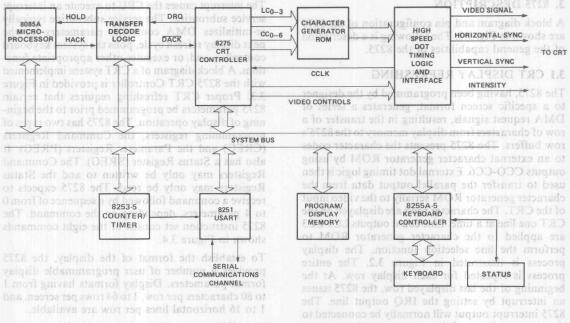
The 8275, having been programmed by the designer to a specific screen format, generates a series of DMA request signals, resulting in the transfer of a row of characters from display memory to the 8275's row buffers. The 8275 presents the character codes to an external character generator ROM by using outputs CCO-CC6. External dot timing logic is then used to transfer the parallel output data from the character generator ROM serially to the video input of the CRT. The character rows are displayed on the CRT one line at a time. Line count outputs LC0-LC3 are applied to the character generator ROM to perform the line selection function. The display process is illustrated in Figure 3.2. The entire process is repeated for each display row. At the beginning of the last displayed row, the 8275 issues an interrupt by setting the IRQ output line. The 8275 interrupt output will normally be connected to the interrupt input of the system central processor. The interrupt causes the CPU to execute an interrupt service subroutine. The service subroutine typically re-initializes DMA controller parameters for the next display refresh cycle, polls the system keyboard controller, and/or executes other appropriate functions. A block diagram of a CRT system implemented with the 8275 CRT Controller is provided in Figure 3.3. Proper CRT refreshing requires that certain 8275 parameters be programmed prior to the beginning of display operation. The 8275 has two types of programming registers, the Command Registers (CREG) and the Parameter Registers (PREG). It also has a Status Register (SREG). The Command Registers may only be written to and the Status Registers may only be read. The 8275 expects to receive a command followed by a sequence of from 0 to 4 parameters, depending on the command. The 8275 instruction set consist of the eight commands shown in Figure 3.4.

To establish the format of the display, the 8275 provides a number of user programmable display format parameters. Display formats having from 1 to 80 characters per row, 1 to 64 rows per screen, and 1 to 16 horizontal lines per row are available.

In addition to transferring characters from memory



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to the CRT screen, the 8275 features cursor position control. The cursor position may be programmed, via X and Y cursor position registers, to any character position on the display. The user may select from four cursor formats. Blinking or nonblinking underline and reverse video block cursors are available.

#### 3.2 CRT TIMING

The 8275 provides two timing outputs, HRTC and VRTC, which are utilized in synchronizing CRT horizontal and vertical oscillators to the 8275 refresh cycle. In addition, whenever HRTC or VRTC is active, a third timing output, VSP (Video Suppress) is true, providing a blinking signal to the dot timing logic. The dot timing logic will normally inhibit the video output to the CRT during the time when video suppress signal is true. An additional timing output, LTEN (Light Enable) is used to provide the ability to force the video output high regardless of the state of VSP. This feature is used by the 8275 to place a cursor on the screen and to control attribute functions. Attributes will be considered in the next section.

The HLGT (Highlight) output allows an attribute function to increase the CRT beam intensity to a level greater than normal. The fifth timing signal. RVV (Reverse Video) will, when enabled, cause the avea see stuping Figure 3-4. 8275's Instruction Set system video output to be inverted.

| COMMAND              | NO. OF<br>PARAMETER<br>BYTES              | NOTES                                                |
|----------------------|-------------------------------------------|------------------------------------------------------|
| RESET Character      | teP<br>Character Ci                       | Display format pa-<br>rameters required              |
| START                |                                           | DMA operation pa-<br>rameters included<br>in command |
| STOP<br>DISPLAY      | O Tist Character Ch                       |                                                      |
| READ<br>LIGHT<br>PEN | 2<br>200000000000000000000000000000000000 |                                                      |
| LOAD                 | 2                                         | Cursor X,Y posi-<br>tion parameters re-<br>quired    |
| ENABLE<br>INTERRUPT  | Character Ch                              |                                                      |
| DISABLE INTERRUPT    | 0                                         |                                                      |
| PRESET COUNTERS      | 0.55                                      | Clears all internal counters                         |

Character attributes were designed to produce the following graphics:

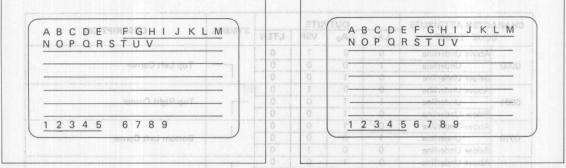
| 101       | ACTER ATTRIBUTE   | 000             | OUT             |                                           | T       | SYMBOL                    | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  |
|-----------|-------------------|-----------------|-----------------|-------------------------------------------|---------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| (         | CODE "CCCC"       | LA <sub>1</sub> | LA <sub>0</sub> | VSP                                       | LTEN    |                           | VUTREOGOM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |  |
|           | Above Underline   | 0               | 0               | 1                                         | 0       |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 0000      | Underline         | 1               | 0               | 0                                         | 0       |                           | Top Left Corner                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
|           | Below Underline   | 0               | -1              | 0                                         | 0       |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
|           | Above Underline   | 0               | 0               | 1                                         | 0       |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 0001      | Underline         | 1               | 1               | 0                                         | 0       |                           | Top Right Corner                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |  |
|           | Below Underline   | 0               | 1               | 0                                         | 0       |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
|           | Above Underline   | 00              | 1               | 0                                         | 0       | 1                         | 12345 6789                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |  |
| 0010      | Underline         | 1               | 0               | 0                                         | 0       |                           | Bottom Left Corner                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |  |
|           | Below Underline   | 0               | 0               | . 1                                       | 0       |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
|           | Above Underline   | 0               | 1               | 0                                         | 0       |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 0011      | TA G Underline 21 | MI THT          | 3013.45         | 0.0                                       | 0       | 3000 3710                 | Bottom Right Corner W 347 30 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |  |
| -         | Below Underline   | 0               | 0               | 1                                         | 0       |                           | (UNDERLINE ATTRIBUTE)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |  |
|           | Above Underline   | 0               | 0               | 1                                         | 0       |                           | 121 Sattly 175 William Nation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  |
| 0100      | Underline         | 0               | 0.0             | 0                                         | DA BISI | S.E. ettip                | Top Intersect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  |
|           | Below Underline   | 0               | 1               | 0                                         | 0       |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
|           | Above Underline   | 0               | 1               | 0                                         | 0       | 1                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 0101      | Underline         | 0 1 14          | 14.41.214       | 0                                         | 0       |                           | Right Intersect TOWNE JAIDS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  |
| the state | Below Underline   | 0               | 11              | 0                                         | 0       |                           | TAIDI TAIDI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  |
|           | Above Underline   | 0               | 1 1             | 0                                         | 0 57    | и быцев в                 | AL ATTRIBUTES-Visual and                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |  |
| 0110      | Underline         | 1               | 0               | 0                                         | 0 /     | lgsil-mo                  | Left Intersect odw .dord // 20000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |  |
| vollo     |                   | 0               | Reters          | 0                                         | 0 80    | iracteristi               | ry by the 32.5, affect the visual ch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |  |
| RTOVOT    | Above Underline   | 11 RO 55        | s shoo          | 0                                         | 0 0     | acters. Ty                | naracter nostaon or field of char                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |  |
| 0111/     | Underline         | 0               | 0               | 0                                         | 1 25    |                           | Bottom Intersect and the levely lo                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |  |
| 7 2 2 3 7 | Below Underline   | 0               | 0               | 1                                         | 0       | \$10 (31 (31)33 A         | of visital attributes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |  |
|           | Above Underline   | 0               | 0               | 1                                         | 0       |                           | ZUBILLIE OG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  |
| 1000      | Underline         | 0               | 0               | 0                                         | 1 91    | reliebba -                | Horizontal Line                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| tingti    |                   | 0 90 01         | 0.00            | 1                                         | 0       | admyz za                  | can be used to generate graph                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  |
| 1015      | Above Underline   | 110010          | Entbid          | 0                                         | 0       | tor, This                 | if the use of a character genera                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |  |
| 1001      | Underline         | 0.              | 1 .             | . 0                                       | 0       | i I della co              | Vertical Line selection badalla                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| DIS TOW   | Below Underline   | 0               | 130             | 0                                         | 0       | 27 401 8                  | phished 0, selectively—and who vide                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |  |
| 1 1370    | Above Underline   | 0               | 9128            | 0                                         | 0       | addns o                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 1010      | Underline         | 0               | 0               | 0                                         | 1       | dino alqr                 | Crossed Lines (VSP), and the Crossed Lines                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |  |
| o tople   | Below Underline   | 0               | DEPUT           | 0                                         | 0       | ic signals                | Crossed Lines                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  |
| merio     | Above Underline   | 0               | 0               | 0                                         | 0       | mdiana a                  | te the proper symbols. Characte                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 1011      | Underline         | 0               | 0               | 0                                         | 0       | highlight                 | Not Recommended *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |  |
| Y-01311   | Below Underline   | 0               | 0               | 0                                         | 0       | diwith t                  | lually. Blinking is accomplished                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |  |
| 11307.51  | Above Underline   | 0               | 0               | 1                                         | 0 21    | (эпецрат                  | Suppression output (VSP). Black                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 1100      | Underline         | 0               | 0               | 1                                         | 0 -     | yd babiy                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| G IIIv    | Below Underline   | 0               | 0               | firths .                                  | 0 0     | i saiiavi                 | ghting is accomplished by act                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  |
| D 1501    | Above Underline   | राहर असी        | no no           | positi                                    | 29      | attribut                  | ght output (HGLT). Characte                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  |
| 1101      | Underline         | REVIEWS         | Unde            | fined                                     | of      |                           | designed to produce thelapallo                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |  |
| drute     | Below Underline   | 17 .(9          |                 | Idino_                                    | 6.13    | maritée én                | in Figure A is                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |  |
| III tin   | Above Underline   | sidi do         | is bels         |                                           |         |                           | 3109PLAL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |  |
| 1110      | B Underline       | di ni i         | _               | fined                                     | 97      | s entredis                | Attribute Codes: The filipelling                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |  |
| dT b      | Below Underline   | buffer          | 275 703         | 46 19 19 19 19 19 19 19 19 19 19 19 19 19 | 69      |                           | d codes which affect the visual ch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |  |
| lé chi    | Above Underline   | read to re      | el vievi        |                                           | +       |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
| 1111      | Underline         | Hguron<br>For n | -               | fined                                     | 13      | elon ba                   | field of characters, starting at the field attribute code [spell] o.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |  |
|           |                   |                 | - Olluc         | - HILL                                    | -13     | DESCRIPTION OF THE PERSON | LINE TO SELECT OF THE PART OF |  |

in size. When a field attribute is placed in the \*Character Attribute Code 1011 is not recommended for normal operation. Since none of the attribute outputs are active, the character Generator will not be disabled, and an indeterminate character will be generated.

Character Attribute Codes 1101, 1110, and 1111 are illegal. Blinking is active when B=1. Highlight is active when H = 1.

caused to blink by activating the

equal to the screen refresh frequestudirth retracter Attributes (CCO-6). The



EXAMPLE OF THE VISIBLE FIELD ATTRIBUTE MODE (UNDERLINE ATTRIBUTE)

EXAMPLE OF THE INVISIBLE FIELD ATTRIBUTE MODE
(UNDERLINE ATTRIBUTE)

Figure 3-6. Field Attribute Examples

#### 3.3 SPECIAL FUNCTIONS

VISUAL ATTRIBUTES—Visual attributes are special codes which, when retrieved from display memory by the 8275, affect the visual characteristics of a character position or field of characters. Two types of visual attributes exist, character attributes and field attributes.

Character Attribute Codes: Character attribute codes can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the Line Attribute outputs (LAO-LA1), the Video Suppression output (VSP), and the Light Enable output (LTEN). The dot timing logic uses these signals to generate the proper symbols. Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the Video Suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the Highlight output (HGLT). Character attributes were designed to produce the graphic symbols shown in Figure 3.5.

Field Attribute Codes: The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the field attribute code up to, and including, the character which precedes the next field attribute code, or up to the end of the frame.

There are six field attributes:

 Blink — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.

- 2. Highlight Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
- 3. Reverse Video Characters following the code are caused to appear in reverse video format by activating the Reverse Video output (RVV).
- 4. Underline Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).
- General Purpose There are two additional 8275 outputs which act as general purpose, independently programmable field attributes. These attributes may be used to select colors or perform other desired control functions.

The 8275 can be programmed to provide visible or invisible field attribute characters as shown in Figure 3.6. If the 8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character. If the 8275 is programmed in the invisible field attribute mode. the 8275 row buffer FIFOs are activated. The FIFOs effectively lengthen the row buffers by 16 characters. making room for up to 16 field attribute characters per display row. The FIFOs are 126 characters by 7 bits in size. When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the next character in the proper FIFO. When a field attribute is placed in the buffer output controller during display, it causes the controller to immediately put a character from the FIFO on the Character Code outputs (CCO-6). The chosen attributes are also activated.

switch enables the light sensor. When the raster sweep coincides with the light sensor position on the display, the light pen output is input and the row and character position coordinates are stored in two 8275 internal registers. These registers can be read by the microprocessor. The state of seasons of the of the seasons 
SPECIAL CODES — Four special codes may be used to help reduce memory, software, or DMA overhead. These codes are placed in character positions in display memory, a starting wor on H

- 1. End Of Row Code Activates VSP. VSP remains active until the end of the line is reached. While VSP is active, the screen is blanked.
- 2. End Of Row-Stop DMA Code Causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the row buffer. It affects the display in the same way as the End of Row Code.
- 3. End Of Screen Code Activates VSP. VSP remains active until the end of the frame is reached.
- 4. End Of Screen-Stop DMA Code Causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the row buffer. It affects the display in the same way as the End of Screen Code. THO THE STATE OF THE

PROGRAMMABLE DMA BURST CONTROL — The 8275 can be programmed to request single-byte DMA transfers of DMA burst transfers of 2, 4, or 8 characters per burst. The interval between bursts is also programmable. This allows the user to tailor the DMA overhead to fit the system needs.

#### 4. DESIGN BACKGROUND

#### 4.1 DESIGN PHILOSOPHY

Since the cost of any CRT system is somewhat proportional to parts count, arriving at a minimum part count solution without sacrificing performance has been the motivating force throughout this design effort. To successfully design a CRT terminal and keep the parts count to a minimum, a few things became immediately apparent.

- 1. An 8085 should be used.
- 2. Address and data buffering should be eliminated.
- 3. Multi-port memory should be eliminated.
- 4. DMA should be eliminated.

Decision 1 is obvious, the 8085's on-board clock generator, bus controller and vectored interrupts greatly reduce the overall part count considerably.

APPLICATIONS lines is kept to a minimum, both the data and address buffers can be eliminated. This easily saves three to eight packages and reduces the power consumption of the design. Both decisions 3 and 4 require a basic understanding of current CRT design concepts.

> In any CRT design, extreme time conflicts are created because all essential elements require access to the bus. The CPU needs to access the memory to control the system and to handle the incoming characters, but, at the same time, the CRT controller needs to access the memory to keep the raster scan display refreshed. To resolve this conflict two common techniques are employed, page buffering and line buffering.

> In the page buffering approach the entire screen memory is isolated from the rest of the system. This isolation is usually accomplished with three-state buffers or two line to one line multiplexers. Of course, whenever a character needs to be manipulated the CPU must gain access to the buffered memory and, again, possible contention between the CPU and the CRT controller results. This contention is usually resolved in one of two ways, (1) the CPU is always given priority, or; (2) the CPU is allowed to access the buffered memory only during horizontal and vertical retrace times.

> Approach 1 is the easiest to implement from a hardware point of view, but if the CPU always has priority the display may temporarily blink or "flicker" while the CPU accesses the display memory. This, of course, occurs because when the CPU accesses the display memory the CRT controller is not able to retrieve a character, so the display must be blanked during this time. Aesethically, this "flickering" is not desirable, so approach 2 is often used.

> The second approach eliminates the display flickering encountered in the previously mentioned technique, but additional hardware is required. Usually the vertical and horizontal blank signals are gated with the buffered memory select lines and this line is used to control the CPU's ready line. So, if the CPU wants to use the buffered memory, its ready line is asserted until horizontal or vertical retrace times. This, of course, will impact the CPU's overall through put.

> Both page buffered approaches require a significant amount of additional hardware and for the most part are not well suited for a minimum parts count type of terminal. This guides us to the line buffered approach. This approach eliminates the separate buffered memory for the display, but, at the same time, introduces a few new problems that must be solved.

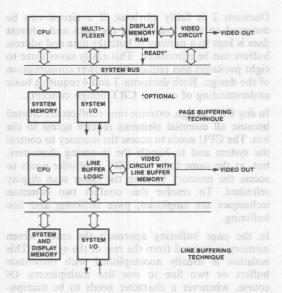


Figure 4-1. Line Buffering Technique

| horizontal     |           |              | memory          |                                         |
|----------------|-----------|--------------|-----------------|-----------------------------------------|
| CLOCK CYCLES   | SEO       | SOUR         | CE STATEMENT !! | and vertical retrace                    |
| -b 10 10 mm    | ment from | PUSH<br>PUSH | PSII 12012      | SAVE H AND FLAGS                        |
| PRO 10 VEW     |           | PUSH         | D tod           | SRYE D RND E TO COM STREET              |
| 10             | - 4       | 1.41         | H, 6000H        | ZERO H AND L                            |
| 10 10 IIId     | VIISCIO   | DAD          | SP              | PUT STOCK POINTER IN H HND L            |
| v merhony.     |           |              | access          | FUT STACK IN D AND E                    |
| -16            | 7         | LHLD         | CURRO           | GET POINTER                             |
| Unc all        | 1198 W 5  | SPHL         | seurs bes       | PUT CURRENT LINE INTO SP                |
| 7              |           | MVI          | AL OCEH         | SET MASK FOR SIM                        |
| entropier is   | 18        | SIH          | THE HALL        | SET SHECIAL TRANSFER BIT                |
| 1211 400 V nio | bit of    | POP          | Here is a       | GDO 40 POPS OF SIGE TOP                 |
|                | 42        | RRC          |                 | SET UP A                                |
| cally, this    | 13 89 A   | SIM          |                 | GO BOOK TO MOSHAL MODE                  |
| 10 0           | 19 14 700 | LXI          | H. 8088H        | 2ERO HLD COMPANION IN THE               |
| 18             | 15        | DAD          | 92              | FROD STACK                              |
| 4              | 16        | XCHG         |                 | PUT STRCK IN H AND L DOZELL             |
| 6              | 17        | SPHL         |                 | FESTORE STACK                           |
| 18             | 18        | LXI          | TH, LAST        | PUT BOTTON DISPLAY IN H AND L           |
| 4 .            | 10        | XCHG         |                 | SWAP REGISTERS                          |
| oned tech-     | 20        | MOA          | A.D             | FUT HIGH OFDER IN A                     |
| villant U.b.   | 21        | CHP          | Whited Is       | SEE IF SHIE AS II                       |
| 7/18           | - 22      | JNZ          | KPTK            | : IF NOT I FRUE                         |
| are pated      | 23        | VCM          | R.E. MONT       | PUT LOW ORDER IN A OV ONLY              |
| this Ane is    | 24        | CMP          | leb unners      | SEE IF SAKE AS L                        |
| 7/18           | 25        | JNZ          | KPTK            | ; IF NOT LERVE                          |
| 10             | . 26 . 31 | LXI          | H. TPDIS        | LIGHT H AND L WITH TOP OF SCREEN HEHORY |
| zi o 16 vbs    | 27 KPTK:  | SHLD         | CURAD           | PUT BACK CURRENT ADDRESS                |
| 7              | 28        | IVN          | R, 18H          | GET MASK BYTE                           |
| race tames.    | 1929 601  | SIM          |                 | SET INTERRUPT MRSK                      |
| 10             | 30        | POP.         | 0               | GED D AND E                             |
| I's ograll     | 31        | POP          | same Ha         | GET H PRID LO SOUR H TED;               |
| 10             | 32        | POP          | PSN             | GET A AND FLAGS                         |
| 4              | 33        | EI           |                 | ; ENABLE INTERRUPTS                     |
| significant    | 34        | RET          |                 | GO BACK                                 |

TOTAL CLOCK CYCLES = 650 (KORST CRSE)

MITH A 6 144 MHZ CRYSTAL TOTAL TIME TO FILL HOW JOH STE JIEG

Description ROW BUFFER ON 8275 = 650 • .325 = 211.25 MICROSECONDS MITES 100 and 3

Figure 4-2. Routine To Load 8275's Row Buffers

In the line buffered approach both the CPU and the CRT controller share the same memory. Every time the CRT controller needs a new character or line of data, normal processing activity is halted and the CRT controller accesses memory and displays the data. Just how the CRT controller needs to acquire the display data greatly affects the performance of the overall system. Whether the CRT controller needs to gain access to the main memory to acquire a single character or a complete line of data depends on the presence or absence of a separate line or row buffer.

If no row buffer is present the CRT controller must go to the main memory to fetch every character. This of course, is not a very efficient approach because the processor will be forced to relinquish the bus 70% to 80% of the time. So much processor inactivity greatly affects the overall system performance. In fact terminals that use this approach are typically limited to around 1200 to 2400 baud on their serial communication channels. This low baud rate is in general not acceptable, hence this approach was not chosen.

If a separate row buffer is employed the CRT controller only has to access the memory once for each displayed character per line. This forces the processor to relinquish the bus only about 20% to 35% of the time and a full 4800 to 9600 baud can be achieved. Figure 4.1 illustrates these different techniques.

The 8275 CRT controller is ideal for implementing the row buffer approach because the row buffer is contained on the device itself. In fact, the 8275 contains two 80-byte row buffers. The presence of two row buffers allow one buffer to be filled while the other buffer is displaying the data. This dual row buffer approach enhances CPU performance even further.

## 4.2 USING THE 8275 WITHOUT DMA

Until now the process of filling the row buffer has only been alluded to. In reality, a DMA technique is usually used. This approach was demonstrated in AP-32 where an 8257 DMA controller was mated to an 8275 CRT controller. In order to minimize component count, this design eliminates the DMA controller and its associated circuitry while replacing them with a special interrupt-driven transfer.

The only real concern with using the 8275 in an interrupt-driven transfer mode is speed. Eighty characters must be loaded into the 8275 every 617 microseconds and the processor must also have time to perform all the other tasks that are required. To minimize the overhead associated with loading the characters into the 8275 a special technique was employed. This technique involves setting a special

transfer bit and executing a string of POP instructions. The string of POP instructions is used to rapidly move the data from the memory into the 8275. Figure 4.2 shows the basic software structure.

In this design the 8085's SOD line was used as the special transfer bit. In order to perform the transfer properly this special bit must do two things: (1) turn processor reads into DACK plus WR for the 8275 and (2) mask processor fetch cycles from the 8275, so that a fetch cycle does not write into the 8275. Conventional logic could have been used to implement this special function, but in this design a small bipolar programmable read only memory was used. Figure 4.3 shows a basic version of the hardware.

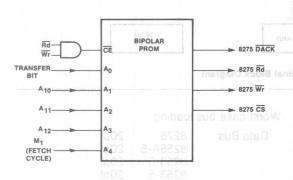


Figure 4-3. Simplified Version of Hardware Decoder

At first, it may seem strange that we are supplying a DACK when no DMA controller exist in the system. But the reader should be aware that all Intel peripheral devices that have DMA lines actually use DACK as a chip select for the data. So, when you want to write a command or read status you assert CS and WR or RD, but when you want to read or write data you assert DACK and RD or WR. The peripheral device doesn't "know" if a DMA controller is in the circuit or not. In passing, it should be mentioned that DACK and CS should not be asserted on the same device at the same time, since this combination yields an undefined result.

This POP technique actually compares quite favorably in terms of time to the DMA technique. One POP instruction transfers two bytes of data to the 8275 and takes 10 CPU clock cycles to execute, for a net transfer rate of one byte every five clock cycles. The DMA controller takes four clock cycles to transfer one byte but, some time is lost in synchronization. So the difference between the two techniques is one clock cycle per byte maximum. If we compare the overall speed of the 8085 to the

speed of the 8080 used in AP-32, we find that at 3 MHz we can transfer one byte every 1.67 microseconds using the 8085 and POP technique vs. 2 microseconds per byte for the 2 MHz 8080 using DMA.

#### 5. CIRCUIT DESCRIPTION

#### 5.1 SCOPE OF THE PROJECT

A fully functional, microprocessor-based CRT terminal was designed and constructed using the 8275 CRT controller and the 8085 as the controlling element. The terminal had many of the functions found in existing commercial low-cost terminals and more sophisticated features could easily be added with a modest amount of additional software. In order to minimize component count LSI devices were used whenever possible and software was used to replace hardware.

#### 5.2 SYSTEM TARGET SPECIFICATIONS

The design specifications for the CRT terminal were as follows:

#### Display Format

- 80 characters per display row
- 25 display rows a mammand a HOZA 30 .

# \* ASCH control characters

- 5 X 7 dot matrix character contained within a 7 X 10 matrix MOSSE NOTE TO THE PROPERTY OF T
- First and seventh columns blanked \uniquid
- Blinking underline cursor

#### Special Characters Recognized All All 0000

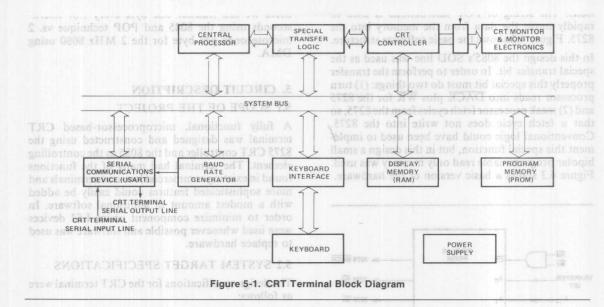
- Control characters
- Line feed
- Carriage Return
- Backspace NA beboone and bushnats vnA
- · Form feed

#### Escape Sequences Recognized

- ESC, A, Cursor up
- ESC, B, Cursor down
- ESC, C, Cursor right
- ESC, D, Cursor left
- ESC, E, Clear screen and A and mi banisinoo
- ESC, H, Home cursor significand batomismoo
- ESC, J, Erase to the end of the screen
- ESC, K, Erase the current line

# Characters Displayed

- 96 ASCII alphanumeric characters



Characters Transmitted 11, 190 21919818119 08 .

- 96 ASCII alphanumeric characters
- ASCII control characters | ASCII control characters |

Program Memory 1010 STREET TO TEXT TO

• 2K bytes of 2716 EPROM xirilem 01 X 7

Display | Buffer | Stack Memory von bank 1811 | 0

• 2K bytes 2114 static memory (4 packages) • Data Rate

· Control characters

· Carriage Return

• 9600 BAUD using 3MHz 8085

CRT Monitor

• Ball Bros TV-12, 12MHz B.W. beel onid •

Keyboard

- Any standard un-encoded ASCII keyboard Screen Refresh Rate
- 60 Hz

#### **5.3 HARDWARE DISCRIPTION**

A block diagram of the CRT terminal is shown in Figure 5.1. The diagram shows only the essential system features. A detailed schematic of the CRT is contained in the Appendix. The terminal was constructed on a simple 6" by 6" wire wrap board. Because of the minimum bus loading no buffering of any kind was needed (see Figure 5.2).

The "heart" of the CRT terminal is the 8085 microprocessor. The 8085 initializes all devices in the system, loads the CRT controller, scans the keyboard, assembles the characters to be trans-

| Worst case bus   | loading:                  |                      |                                   |
|------------------|---------------------------|----------------------|-----------------------------------|
| Data Bus:        | 8275<br>8255A-5<br>8253-5 | 20pf<br>20pf<br>20pf | My MA<br>ME YOU HOY ZEG<br>CYCLE) |
| rebood of second | 8253-5<br>8251A<br>x 2114 | 20pf                 |                                   |
|                  | 2716<br>8212              | 12pf<br>12pf         |                                   |
| are supplying a  |                           | 114pf max            |                                   |

Only As - A<sub>15</sub> are important since A<sub>0</sub> - A<sub>7</sub> are latched by the 8212

Address Bus: 4x 2114 20pf 2716 6pf 26pf max

This loading assures that all components will be compatible with a 3MHz 8085 and that no wait states will be required

Figure 5-2. Bus Loading

mitted, decodes the incoming characters and determines where the character is to be placed on the screen. Clearly, the processor is quite busy.

A standard list of LSI peripheral devices surround the 8085. The 8251A is used as the serial communication link, the 8255A-5 is used to scan the keyboard and read the system variables through a set of

switches, and the 8253 is used as a baud rate generator and as a "horizontal pulse extender" for the 8275

The 8275 is used as the CRT controller in the system, and a 2716 is used as the character generator. To handle the high speed portion of the terminal the 8275 is surrounded by a small handful of TTL. The program memory is contained in one 2716 EPROM and the data and screen memory use four 2114-type RAMs.

All devices in this system are memory mapped. A bipolar PROM is used to decode all of the addresses for the RAM, ROM, 8275, and 8253. As mentioned earlier, the bipolar prom also turns READs into DACK's and WR's for the 8275. The 8255 and 8253 are decoded by a simple address line chip select method. The total package count for the system is 20, not including the serial line drivers. If this same terminal were designed using the MCS-85 family of integrated circuits, additional part savings could have been realized. The four 2114's could have been replaced by two 8185's and the 8255 and the 2716 program PROM could have been replaced by one 8755. Additionally, since both the 8185 and the 2716 have address latches no 8212 would be needed so the total parts count could be reduced by three or four packages.

#### 5.4 SYSTEM OPERATION

The 8085 CPU initializes each peripheral to the appropiate mode of operation following system reset. After initialization, the 8085 continually polls the 8251A to see if a character has been sent to the terminal. When a character has been received, the 8085 decodes the character and takes appropriate action. While the 8085 is executing the above "foreground" programs, it is being interrupted once every 617 microseconds by the 8275. This "background" program is used to load the row buffers on the 8275. The 8085 is also interrupted once every frame time, or 16.67 ms, to read the keyboard and the status of the 8275.

As discussed earlier, a special POP technique was used to rapidly move the contents of the display RAM into the 8275's row buffers. The characters are then synchronously transferred to the character code outputs CC0-CC6, connected to the character generator address lines A3-A9 (Figure 5.3). Line count outputs LC0-LC2 from the 8275 are applied to the character generator address lines, A0-A2. The 8275 displays character rows one line at a time. The line count outputs are used to determine which line of the character selected by A3-A8 will be displayed. Following the transfer of the first line to the dot timing logic, the line count is incremented and the second line of the character row is selected. This

process continues until the last line of the row is transferred to the dot timing logic.

The dot timing logic latches the output of the character generator ROM into a parallel in, serial out synchronous shift register. This shift register is clocked at the dot clock rate (11.34 MHz) and its output constitutes the video input to the CRT.

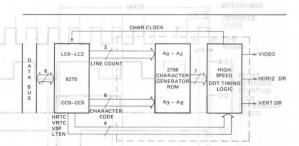


Figure 5-3 Character Generator/Dot Timing Logic Block Diagram

Table 5-1

| PARAMETER                          | RANGE                  |
|------------------------------------|------------------------|
| Vertical Blanking Time<br>(VRTC)   | 900 μsec nominal       |
| Vertical Drive Pulsewidth          | 300 μsec ≤ PW ≤ 1.4 ms |
| Horizontal Blanking Time<br>(HRTC) | 11 μsec nominal        |
| Horizontal Drive Pulsewidth        | 25 μsec ≤ PW ≤ 30 μsec |
| Horizontal Repetition Rate         | 15,750 ±500 pps        |

#### 5.5 SYSTEM TIMING

Before any specific timing can be calculated it is necessary to determine what constraints the chosen CRT places on the overall timing. The requirements for the Ball Bros. TV-12 monitor are shown in Table 5.1. The data from Table 5.1, the 8275 specifications, and the system target specifications are all that is needed to calculate the system's timing.

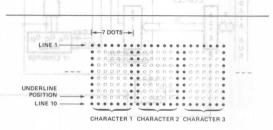


Figure 5-4. Row Format

First, let's select and "match" a few numbers. From our target specifications, we see that each character is displayed on a 7 X 10 field, and is formed by a 5 X 7 dot matrix (Figure 5.4). The 8275 allows the vertical retrace time to be only an integer multiple of

the horizontal character line. This means that the total number of horizontal lines in a frame equals 10 times the number of character lines plus the vertical retrace time, which is programmed to be either 1, 2, 3, or 4 character lines. Twenty-five display lines

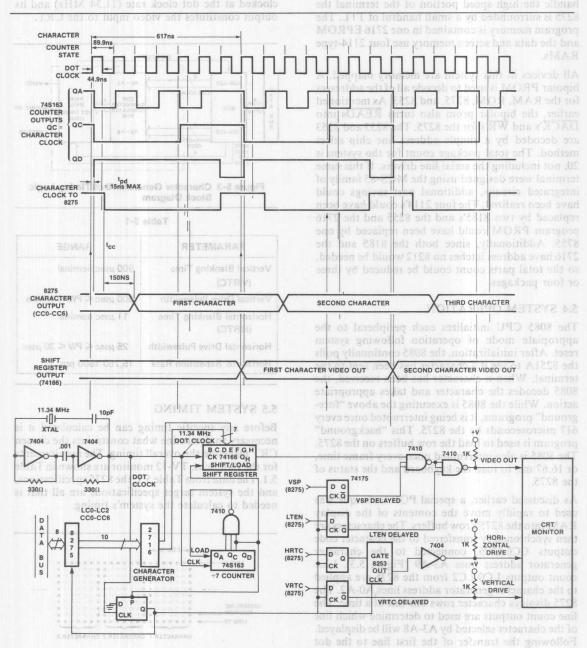


figure 5-5. Dot Timing Logic streaments is incremente signal gnimit

require 250 horizontal lines. So, if we wish to have a horizontal frequency in the neighborhood of 15,750 Hz we must choose either one or two character lines for vertical retrace. To allow for a little more margin at the top and bottom of the screen, two character lines were chosen for vertical retrace. This choice yields a net 250 + 20 = 270 horizontal lines per frame. So, assuming a 60 Hz frame:

60 Hz \* 270 = 16,200 Hz (horizontal frequency)

This value falls within our target specification of 15,750 Hz with a 500 Hz variation and also assures timing compatibility with the Ball monitor since, 20 horizontal sync times yield a vertical retract time of:

61.7 microseconds X 20 horizontal sync times = 1.2345 milliseconds

This number meets the nominal VRTC and vertical drive pulse width time for the Ball monitor. A horizontal frequency of 16,200 Hz implies a 1/16,200 = 61.73 microsecond period.

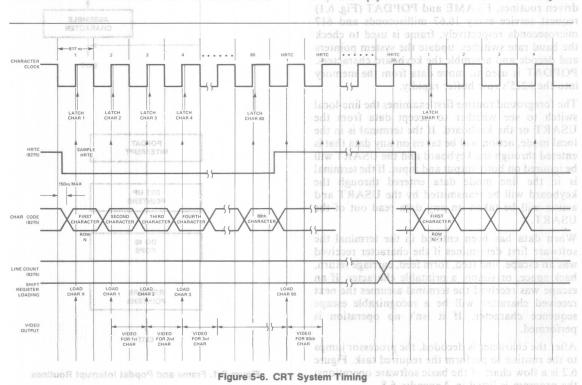
It is now known that the terminal is using 250 horizontal lines to display data and 20 horizontal lines to allow for vertical retrace and that the horizontal frequency is 16,200 Hz. The next thing that needs to be determined is how much time must

be allowed for horizontal retrace. Unfortunately, this number depends almost entirely on the monitor used. Usually, this number lies somewhere between 15 and 30 percent of the total horizontal line time, which in this case is 1/16,200 Hz or 61.73 microseconds. Since in most designs a fixed number of characters can be displayed on a horizontal line, it is often useful to express retrace as a given number of character times. In this design, 80 characters can be displayed on a horizontal line and it was empirically found that allowing 20 horizontal character times for retrace gave the best results. So, in reality, there are 100 character times in every given horizontal line, 80 are used to display characters and 20 are used to allow for retrace. It should be noted that if too many character times are used for retrace, less time will be left to display the characters and the display will not "fill out" the screen. Conversely, if not enough character times are allowed for retrace, the display may "run off" the screen.

One hundred character times per complete horizontal line means that each character requires #37242.

61.73 microseconds /100 character times = 617.3 nanoseconds.

If we multiply the 20 horizontal retrace times by the



2-453

microseconds was all addition and where

This value falls short of the 25 to 30 microseconds required by the horizontal drive of the Ball monitor. To correct for this, an 8253 was programmed in the one-shot mode and was used to extend the horizontal drive pulsewidth.

Now that the 617.3 nanosecond character clock period is known, the dot clock is easy to calculate. Since each character is formed by placing 7 dots along the horizontal.

DOT CLOCK PERIOD = 617.3 ns (CHARACTER CLK PERIOD)/ 7 DOTS DOT CLOCK PERIOD = 88.183 nanoseconds DOT CLOCK FREQUENCY = 1/PERIOD = 11.34 MHz

Figures 5.5 and 5.6 illustrate the basic dot timing and the CRT system timing, respectively.

#### 6. SYSTEM SOFTWARE do does ladt agesta sail

#### 6.1 SOFTWARE OVERVIEW

As mentioned earlier the software is structured on a "foreground-background" basis. Two interrupt-driven routines, FRAME and POPDAT (Fig. 6.1) request service every 16.67 milliseconds and 617 microseconds respectively, frame is used to check the baud rate switches, update the system pointers and decode and assemble the keyboard characters. POPDAT is used to move data from the memory into the 8275's row buffer rapidly.

The foreground routine first examines the line-local switch to see whether to accept data from the USART or the keyboard. If the terminal is in the local mode, action will be taken on any data that is entered through the keyboard and the USART will be ignored on both output and input. If the terminal is in the line mode data entered through the keyboard will be transmitted by the USART and action will be taken on any data read out of the USART.

When data has been entered in the terminal the software first determines if the character received was an escape, line feed, form feed, carriage return, back space, or simply a printable character. If an escape was received the terminal assumes the next received character will be a recognizable escape sequence character. If it isn't no operation is performed.

After the character is decoded, the processor jumps to the routine to perform the required task. Figure 6.2 is a flow chart of the basic software operations; the program is listed in Appendix 6.8.

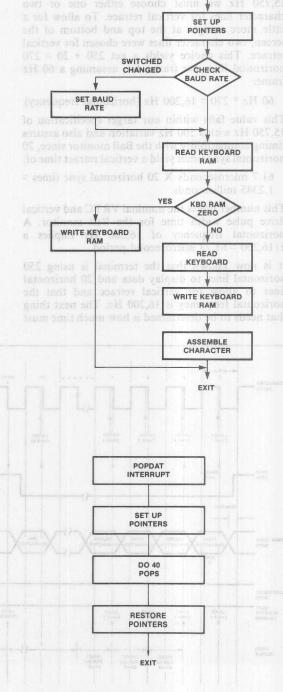


Figure 6-1. Frame and Popdat Interrupt Routines

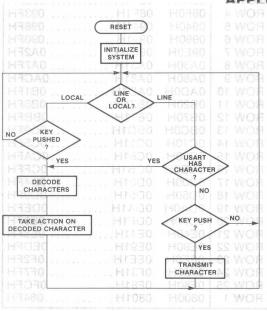


Figure 6-2. Basic Terminal Software

#### 6.2 SYSTEM MEMORY ORGANIZATION

The display memory organization is shown in Figure 6.3. The display begins at location 0800H in memory and ends at location 0FCFH. The 48 bytes of RAM from location 0FD0H to 0FFFH are used as system stack and temporary system storage. 2K bytes of PROM located at 0000H through 07FFH contain the systems program.

#### 6.3 MEMORY POINTERS AND SCROLLING

To calculate the location of a character on the screen, three variables must be defined. Two of these variables are the X and Y position of the cursor (CURSX, CURSY). In addition, the memory address defining the top line of the display must be known, since scrolling on the 8275 is accomplished simply by changing the pointer that loads the 8275's row buffers from memory. So, if it is desired to scroll the display up or down all that must be changed is one 16-bit memory pointer. This pointer is entered into the system by the variable TOPAD (TOP Address) and always defines the top line of the display. Figure 6.4 details screen operation during scrolling.

| TIONS         |       |       |         |
|---------------|-------|-------|---------|
| ROW 1         | 0800H | 0801H | 084FH   |
| ROW 2         | 0850H | 0851H |         |
| ROW 3         | 08A0H | 08A1H |         |
| ROW 4         | 08F0H | 08F1H |         |
| ROW 5         | 0940H | 0941H |         |
| ROW 6         | 0990H | 0991H |         |
| ROW 7         | 09E0H | 09E1H | . 0A2FH |
| ROW 8         | 0A30H | 0A31H | 0 4 1 1 |
| ROW 9         | 0A80H | 0A81H | .OACFH  |
| ROW 10        | 0AD0H | 0AD1H |         |
| ROW 11        | 0B20H | 0B21H | . OB6FH |
| ROW 12        | 0B70H | 0B71H | . OBBFH |
| <b>ROW 13</b> | 0BC0H | 0BC1H | . OCOFH |
| ROW 14        | 0C10H | 0C11H | OCEFII  |
| ROW 15        | 0C60H | 0C61H | .0CAFH  |
| ROW 16        | 0CB0H | 0CB1H | . OCFFH |
| ROW 17        | 0D00H | 0D01H | . 0D4FH |
| ROW 18        | 0D50H | 0D51H | . 0D9FH |
| <b>ROW 19</b> | 0DA0H | 0DA1H | . ODEFH |
| ROW 20        | 0DF0H | 0DF1H | 0E3FH   |
| ROW 21        | 0E40H | 0E41H | 0E8FH   |
| ROW 22        | 0E90H | 0E91H | . OEDFH |
| ROW 23        | 0EE0H | 0EE1H | 0F2FH   |
| ROW 24        | 0F30H | 0F31H | 0F7FH   |
| ROW 25        | 0F80H | 0F81H | . OFCFH |

Figure 6-3. Screen Display After Initialization

Subroutines CALCU (Calculate) and ADX (ADd X axis) use these three variables to calculate an absolute memory address. The subroutine CALCU is used whenever a location in the screen memory must be altered.

#### 6.4 SOFTWARE TIMING

One important question that must be asked about the terminal software is, "How fast does it run". This is important because if the terminal is running at 9600 baud, it must be able to handle each received character in 1.04 milliseconds. Figure 6.5 is a flowchart of the subroutine execution times. It should be pointed out that all of the times listed are "worst case" execution times. This means that all routines assume they must do the maximum amount of data manipulation. For instance, the PUT routine assumes that the character is being placed in the last column and that a line feed must follow the placing of the character on the screen.

How fast do the routines need to execute in order to assure operation at 9600 baud? Since POPDAT interrupts occur every 617 microseconds, it is possible to receive two complete interrupt requests in every character time (1042 microseconds) at 9600

| ROW 1    | 0800H  | 0801H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 084FH   | ROW 2            | 0850H 0851H089F                     |
|----------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------------------|-------------------------------------|
| ROW 2    | 0850H  | 0851H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 3            | 08A0H 08A1H08EF                     |
| ROW 3    | 08A0H  | 08A1HH0080                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |         | ROW 4            | 08F0H 08F1H093F                     |
| ROW 4    | 08F0H  | 08F1HH0380                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 093FH   | ROW 5            | 0940H 0941H 098F                    |
| ROW 5    | 0940H  | 0941H HOASO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |         | ROW 6            | 0990H 0991H 090F                    |
| ROW 6    | 0990H  | 0991H H9580                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |         | ROW 7            | 09E0H 09E1H 0A2F                    |
| ROW 7    | 09E0H  | 09E1H HONGO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |         | ROW 8            | 0A30H 0A31H 0A7F                    |
| ROW 8    | 0A30H  | 0A31H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0A7FH   | ROW 9            | 0A80H 0A81H0ACF                     |
| ROW 9    | 0A80H  | 0A81H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 10           | 0AD0H 0AD1H 0B1F                    |
| ROW 10   | 0AD0H  | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | ORIEH   | ROW 11           | 0B20H 0B21H0B6F                     |
| ROW 10   | 0B20H  | 0B21HH08A0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | OPEEU   | ROW 12           | 0B70H 0B71H0BBF                     |
| ROW 12   | 0B70H  | 0B71H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | ODDEL   | ROW 12           | 0BC0H 0BC1H 0C0F                    |
| 11177000 | 0BC0H  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         | ROW 14           | 0C10H 0C11H0C5F                     |
| ROW 13   |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         | ROW 15           | 0C60H 0C61H0CAF                     |
| ROW 14   | 0C10H  | 0C11H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | UCSFH   | ROW 16           | OCBOH OCB1HOCFF                     |
| ROW 15   | 0C60H  | 0C61H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | UCAFH   | ROW 16           |                                     |
| ROW 16   | 0CB0H  | and the second s |         |                  | mis 1 000000 000000                 |
| ROW 17   | 0D00H  | 0D01H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 18           |                                     |
| ROW 18   | 0D50H  | 0D51H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0D9FH   | ROW 19           | ODAOH ODA1HODEF                     |
| ROW 19   | 0DA0H  | 0DA1H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | UDEFH   | ROW 20           | 0DF0H 0DF1H0E3F                     |
| ROW 20   | 0DF0H  | 0DF1HH0300                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | UE3FH   | ROW 21           | 0E40H 0E41H0E8F                     |
| ROW 21   | 0E40H  | 0E41HH.O.A.C.O.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         | ROW 22           | 0E90H 0E91H0EDF                     |
| ROW 22   |        | 0E91H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 23           | 0EE0H 0EE1H0F2F                     |
| ROW 23   |        | 0EE1H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 24           | 0F30H 0F31H0F7F                     |
| ROW 24   |        | 0F31H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0F7FH   | ROW 25           | 0F80H 0F81H 0FCF                    |
| ROW 25   |        | 0F81HH0330                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | HOW 24+ | ROW 1            | 0800H 0801H 084F                    |
|          | Aft    | ter Initialization-10870                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | ROW 25  |                  | After 1 Scroll                      |
| ROW 3    | 08A0H  | 08A1H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | OSEEH   | ROW 4            | 08F0H = 08F1H = 2.5 = 093FI         |
| ROW 4    | 08F0H  | 08F1H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 5            | 0940H 0941H 098FI                   |
| ROW 5    | 0940H  | 0941H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 6            | 0990H 0991H 090FF                   |
| ROW 6    | 0990H  | 0991H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 7            |                                     |
| ROW 7    | 09E0H  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 042FH   | ROW 8            | 09E0H 09E1H 0A2FH 0A30H 0A31H 0A7FH |
| ROW 8    | 0A30H  | DA31H SSTIT SEST                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0A7FH   | ROW 9            | 0A80H 0A81H                         |
| ROW 9    | 0A80H  | 0A31H<br>0A81H<br>0AD1H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | DACEH   | ROW 10           | OADOH OAD1H OB1FI                   |
| ROW 10   | 0AD0H  | DADIHOLE TEVEN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | ORIFH   | ROW 11           | 0B20H 0B21H 0B6FF                   |
| ROW 11   | 0B20H  | 0B21Hb915                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | OBSEH   | ROW 12           | 0B70H 0B71H 0BBFI                   |
| ROW 12   | 0B2011 | 0B71H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 12           |                                     |
| ROW 13   | 0BC0H  | 0BC1H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | OCOEH   | ROW 14           | 0BC0H 0BC1H                         |
| ROW 14   | 000011 | 0C11H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0C5FH   | ROW 14           | 0C10H 0C11H MOX.4 0C5FI             |
| ROW 15   | 0060H  | 0C61H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | OCAFH   | ROW 15           | 0C60H 0C61H 0CAFF                   |
| ROW 16   |        | OCB1H Susped in                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         | ROW 16           |                                     |
| ROW 17   | UDOUH  | donoth ed laum it                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | ODVEH   | ROW 17           | 0D00H 0D01H 0D4FH 0D50H 0D51H 0D9FH |
| ROW 17   |        | 0D51H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         | ROW 18           | 0D00H 0D01H0D9FI                    |
| ROW 19   | UD VOH | 0DA1H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | ODEEH   | ROW 19<br>ROW 20 | ODAOH ODA1H                         |
| ROW 20   | ODAOH  | 0DF1H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | OF SELL |                  | 0DF0H 0DF1H0E3FI                    |
| ROW 21   | 0E40H  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 000000  | ROW 21           | 0E40H 0E41H0E8FI                    |
| ROW 22   |        | 0E91H                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | OFFI    | ROW 22<br>ROW 23 | 0E90H 0E91H 0EE0H 0EE1H 0F2FI       |
|          |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |                  |                                     |

ROW 25 | 0F80H | 0F81H ..... 0FCFH

OEE0H OEE1H ....OF2FH

0F30H 0F31H281849911.840F7FH4

0800H 0801H ..... 084FH

**ROW 23** 

ROW 24

ROW 1

ROW 2

ROW 24 0F30H 0F31H .....0F7FH

0F80H 0F81H ..... 0FCFH

0800H 0801H ..... 084FH 0850H 0851H .....089FH

08A0H 08A1H .....08EFH

After 2 Scrolls

After 2 Scrolls

After 3 Scrolls

After 4 Scrolls

After 5 Scrolls

After 6 Scrolls

After 6 Scrolls

After 6 Scrolls

After 6 Scrolls

After 7 Scrolls

After

**ROW 25** 

ROW 1

ROW 2

ROW 3

baud. Each POPDAT interrupt executes in 211 microseconds maximum. This means that each routine must execute in:

1042 - 2 \* 211 = 620 microseconds

By adding up the times for any loop, it is clear that all routines meet this speed requirement, with the exception of ESC J. This means that if the terminal is operating at 9600 baud, at least one character time must be inserted after an ESC J sequence.

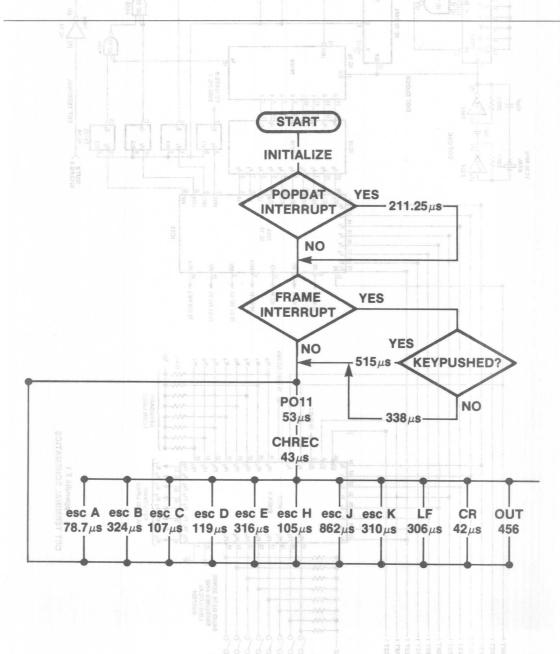
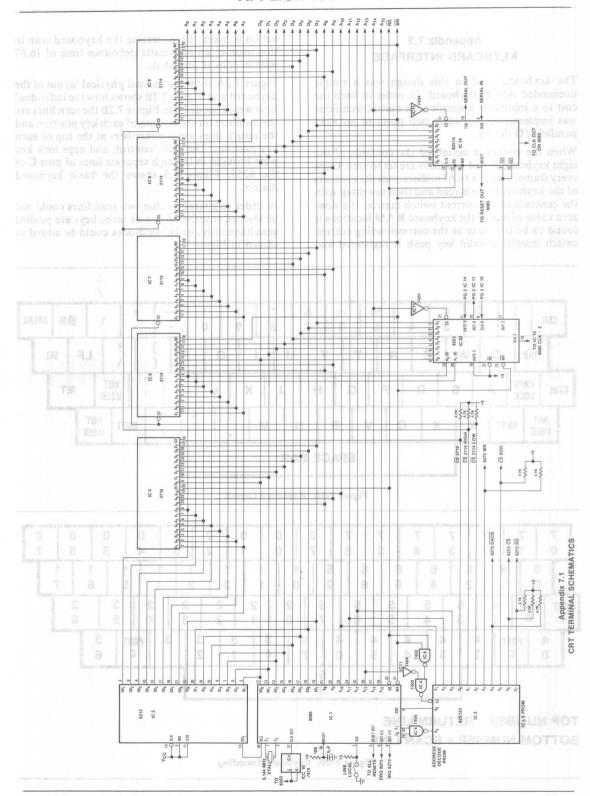


Figure 6-5. Timing Flowchart



# Appendix 7.2 KEYBOARD INTERFACE

The keyboard used in this design was a simple unencoded ASCII keyboard. In order to keep the cost to a minimum a simple scan matrix technique was implemented by using two ports of an 8255 parallel I/O device.

When the system is initialized the contents of the eight keyboard RAM locations are set to zero. Once every frame, which is 16.67 milliseconds the contents of the keyboard ram is read and then rewritten with the contents of the current switch matrix. If a non-zero value of one of the keyboard RAM locations is found to be the same as the corresponding current switch matrix, a valid key push is registered and

action is taken. By operating the keyboard scan in this manner an automatic debounce time of 16.67 milliseconds is provided.

Figure 7.2A shows the actual physical layout of the keyboard and Figure 7.2B shows how the individual keys were encoded. On Figure 7.2B the scan lines are the numbers on the bottom of each key position and the return lines are the numbers at the top of each key position. The shift, control, and caps lock key were brought in through separate lines of port C of the 8255. Figure 7.3 shows the basic keyboard matrix.

In order to guarantee that two scan lines could not be shorted together if two or more keys are pushed simultaneously, isolation diodes could be added as shown in Figure 7.4.

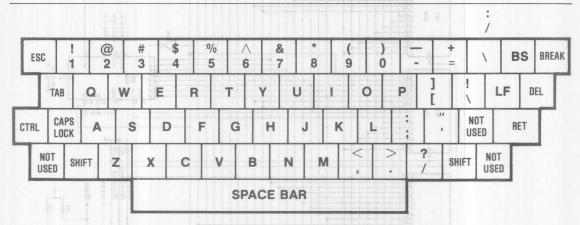
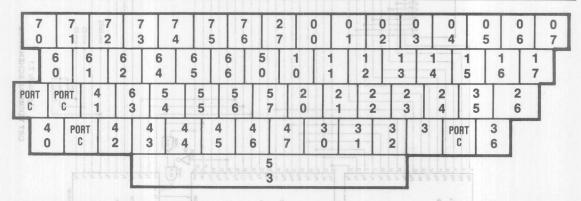


Figure 7-2A. Keyboard Layout



TOP NUMBER = RETURN LINE BOTTOM NUMBER = SCAN LINE

Figure 7-2B. Keyboard Encoding

Appendix 7.3 ESCAPE/CONTROL/DISPLAY CHARACTER SUMMARY

|      | CONT  | 24111 | 7        |     |     | YABL                        |                 |     | 4          | -                    |             | CAPE<br>UENCE  |                 |           |
|------|-------|-------|----------|-----|-----|-----------------------------|-----------------|-----|------------|----------------------|-------------|----------------|-----------------|-----------|
| BIT  | 000   | 001   | 010      | 011 | 100 | <sup>1</sup> 0 <sub>1</sub> | <sup>1</sup> 10 | 111 | 010        | 30/81 <sub>1</sub> A | 100         | 101            | 11 <sub>0</sub> | 111       |
| 0000 | NUL @ | DLE   | SP       | φ   | @   | PV                          |                 | Р   | Į x        | 2                    | A           | 3              | 200             |           |
| 0001 | SOH A | DCI Q | 4        |     | А   | Ο.                          | A               | Q   | 30600      |                      | 1           |                | 22              |           |
| 0010 | STX B | DC2 R | "\       | 2   | В   | R                           | В               | R   | 1          |                      | ₩ В         | V-0            |                 |           |
| 0011 | ETX C | DC3 S | #        | 3   | С   | S                           | С               | S   | 8          | W                    | Q           |                |                 |           |
| 0100 | EOT D | DC4 T | \$       | 4   | D   | Т                           | D               | T   | -          |                      |             | 8              |                 |           |
| 0101 | ENQ E | NAK   | %        | 5   | E   | U                           | E               | U   | 4 %        | 1-4                  | CLR E       | 13             |                 |           |
| 0110 | ACK F | SYN V | &        | 6   | F   | V                           | F               | V   |            |                      |             |                |                 |           |
| 0111 | BEL G | ETB W | ,        | 7   | G   | W) o                        | G               | W   | re 7-3. Ke | Figu                 |             |                |                 |           |
| 1000 | BS H  | CAN   | (        | 8   | Н   | X                           | Н               | X   |            |                      | HOME H      |                |                 |           |
| 1001 | нт    | EM Y  | )        | 9   | 1   | Υ                           | 1               | Y   |            |                      | 0.55        |                |                 |           |
| 1010 | LF J  | SUB Z | *        | :   | J   | Z                           | J               | Z   |            |                      |             | OBO M          | Aq              |           |
| 1011 | VT K  | ESC   | J MAG    | 18: | К   | [                           | К               |     | 13370      | DO OLVIS             | ezanEL oid  | oftheld        | earlier al      | batata a  |
| 1100 | FF L  | FS /  | ,        | <   | L   | \                           | L               |     | Was        | device               | type e      | MO-nor         | n s olmi        | e 8275    |
| 1101 | CR M  | GS    | ->       | =   | М   | ]                           | М               |     | 4 - 4      | 1                    | DOMESTIC OF | of the service | rtain pro       | traing co |
| 1110 | SO_N  | RS ^  | 45.07/14 | >   | N   | Λ                           | N               |     |            | well as fi           |             |                | for the sy      | adresses  |
| 1111 | S1 O  | us -  | 7        | ?   | 0   | -                           | 0               |     | 1          |                      |             | Jio            | Ultipii         | sisq ccs  |

device was chosen simply because it is the only "by
eight" prom available in a 16 pm package. The
connection of the gram is shown in detail in Figure
7.5 and its truth table is shown in Figure 7.6. Note
that when a fetch cycle (Mijospino qui berongi sia Jud betsenge ed nas sent) of the SOD line is the only thing that
determines if memory reads will be written into the
8275s row buffers. This is done by pulling both
DACK and WRITE low on the 8275.

Also note that all of the outputs of the bipolar prom MUST BE PULLED HIGH by a resistor. This

Floure 7-4. Isolating Scan Lines With Diodes.

disabled

NOTE:

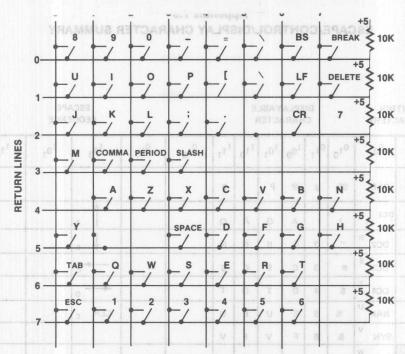


Figure 7-3. Keyboard Matrix

# Appendix 7.4 PROM DECODING

As stated earlier, all of the logic necessary to convert the 8275 into a non-DMA type of device was performed by a single small bipolar prom. Besides turning certain processor READS into DACKS and WRITES for the 8275, this 32 by 8 prom decoded addresses for the system ram, rom, as well as for the 8255 parallel I/O port.

Any bipolar prom that has a by eight configuration could function in this application. This particular device was chosen simply because it is the only "by eight" prom available in a 16 pin package. The connection of the prom is shown in detail in Figure 7.5 and its truth table is shown in Figure 7.6. Note that when a fetch cycle (M1) is not being performed, the state of the SOD line is the only thing that determines if memory reads will be written into the 8275's row buffers. This is done by pulling both DACK and WRITE low on the 8275.

Also note that all of the outputs of the bipolar prom MUST BE PULLED HIGH by a resistor. This prevents any unwanted assertions when the prom is disabled.

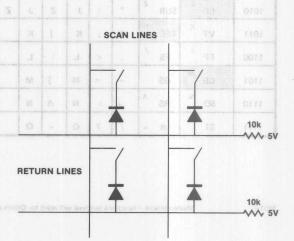


Figure 7-4. Isolating Scan Lines With Diodes

1000

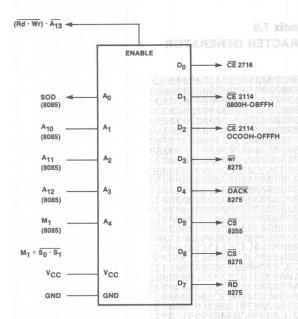


Figure 7-5. Bipolar Prom (825123) Connection

Figure 7-6. Truth Table Bipolar Prom

# 8.7 xibseqqA Appendix 7.5 9370A9AHO 30 9 CHARACTER GENERATOR

As previously mentioned, the character generator used in this terminal is a 2716 or 2758 EPROM. A 1K by 8 device is sufficient since a 128 character 5 by 7 dot matrix only requires 8K of memory. Any "standard" or custom character generator could have been used.

The three low-order line count outputs (LC0-LC2) from the 8275 are connected to the three low-order address lines of the character generator and the seven character generator outputs (CC0-CC6) are connected to A3-A9 of the character generator. The output from the character generator is loaded into a shift register and the serial output from the shift register is the video output of the terminal.

Now, let's assume that the letter "E" is to be displayed. The ASCII code for "E" is 45H. So, 45H is presented to address lines A2-A9 of the character generator. The scan lines will now count each line from zero to seven to "form" the character as shown in Fig. 7.7. This same procedure is used to form all 128 possible characters.

It should be obvious that "custom" character fonts could be made just by changing the bit patterns in the character generator PROM. For reference, Appendix 7.6 contains a HEX dump of the character generator used in this terminal.

45H = 01000101 Address to Prom = 01000101 SL2 SL1 SL0 = 228H - 22FH

Depending on state of Scan lines.

Character generator output

| Rom Address | Rom Hex | Output | Bi  | t Ou | tput* |   |
|-------------|---------|--------|-----|------|-------|---|
| 228H        | 3E      | 0      | 1 2 | 3 4  | 5 6   | 7 |
| 229H        | 02      |        | XX  | XX   | X     |   |
| 22AH        | 02      |        | X   |      |       |   |
| 22BH        | 0E      |        | X   |      |       |   |
| 22CH        | 02      |        | XX  | X    |       |   |
| 22DH        | 02      |        | X   |      |       |   |
| 22EH        | 3E      |        | X.  |      |       |   |
| 22FH 0000   | 00      |        | XX  | 20   | X     |   |
|             | FUNIT   |        |     |      |       |   |

Bits 0, 6 and 7 are not used.

Figure 7-7. Character Generation

<sup>\*</sup> note bit output is backward from convention.

# Appendix 7.6 ROTARBUBD RETHEX DUMP OF CHARACTER GENERATOR

# Appendix 7.7 COMPOSITE VIDEO

In this design, it was assumed that the monitor required a separate horizontal drive, vertical drive, and video input. However, many monitors require a composite video signal. The schematic shown in Figure 7.8 illustrates how to generate a composite video signal from the output of the 8275.

The dual one-shots are used to provide a small delay and the proper horizontal and vertical pulse to the composite video monitor. The delay introduced in the vertical and horizontal timing is used to "center" the display. VR1 and VR2 control the amount of delay. IC3 is used to mix the vertical and horizontal retrace and Q1 along with the R1, R2, and R3 mix the video and the retrace signal and provide the proper DC levels.

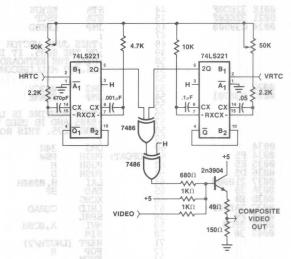


Figure 7-8. Composite Video

# Appendix 7.8 SOFTWARE LISTINGS

ISIS-II 8080/8085 MACRO ASSEMBLER, X108

| LOC                                                                           | OBJ                                                                                                     | SEQ                                                                                                                                                                                             | SOURCE STATEMENT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18001<br>1801<br>1802<br>1803<br>A000<br>6000<br>6000<br>1400<br>0F80<br>0FD8 |                                                                                                         | 1 \$MOD85 2 3 4 5 6 7 7 8 9 10 PORTA 11 PORTB 12 PORTC 13 CNWD55 14 USTF 15 USTD 16 CNT0 17 CNT1 18 CNT2 19 CNTM 20 CRTS 21 CRTM 22 INT75 23 TPDIS 24 BTDIS 25 LAST 26 CURBO) 27 LNGTH 28 STPTR | MACROFILE ;NO DMA 8275 SOFTWARE ALL I/O IS MEMORY MAPPED ;SYSTEM ROM 0000H TO 07FFH ;SYSTEM RAM 0800H TO 07FFH ;8275 READ 1400H TO 13FFH ;8275 READ 1400H TO 13FFH ;8255 READ MARITE 1800H TO 1FFF ;8253 ENABLED BY A14 ;8251 ENABLED BY A15 EQU 1801H ;8255 PORT A ADDRESS EQU 1801H ;8255 PORT B ADDRESS EQU 1802H ;8255 PORT C ADDRESS EQU 1803H ;8255 PORT C ADDRESS EQU 1803H ;8255 PORT C ADDRESS EQU 1803H ;8251 DATA EQU 6000H ;8251 DATA EQU 6000H ;8253 COUNTER 0 EQU 6000H ;8253 COUNTER 0 EQU 6000H ;8253 COUNTER 2 EQU 6000H ;8253 COUNTER 2 EQU 6000H ;8253 COUNTER 2 EQU 6000H ;8255 CONTROL ADDRESS EQU 1000H ;8275 MODE MORD EQU 1000H ;8275 CONTROL ADDRESS EQU 1000H ;8275 MODE ADDRESS EQU 1000H ;8275 INTERRUPT CLEAR EQU 1000H ;8275 INTERRUPT CLEAR EQU 06F80H ;FIRST BYTE AFTER DISPLAY EQU 06F80H ;FIRST BYTE AFTER DISPLAY EQU 18H ;BOTTOM Y CURSOR EQU 06F80H ;ENGTH OF ONE LINE EQU 06F80H ;ENGTH OF ONE LINE EQU 06F80H ;LENGTH OF ONE LINE EQU 06F80H ;LENGTH OF ONE LINE EQU 06F80H ;LENGTH OF ONE LINE |
|                                                                               |                                                                                                         | 29<br>30 1 (1944)                                                                                                                                                                               | START PROGRAM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                                                                               |                                                                                                         | 31<br>32<br>32<br>32<br>32<br>32                                                                                                                                                                | ; ALL VARIABLES ARE INITIALIZED BEFORE ANYTHING ELSE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 9000<br>9000<br>9000<br>9000<br>9001<br>9001<br>9001<br>9001                  | 1 31 E00F<br>4 210008<br>7 22E30F<br>7 22E80F<br>9 3E00<br>7 32E10F<br>2 32E20F<br>5 32E80F<br>8 32E70F | 33<br>34<br>35<br>36<br>37<br>38<br>39<br>40<br>41<br>42<br>42<br>43                                                                                                                            | DI ;DISABLE INTERRUPTS LXI H,TPDIS ;LOAD STACK POINTER LXI H,TPDIS ;LOAD H&L WITH TOP OF DISPLAY SHLD CURAD ;SET TOP = TOP OF DISPLAY SHLD CURAD ;STORE THE CURRENT ADDRESS MVI A,ØØH ;ZERO A STA CURSY ;ZERO CURSOR Y POINTER STA CURSX ;ZERO CURSOR X POINTER STA KBCHR ;ZERO KBD CHARACTER STA USCHR ;ZERO USART CHAR BUFFER STA KEYDWN ;ZERO KEY DOWN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

| 001E 32ED0F<br>0021 32EE0F<br>0024 C39800                                                                                                                                                                                                   | 44<br>45<br>46<br>47                                                                                          | STA<br>STA<br>JMP                                                  | KEYOK<br>ESCP<br>LPKBD                                             | ZERO KEYOK<br>ZERO ESCAPE<br>JUMP AND SET EVERYTHING UP                                                                                                                                                                                                                                                                                     |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 70K 70L8221 20 Eq. ( VR                                                                                                                                                                                                                     | 47<br>48<br>49<br>50<br>51<br>52                                                                              | THIS<br>OF THE<br>READ<br>16.6                                     | JUMP VECTOR I<br>HE 8085. IT IS<br>THE KEYBOARD.<br>67 MILLISECONI | IS LOCATED AT THE RST 5.5 LOCATION USED TO READ THE 8275 STATUS AND THIS ROUTINE IS EXECUTED ONCE EVERY SS.                                                                                                                                                                                                                                 |
| 002C<br>002C C36701                                                                                                                                                                                                                         | 53<br>54<br>55<br>56<br>57                                                                                    | THIS                                                               | 002CH<br>FRAME<br>ROUTINE IS LO                                    | and video input. However, many monitors require a composite video signal. The schematic shown in                                                                                                                                                                                                                                            |
| 034<br>034<br>035<br>035<br>036<br>037<br>210000<br>037<br>210000<br>033<br>38<br>38<br>030<br>224880F<br>035<br>936<br>940<br>382<br>382<br>383<br>384<br>385<br>386<br>387<br>387<br>387<br>387<br>387<br>387<br>387<br>387<br>387<br>387 | 57<br>58<br>60<br>61 POPDAT:<br>62<br>63<br>64<br>65<br>66<br>67<br>68<br>69<br>71<br>72<br>73                | THE ORG PUSH PUSH LXI DAD XCHG LHLD SPHL MVI SIM                   | WAN TO NOWN I                                                      | ; SAVE A AND FLAGS ; SAVE A AND FLAGS ; SAVE HAND L ; SAVE DAND E ; ZERO HAND L ; PUT STACK POINTER IN HAND L ; PUT STACK FON THE SAME PUT CURRENT LINE INTO SP ; SET MASK FOR SIM                                                                                                                                                          |
| 70045 E1<br>70045 E1<br>70046 E1<br>70047 E1<br>70049 E1<br>70049 E1<br>70040 E1<br>70040 E1<br>70040 E1<br>70040 E1<br>70040 E1<br>70050 E1<br>70050 E1<br>70050 E1                                                                        | 75+<br>76+<br>77+<br>78+<br>79+<br>80+<br>81+<br>82+<br>83+<br>84+<br>85+<br>86+<br>87+<br>89+<br>901+<br>93+ | POP<br>POP                                                         | RE ALL I/OHIS O GTEEN H O GEEFEN H                                 | SOFTWARE SIS-II 8869/8885 MACRO ASSEMBLER, XIBS OC OBJ SEQ SOURCE STATEMENT 1 SMODSS MACROFILE 2 MODSS MACROFILE 2 MODSS MACROFILE 2 MODSS MACROFILE 3 MODSS MACROFILE                                                                                                                                                                      |
| 0056 E1 0058 E1 0058 E1 0058 E1 0058 E1 0058 E1 0058 E1 0059 E1                                                                                                     | 94+<br>95+<br>96+<br>97+<br>98+<br>99+<br>100+<br>101+<br>102+<br>103+                                        | POP<br>POP<br>POP<br>POP<br>POP<br>POP<br>POP<br>POP<br>POP<br>POP | HIST OF HER                                                        | 1                                                                                                                                                                                                                                                                                                                                           |
| 0069 E1 00068 BF 0006C 30 0006D 21,0000 0070 39 0071 EB 00076 EB 0077 7A 0078 BC 0077 7A 0078 BC 0077 C28400 0070 BD 0070 BD 00070 C28400 0070 BD 00070 C28400 0084 22E80F 0087 3E18                                                        | 112+<br>113+<br>114<br>115<br>116<br>117<br>118<br>119<br>120<br>121                                          | POP<br>POP<br>RRC<br>SIM<br>LXI<br>DAD<br>XCHG<br>SPHL             | H,0000H<br>SP<br>H,LAST<br>A,D<br>H,FTK<br>A,E<br>L                | ;SET UP A ;GO BACK TO NORMAL MODE ;ZERO HL ;ADD STACK ;PUT STACK IN H AND L ;RESTORE STACK ;PUT BOITOM DISPLAY IN H AND L ;SWAP REGISTERS ;PUT HIGH ORDER IN A ;SEE IF SAME AS H ;IF NOT LEAVE ;PUT LOW ORDER IN A ;SEE IF SAME AS L ;IF NOT LEAVE ;LOAD H AND L WITH TOP OF SCREEN MEMORY ;PUT BACK CURRENT ADDRESS ;SET MASK ;OUTPUT MASK |

| 008A D1 13<br>008B E1 13<br>008C F1 13<br>008D FB 13<br>008E C9 13                                                                                                                                     | 2<br>3<br>4<br>5<br>7<br>8<br>9                                                                                                                                                  | POP D<br>POP H<br>POP PSW<br>EI GMAILEINE                                                                                        | GET D AND E GET H AND L GET A AND FLAGS TURN ON INTERRUPTS GO BACK UTINE FOR THE FRAME INTERRUPT SET MASK                                                                                                                                                       | 00F9 218110<br>00F9 3608<br>00FE 28                                                                                                                                                              |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0/08F 3E18 13<br>0/08F 3E18 14<br>0/091 3Ø 14<br>0/092 C1 14<br>0/093 D1 14<br>0/094 E1 14<br>0/095 F1 14<br>0/097 C9 14                                                                               | BYPASS:                                                                                                                                                                          | THIS IS THE EXIT ROUSE A, 18H SIM POP B POP D POP H POP PSW EI                                                                   | TURN ON INTERRUPTS ;GO BACK  UTINE FOR THE FRAME INTERRUPT ;SET MASK ;OUTPUT THE MASK ;GET B AND C ;GED D AND E ;GET H AND L ;GET A AND FLAGS ;ENABLE INTERRUPTS ;GO BACK  A OF RAM THAT IS USED                                                                | 8101 3656<br>8103 3689<br>8108 23689<br>8108 CDB803<br>8108 3689                                                                                                                                 |
| 15                                                                                                                                                                                                     | Ø                                                                                                                                                                                | FOR KEYBOARD DEBOUN                                                                                                              |                                                                                                                                                                                                                                                                 | 9115 £8<br>6177 36<br>8186 3818                                                                                                                                                                  |
| 90A1 210008 15<br>90A4 01000F 16<br>90A9 23<br>90AA 7C 16<br>90AB 88 16<br>90AC C2A700 16<br>90B0 89 16<br>90B1 C2A700 16                                                                              | 55<br>66<br>77<br>88<br>99<br>90<br>12<br>12<br>13<br>14<br>14<br>15<br>15<br>15<br>16<br>16<br>17<br>18<br>18<br>18<br>18<br>18<br>18<br>18<br>18<br>18<br>18<br>18<br>18<br>18 | ;THIS ROUTINE CLEARS;SPACE CODES (20H) I ;LXI H,TPDIS LXI B,LAST MVI M,20H INX H MOV A,H CMP B JNZ LOOPF MOV A,L CMP C JNZ LOOPF | THE ENTIRE SCREEN BY PUTTING N EVERY LOCATION ON THE SCREEN.  ;PUT TOP OF SCREEN IN HL ;PUT BOTTOM IN BC ;PUT SPACE IN M ;INCREMENT POINTER ;GET H ;SEE IF SAME AS B ;IF NOT LOOP AGAIN ;GET L ;SEE IF SAME AS C ;IF NOT LOOP AGAIN                             | 0113 20<br>0114 E686<br>0116 C22181<br>0119 36016<br>0121 3662<br>0122 3663<br>0124 E630<br>0126 E630<br>0126 E630<br>0126 E630<br>0127 3600<br>0128 3200<br>0128 3200<br>0138 3200<br>0131 3650 |
| ØØB4 3E8B 17<br>ØØB6 32Ø318 17                                                                                                                                                                         | Z MLADA                                                                                                                                                                          | MVI A,8BH<br>STA CNWD55                                                                                                          | MOVE 8255 CONTROL WORD INTO A                                                                                                                                                                                                                                   | 0139 CALSGI                                                                                                                                                                                      |
| 00B9 2101A0 17<br>00BC 3680 17<br>00BE 3600 17<br>00C0 3640 18<br>00C2 3640 18<br>00C2 3640 18<br>00C2 3640 18                                                                                         | 76<br>77<br>78 MAOW 3M<br>79 EO<br>30 STIME<br>81 YOAR<br>82<br>83                                                                                                               | LXI H,USTF MVI M,80H MVI M,80H MVI M,40H NOP MVI M,0EAH MVI M,05H                                                                | GET 8251 FLAG ADDRESS DUMMY STORE TO 8251 RESET 8251 RESET 8251 RESET 8251 WAIT LOAD 8251 MODE WORD LOAD 8251 COMMAND WORD                                                                                                                                      | 8143 E680<br>0145 CA4581<br>0148 CA4582<br>0148 SA01A0<br>0150 CA4681<br>0153 SA070<br>0150 CA4681                                                                                               |
| 00C7 3E32 18<br>00C9 320360 18<br>00CC 3E32 18<br>00CC 3E32 18<br>00CD 320060 19<br>00D1 3E00 19<br>00D3 320060 19<br>00D6 CDDC00 15<br>00D9 C3F900 19                                                 | 35<br>36<br>37<br>38<br>38<br>39<br>30<br>31<br>32<br>33<br>EDA                                                                                                                  | ;8253 INITIALIZATION ;MVI A,32H STA CNTM MVI A,32H STA CNTØ MVI A,00H STA CNTØ CALL STBAUD JMP IN75                              | ;CONTROL WORD FOR 8253 ;PUT CONTROL WORD INTO 8253 ;LSB 8253 ;PUT IT IN 8235 ;MSB 8253 ;PUT IT IN 8253 ;GO DO BAUD RATE ;GO DO BAUD RATE ;GO DO RATE ;GO THE NUMBERS NEEDED TO LOAD                                                                             | 913C 3A88A8<br>815F 857F<br>815A 23878F<br>815A C34582<br>815A C34582                                                                                                                            |
| 15                                                                                                                                                                                                     | 70                                                                                                                                                                               | THIS ROUTINE READS<br>OF THE 8255 AND LOO<br>THE 8253 TO PROVIDE                                                                 | THE BAUD RATE SWITCHES FROM PORT C<br>KS UP THE NUMBERS NEEDED TO LOAD<br>THE PROPER BAUD RATE.                                                                                                                                                                 | 0168 3A0114                                                                                                                                                                                      |
| 00DC 3A0218 20<br>00DF E60F 20<br>00E1 32EC0F 20<br>00E4 07<br>00E5 21C505 20<br>00E8 1600 20<br>00EA 5F 20<br>00EB 19 20<br>00EC 110360 20<br>00EF 3EB6 20<br>00EF 21B 21<br>00F2 1B 21<br>00F3 7E 21 | 50 STBAUD:                                                                                                                                                                       | LDA PORTC ANI ØFH STA BAUD RLC LXI H, BDLK MVI D, ØØH MOV E, A DAD D LXI D, CNTM MVI A, ØB6H STAX D DCX D MOV A, M STAX D INX H  | READ BAUD RATE SWITCHES STRIP OFF 4 MSB'S SAVE IT MOVE BITS OVER ONE PLACE GET BAUD RATE LOOK UP TABLE ZERO D PUT A IN E GET OFFSET POINT DE TO 8253 GET CONTROL WORD STORE IN 8253 POINT AT #2 COUNTER GET LSB BAUD RATE PUT IT IN 8253 POINT AT MSB BAUD RATE | 815E ZAE38F<br>8171 Z2E88F<br>6174 3A8218<br>6175 E68F<br>8176 A77<br>8170 E8<br>8170 E8                                                                                                         |
| 00F8 C9 21                                                                                                                                                                                             | 14<br>15 MWOD EI<br>17A GMUT M<br>18 GRADSKS                                                                                                                                     | MOV A,M<br>STAX D<br>RET                                                                                                         | GET MSB BAUD RATE<br>PUT IT IN 8253<br>GO BACK                                                                                                                                                                                                                  |                                                                                                                                                                                                  |

| 017E C4DC00 298 CNZ STBAUD ;IF NOT SAME DO SOMETHING 299 ;READ KEYBOARD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                        |                                                                                      |                                                                                          | AFFLICA                                                                                | 110113                                                                                                                                                                          |                                                      |                                                      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Ø1Ø1 3<br>Ø1Ø3 3<br>Ø1Ø5 3<br>Ø1Ø7 2<br>Ø1Ø8 0<br>Ø1ØB 3                               | 3658<br>3689<br>36DD<br>23<br>CDB8Ø3<br>36EØ<br>3623                                 | 225 H STM 3<br>226<br>227<br>228<br>229<br>230<br>231                                    | MVI M,58H<br>MVI M,89H<br>MVI M,0DDH<br>INX H<br>CALL EDCUR<br>MVI M,0E0H<br>MVI M,23H | SCREEN PARAMETER BYTE 1 SCREEN PARAMETER BYTE 2 SCREEN PARAMETER BYTE 3 SCREEN PARAMETER BYTE 4 HL=1001H LOAD THE CURSOR PRESET COUNTERS START DISPLAY                          | 8138<br>10<br>10<br>11<br>11                         |                                                      |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                        |                                                                                      | 232<br>233<br>234<br>235                                                                 | THIS ROUTINE READS E<br>AND TAKES PROPER ACT<br>SWITCH IS SET                          | BOTH THE KEYBOARD AND THE USART<br>FION DEPENDING ON HOW THE LINE-LOCAL                                                                                                         | . ec                                                 | Teno                                                 |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 010F<br>0111<br>0112                                                                   | 3E18<br>3Ø<br>FB                                                                     | 236<br>237 SETUP:<br>238<br>239<br>240<br>241                                            | MVI A,18H<br>SIM<br>EI                                                                 | ;SET MASK<br>;LOAD MASK<br>;ENABLE INTERRUPTS                                                                                                                                   | 326868<br>328668<br>328168                           |                                                      |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 0113 2<br>0114 0<br>0116 0<br>0119 3<br>011C H<br>011E 0<br>0121 3<br>0124 0<br>0129 3 | 20<br>E680<br>C22101<br>3A01A0<br>E602<br>C25C01<br>3AEA0F<br>E680<br>C23101<br>3E00 | 242<br>243 RXRDY:<br>244<br>245<br>246<br>247<br>248<br>249 KEYINP:<br>250<br>251<br>251 | ANI 80H JNZ KEYINP LDA USTF ANI 02H JNZ OK7 LDA KEYDWN ANI 80H JNZ KEYS MVT A 00H      | ;GET LINE LOCAL ;IS IT ON OR OFF? ;LEAVE IF IT IS ON ;READ 8251 FLAGS ;LOOK AT RXRDY ;IF HAVE CHARACTER GO TO WORK ;GET KEYBOARD CHARACTER ;IS IT THERE ;IF KEY IS PUSHED LEAVE | 21 0008<br>01000F<br>23520<br>7C<br>23               | GGAL<br>BGAT<br>BGAS<br>BGAS<br>BGAS<br>BGAS         |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Ø12B<br>Ø12E<br>Ø131<br>Ø134<br>Ø135                                                   | 32EDØF<br>C313Ø1<br>3AEDØF<br>4F<br>3AEBØF                                           | 253<br>254<br>255 KEYS: 256<br>257                                                       | STA KEYOK JMP RXRDY LDA KEYOK MOV C,A LDA KBCHR                                        | CLEAR KEYOK LOOP AGAIN WAS KEY DOWN SAVE A IN C GET KEYBOARD CHARACTER                                                                                                          | 75<br>89<br>C2A786                                   | GOB1                                                 |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 0139<br>013C<br>013F<br>0142<br>0143                                                   | CA1301<br>32EDØF<br>32E7ØF<br>20<br>E680                                             | 258<br>259<br>260<br>261<br>262<br>263                                                   | JZ RXRDY<br>STA KEYOK<br>STA USCHR<br>RIM<br>ANI 80H                                   | ;IS IT THE SAME AS KEYOK<br>;IF SAME LOOP AGAIN<br>;IF NOT SAVE IT<br>;SAVE IT<br>;GET LINE LOCAL<br>:WHICH WAY                                                                 | 320318                                               |                                                      |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 0145 0<br>0148 0<br>014E E<br>0150 0                                                   | CA4BØ1<br>C34EØ2<br>3AØ1AØ<br>E6Ø1<br>CA4BØ1<br>3AE7ØF<br>32ØØAØ                     | 264<br>265<br>266 TRANS:<br>267<br>268<br>269<br>270                                     | JZ TRANS JMP CHREC LDA USTF ANI Ø1H JZ TRANS LDA USCHR STA USTD                        | LEAVE IF LINE TIME TO DO SOME WORK GET USART FLAGS READY TO TRANSMIT? LOOP IF NOT READY GET CHARACTER PUT IN USART                                                              | 2101A6<br>3588<br>3568<br>3548<br>80<br>368A<br>368A | 6689<br>6680<br>6603<br>6602<br>6602<br>6603<br>6603 |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Ø15C 3<br>Ø15F 8<br>Ø161 3<br>Ø164 6                                                   | 3AØØAØ<br>E67F<br>32E7ØF<br>C34EØ2                                                   | 272 OK7:<br>273<br>274<br>275<br>276                                                     | LDA USTD ANI 07FH STA USCHR JMP CHREC                                                  | ; LEAVE ; LEAVE ; LEAVE                                                                                                                                                         | 3832<br>328368<br>3832                               | 8 8C7<br>88C9<br>88CC                                |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Ø167 E<br>Ø168 E<br>Ø169 E<br>Ø16A C<br>Ø16B 3                                         | F5<br>E5<br>D5<br>C5<br>3AØ114                                                       | 277<br>278<br>279<br>280 FRAME:<br>281<br>282<br>283<br>284                              | THIS ROUTINE CHECKS; SCREEN POINTERS AND PUSH PUSH H PUSH D PUSH B LDA INT75           | THE BAUD RATE SWITCHES, RESETS THE READS AND LOOKS UP THE KEYBOARD.  ;SAVE A AND FLAGS ;SAVE H AND L ;SAVE D AND E ;SAVE B AND C ;READ 8275 TO CLEAR INTERRUPT                  | 326666<br>32666<br>32666<br>CDDC66<br>C3F966         |                                                      |
| 299 CNZ STBAUD ; IF NOT SAME DO SOMETHING 300 ; READ KEYBOARD 301                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Ø16E 2<br>Ø171 2                                                                       | 2AE3ØF<br>22E8ØF                                                                     | 285<br>286<br>287<br>288<br>289<br>290                                                   | SET UP THE POINTERS LHLD TOPAD SHLD CURAD                                              | ;LOAD TOP IN H AND L<br>;STORE TOP IN CURRENT ADDRESS                                                                                                                           | 3A0218<br>E60F<br>32EC0F<br>07                       | 000C<br>000F<br>00E1                                 |
| 300 CC READ KEYBOARD G XATE EIG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Ø174 3<br>Ø177 E<br>Ø179 4<br>Ø17A 3<br>Ø17D E<br>Ø17E 0                               | 3A0218<br>E60F<br>47<br>3AEC0F<br>B8<br>C4DC00                                       | 298                                                                                      | CNZ STBAUD                                                                             | ;READ BAUD RATE SWITCHES<br>;STRIP OFF 4 MSB'S<br>;SAVE IN B<br>;GET BAUD RATE<br>;SEE IF SAME AS B<br>;IF NOT SAME DO SOMETHING                                                | 1.8                                                  |                                                      |
| ## 1342 ## 1362 ## 1362 ## 1364 ## 1364 ## 1364 ## 1364 ## 1364 ## 1364 ## 1364 ## 1364 ## 1364 ## 1365 ## 1365 ## 1365 ## 1365 ## 1365 ## 1365 ## 1365 ## 1365 ## 1365 ## 1365 ## 1365 ## 1365 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 1366 ## 136 | Ø184 E<br>Ø186 C<br>Ø189 C                                                             | E640<br>C2C201<br>CD8F01                                                             | 300<br>301<br>302<br>303<br>304<br>305                                                   | READ KEYBOARD  LDA KEYDWN ANI 40H JNZ KYDOWN CALL RDKB                                 | SET THE FLAGS<br>IF KEY IS DOWN JUMP AROUND<br>GO READ THE KEYBOARD                                                                                                             | 12<br>72<br>12<br>12                                 | 0023<br>0024<br>8025<br>8025<br>8027<br>8028         |

| NISE SIEFAR                             | 307               | RDKR.       | LYT         | H SHOON                     | POTNIT HE AM VEVOARD DAM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                           |
|-----------------------------------------|-------------------|-------------|-------------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| Ø192 3AØ218                             | 308               | CHARACTER   | LDA         | PORTC                       | POINT HL AT KEYBOARD RAM GET COMTROL AND SHIFT SAVE IN MEMORY SET UP A OUTPUT A SAVE A IN B READ KEYBOARD INVERT A SET THE FLAGS LEAVE IF KEY IS DOWN GET SCAN LINE BACK ROTATE IT OVER ONE DO IT AGAIN ZERO A SAVE KEY DOWN LEAVE POINT AT RETURN LINE PUT A BACK SAVE RETURN LINE IN MEMORY POINT H AT SCAN LINE SAVE KEY DOWN LEAVE SAVE KEY DOWN LEAVE GET SCAN LINE IN MEMORY POINT H AT SCAN LINE SAVE KEY DOWN LEAVE GET SCAN LINE INDERSET KEY DOWN LEAVE GET FCAN LINE GET RETURN LINE GET RETURN LINE GET RETURN LINE GET RETURN LINE GET FLAGS IF DIFFERENT KEY HAS CHANGED GET KEY DOWN HAS THIS BEEN DONE BEFORE? LEAVE IF IT HAS GET READY TO ZERO B ZERO B ROTATE A DO IT AGAIN POINT H AT SCAN LINES GET READY TO ZERO B ZERO B ROTATE A DO IT AGAIN POINT H AT SCAN LINES GET READY TO LOOP START C COUNTING ROTATE A JUMP TO LOOP GET RETURN LINES GET READY TO LOOP START C COUNTING ROTATE A JUMP TO LOOP GET RETURN LINES GET SCAN AND RETURN LINES GET SCAN AND RETURN LINES SAVE A IN B GET SHIFT CONTROL SET BIT IF SET LEAVE READ IT AGAIN STRIP CONTROL SAVE A IN D STRIP CONTROL SAVE A IN D STRIP CONTROL SAVE A IN D STRIP SHIFT SAVE A GET SHIFT CONTROL SAVE A IN D STRIP SHIFT SAVE A GET SHIFT CONTROL SAVE A IN D STRIP CONTROL SAVE A IN D STRIP CONTROL SAVE A IN D STRIP SHIFT SAVE A GET SHIFT CONTROL SAVE A IN D STRIP SHIFT SAVE A GET SHIFT CONTROL SATE SHIFT SAVE A GET SAME? IF SET LEAVE PUT TARGET IN E ZERO D GET LOOKUP TABLE |                                           |
| 0196 3ÉFE                               | 310               |             | MVI         | A, ØFEH                     | SET UP A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                           |
| 0198 320018<br>019B 47                  | 311<br>312        | LOOPK:      | STA<br>MOV  | PORTA<br>B. A               | OUTPUT A VOM COUGAS POL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 1225 78<br>1226 6560                      |
| Ø19C 3AØ118                             | 313               | TIME OUI    | LDA         | PORTB                       | READ KEYBOARD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 231 DA2302                                |
| ØlAØ B7                                 | 315               | 211         | ORA         | ASWAS                       | SET THE FLAGS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 236 022302                                |
| Ø1A4 78                                 | 316<br>317        | 6.74        | JNZ         | SAVKEY<br>A.B               | LEAVE IF KEY IS DOWN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 1239 D628<br>1238 C32342                  |
| Ø1A5 Ø7                                 | 318               |             | RLC         | TOODA                       | ROTATE IT OVER ONE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                           |
| 01A9 3E00                               | VI 1320           | A COMA ?    | MVI         | A,ØØH                       | ; ZERO A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                           |
| ØLAE C9                                 | 321               |             | RET         | KEYDWN                      | ;SAVE KEY DOWN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1236 3680                                 |
| Ø1AF 23<br>Ø1BØ 2F                      | 323               | SAVKEY:     | INX         | HIW HO:                     | POINT AT RETURN LINE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 1248 BB                                   |
| Ø1B1 77                                 | 325               | 100 81 1    | MOV         | M,A                         | SAVE RETURN LINE IN MEMORY                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 243 47                                    |
| Ø1B3 70                                 | 326               |             | MOV         | M,B                         | ; POINT H AT SCAN LINE<br>:SAVE SCAN LINE IN MEMORY                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 247 3546                                  |
| Ø1B4 3E4Ø<br>Ø1B6 32EAØF                | 328               | FER -       | MVI         | A, 40H                      | SET A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 249 BB                                    |
| Ø1B9 C9                                 | 330               | 10101010    | RET         | MOAS OD;                    | ; LEAVE KEY DOWN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 24B C31102                                |
| Ø1BC 32EAØF                             | 331               | KYCHNG:     | MVI<br>STA  | A,00H                       | ZERO Ø                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                           |
| Ø1BF C38FØØ<br>Ø1C2 21F1ØF              | 333               | KADOMI»     | JMP         | BYPASS 30                   | LEAVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                           |
| Ø1C5 7E                                 | 335               | KIDOMA.     | VOM         | A,M                         | PUT SCAN LINE IN A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                           |
| Ø1C9 2B                                 | 337               |             | DCX         | PORTA                       | OUTPUT SCAN LINE TO PORT A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 253 CATEBRE                               |
| ØICD B6                                 | 338<br>339        |             | LDA<br>ORA  | FORTB                       | GET RETURN LINES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1259 FERA                                 |
| Ø1CE 2F<br>Ø1CF B7                      | 340               |             | CMA 3M      | IJ of Co.                   | INVERT A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | FESS CARSES                               |
| ØlDØ CABAØ1                             | 342               | 0           | JZ MA       | KYCHNG                      | ; IF DIFFERENT KEY HAS CHANGED                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                           |
| Ø1D6 E6Ø1                               | 343<br>344        |             | ANI         | KEYDWN<br>Ø1H               | GET KEY DOWN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 1265 CAADUS                               |
| Ø1D8 C28F00<br>Ø1DB 3AØ118              | 345<br>346        |             | JNZ         | BYPASS                      | LEAVE IF IT HAS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 125A CASEGS                               |
| Ølde Ø6FF                               | 347               | UDa         | MVI         | B, ØFFH                     | GET READY TO ZERO B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                           |
| ØIEI ØF                                 | 349               | UP:         | RRC         | AD SIAR CO                  | ROTATE A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 272 87                                    |
| Ø1E5 23                                 | 350               | ER IS PRI   | JC<br>INX   | UP 332:                     | DO IT AGAIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 275 CATTOA                                |
| ØlE6 7E<br>ØlE7 ØEFF                    | 352               | TRABUICA    | MOV         | A,M                         | GET SCAN LINES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1278 CBBFW1                               |
| ØlE9 ØC                                 | 354               | UP1:        | INR         | I CANDER SHT ETS            | START C COUNTING                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                           |
| ØlEB DAE9Ø1                             | 356               | COMMAND     | JC JC       | OLLOWING AN ESCA            | ;ROTATE A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                           |
| Ø1EF 07                                 | 357<br>358        |             | MOV         | A,B                         | GET RETURN LINES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1278 3848                                 |
| 01F0 07<br>01F1 07                      | 359<br>369        |             | RLC         | RESET                       | MOVE OVER TWICE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                           |
| 01F2 B1                                 | 361               |             | ORA         | C WHOG:                     | OR SCAN AND RETURN LINES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1283 FEA2                                 |
| 01F4 3A0218                             | 363               | NA          | LDA         | PÓRTC                       | ;SAVE A IN B<br>:GET SHIFT CONTROL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 1288 5842                                 |
| Ølf9 4F                                 | 364<br>365        |             | MOV         | 40H<br>C. A                 | ; IS CONTROL SET                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | RABA CAGREZ<br>128D FEAR                  |
| ØIFA JAEFØF<br>ØIFD 57                  | изпиоз67          | FT OF TH    | LDA         | SHOON                       | GET SHIFT CONTROL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 128F CADSII2                              |
| 01FE E640                               | 368               | AACTER<br>E | ANI         | 40H 00                      | STRIP CONTROL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1294 CA2703                               |
| 0201 CA3E02                             | 370               |             | JZ          | CNTDWN                      | ;SET BIT<br>:IF SET LEAVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | เวียง ดัดสิสตล                            |
| 0207 E620                               | 371<br>372        | HARACTER    | LDA<br>AN I | PORTC                       | READ IT AGAIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 129C FEM3                                 |
| 0209 4F<br>020A 7A                      | 373               | ARACTER     | MOV         | C, A                        | SAVE A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | IZA1 EE44                                 |
| 020B E620                               | 375               | THE LEFT    | ANI         | 20H                         | ;GET SHIFT CONTROL<br>;STRIP CONTROL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | TAG FEAS                                  |
| 020E CA4702<br>0211 58                  | 376<br>377        |             | JZ JZ       | C<br>SHDWN                  | ARE THEY THE SAME?                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                           |
| 0211 58<br>0212 1600<br>0214 210705     | 378<br>379        | SCR:        | MOV         | E,B                         | PUT TARGET IN E                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                           |
| 0214 210705<br>0217 19                  | 379<br>380<br>381 | CHARACTE    | LXI<br>DAD  | D, ØØH<br>H, KYLKUP         | GET LOOKUP TABLE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                           |
| Ø218 7£                                 | 382               | one an A    | MOV         | A.M                         | GET CHARACTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1281 FE18                                 |
| 0219 47<br>021A 3A0218                  | 383<br>384        | MOTT        | MOV<br>LDA  | B.A<br>PÓRTC                | · DUP CHADACTED TALD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                           |
| 021D E610                               | 385<br>386        |             | ANI         | 10H                         | GET PORTC<br>STRIP BIT<br>CAPS LOCK                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1287 32818F<br>128A CD3883                |
| 0222 78<br>0223 32EBØF                  | 387               | Company 200 | JZ<br>MOV   | CAPLOC<br>A, B<br>KBCHR     | CAPS LOCK<br>GET A BACK<br>SAVE CHARACTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                           |
| 0223 32EB0F<br>0226 3EC1<br>0228 32EA0F | 387<br>388<br>389 | STKEY:      | MVI         | KBCHR<br>A.ØC1H             | SAVE CHARACTER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                           |
| 0228 32EA0F<br>022B C38F00              | 390               |             | STA<br>JMP  | A, ØC1H<br>KEYDWN<br>BYPASS | SAVE KEY DOWN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | FRANKE, LUKE                              |
|                                         | 391<br>392<br>393 | J SHT 30    | B 1 - 7 3 G | 1979 PROFESSION 1975        | LEAVE N IS PUSHED THIS ROUTINE SEES IF                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1206 228566<br>1209 001504<br>1200 038691 |

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;ROUTINE ASSUMES THAT THE CHARACTER IS LOWER CASE ASCII
;AND SUBTRACTS 20H, WHICH CONVERTS THE CHARACTER TO
;UPPER CASE ASCII
  397
398
   MOV
  GET A BACK
HOW BIG IS IT?
LEAVE IF IT'S TOO SMALL
IS IT TOO BIG
LEAVE IF TOO BIG
Ø22E 78
Ø22F FE6Ø
  399
  CAPLOC:
  A,B
60H
  400
  CPI
0231 DA2302
0234 FE7B
0236 D22302
0239 D620
023B C32302
  JC
CPI
JNC
SUI
  401
  STKEY
7BH
   402 403
  STKEY
  404
  20H
STKEY
   ADJUST A
  405
406
407
  JMP
   THE ROUTINES SHOWN AND CATOWN SET BIT 6 AND 7 RESPECTIVLY
  408
   : IN THE ACC.
  409
 Ø23E 3E8Ø
  410 CNTDWN:
   A,80H
  ;SET BIT 7 IN A
;OR WITH CHARACTER
;MAKE SURE SHIFT IS NOT SET
;PUT IT BACK IN B
   MVI
0240 B0
0241 E6BF
0241 E6BF
0243 47
0244 C31102
0247 3E40
0249 B0
  ORA
  ØBFH
  B.A
SCR
  414
   GO BACK
SET BIT 6 IN A
OR WITH CHARACTER
   JMP
   415 SHDWN:
416
417
418
   A, 40H
  MVI
   B
  ORA
 024A 47
024B C31102
   B.A
SCR
   MOV
   PUT IT BACK IN B
  JMP
   GO BACK
  419
  ; THIS ROUTINE CHECKS FOR ESCAPE CHARACTERS, LF, CR, ; FF, AND BACK SPACE
  420
   ; ESCAPE SET?
; SEE IF IT IS
; LEAVE IF IT IS
; GET CHARACTER
; LINE FEED
; C) TO LINE FEED
; FORM FEED
 Ø24E 3AEEØF
  423 CHREC:
   LDA
024E 3AEEØF

0251 FE8Ø

0253 CA7BØ2

0256 3AE7ØF

0259 FEØA

025E CAF6Ø3

026E FEØC

026Ø CACAØ3

0263 FEØD

0265 CAADØ3

0268 FEØS

0268 FEØS

0268 CA6EØ3

0269 FEJB

0265 CAABØ3
  ESCP
  CPI
   8ØH
ESSO
USCHR
  424
425
426
427
428
429
430
431
432
433
434
435
436
437
  LDA
  ØAH
LNFD
  JZ
CPI
   ØCH
FMFD
   GO TO FORM FEED
CR
DO A CR
BACK SPACE
DO A BACK SPACE
  JZ
CPI
   ØDH
CGRT
  JZ
CPI
  Ø8H
LEFT
1BH
  JZ
CPI
   ESCAPE
DO AN ESCAPE
CLEAR CARRY
 026F CAA503
0272 B7
   JZ
  ESKAP
   ORA
  A
 0273 C6E0
0275 DA7704
0278 C30F01
  438
  ADI
  ØEØH
  ;SEE IF CHARACTER IS PRINTABLE
;IF PRINTABLE DO IT
;GO BACK AND READ USART AGAIN
  439
440
441
442
443
  CHRPUT
   JMP
   THIS ROUTINE RESETS THE ESCAPE LOCATION AND DECODES THE CHARACTERS FOLLOWING AN ESCAPE. THE COMMANDS ARE COMPATABLE WITH INTELS CREDIT TEXT EDITOR
  444
0278 3E00
027D 32EE0F
0280 3AE70F
  446 ESSQ:
447
448
   A, ØØH
ESCP
USCHR
   ;ZERO A
;RESET ESCP
;GET CHARACTER
;DOWN
   STA
   LDA
 Ø283 FE42
  449
  JOWN

MOVE CURSOR DOWN

CLEAR SCREEN CHARACTER

CLEAR THE SCREEN

CLEAR THE SCREEN

CLEAR THE REST OF SCREEN

CLEAR THE REST OF THE SCREEN

CLEAR LINE CHARACTER

GO CLEAR A LINE

CURSOR UP CHARACTER

MOVE CURSOR UP

CURSOR TO THE RIGHT

CURSOR RIGHT CHARACTER

MOVE CURSOR TO THE RIGHT

CURSOR LEFT CHARACTER

MOVE CURSOR TO THE LEFT

HOME CURSOR TO THE LEFT

HOME THE CURSOR

LEAVE
  CPI
  42H
0283 FE42
0285 CAAE02
0288 FE45
028A CACF02
028D FE4A
028F CADE02
  450
451
452
453
454
455
456
457
458
460
461
   DOWN
45H
CLEAR
  CPI
   CPI
  4AH
  JZ
  CLRST
028F CAD502
0292 FE4B
0294 CA2703
0297 FE41
0299 CA3303
029C FE43
029E CA4503
02A1 FE44
02A3 CA6E03
02A6 FE48
   4BH
CLRLIN
41H
  JZ
CPI
  JZ
CPI
JZ
CPI
   UPCUR
43H
RIGHT
   44H
LEFT
  462
463
464
465
466
467
  JZ
CPI
  48H
 02A8 CA9703
  HOME
  02AB C30F01
  JMP
   SETUP
   THIS ROUTINE MOVES THE CURSOR DOWN ONE CHARACTER LINE
  468
   ;PUT CURSOR Y IN A
;SEE IF ON BOTTOM OF SCREEN
;LEAVE IF ON BOTTOM
;INCREMENT Y CURSOR
;SAVE NEW CURSOR
;LOAD THE CURSOR
;CALCULATE ADDRESS
;GET FIRST LOCATION OF THE LINE
;SEE IF CLEAR SCREEN CHARACTER
;LEAVE IF IT IS NOT
;SAVE BEGINNING OF THE LINE
;CLEAR THE LINE
;LEAVE
 Ø2AE 3AE1ØF
  469 DOWN:
   LDA
   CURSY
 02B1 FE18
02B3 CA0F01
  CPI
   CURBOT
  471
  JZ
  SETUP
INR
STA
CALL
CALL
MOV
CPI
JNZ
  472
473
474
475
476
477
478
479
480
   ACURSY
  LDCUR
   CALCU
   A,M
ØFØH
   SETUP
LOC80
CLLINE
  SHLD
   JMP
  SETUP
  482
   BI CHA HAY
```

|                                                                                                                                             | 483                                                                 | THIS ROUTINE CLEARS                                                                      | THE SCREEN.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | TOCRAE SIZER                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 02CF CDE403<br>02D2 C30F01                                                                                                                  | 484<br>485 CLEAR:<br>486                                            | CALL CLSCR<br>JMP SETUP                                                                  | GO CLEAR THE SCREEN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | MATE CARDOS                                                                         |
|                                                                                                                                             | 487<br>488<br>489                                                   | THIS ROUTINE CLEARS A                                                                    | ALL LINES BENEATH THE LOCATION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                     |
| 02D5 CDA504<br>02D8 CDCD04<br>02DB 01204F                                                                                                   | 490<br>491 CLRST:<br>492<br>493                                     | CALL CALCU<br>CALL ADX<br>LXI B,4F20H                                                    | ;CALCULATE ADDRESS<br>;ADD X POSITION<br>:PUT SPACE AND LAST X IN B AND C                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 937F 32E10E<br>9382 3EAF<br>9384 32E20F                                             |
| 02DE 3AE20F<br>02E1 B8<br>02E2 CAEC02<br>02E5 3C<br>02E6 23<br>02E7 71                                                                      | 494<br>495<br>496<br>497 LLP:<br>498<br>499                         | LDA CURSX CMP B JZ OVR1 INR A INX H MOV M,C                                              | GET X CURSOR SEE IF AT END OF LINE LEAVE IF X IS AT END OF LINE MOVE A OVER ONE X POSITION INCREMENT MEMORY POINTER PUT A SPACE IN MEMORY                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 8386 C308601<br>8391 CD8603<br>8391 CD8603<br>8394 C308601                          |
| 02E9 B8<br>02E9 C2E502<br>02EC 01D00F<br>02EF 23<br>02F0 78<br>02F1 BC<br>02F2 C2FD02                                                       | 500<br>501<br>502 OVR1:<br>503<br>504<br>505<br>506                 | CMP B JNZ LLP LXI B, LAST INX H MOV A, B CMP H JNZ CONCL                                 | SEE IF A = 4FH ; IF NOT LOOP AGAIN ; PUT LAST LINE IN BC ; POINT HL TO LAST LINE ; GET B ; SAME AS H? ; LEAVE IF NOT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0397 3880F<br>0390 33820F<br>0390 33910F<br>0398 COBBRS                             |
| 02F6 BD<br>02F7 C2FD02<br>02FA 210008<br>02FD 3AE10F<br>0300 FE18<br>0302 CA0F01                                                            | 507<br>508<br>509<br>510<br>511 CONCL:<br>512<br>513                | MOV A,C CMP L JNZ CONCL LXI H,TPDIS LDA CURSY CPI CURBOT JZ SETUP                        | GET C SAME AS L? LEAVE IF NOT GET TOP OF DISPLAY GET Y CURSOR IS IT ON THE BOTTOM LEAVE IF IT IS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                     |
| 0306 47<br>0307 115000<br>030A 36F0<br>030C 78<br>030D FE18<br>030F CA0F01<br>0312 3C                                                       | 515<br>516<br>517 CLOOP:<br>518<br>519 2VS8 0<br>520<br>521         | MOV B, A LXI D, LNGTH MVI M, ØFØH MOV A, B CPI CURBOT JZ SETUP INR A                     | ; SAVE IT DOWN ONE LINE; SAVE CURSOR IN B FOR LATER; PUT LENGTH OF ONE LINE IN D; PUT EOR IN MEMORY; GET CURSOR; ARE WE ON THE BOTTOM; LEAVE IF WE ARE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                     |
| 0313 19<br>0314 47<br>0315 7C<br>0316 FEØF<br>0318 C20A03<br>031B 7D<br>031C FEDØ<br>031C FEDØ<br>031E C20A03<br>0321 210008<br>0324 C30A03 | 522<br>523<br>524<br>525<br>525<br>527<br>528<br>528<br>5230<br>531 | DAD D MOV B,A MOV A,H CPI ØFH JNZ CLOOP MOV A,L CPI ØDØH JNZ CLOOP LXI H,TPDIS JMP CLOOP | GO CLEAR THE SCREEN  GO CLEAR THE SCREEN  GO BACK  ALL LINES BENEATH THE LOCATION  CALCULATE ADDRESS  ADD X POSITION  PUT SPACE AND LAST X IN B AND C  GET X CURSOR  SEE IF AT END OF LINE  LEAVE IF X IS AT END OF LINE  MOVE A OVER ONE X POSITION  INCREMENT MEMORY POINTER  PUT A SPACE IN MEMORY  SEE IF A = 4FH  IF NOT LOOP AGAIN  PUT LAST LINE IN BC  POINT HL TO LAST LINE  GET B  SAME AS H?  LEAVE IF NOT  GET C  SAME AS L?  LEAVE IF NOT  GET TOP OF DISPLAY  GET Y CURSOR  IS IT ON THE BOTTOM  LEAVE IF IT IS  MOVE IT DOWN ONE LINE  SAVE CURSOR IN B FOR LATER  PUT LENGTH OF ONE LINE IN D  PUT EOR IN MEMORY  GET CURSOR Y  ARE WE ON THE BOTTOM  LEAVE IF WE ARE  MOVE CURSOR DOWN ONE  GET NEXT LINE  SAVE A  PUT H IN A  COMPARE TO HIGH LAST  LEAVE IF IT S NOT  PUT LIN A  COMPARE TO LOW LAST  LEAVE IF IT S NOT  PUT TOP DISPLAY IN H AND L  CALCULATE ADDRESS  STORE H AND L TO CLEAR LINE | 8388 3280<br>8380 328207<br>8300 328016<br>8303 34816<br>8305 32816<br>8305 028616  |
|                                                                                                                                             | 533<br>534                                                          | THIS ROUTINE CLEARS                                                                      | THE LINE THE CURSOR IS ON.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                     |
| 0327 CDA504<br>032A 22E50F<br>032D CD1504<br>0330 C30F01                                                                                    | 535 CLRLIN:<br>536<br>537<br>538                                    | CALL CALCU SHLD LOC80 CALL CLLINE JMP SETUP                                              | CALCULATE ADDRESS STORE H AND L TO CLEAR LINE CLEAR THE LINE GO BACK                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | ### ### ##############################                                              |
|                                                                                                                                             | 539<br>540                                                          | THIS ROUTINE MOVES TO                                                                    | HE CURSOR UP ONE LINE.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 6308 32019P                                                                         |
| 0333 3AE10F<br>0336 FE00<br>0338 CA0F01<br>033B 3D<br>033C 32E10F<br>033F CDB803<br>0342 C30F01                                             | 542 UPCUR:<br>543<br>544<br>545<br>546<br>547                       | LDA CURSY CPI ØØH JZ SETUP DCR A STA CURSY CALL LDCU                                     | ;LOOP AGAIN THE LINE THE CURSOR IS ON. ;CALCULATE ADDRESS ;STORE H AND L TO CLEAR LINE ;CLEAR THE LINE ;GO BACK HE CURSOR UP ONE LINE. ;GET Y CURSOR ;IS IT ZERO ;IF IT IS LEAVE ;MOVE CURSOR UP ;SAVE NEW CURSOR ;LOAD THE CURSOR ;LEAVE HE CURSOR ONE LOCATION TO THE RIGHT ;GET X CURSOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 03E4 3EF6                                                                           |
|                                                                                                                                             | 549<br>550                                                          | THIS ROUTINE MOVES TO                                                                    | HE CURSOR ONE LOCATION TO THE PICHT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                     |
| 034A C26403<br>034D 3AE10F<br>0350 FE18<br>0352 CA5903<br>0355 3C<br>0356 32E10F                                                            | 554<br>555<br>555<br>556<br>557<br>558<br>559                       | JNZ NTOVER LDA CURSY CPI CURBOT JZ GD18                                                  | ;IS IT ALL THE WAY OVER? ;IF NOT JUMP AROUND ;GET Y CURSOR ;SEE IF ON BOTTOM ;IF WE ARE JUMP ;INCREMENT Y CURSOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 03EC 115000<br>03EC 115000<br>03EC 19<br>03E 0 19<br>03E 0 02EF 03<br>03E 0 02EF 03 |
| 0359 3E00<br>035B 32E20F<br>035E CDB803<br>0361 C30F01<br>0364 3C<br>0365 32E20F                                                            | 560 GD18:<br>561<br>562<br>563<br>564 NTOVER:<br>565                | MVI A,00H<br>STA CURSX<br>CALL LICUR<br>JMP SETUP<br>INR A<br>STA CURSX                  | ; ZERO A ; ZERO X CURSOR ; LOAD THE CURSOR ; LEAVE ; INCREMENT X CURSOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | GERG CORCHE                                                                         |
| 0368 CDB803<br>036B C30F01                                                                                                                  | 566<br>567<br>568                                                   | JMP SETUP                                                                                | ;LOAD THE CURSOR<br>;LEAVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | GARR PEIS                                                                           |
|                                                                                                                                             | 569                                                                 | THIS ROUTINE MOVES TO                                                                    | HE CURSOR LEFT ONE CHARACTER POSITIO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | MARS 32818ING                                                                       |

| 0373 C28D03 573<br>0376 3AE10F 574<br>0379 FE00 575<br>0378 CA0F01 576                                                                          | JNZ<br>LDA<br>CPI<br>JZ                                               | NOVER<br>CURSY<br>ØØH<br>SETUP                                                           | ;IS IT ALL THE WAY OVER ;IF NOT JUMP AROUND ;GET CURSOR Y ;IS IT ZERO? ;IF IT IS JUMP                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 2F CDE463<br>02 C30F81                                            |
|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 037F 32E10F 578<br>0382 3E4F 579<br>0384 32E20F 580<br>0387 CD8803 581<br>038A C30F01 582                                                       | STA<br>MVI<br>STA<br>CALI                                             | CURSY A,4FH CURSX L LDCUR SETUP                                                          | SAVE IT<br>GET LAST X LOCATION<br>SAVE IT<br>LOAD THE CURSOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | DS CDRS64<br>DB CDCD64<br>DB 61264F<br>DC 3AE26F                  |
| 038D 3D 583 N<br>038E 32E20F 584<br>0391 CDB803 585<br>0394 C30F01 586                                                                          | NOVER: DCR<br>STA<br>CALI<br>JMP                                      | A CURSX<br>L LDCUR<br>SETUP                                                              | ;ADJUST X CURSOR<br>;SAVE CURSOR X<br>;LOAD THE CURSOR<br>;LEAVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 62 588062<br>85 3C<br>86 23<br>87 71                              |
| 588<br>589                                                                                                                                      | TH                                                                    | IS ROUTINE HOMES THE                                                                     | CURSOR.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                   |
| Ø397     3EØØ     59Ø 8       Ø399     32E2ØF     591       Ø39C     32E1ØF     592       Ø39F     CDB8Ø3     593       Ø3A2     C3ØFØ1     594 | HOME: MVI<br>STA<br>STA<br>CALI<br>JMP                                | A,00H<br>CURSX<br>CURSY<br>LUCUR<br>SETUP                                                | ZERO A<br>ZERO X CURSOR<br>ZERO Y CURSOR<br>LOAD THE CURSOR<br>LEAVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                   |
| 595<br>596                                                                                                                                      | TH                                                                    | IS ROUTINE SETS THE                                                                      | ESCAPE BIT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | čá šá<br>carpas                                                   |
| ### ### ### ### ### ### ### ### ### ##                                                                                                          | ESKAP: MVI<br>STA<br>JMP                                              | A,80H<br>ESCP<br>SETUP                                                                   | ;LOAD A WITH ESCAPE BIT<br>;SET ESCAPE LOCATION<br>;GO BACK AND READ USART                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | PA 219896<br>PD 3AE19F<br>80 FE18<br>RZ CASPBI                    |
| 602<br>603                                                                                                                                      | TH                                                                    | IS ROUTINE DOES A CR                                                                     | A HON EIG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 86 47<br>80 47                                                    |
| 03AD 3E00 604 0<br>03AF 32E20F 605<br>03B2 CD8803 606<br>03B5 C30F01 607                                                                        | CGRT: MVI<br>STA<br>CALI<br>JMP                                       | A,00H<br>CURSX<br>LDCUR<br>SETUP                                                         | ;ZERO A<br>;ZERO CURSOR X<br>;LOAD CURSOR INTO 8275<br>;POLL USART AGAIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | GA 3RFB<br>GC 78<br>GD FE18<br>GF CASFGI                          |
| 609<br>610                                                                                                                                      | TH                                                                    | IS ROUTINE LOADS THE                                                                     | CURSOR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                   |
| 03B8 3E80 511 1<br>03BA 320110 612<br>03BD 3AE20F 613<br>03C0 320010 614<br>03C3 3AE10F 615<br>03C6 320010 616<br>03C9 C9 617                   | LDCUR: MVI<br>STA<br>LDA<br>STA<br>LDA<br>STA<br>RET                  | A,80H<br>CRTS<br>CURSX<br>CRTM<br>CURSY<br>CRTM                                          | ;PUT 80H INTO A<br>;LOAD CURSOR INTO 8275<br>;GET CURSOR X<br>;PUT IT IN 8275<br>;GET CURSOR Y<br>;PUT IT IN 8275                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 15 7C<br>16 FE3F<br>18 C20A93<br>16 TD<br>11 C20A93<br>21 21 8898 |
| 619<br>629                                                                                                                                      | TH                                                                    | IS ROUTINE DOES A FO                                                                     | RM FEED                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                   |
| ### ### ### ### ### ### ### ### ### ##                                                                                                          | FMFD: CALI<br>LXI<br>SHLI<br>CALI<br>MVI<br>STA<br>STA<br>CALI<br>JMP | L CLSCR<br>H, TPDIS<br>D LOCSØ<br>CLLINE<br>A, ØØH<br>CURSX<br>CURSY<br>L LDCUR<br>SETUP | ; IS IT ALL THE WAY OVER ; IF NOT JUMP AROUND ; GET CURSOR Y ; IS IT ZERO? ; IF IT IS JUMP ; MOVE CURSOR Y UP ; SAVE IT ; GET LAST X LOCATION ; SAVE IT ; LOAD THE CURSOR ; ADJUST X CURSOR ; SAVE CURSOR ; LEAVE ; CURSOR. ; ZERO A ; ZERO X CURSOR ; ZERO Y CURSOR ; LEAVE ; CURSOR ; LEAVE  ESCAPE BIT ; LOAD A WITH ESCAPE BIT ; SET ESCAPE LOCATION ; GO BACK AND READ USART  ; ZERO A ; ZERO CURSOR X ; LOAD CURSOR INTO 8275 ; POLL USART AGAIN  CURSOR ; PUT 80H INTO A ; LOAD CURSOR Y ; PUT IT IN 8275 ; GET CURSOR Y ; PUT IT IN 8275 ; GET CURSOR Y ; PUT IT IN 8275  RM FEED  ; CALL CLEAR SCREEN ; PUT TOP DISPLAY IN HL ; PUT IT IN LOCAD ; CLEAR TOP LINE ; ZERO A ; ZERO CURSOR Y ; LOAD THE CURSOR ; BACK TO USART  E SCREEN BY WRITING END OF ROW RST LOCATION OF ALL LINES ON  ; PUT EOR CHARACTER IN A ; LOAD B MITH MAX Y ; COAD B MITH MAX Y ; GO TO MAX PLUS ONE ; LOAD B MITH MAX Y ; GO TO MAX PLUS ONE ; LOAD B MITH MAX Y ; CHANGE POINTER BY 80D ; COUNT THE LOOPS ; CONTINUE IF NOT ZERO ; GO BACK | 27 CDASGE<br>2A 22ESGE<br>2D CD15GA<br>3G CSEEGI                  |
| 630<br>631<br>632<br>633                                                                                                                        | THI                                                                   | IS ROUTINE CLEARS TH<br>ARACTERS INTO THE FI<br>E SCREEN.                                | E SCREEN BY WRITING END OF ROW<br>RST LOCATION OF ALL LINES ON                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 36 FERR<br>38 CARFEI -<br>38 3D                                   |
| 03E4 3EFØ 635 0<br>03E6 0618 636<br>03E8 04 637<br>03E9 210008 638                                                                              | CLSCR: MVI<br>MVI<br>INR                                              | A, 0F0H<br>B, CURBOT<br>B                                                                | ;PUT EOR CHARACTER IN A<br>;LOAD B WITH MAX Y<br>;GO TO MAX PLUS ONE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 3F CD8863                                                         |
| 03EC 115000 639<br>03EF 77 640 1<br>03F0 19 641<br>03F1 05 642<br>03F2 C2EF03 643<br>03F5 C9 644                                                | LXI<br>LOADX: MOV<br>DAD<br>DCR<br>JNZ<br>RET                         | D, INGTH<br>M, A<br>D<br>B<br>LOADX                                                      | MOVE 50H = 80D INTO D AND E MOVE EOR INTO MEMORY COUNT THE LOOPS COUNT THE LOOPS CONTINUE IF NOT ZERO GO BACK                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 145 3AE268<br>148 FEAF<br>141 3AE188<br>141 3AE188<br>152 CA5983  |
| 645<br>646<br>647                                                                                                                               | TH                                                                    | IS ROUTINE DOES A LI                                                                     | NE FEED                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                   |
| Ø3F6 CDFCØ3 648 I<br>Ø3F9 C3ØFØ1 649<br>65Ø                                                                                                     | JMP                                                                   |                                                                                          | ;CALL ROUTINE<br>;POLL FLAGS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                   |
| 651<br>652                                                                                                                                      | LIN                                                                   | NE FEED                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | isi caarai                                                        |
|                                                                                                                                                 | LNFD1: LDA<br>CPI<br>JZ<br>INR<br>STA                                 | CURSY<br>CURBOT<br>ONBOT<br>A<br>CURSY                                                   | GET Y LOCATION OF CURSOR<br>SEE IF AT BOTTOM OF SCREEN<br>IF WE ARE, LEAVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                   |

| Ø414 C9                                                                                                                                                          | 662<br>663<br>664<br>665<br>666                                                                             | RET<br>THIS ROUTINE C<br>IS IN LOCAD. F<br>CLEAR THE LINE                                                           | LEARS THE LINE WHO                                                                                                   | SE FIRST ADDRESS<br>RE USED TO RAPIDLY                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0415 F3<br>0416 2AE50F<br>0419 115000<br>041C 19<br>041D EB<br>041E 210000<br>0421 39<br>0422 EB<br>0423 F9<br>0424 212020                                       | 668 CLLINE: 669 670 671 672 673 674 675 676                                                                 | DI LHLD LOC80 LXI D, LNGTH DAD D XCHG LXI H,0000H DAD SP XCHG SPHL LXI H,2020H                                      | ;NO INTER ;GET LOC8; H ;GET OFFS ;ADD OFFS ;PUT STAR; ZERO HL ;GET STAC; ;PUT STAC; ;PUT STAC; ;PUT STAC; ;PUT STAC; | SE FIRST ADDRESS RE USED TO RAPIDLY RUPTS HERE  OF ET T IN DE K K IN DE T IN SP ES IN HL LEAR THE LINE                                                                          | 0478 PERG<br>0470 2255GF<br>0480 COLSGA<br>0480 COLSGA<br>0480 3457GF<br>0480 3457GF<br>0480 3462GF<br>0460 3462GF                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                                                                                                                                                                  | 679<br>68Ø                                                                                                  | NOW DO 40 PUSH                                                                                                      | INSTRUCTIONS TO C                                                                                                    | LEAR THE LINE                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 0427 E5<br>0428 E5<br>0429 E5                                                                                                                                    | 681<br>682<br>683<br>684+<br>685+<br>686+<br>687+                                                           | ENUM<br>DUCH H                                                                                                      |                                                                                                                      | 779 382                                                                                                                                                                         | 849C SEESE<br>849C COBESS<br>848C COBESS<br>8482 CSSFSI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 042A E5<br>042B E5                                                                                                                                               | 687+<br>688+                                                                                                | PUSH H<br>PUSH H                                                                                                    | THE CURSOR IS ON. 1                                                                                                  | 174 THAT                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 042C E5<br>042D E5<br>042F E5<br>0431 E5<br>0431 E5<br>0432 E5<br>0434 E5<br>0434 E5<br>0436 E5<br>0437 E5<br>0437 E5<br>0438 E5<br>0438 E5<br>0438 E5           | 689+ 690+ 691+ 692+ 693+ 694+ 695+ 696+ 697+ 698+ 698+ 770+ 770+ 770+ 7705+                                 | PUSH H            | B, EMTAB<br>CÜRSY<br>C, A<br>C, A<br>B, A<br>C, A<br>H, A<br>A, A<br>B, A<br>B, A<br>B, A<br>B, A                    | 777 CARCUS LIXE 778 PR.C. 780 PR.C. 781 PR.C. 782 PR.C. 783 PR.C. 785 PR.C. 787 PR.C. 787 PR.C. 788 PR.C. | ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 210504  ### 21 |
| 043D E5<br>043E E5<br>043F E5<br>044W E5<br>0441 E5<br>0442 E5<br>0443 E5<br>0444 E5<br>0446 E5<br>0447 E5                                                       | 707+<br>708+<br>709+<br>710+<br>711+                                                                        | PUSH H<br>PUSH H          | TOPAD H, GF0308 FIX B, GF8308 D H, GF8308                                                                            | 793 XCNG<br>794 LAT<br>795 DAD<br>796 JC<br>797 XCNG                                                                                                                            | 6495 86<br>64402 19<br>64402 19<br>64405 88<br>64405 88<br>64405 21368<br>64406 19<br>6400 09                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 0445 E5<br>0446 E5<br>0447 E5<br>0448 E5<br>0449 E5<br>044B E5<br>044B E5<br>044C E5<br>044C E5<br>044C E5<br>044F E5<br>044F E5<br>0451 F8                      | 7174<br>7194<br>7194<br>7204<br>7214<br>7224<br>7234<br>724<br>725<br>726<br>727<br>728                     | PUSH H PUSH H PUSH H PUSH H PUSH H PUSH H XCHG SPHL EI RET                                                          | ;PUT STAC<br>;PUT IT B<br>;ENABLE II<br>;GO BACK                                                                     | K IN HL ACK IN SP WITERRUPTS  E SCREEN THIS ROUTIN                                                                                                                              | 64CD 3NS28F<br>64D2 64G6<br>64D2 4F<br>64D2 99<br>64D4 C9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                                                                                                                                                                  | 729<br>730                                                                                                  | IF CURSOR IS C                                                                                                      | ON THE BOTTOM OF THE<br>PLEMENT THE LINE FE                                                                          | E SCREEN THIS ROUTIN                                                                                                                                                            | IE GDDB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 0453 2AE30F<br>0456 22E50F<br>0459 115000<br>045C 19<br>045D 01D00F<br>0461 B8<br>0462 C26D04<br>0465 7D<br>0466 B9<br>0467 C26D04<br>0465 210008<br>0460 22E30F | 731<br>732<br>733<br>734<br>735<br>736<br>737<br>738<br>739<br>740<br>741<br>741<br>742<br>743<br>744 ARND: | LHLD TOPAD SHLD LOC80 LXI D, LNGTH DAD D LXI B, LAST MOV A, H CMP B JNZ ARND MOV A, L CMP C C JNZ ARND LXI H, TPDIS | ;GET TOP / ;SAVE IT / ;LINE LEN / ;ADD HL + ;GET BOTT / ;GET H / ;SAME AS   ;LEAVE IF / ;GET L / ;SAME AS            | ADDRESS IN LOC80 SITH DE OM LINE B NOT SAME C NOT SAME                                                                                                                          | 6415 0088 6637 6637 6637 6637 66415 66415 66415 66415 66415 66415                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

```
745
746
747
748
749
0470 CD1504
0473 CD8803
0476 C9
  CALL
CALL
RET
  CLEAR LINE
   LOAD THE CURSOR
   LDCUR
   THIS ROUTINE PUTS A CHARACTER ON THE SCREEN AND INCREMENTS THE X CURSOR POSITION. A LINE FEED IS INSERTED IF THE INCREMENTED CURSOR EQUALS 81D
  749
759
751
752
753
754
755
755
756
757
758
760
761
761
763
763
764
765
766
   ;CALCULATE SCREEN POSITION
;GET FIRST CHARACTER
;IS IT A CLEAR LINE
;SAVE LINE TO CLEAR
;CLEAR LINE
;GET LINE
;ADD CURSOR X
;GET CHARACTER
;PUT IT ON SCREEN
;GET CURSOR X
;INCREMENT CURSOR X
;HAS IT GONE TOO FAR?
;IF NOT GOOD
;DO A LINE FEED
;DO A CURSOR
0477 CDA504
047A 7E
  CHRPUT: CALL
   CALCU
  MOV
CPI
SHLD
CZ
  A,M
ØFØH
LOC8Ø
CLLINE
LOC8Ø
047B FEF0
047D 22E5
047B FEFØ
047D 22E5ØF
048Ø CC15Ø4
048Ø CD50Ø4
0489 3AE5ØF
0486 CDCDØ4
0489 3AE7ØF
048C 77
048D 3AE2ØF
0491 FE5Ø
0491 FE5Ø
0493 C29CØ4
0496 CDFCØ3
0499 C3ADØ3
   LHLD
   ADX
USC IR
   LDA
   MOV
   M, A
CURSX
   LDA
  CPI
JNZ
CALL
JMP
  LNGTH
   OK1
LNFD1
CGRT
   766
767
  767
768 OK1:
769
770
771
772
773
774
775
049C 32E20F
049F CD8803
04A2 C30F01
  SAVE CURSOR
LOAD THE CURSOR
   STA
   CURSX
   JMP
   SETUP
   LEAVE
   THIS ROUTINE TAKES THE TOP ADDRESS AND THE Y CURSOR LOCATION AND CALCULATES THE ADDRESS OF THE LINE THAT THE CURSOR IS ON. THE RESULT IS RETURNED IN H AND L AND ALL REGISTERS ARE USED.
   776
7777
778
779
781
782
783
784
785
787
787
787
799
7991
7993
7994
7796
7796
7797
04A5 21D504
04A8 3AE10F
04AB 07
04AC 0600
04AE 4F
  CALCU:
   H, LINTAB
CURSY
   GET LINE TABLE INTO H AND L
GET CURSOR INTO A
SET UP A FOR LOOKUP TABLE
   LDA
   GET CURSUR INTO A
SET UP A FOR LOOKUP TABLE
ZERO B
PUT CURSOR INTO A
ADD LINE TABLE TO Y CURSOR
PUT LOW LINE TABLE INTO A
PUT LOW LINE TABLE INTO C
CHANGE MEMORY POINTER
PUT HIGH LINE TABLE INTO B
TWOS COMPLEMENT SCREEN LOCATION
SUBTRACT OFFSET
SAVE HL IN DE
GET TOP ADDRESS IN H AND L
GET DISPLACED ADDRESS
SAVE IT IN D
TWOS COMPLEMENT SCREEN LOCATION
SEE IF WE ARE OFF THE SCREEN
IF WE ARE FIX IT
GET DISPLACED ADDRESS BACK
GO BACK
SCREEN BOUNDRY
  B,00H
C,A
B
   MVI
   MOV
DAD
MOV
MOV
04AE 4F
04AF 09
04B0 7E
04B1 4F
04B2 23
04B3 7E
04B4 47
04B5 2100F8
04B8 09
   A,M
C,A
H
   INX
   A,M
B,A
H,ØF8ØØH
  MOV
LXI
DAD
XCHG
LHLD
DAD
   B
 Ø4B9
Ø4BA
Ø4BD
                EB
2AE3ØF
19
   TOPAD
04BD 19
04BE EB
04BF 2130F0
04C2 19
04C3 DAC804
04C6 EB
04C7 C9
   XCHG
LXI
DAD
   H, ØFØ3ØH
   JC
XCHG
   FIX
04C7 C9
04C8 2130F8
04CB 19
04CC C9
  798
   RET
  799 FIX:
   LXI
  SCREEN BOUNDRY
   H, ØF83ØH
  800
801
802
   RET
  GO BACK
  803
804
805
   THIS ROUTINE ADDS THE X CURSOR LOCATION TO THE ADDRESS THAT IS IN THE H AND L REGISTERS AND RETURNS THE RESULT; IN H AND L
04CD 3AE20F
04D0 0600
  8Ø7
8Ø8
  CURSX
B,00H
C,A
B
  ADX:
  LDA
  GET CURSOR
   MVI
Ø4D2
Ø4D3
Ø4D4
                4F
  809
810
811
812
813
814
   MOV
  PUT CURSOR X IN C
ADD CURSOR X TO H AND L
LEAVE
  RET
   THIS TABLE CONTAINS THE OFFSET ADDRESSES FOR EACH OF THE 25 DISPLAYED LINES.
   814 ; OF THE 25 DISPLAYED LINES.
815
816 LINTAB: LINNUM SET 0
817
818 DW TPDIS+(LNGTH*LINNUM)
819 LINNUM SET (LINNUM+1)
820 ENDM
821+ DW TPDIS+(LNGTH*LINNUM)
821+ LINNUM TPDIS+(LNGTH*LINNUM)
821+ LINNUM TPDIS+(LNGTH*LINNUM)
agaa
Ø4D5 ØØØ8
  DW TPDIS+(LNGTH*LINNUM)
LINNUM SET (LINNUM+1)
0001
  822+
   LINNUM SET (LINNUM+1)
DW TPDIS+(LNGTH*LINNUM)
LINNUM SET (LINNUM+1)
DW TPDIS+(LNGTH*LINNUM)
LINNUM SET (LINNUM+1)
DW TPDIS+(LNGTH*LINNUM)
LINNUM SET (LINNUM+1)
DW TPDIS+(LNGTH*LINNUM)
LINNUM SET (LINNUM+1)
DW TPDIS+(LNGTH*LINNUM)
  823+
824+
825+
826+
827+
Ø4D7 5008
0002
Ø4D9 AØØ8
agas
04DB F008
0004
   828+
829+
83Ø+
Ø4DD 4009
0005
Ø4DF 9009
  831+
```

|                                                                | and the second control of the second con- |              |                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                     |            |                    |
|----------------------------------------------------------------|-------------------------------------------|--------------|----------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------|--------------------|
| 0006<br>0451 F000                                              | 832+                                      |              | SET (LINNUM+1)                                                                                           | 798,898                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                     |            |                    |
| 04E1 E009<br>0007                                              | 834+                                      | LINNUM       | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)                                                                        | 86日。29日                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                     |            |                    |
| 04E3 300A<br>0008<br>04E5 800A                                 | 836+                                      | DW<br>LINNUM | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)                                                                        | HAA HAA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                     |            |                    |
| 0009                                                           | 837+<br>838+<br>839+                      | DW<br>LINNUM | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)<br>TPDIS+(LNGTH*LI                                                     | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     |            |                    |
| 04E7 D00A<br>000A<br>04E9 200B                                 | 840+ 32A0                                 | LINNUM       | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)<br>TPDIS+(LNGTH*LI                                                     | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     |            |                    |
| ØØØB                                                           | 841+<br>842+                              | LINNUM       | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)<br>TPDIS+(LNGTH*LI                                                     | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 80.                 |            |                    |
| 04EB 700B<br>000C                                              | 844+                                      | LINNUM       | SET (LINNUM+1)                                                                                           | MEN JREE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                     |            |                    |
| 04ED C00B<br>000D                                              | 846+                                      | DW<br>LINNUM | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)                                                                        | LIBOR TO THE PARTY OF THE PARTY | 80                  |            |                    |
| 04EF 100C<br>000E                                              | 848+                                      | LINNUM       | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                     |            |                    |
| 04F1 600C<br>000F                                              | 85Ø+                                      | LINNUM       | SET (LINNUM+1)                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 80                  |            |                    |
| 04F3 B00C<br>0010                                              | 851+<br>852+                              | LINNUM       | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)<br>TPDIS+(LNGTH*LI                                                     | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     |            |                    |
| 04F5 000D<br>0011                                              | 853+<br>854+                              | LINNUM       | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)<br>TPDIS+(LNGTH*LI                                                     | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     |            |                    |
| 04F7 500D<br>0012                                              | 855+                                      | LINNUM       | SET (LINNUM+1)                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                     |            | STATE OF           |
| 04F9 A00D                                                      | 857+<br>858+                              | DW           | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 80                  |            |                    |
| 04FB F00D                                                      | 850+                                      | LINNUM       | TPDIS+(LNGTH*LI                                                                                          | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     |            |                    |
| 04FD 400E<br>0015                                              | 852+                                      | DW<br>LINNUM | SET (LINNUM+1)<br>TPDIS+(LNGTH*LI<br>SET (LINNUM+1)                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                     | \$40       |                    |
| 04FF 900E<br>0016                                              | 864+                                      | LINNUM       | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)                                                                        | HOA RPP                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                     |            |                    |
| 0501 E00E<br>0017                                              |                                           | DW<br>LINNUM | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)<br>TPDIS+(LNGTH*LI                                                     | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     |            |                    |
| 0503 300F<br>0018                                              | 867+<br>868+                              | DW<br>LINNUM | TPDIS+(LNGTH*LI<br>SET (LINNUM+1)<br>TPDIS+(LNGTH*LI                                                     | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     |            | dg 8558            |
| 0505 800F<br>0019                                              | 869+<br>87Ø+<br>871                       | LINNUM       |                                                                                                          | NNUM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     |            |                    |
|                                                                | 872<br>873<br>874<br>875<br>876<br>877    | THIS THAT A  | ARD LOOKUP TABLE TABLE CONTAINS AL RE TRANSMITTED B MARACTERS ARE ORG HE SCAN LINES, BI IS SHIFT AND BIT | Y THE TERMIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | IAL<br>IAT RITE a 1 | TURN LINES |                    |
| Ø5Ø7 38<br>Ø5Ø8 39                                             | 878<br>879 KYLKUP:                        | ĎВ           | 38Н, 39Н                                                                                                 | ;8 AND 9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                     |            |                    |
| 0509 30<br>050A 2D                                             | 88Ø                                       | DB           | 3ØH, 2DH                                                                                                 | ;0 AND -                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                     |            |                    |
| 050B 3D<br>050C 5C                                             | 881                                       | DB           | 3DH,5CH                                                                                                  | ;= AND \                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                     |            |                    |
| Ø5ØD Ø8<br>Ø5ØE ØØ                                             | 882 DMTH                                  | DB           | Ø8H,ØØH                                                                                                  | BS AND BRE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | AK                  |            |                    |
| 050F 75<br>0510 69                                             | 883 EMURTO                                | DB           | 75H,69H                                                                                                  | ;LOWER CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                     |            |                    |
| 0511 6F<br>0512 70<br>0513 5B                                  | 884                                       | DB           | 6FH,7ØH                                                                                                  | ;LOWER CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | O AND P             |            |                    |
| 0513 58<br>0514 5C                                             | 885                                       | DB           | 5BH,5CH                                                                                                  | ;[ AND \                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                     |            |                    |
| Ø515 ØA<br>Ø516 7F                                             | 886                                       | DB           | ØAH,7FH                                                                                                  | ;LF AND DEL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | ETE                 |            |                    |
| Ø517 6A<br>Ø518 6B                                             | 887                                       | DB           | 6АН, 6ВН                                                                                                 | ;LOWER CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | J AND K             |            | 24 5950<br>1568 48 |
| Ø519 6C<br>Ø51A 3B                                             |                                           | DB           | 6СН, ЗВН                                                                                                 | ;LOWER CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | L AND ;             |            |                    |
| Ø51B 27<br>Ø51C ØØ                                             | 889 TO THE GIVE                           | DB           | 27н,00н                                                                                                  | ; AND NOTH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | ING                 |            |                    |
| 051D 0D<br>051E 37                                             | 890                                       | DB           | ØDH, 37H                                                                                                 | ;CR AND 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                     |            |                    |
| 051F 6D                                                        | 891                                       | DB           | 6DH, 2CH                                                                                                 | ;LOWER CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | M AND COMM          | A          |                    |
| Ø521 2E<br>Ø522 2F                                             | 892                                       | DB 0 0       | 2EH, 2FH                                                                                                 | PERIOD AND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | SLASH               |            |                    |
| 0521 2E<br>0522 2F<br>0523 00<br>0524 00                       | 893                                       | DB           | ØØH,ØØH                                                                                                  | BLANK AND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | NOTHING             | 361        |                    |
| 0525 00                                                        | 894                                       | DB           | ØØН, ØØН                                                                                                 | ;NOTHING AN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | D NOTHING           |            |                    |
| 0520 00<br>0527 00<br>0528 61<br>0529 7A<br>052A 78<br>052B 63 | 895 801700                                | DB           | ØØH,61H                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | D LOWER CAS         | E A        |                    |
| Ø529 7A<br>Ø52A 78                                             |                                           | DB GMA       | 7AH, 78H                                                                                                 | ;LOWER CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Z AND X             | BAC        |                    |
| Ø52B 63<br>Ø52C 76<br>Ø52D 62                                  |                                           | DB           | 63Н,76Н                                                                                                  | ;LOWER CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | C AND V             |            |                    |
| 052D 62<br>052E 6E                                             |                                           | DB ®         | 52H,6EH                                                                                                  | ; LOWER CASE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                     |            |                    |
|                                                                |                                           |              | 1 GMA "t                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                     |            |                    |

| Ø52F 79<br>Ø53Ø ØØ            | 899           | DB                       | 79H,00H       | ;LOWER CASE Y AND NOTHIN | G 0553         |
|-------------------------------|---------------|--------------------------|---------------|--------------------------|----------------|
| 0531 00                       | 900           | DB                       | ØØH,2ØH       | ;NOTHING AND SPACE       |                |
| Ø532 2Ø<br>Ø533 64            | 901           | DB                       | 64H,65H       | ;LOWER CASE D AND F      | EB ANNS S      |
| Ø534 66<br>Ø535 67            | 902           | DB                       | 67H,68H       | ;LOWER CASE G AND H      |                |
| Ø536 68<br>Ø537 ØØ            | 903           | DB                       | 00H,71H       | ;TAB AND LOWER CASE Q    | 2669 84        |
| Ø538 71<br>Ø539 77            | 904           | DB                       | 77H,73H       | LOWER CASE W AND S       |                |
| Ø53A 73<br>Ø53B 65<br>Ø53C 72 | 9ø5           | DB                       | 65H,72H       | ;LOWER CASE E AND R      | 0 CEBB 88      |
| Ø53D 74                       | 906           | DB                       | 74H,00H       | ;LOWER CASE T AND NOTHIN |                |
| 053E 00<br>053F 1B            | 907           | DB                       | 1BH, 31H      | ;ESCAPE AND 1            | AS DEED SA     |
| Ø54Ø 31<br>Ø541 32            | 9ø8           | DB                       | 32H,33H       | ; 2 AND 3                |                |
| Ø542 33<br>Ø543 34            | 909           | DB                       | 34H,35H       | A AND 5                  |                |
| Ø544 35<br>Ø545 36            | 910           | DB                       | 36H,00H       | ; 6 AND NOTHING          |                |
| 0546 00<br>0547 2A            | 911           | DB                       | 2AH, 28H      | ;* AND )                 |                |
| Ø548 28<br>Ø549 29            | 912           | DB                       | 29H,5FH       | PUND - PUND - +1         | 85 ARRD 85     |
| Ø54A 5F<br>Ø54B 2B            | 913           | DB                       | 28H,00H       | ;+ AND NOTHING           |                |
| Ø54C ØØ<br>Ø54D Ø8            | 914           | DB                       | Ø8H,ØØH       | BS AND BREAK             |                |
| Ø54E ØØ<br>Ø54F 55            | 915           | DB                       | 55H,49H       | ;U AND I                 |                |
| Ø55Ø 49<br>Ø551 4F            | 916           | DB                       | 4FH,5ØH       | ;O AND P                 | 85<br>86<br>86 |
| Ø552 5Ø<br>Ø553 5D            | 917           | DB                       | 5DH, ØØH      | ;1 AND NO CHARACTER      |                |
| Ø554 ØØ<br>Ø555 ØA            | 918           | DB                       | ØAH,7FH       | ;LF AND DELETE           |                |
| Ø556 7F<br>Ø557 4A            | 919           | DB                       | 4AH, 4BH 3.18 | ;J AND K                 |                |
| Ø558 4B<br>Ø559 4C            | 920           | DB                       | 4CH, 3AH      | ;L AND :                 |                |
| Ø55A 3A<br>Ø55B 22            | 921           | DB                       | 22H,00H       | ;" AND NO CHARACTER      |                |
| Ø55C ØØ<br>Ø55D ØD            | 922           | DB                       | ØDH, 26H      | ;CR AND &                | 87<br>87       |
| Ø55E 26<br>Ø55F 4D            | 923           | DB                       | 4DH, 3CH      | ;M AND <                 |                |
| Ø56Ø 3C<br>Ø561 3E            | 924           | DB                       | 3EH, 3FH      | ;> AND ?                 | 88 20 88       |
| Ø562 3F<br>Ø563 ØØ            | 925           | DB                       | 00H,00H       | BLANK AND NOTHING        | 88             |
| Ø564 ØØ<br>Ø565 ØØ            | 926           | DB                       | ØØH,ØØH       | ;NOTHING AND NOTHING     |                |
| 0566 00<br>0567 00            |               | DB 38                    |               | ;NOTHING AND A           |                |
| Ø568 41<br>Ø569 5A            |               | and the same of the same | 5AH, 58H      | ;Z AND X                 |                |
| Ø56A 58<br>Ø56B 43            | 929           | DB                       | 43H,56H       | ;C AND V                 | 88             |
| Ø56C 56<br>Ø56D 42            | 930           |                          | 42H, 4EH      | ;B AND N                 | 88 AN          |
| Ø56E 4E<br>Ø56F 59            |               |                          | 59Н, ØØН      | ;Y AND NOTHING           | 88<br>66       |
| Ø57Ø ØØ<br>Ø571 ØØ            | 932           | OMA <sub>DB</sub> 38     | ØØH, 2ØH      | ;NO CHARACTER AND SPACE  | 88 S8 88       |
| Ø572 2Ø<br>Ø573 44            | 933           | DB                       | 44H,46H       | HBB*HIZ on               |                |
| Ø574 46<br>Ø575 47            |               |                          | CR AND 7      | ;D AND F                 | 89<br>37       |
| Ø576 48<br>Ø577 ØØ            | 934           |                          | 47H,48H       | G AND H                  | 6D 89          |
| Ø578 51<br>Ø579 57            | 935           | DB DB                    |               | ; TAB AND Q              | 2E 89          |
| 057A 53                       | 936           | DB NOTHING               | 57H,53H       | ;W AND S                 |                |
| Ø57B 45<br>Ø57C 52<br>Ø57D 54 | 937           | DB                       |               | E AND R                  |                |
| 05/E 00                       | 938<br>A 38AD | DB DB                    | 54H,00H       | T AND NO CONNECTION      |                |
| 057F 1B<br>0580 21<br>0581 40 | 939           | S CMA N 28               | 1BH,21H       | ESCAPE AND !             | 89             |
| 0582 23                       | 940           | V CIVA D SE              | 4ØH,23H       | ;@ AND #                 |                |
| 0584 25                       | 941           | A CIVA EI SE             | 24H,25H       | Transfer Country         | 62 89          |
| Ø585 5E                       | 942           | DB                       | 5EH,00H       | ; AND NO CONNECTION      |                |

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| Ø586 Ø                        | Ø          |            |      |                 | : 58                            |                                 |
|-------------------------------|------------|------------|------|-----------------|---------------------------------|---------------------------------|
|                               |            | 943<br>944 | THIS | IS WHERE THE CO | ONTROL CHARACTERS ARE LOOKED UP |                                 |
| 1587 Ø                        | Ø          | 945<br>946 | ĎВ   | ØØH,ØØH         | DISTANCE CONTRACTOR             |                                 |
| 0588 Ø<br>0589 Ø              | Ø          | 947        | DB   | 00H,00H         | 192 CURSK: DS I                 |                                 |
| 058A Ø                        | 0)         | 948        | DB   |                 | PRINCIPAL DESCRIPTION,          |                                 |
| 58C Ø                         | Ø          | 949        | DB   | ØØН,ØØН         | S au tamp 996                   |                                 |
| 58E Ø<br>58F 1                | Ø          |            |      | ØØН,ØØН         | 198 KBCHR: DB                   | 100                             |
| 0590 Ø                        | 9          | 950        | DB   | 15н,09н         | BOULKEADK: TECHNO TOWN OF       |                                 |
| 9591 Ø<br>9592 1              | Ø          | 951        | DB   | ØFH,10H         | CONTROL O AND P                 |                                 |
| 9593 Ø                        | C          | 952        | DB   | ØBH, ØCH        | CONTROL [ AND ] MINTER EN       |                                 |
| 9595 Ø                        | F          | 953        | DB   | ØAH,7FH         | ;LF AND DELETE                  |                                 |
| 9597 Ø.<br>9598 Ø.<br>9599 Ø. | В          | 954        | DB   | ØAH, ØBH        | ; CONTROL J AND K               | STORMAS DITER                   |
| 159A 0                        | Ø          | 955        | DB   | 0CH,00H         | ;CONTROL L AND NOTHING          | STEERINAL SYMBOLS               |
| 059B 0<br>059C 0<br>059D 0    | Ø          | 956        | DB   | ØØН,ØØН         | ;NOTHING                        |                                 |
| 159E Ø                        | Ø a ppaner | 957        | DB   | ØDH,ØØH         | ;CR AND NOTHING                 | BER SYMBOLS                     |
| 159F Ø                        | A CHARLES  | 958        | DB   | ØDH, ØØH        | CONTROL M AND COMMA             |                                 |
| 5A1 Ø<br>15A2 Ø<br>15A3 Ø     | 0 0000     | 959        | DB   | ØØH,ØØH         | NOTHING CONDITIONS              | INTM A SDB3 C                   |
| 15A4 0                        | OI .       | 960        | DB   | ØØH, ØØH        | NOTHING                         |                                 |
| 5A5 Ø                         | MATINI.    | 961        | DB   | 00H,00H         | ; NOTHING AND NOTHING           | TEYDAN A GEEA                   |
| 5A7 1<br>5A8 1                | A 10840    | 962        | DB   | 1AH,18H         | CONTROL Z AND X                 | D BEER A CTAN.<br>BYED A GOSS W |
| 5A9 Ø<br>5AA 1                | 3 NOOHE    | 963        | DB   | Ø3H,16H         | CONTROL C AND V                 |                                 |
| 5AB Ø                         | 2          | 964        | DB   | Ø2H,ØEH         | CONTROL B AND N                 | STRAUD A GMDC S                 |
| SAD 1<br>SAE Ø                | 9          | 965        | DB   | 19H,00H         | CONTROL Y AND NOTHING           | ASSEMBLY COMPLETE,              |
| 5AF Ø<br>5BØ 2                | Ø          | 966        | DB   | 00H,20H         | ; NOTHING AND SPACE             |                                 |
| 5B1 Ø<br>5B2 Ø                | 4          | 967        | DB   | Ø4H,Ø6H         | CONTROL D AND F                 |                                 |
| 5B3 Ø<br>5B4 Ø                | 7          | 968        | DB   | 07H,08H         | CONTROL G AND H                 |                                 |
| 5B5 Ø<br>5B6 1                | Ø          | 969        | DB   | ØØH,11H         | ; NOTHING AND CONTROL O         |                                 |
| 5B7 1<br>5B8 1                | 7          | 970        | DB   | 17H,13H         | CONTROL W AND S                 |                                 |
| 5B9 Ø                         | 6          | 971        | DB   | Ø6H,12H         | CONTROL E AND R                 |                                 |
| 5BA 1:<br>5BB 1:<br>5BC Ø     | <u>4</u>   | 972        | DB   | 14H,00H         | CONTROL W AND NOTHING           |                                 |
| 5BD 18<br>5BE 11              | В          | 973        | DB   | 1BH,1DH         | ; ESCAPE AND HOME (CREDIT)      |                                 |
| 5BF 11<br>5CØ 10              | Ε          | 974        | DB   | 1EH,1CH         | ;CURSOR UP AND DOWN (CREDIT)    |                                 |
| 5C1 14                        | 4          | 975        | DB   | 14H,1FH         | ;CURSOR RIGHT AND LEFT(CREDI    | T)                              |
| 5C2 11<br>5C3 01<br>5C4 01    | Ø          | 976        | DB   | ØØH,ØØH         | NOTHING                         | -/                              |
| 501 0                         | 0          | 977<br>978 | ;    |                 |                                 |                                 |
| 5C5 00                        | 7          | 979        |      |                 | 53 BAUD RATE GENERATOR          |                                 |
| 5C5 Ø6<br>5C6 Ø5<br>5C7 6     | 5          | 980 BDLK:  | ĎВ   | 00H,05H,69H,0   | 3H ;75 AND 110 BAUD             |                                 |
| 5C8 Ø3                        | 2          | 001        | 200  |                 |                                 |                                 |
| 5CA 02<br>5CB 4               | 2          | 981        | DB   | 80H,02H,40H,0   | 1H ;150 AND 300 BAUD            |                                 |
| 5CC ØI                        | 1          | 992        | DB   | as are con-     |                                 |                                 |
| SCE Ø                         | 7          | 982        | DB   | ØAØH,ØØH        | ;600 BAUD                       |                                 |
| 5CF 50<br>5DØ Ø0<br>5D1 28    |            | 983        | DB   | 50H,00H         | ;1200 BAUD                      |                                 |
| 5D2 00<br>5D3 14              | 3          | 984        | DB   | 28H,00H         | ;2400 BAUD                      |                                 |
| 5D4 Ø8                        | )          | 985        | DB   | 14H,00H         | ;4800 BAUD                      |                                 |
| 5D5 ØA<br>5D6 ØØ              | N .        | 986        | DB   | ØAH,ØØH         | ;9600 BAUD                      |                                 |

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|                                                                                                                                                                                                    | APPLIC                                                                                                                                                                                                                                                                                                                                                                                     | ATIONS                                                                                                                                                                                              |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0001<br>0002                                                                                                                                                                                       | 992 CURSX: DS 1<br>993 TOPAD: DS 2                                                                                                                                                                                                                                                                                                                                                         | H96, H90                                                                                                                                                                                            | 80                                                                                                                          |                                                                                |                                                                                                                                                                                                                 |
| 0002<br>0001                                                                                                                                                                                       | 994 LOC8Ø: DS 2<br>995 USCHR: DS 1                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                     |                                                                                                                             | 948                                                                            |                                                                                                                                                                                                                 |
| 0002<br>0001                                                                                                                                                                                       | 997 KEYDWN: DS 1                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                     |                                                                                                                             | 949                                                                            |                                                                                                                                                                                                                 |
| 0001<br>0001                                                                                                                                                                                       | 999 BAUD: DS 1                                                                                                                                                                                                                                                                                                                                                                             | 158,698                                                                                                                                                                                             |                                                                                                                             | 958                                                                            |                                                                                                                                                                                                                 |
| 0001<br>0001                                                                                                                                                                                       | 1000 KEYOK: DS 1<br>1001 ESCP: DS 1                                                                                                                                                                                                                                                                                                                                                        | OPH, 10%                                                                                                                                                                                            |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
| 0001<br>0001                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                     |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
| 0001                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                            | SAH, 7FH                                                                                                                                                                                            |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
| PUBLIC SYMBOLS                                                                                                                                                                                     | CONTROL J AND K                                                                                                                                                                                                                                                                                                                                                                            | HEB LAB                                                                                                                                                                                             | 80                                                                                                                          | 954                                                                            |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | CONTROL L AND NOTHING                                                                                                                                                                                                                                                                                                                                                                      | HOD,HOD                                                                                                                                                                                             | 80                                                                                                                          |                                                                                |                                                                                                                                                                                                                 |
| EXTERNAL SYMBOLS                                                                                                                                                                                   | DMIRTON;                                                                                                                                                                                                                                                                                                                                                                                   | HOO, HOO                                                                                                                                                                                            | acı                                                                                                                         |                                                                                |                                                                                                                                                                                                                 |
| US ER SYMBOLS ADX A 04CD CAPLOC A 022E CLRLIN A 0327 CNIM A 6003 CURSX A 0FE2 FMFD A 03CA KEYDWN A 0FEA KYLKUP A 0507 LNFD A 03F6 LPKBD A 0098 POPDAT A 0014 RXRDY A 0113 STBAUD A 00CC UP1 A 01E9 | ARND A 046D BAUD A 0FEC CGRT A 03AD CHREC A 024E CLRST A 02D5 CLSCR A 03E4 CNWD55 A 1803 CONCL A 02PD CURSY A 0FE1 DOWN A 02AE FRAME A 0167 GD18 A 0359 KEYINP A 0121 KEYOK A 0FED LOCUR A 03BB LNFD1 A 03FC LNGTH A 0050 NOVER A 03BD NTOVER A 038D NTOVER A 03BD NTOVER A 0364 PORTA A 1800 PORTB A 1801 SAVKEY A 01AF SCNLIN A 0FF1 STKEY A 0223 STPTR A 0FE0 UPCUR A 0333 USCHR A 0FE7 | BDLK A 05C5<br>CHRPUT A 0477<br>CNT0 A 5000<br>CRTM A 1000<br>ESCP A 075E<br>HOME A 0397<br>KEYS A 0131<br>LEFT A 036E<br>LOADX A 03EF<br>OKI A 049C<br>PORTC A 0211<br>TOPAD A 07E3<br>USTD A A000 | BTDIS<br>CLEAR<br>CLEAR<br>CNTI<br>CRIS<br>ESKAP<br>IN75<br>KPTK<br>LINNU<br>LOC80<br>OK7<br>RDKB<br>SETUP<br>TPDIS<br>USTF | A 5001<br>A 1001<br>A 03A5<br>A 0084<br>M A 0019<br>A 015C<br>A 015F<br>A 010F | BYPASS A 008F<br>CLLINE A 0415<br>CNT2 A 5002<br>CURAD A 0FE8<br>ESSO A 027B<br>INT75 A 1401<br>KYCHNG A 01BA<br>LINTAB A 0405<br>LOOPF A 00A7<br>ONBOT A 0453<br>RETLIN A 0459<br>SHCON A 0FEF<br>TRANS A 0148 |
| ASSEMBLY COMPLET                                                                                                                                                                                   | TE, NO ERRORS ON GIVA Y JOHTHOOS                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                     |                                                                                                                             | 989                                                                            |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | SMOTHING AND SPACE                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                     |                                                                                                                             |                                                                                | SSAF 88                                                                                                                                                                                                         |
|                                                                                                                                                                                                    | CONTROL D AND F                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                     | DB                                                                                                                          |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | CONTROL G AND H                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                     |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | MOTHING AND CONTROL Q                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                     |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | CONTROL W AND S                                                                                                                                                                                                                                                                                                                                                                            | 178,138                                                                                                                                                                                             |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | CONTROL E AND R                                                                                                                                                                                                                                                                                                                                                                            | B6H,12H                                                                                                                                                                                             |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | #CONTROL W AND NOTHING                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                     |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | (TICHED) SWOH OWA PRADER:                                                                                                                                                                                                                                                                                                                                                                  | HOI, HOI                                                                                                                                                                                            |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | CURSOR UP AND DOWN (CREDITS)                                                                                                                                                                                                                                                                                                                                                               | TEH* TCH                                                                                                                                                                                            |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | ; CURSOR RIGHT AND LEFT (CREDIT)                                                                                                                                                                                                                                                                                                                                                           | 14H,1FH                                                                                                                                                                                             | 80                                                                                                                          |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                            | 201,00H                                                                                                                                                                                             |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | ES BAUD RATE GENERATOR                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                     |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | 34 122 MAD 110 BAND                                                                                                                                                                                                                                                                                                                                                                        | Edite o friendling                                                                                                                                                                                  |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | CLUA BOS CHA DELL                                                                                                                                                                                                                                                                                                                                                                          | B. HOA. NOR. HOR                                                                                                                                                                                    |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                            | .,,,                                                                                                                                                                                                |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | QUAR 600;                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                     |                                                                                                                             | 382                                                                            |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | ;1290 BAUD                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                     |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | 12408 BAND                                                                                                                                                                                                                                                                                                                                                                                 | H50 x H0S                                                                                                                                                                                           |                                                                                                                             |                                                                                | 8508 88<br>8501 28                                                                                                                                                                                              |
|                                                                                                                                                                                                    | GUAS 88841                                                                                                                                                                                                                                                                                                                                                                                 | 144,098                                                                                                                                                                                             |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |
|                                                                                                                                                                                                    | OUA8 NUPP:                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                     |                                                                                                                             |                                                                                |                                                                                                                                                                                                                 |

# XIDNOGRAM INTEL PERIPHERAL COMPONENTS

| Communications                                                                        |                                                                                                                |
|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|
|                                                                                       |                                                                                                                |
| Description Programmable Communication Interface MUAR F.—Multifunctional Asynchronous | 8255 Programmable Peripheral Interface (see<br>also 8155, MICS 85 support; 8256 Date<br>Com. for parallel I/O) |
| Receiver/Transmitter                                                                  | 8279 Keyboard/Display Interface (see also                                                                      |
| Programmable HDLC/SDLC Protocol                                                       | 8278—Slave Processors)                                                                                         |
| Controlter                                                                            | Math Processors                                                                                                |
| Dual Channel Multiprotocol Controller<br>18t Local Area Network Communications        | 8231A Arithmetic Processina Unit                                                                               |
| GPIB (EEEE 488) Talker/Listener                                                       |                                                                                                                |
| GPIB Controller                                                                       | Floppy Disk Controllers                                                                                        |
|                                                                                       |                                                                                                                |
| netics                                                                                | 8271 Programmable Floppy Disk Controller<br>8272 Single/Double Density FDC                                     |
| Bubble Memory Controller                                                              | Display Controllers                                                                                            |
| Current Pulse Generator for Bubble<br>Memorles                                        | 8275 Programmable CRT Controller                                                                               |
| Dual Formatter/Sense Amp for Bubble                                                   | 8276 Small System CRT Controller GDC Graphics Display Controller (see also                                     |
| Memorius  Coil Pre-Orivor for Bubble Memories                                         | 8279 in Timer Counters/Parallel I/O/                                                                           |
| Quad VAIOS Drive Transistors for Bubble                                               | Keyboard Controllers)                                                                                          |
|                                                                                       | DMA Controllers/Interrupt Controllers                                                                          |
| Processors                                                                            | 8237 High Performance Programmable DMA                                                                         |
| ersal Poripheral Interface)                                                           | Controller                                                                                                     |
| Universal Peripheral Interface 1K ROM<br>Universal Peripheral Interface 2K ROM        | 8257 Programmable DMA Controller 8259A Programmable interrupt Controller (see also 8256 Data Com. section for  |
| Remote Universal Peripheral Interface 4K ROM                                          | interrupt controllers)                                                                                         |
| Universal Peripheral Interface 1K EPROM                                               | MCS-80 Bipolar Support                                                                                         |
| Universal Peripheral Interface 2K EPROM                                               | 8216/8226 4-Bit Parallel Bidirectional Bus Driver                                                              |
| ial Function Slave Processors                                                         | 8218 Bus Controller                                                                                            |
| Arithmetic Processing Unit                                                            | 8224 Clock Generator<br>8228/8238 System Controller and Bus Driver                                             |
|                                                                                       |                                                                                                                |
| I/O Expander for 8041A Keyboard Controller                                            | MCS 85 Bipolar Support                                                                                         |
| Nayboan Controllar Data Encryption Unit                                               | 8212 8-Bit Input/Output Port                                                                                   |
| Dot Matrix Printer Controller                                                         | 8219 Bus Controller                                                                                            |
| M Memory Controllers                                                                  | IAPX 88, 86 Bipolar Support                                                                                    |
| 4K/16K Lynamic RAM Controller                                                         | 8282/8283 Octal Latches                                                                                        |
| 16K/64K Dynamic RAM Controller                                                        | 8284A Clock Generator                                                                                          |
| Error Correction Unit                                                                 | 8286/8287 Octal Bus Transceivers                                                                               |
| r Counters/Parallel I/O/                                                              | 8288 Bus Controller<br>8289 Bus Arbiter                                                                        |
|                                                                                       | Muxed, Memory/I/O Components for                                                                               |
| Programmable Interval Timer<br>High P ormance Programmable Interval                   | MCS 85, IAPX 88                                                                                                |
|                                                                                       | 8155/8156 2048-Bit Static MOS RAM with I/O                                                                     |

# INTEL PERIPHERAL COMPONENTS

| Data                         | Communications                                                                                                                                                      |                                         | Description                                                                                                                                                          |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8251A                        | Description Programmable Communication Interface                                                                                                                    | 8255                                    | Programmable Peripheral Interface (see<br>also 8155, MCS 85 support; 8256 Data                                                                                       |
| 8256                         | MUART—Multifunctional Asynchronous Receiver/Transmitter                                                                                                             | 8279                                    | Com. for parallel I/O) Keyboard/Display Interface (see also                                                                                                          |
| 8273                         | Programmable HDLC/SDLC Protocol                                                                                                                                     |                                         | 8278—Slave Processors)                                                                                                                                               |
| 8274                         | Controller  Dual Channel Multiprotocol Controller                                                                                                                   | Math Pr                                 | ocessors                                                                                                                                                             |
|                              | t Local Area Network Communications GPIB (IEEE 488) Talker/Listener                                                                                                 | 8231A<br>8232                           | Arithmetic Processing Unit<br>Floating Point Processor                                                                                                               |
| 8292                         | GPIB Controller                                                                                                                                                     | Floppy I                                | Disk Controllers                                                                                                                                                     |
| 8293<br>Magn                 | GPIB Transceiver                                                                                                                                                    | 8271<br>8272                            | Programmable Floppy Disk Controller<br>Single/Double Density FDC                                                                                                     |
| 7220                         | Bubble Memory Controller                                                                                                                                            | Display                                 | Controllers                                                                                                                                                          |
| 7230<br>7242<br>7250<br>7254 | Current Pulse Generator for Bubble Memories Dual Formatter/Sense Amp for Bubble Memories Coil Pre-Driver for Bubble Memories Quad VMOS Drive Transistors for Bubble | 8275<br>8276<br>GDC                     | Programmable CRT Controller<br>Small System CRT Controller<br>Graphics Display Controller (see also<br>8279 in Timer Counters/Parallel I/O/<br>Keyboard Controllers) |
|                              | Memories                                                                                                                                                            | DMA Co                                  | ntrollers/Interrupt Controllers                                                                                                                                      |
|                              | Processors<br>ersal Peripheral Interface)                                                                                                                           | 8237                                    | High Performance Programmable DMA<br>Controller                                                                                                                      |
| 8041A<br>8042<br>RUPI        | Universal Peripheral Interface 1K ROM<br>Universal Peripheral Interface 2K ROM<br>Remote Universal Peripheral Interface<br>4K ROM                                   | 8257<br>8259A                           | Programmable DMA Controller<br>Programmable Interrupt Controller (see<br>also 8256 Data Com. section for<br>interrupt controllers)                                   |
| 8741A                        | Universal Peripheral Interface 1K EPROM                                                                                                                             | MCS 80                                  | Bipolar Support                                                                                                                                                      |
| 8742                         | Universal Peripheral Interface 2K EPROM                                                                                                                             | 8216/8226                               | 4-Bit Parallel Bidirectional Bus Driver                                                                                                                              |
| Specia                       | al Function Slave Processors                                                                                                                                        | 8218                                    | Bus Controller                                                                                                                                                       |
| 8231A<br>8232                | Arithmetic Processing Unit<br>Floating Point Processor                                                                                                              | 8224<br>8228/8238                       | Clock Generator System Controller and Bus Driver                                                                                                                     |
| 8243<br>8278                 | I/O Expander for 8041A Keyboard Controller                                                                                                                          | MCS 85                                  | Bipolar Support                                                                                                                                                      |
| 8294<br>8295                 | Data Encryption Unit Dot Matrix Printer Controller                                                                                                                  | 8212<br>8219                            | 8-Bit Input/Output Port<br>Bus Controller                                                                                                                            |
| DRAM                         | Memory Controllers                                                                                                                                                  | iAPX 88,                                | 86 Bipolar Support                                                                                                                                                   |
| 8202A<br>8203<br>8206        | 4K/16K Dynamic RAM Controller<br>16K/64K Dynamic RAM Controller<br>Error Correction Unit                                                                            | 8282/8283<br>8284A<br>8286/8287<br>8288 | Octal Latches Clock Generator Octal Bus Transceivers Bus Controller                                                                                                  |
|                              | Counters/Parallel I/O/<br>ard Controllers                                                                                                                           | 8289                                    | Bus Arbiter                                                                                                                                                          |
| 8253                         | Programmable Interval Timer                                                                                                                                         | Muxed, I<br>MCS 85,                     | Memory/I/O Components for iAPX 88                                                                                                                                    |
|                              | High Performance Programmable Interval Timer                                                                                                                        | •                                       | 2048-Bit Static MOS RAM with I/O Ports and Timer                                                                                                                     |